

# MC14572UB

## Hex Gate

The MC14572UB hex functional gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. The chip contains four inverters, one NOR gate and one NAND gate.

### Features

- Diode Protection on All Inputs
- Single Supply Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- NOR Input Pin Adjacent to  $V_{SS}$  Pin to Simplify Use As An Inverter
- NAND Input Pin Adjacent to  $V_{DD}$  Pin to Simplify Use As An Inverter
- NOR Output Pin Adjacent to Inverter Input Pin For OR Application
- NAND Output Pin Adjacent to Inverter Input Pin For AND Application
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable\*
- This Device is Pb-Free and is RoHS Compliant

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	$V_{DD}$	-0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	$V_{in}, V_{out}$	-0.5 to $V_{DD}$ + 0.5	V
Input or Output Current (DC or Transient) per Pin	$I_{in}, I_{out}$	±10	mA
Power Dissipation, per Package (Note 1)	$P_D$	500	mW
Ambient Temperature Range	$T_A$	-55 to +125	°C
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Lead Temperature (8-Second Soldering)	$T_L$	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Package: -7.0 mW/°C From 65°C To 125°C

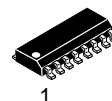
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



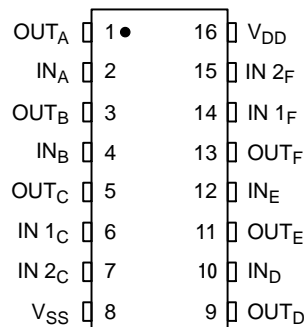
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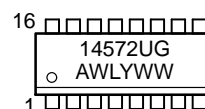


SOIC-16  
D SUFFIX  
CASE 751B

### PIN ASSIGNMENT



### MARKING DIAGRAM



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

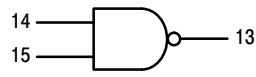
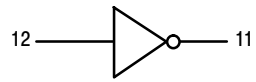
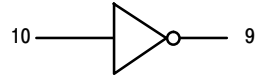
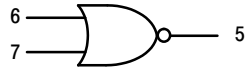
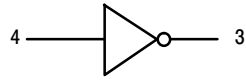
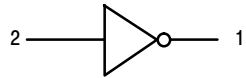
### ORDERING INFORMATION

Device	Package	Shipping†
MC14572UBDG	SOIC-16 (Pb-Free)	48 Units / Rail
MC14572UBDR2G	SOIC-16 (Pb-Free)	2500/Tape & Reel
NLV14572UBDR2G*	SOIC-16 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

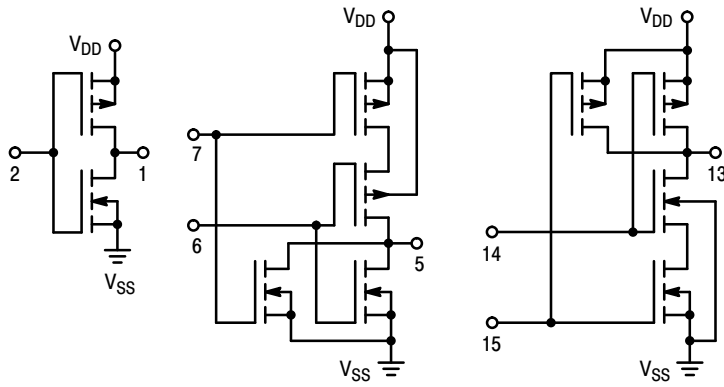
# MC14572UB

## LOGIC DIAGRAM



$V_{DD}$  = PIN 16  
 $V_{SS}$  = PIN 8

## CIRCUIT SCHEMATIC



# MC14572UB

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (Note 2)	Max	Min	Max		
Output Voltage "0" Level V <sub>in</sub> = V <sub>DD</sub> or 0	V <sub>OL</sub>	5.0	–	0.05	–	0	0.05	–	0.05	Vdc	
		10	–	0.05	–	0	0.05	–	0.05		
15		–	0.05	–	0	0.05	–	0.05			
V <sub>in</sub> = 0 or V <sub>DD</sub> "1" Level	V <sub>OH</sub>	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc	
		10	9.95	–	9.95	10	–	9.95	–		
		15	14.95	–	14.95	15	–	14.95	–		
Input Voltage "0" Level (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	V <sub>IL</sub>	5.0	–	1.0	–	2.25	1.0	–	1.0	Vdc	
		10	–	2.0	–	4.50	2.0	–	2.0		
15		–	2.5	–	6.75	2.5	–	2.5			
"1" Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IH</sub>	5.0	4.0	–	4.0	2.75	–	4.0	–	Vdc	
		10	8.0	–	8.0	5.50	–	8.0	–		
		15	12.5	–	12.5	8.25	–	12.5	–		
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source	I <sub>OH</sub>	5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	mAdc
			5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
	10		–0.62	–	–0.5	–0.9	–	–0.35	–		
	15	–1.8	–	–1.5	–3.5	–	–1.1	–			
Sink	I <sub>OL</sub>	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc	
		10	1.6	–	1.3	2.25	–	0.9	–		
		15	4.2	–	3.4	8.8	–	2.4	–		
Input Current	I <sub>in</sub>	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	–	–	–	–	5.0	7.5	–	–	pF	
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc	
		10	–	0.5	–	0.0010	0.5	–	15		
		15	–	1.0	–	0.0015	1.0	–	30		
Total Supply Current (Notes 3, 4) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0 10 15	$I_T = (1.89 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (3.80 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (5.68 \mu\text{A/kHz}) f + I_{DD}$							μAdc	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:  $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V f k$  where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> – V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.006.

# MC14572UB

## SWITCHING CHARACTERISTICS (Type 5) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	Min	Typ (Note 6)	Max	Unit
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	$t_{TLH}$	5.0 10 15	– – –	180 90 65	360 180 130	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{THL}$	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 5 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 17 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 15 \text{ ns}$	$t_{PLH}, t_{PHL}$	5.0 10 15	– – –	90 50 40	180 100 80	ns

5. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

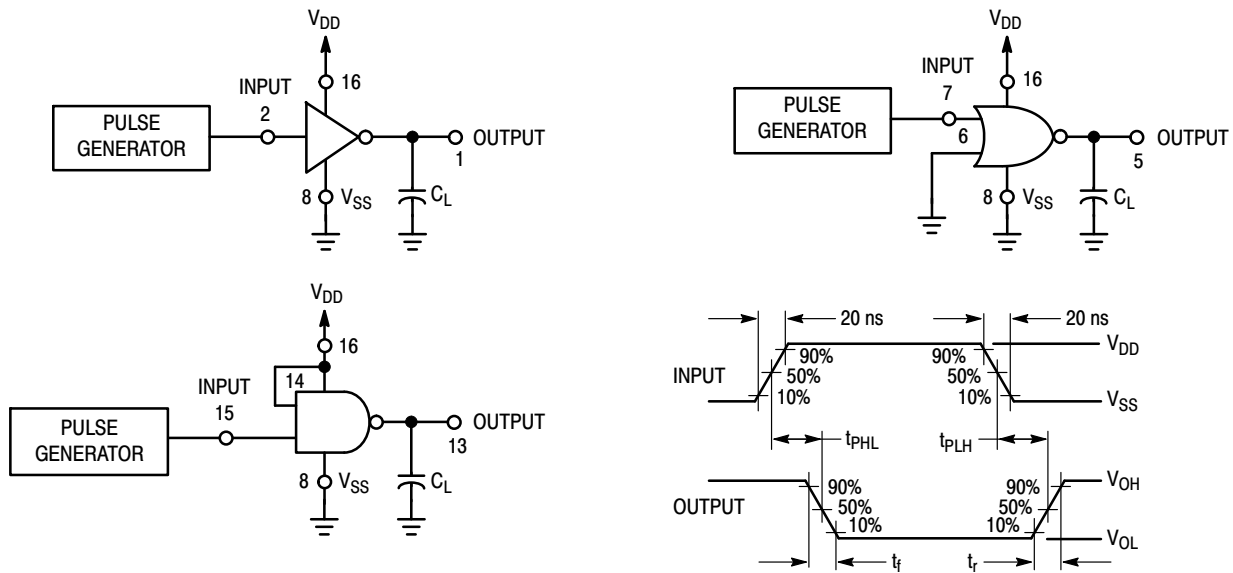
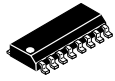


Figure 1. Switching Time Test Circuits and Waveforms

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

## SOIC-16 CASE 751B-05 ISSUE K

DATE 29 DEC 2006



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

- |  |  |  |  |
|--|--|--|--|
| <p>STYLE 1:</p> <p>PIN 1. COLLECTOR</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. NO CONNECTION</p> <p>5. EMITTER</p> <p>6. BASE</p> <p>7. COLLECTOR</p> <p>8. COLLECTOR</p> <p>9. BASE</p> <p>10. EMITTER</p> <p>11. NO CONNECTION</p> <p>12. EMITTER</p> <p>13. BASE</p> <p>14. COLLECTOR</p> <p>15. EMITTER</p> <p>16. COLLECTOR</p>                           | <p>STYLE 2:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. NO CONNECTION</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. NO CONNECTION</p> <p>7. ANODE</p> <p>8. CATHODE</p> <p>9. CATHODE</p> <p>10. ANODE</p> <p>11. NO CONNECTION</p> <p>12. CATHODE</p> <p>13. CATHODE</p> <p>14. NO CONNECTION</p> <p>15. ANODE</p> <p>16. CATHODE</p> | <p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. BASE, #1</p> <p>3. EMITTER, #1</p> <p>4. COLLECTOR, #1</p> <p>5. COLLECTOR, #2</p> <p>6. BASE, #2</p> <p>7. EMITTER, #2</p> <p>8. COLLECTOR, #2</p> <p>9. COLLECTOR, #3</p> <p>10. BASE, #3</p> <p>11. EMITTER, #3</p> <p>12. COLLECTOR, #3</p> <p>13. COLLECTOR, #4</p> <p>14. BASE, #4</p> <p>15. EMITTER, #4</p> <p>16. COLLECTOR, #4</p>   | <p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. COLLECTOR, #1</p> <p>3. COLLECTOR, #2</p> <p>4. COLLECTOR, #2</p> <p>5. COLLECTOR, #3</p> <p>6. COLLECTOR, #3</p> <p>7. COLLECTOR, #4</p> <p>8. COLLECTOR, #4</p> <p>9. BASE, #4</p> <p>10. EMITTER, #4</p> <p>11. BASE, #3</p> <p>12. EMITTER, #3</p> <p>13. BASE, #2</p> <p>14. EMITTER, #2</p> <p>15. BASE, #1</p> <p>16. EMITTER, #1</p> |
| <p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1</p> <p>2. DRAIN, #1</p> <p>3. DRAIN, #2</p> <p>4. DRAIN, #2</p> <p>5. DRAIN, #3</p> <p>6. DRAIN, #3</p> <p>7. DRAIN, #4</p> <p>8. DRAIN, #4</p> <p>9. GATE, #4</p> <p>10. SOURCE, #4</p> <p>11. GATE, #3</p> <p>12. SOURCE, #3</p> <p>13. GATE, #2</p> <p>14. SOURCE, #2</p> <p>15. GATE, #1</p> <p>16. SOURCE, #1</p> | <p>STYLE 6:</p> <p>PIN 1. CATHODE</p> <p>2. CATHODE</p> <p>3. CATHODE</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. CATHODE</p> <p>7. CATHODE</p> <p>8. CATHODE</p> <p>9. ANODE</p> <p>10. ANODE</p> <p>11. ANODE</p> <p>12. ANODE</p> <p>13. ANODE</p> <p>14. ANODE</p> <p>15. ANODE</p> <p>16. ANODE</p>                                 | <p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH</p> <p>2. COMMON DRAIN (OUTPUT)</p> <p>3. COMMON DRAIN (OUTPUT)</p> <p>4. GATE P-CH</p> <p>5. COMMON DRAIN (OUTPUT)</p> <p>6. COMMON DRAIN (OUTPUT)</p> <p>7. COMMON DRAIN (OUTPUT)</p> <p>8. SOURCE P-CH</p> <p>9. SOURCE P-CH</p> <p>10. COMMON DRAIN (OUTPUT)</p> <p>11. COMMON DRAIN (OUTPUT)</p> <p>12. COMMON DRAIN (OUTPUT)</p> <p>13. GATE N-CH</p> <p>14. COMMON DRAIN (OUTPUT)</p> <p>15. COMMON DRAIN (OUTPUT)</p> <p>16. SOURCE N-CH</p> |  |

### SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

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