DESCRIPTION

Demonstration Circuit 743 (DC743) is a Triple High Speed Video Amplifier featuring the LT6553. This circuit is designed to demonstrate AC-coupled performance in single-supply operation. Table 1 indicates the performance that is achieved with this evaluation board.

Design files for this circuit board are available. Call the LTC factory.

Table 1. Performance Summary (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Supply Voltage	Recommended Min/Max	+7V/+12V
Input Impedance, INR, ING, INB		75Ω to ground, ac-coupled internal signals
Output Impedance, OUTR, OUTG, OUTB		75Ω, ac-coupled
CAL trace Impedance		75Ω nominal
Gain	Outputs terminated into 75Ω	0dB nominal
	Outputs terminated into High impedance	+6dB nominal
Bandwidth	–3dB, Small Signal	7Hz-600MHz typical
Crosstalk	Worst-case All Hostile, 10MHz	–75dB typical
	Worst-case All Hostile, 100MHz	–50dB typical
Input Signal Voltage Range (note: feedback resistor connections tied to ground on printed circuit)	+9.0V Supply, No Output Clipping	±1.25V about average dc +7V/–3V dc component
On/Off Control Input	Logic Low Voltage (Amplifiers ON), DGND = 0V	≤0.8V
	Logic High Voltage (Amplifiers OFF), DGND = 0V	≥2.0V (5.5V max)

OPERATING PRINCIPLES

DC743 provides three identical channels of wideband signal amplification suitable for driving HDTV or high-resolution RGB video display cables. Each amplifier section of the LT6553 provides a fixed gain of 2, and with series "back-termination" at the outputs (included on the board), results in unity gain transmission of a video signal to a destination load. Each input is terminated to analog ground to properly load the input signal cable. The inputs are AC-coupled on board to eliminate input biasing requirements. The outputs are also AC-coupled to eliminate the amplifier DC bias.

To minimize ingress of external digital ground noise, the DGND logic reference input is decoupled from analog ground within the LT6553. DC743 includes a jumper, JP2, which allows the DGND to be strapped to the local analog ground (AGND); for example, when the logic source is floating or none is used during the evaluation. DGND may be left uncommitted with JP2 in the FLOAT position.

Another jumper, JP1, allows the LT6553 to be forced to an ENABLE condition. If JP1 is left in the EXTernal position, then enabling the LT6553 is accomplished by pull-

ing down the EN connection to a level near that of DGND via connection to E1 or J1. A pull-up resistor internal to the LT6553 will provide a default shutdown mode of operation if the control input is left open-circuit. NOTE: a 30kΩ resistance is included on-board to protect the part from having greater than 5.5V between EN and DGND during EN disconnection; refer to LT6553 datasheet for application details regarding this.

A CAL trace is also provided on DC743 to provide a means of precision calibration for a Network Analyzer (use the CAL connections when performing the "THRU" transmission calibration). The CAL trace has the same electrical performance and delay as the transmission lines of the three signal channels, thereby allowing circuit board and connector effects to be eliminated from the transmission measurements.

Figure 4 shows the material list of the components used by DC743, and Figure 5 shows the electrical interconnection.

QUICK START PROCEDURE

Demonstration Circuit 743 is easy to set up to evaluate the performance of the LT6553. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

NOTE: Due to the Ultra High Frequencies (UHF) involved, RF measurement practices are required to accurately evaluate the performance of the LT6553.

1. Place jumpers in the following positions:

   JP1 ENABLE

   JP2 AGND

2. Prior to connecting the power supply, preset the output voltage to +9V, or to the desired level, if different.
3. With power off, connect the power supply to V+ and AGND using banana-plug cables.
4. If using a Network Analyzer, perform the THRU transmission cal with all cabling, adapters, impedance converters, etc. in place, and using the DC743 CAL trace as the reference 0dB path.
5. Energize the power supply.
6. Connect the Network Analyzer (if used) to the appropriate channels to measure frequency response and crosstalk as desired. Figure 2 shows a typical transmission plot.
7. For video-signal evaluation, connect a component-video signal source to the inputs and a monitor and/or video analyzer to the outputs, using equal-length cabling amongst the three video channels. Figure 3 shows a typical pulse response.
8. To evaluate the shutdown mode, disconnect or relocate the JP1 jumper to the EXT position (with no connections made at EN, or if present, a logic high provided).

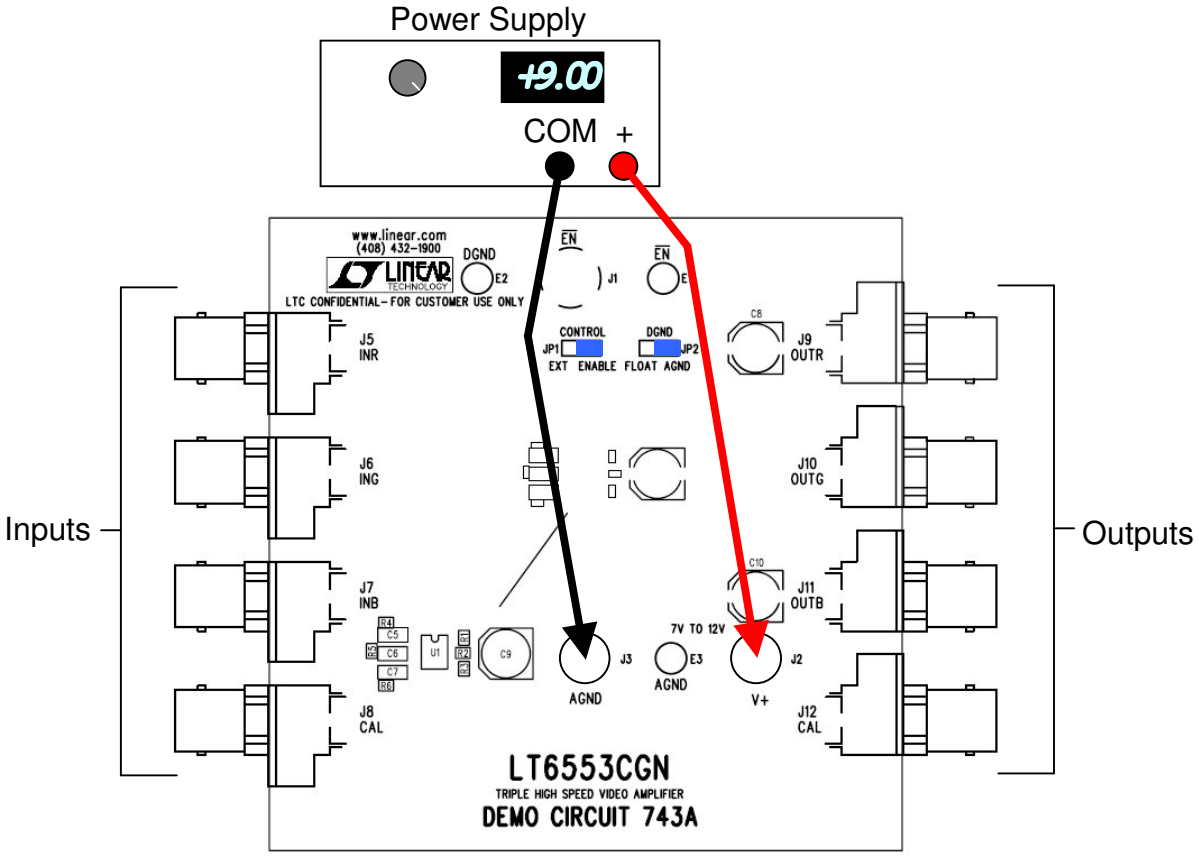

Figure 1. Recommended Demo Circuit Setup

Figure 2. Typical Transmission Frequency Response

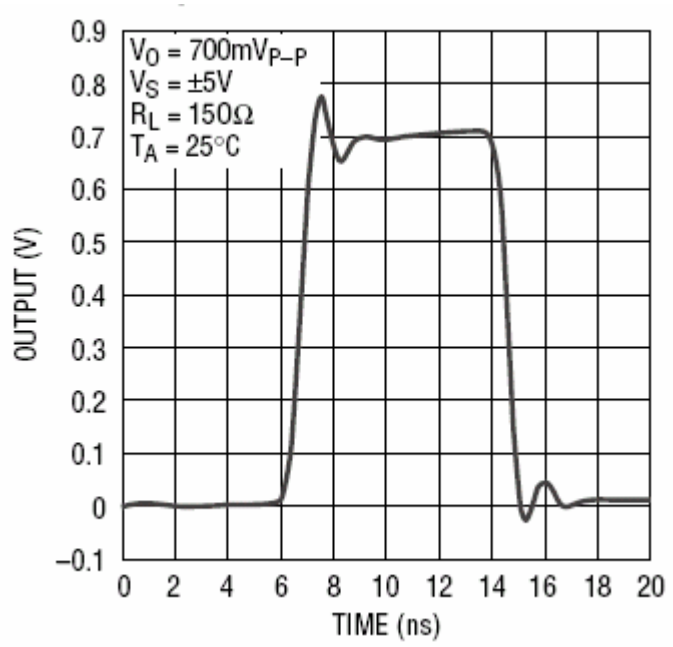

Figure 3. Typical Time-Domain Transmission Response

Item	Qty	Ref	Desc	Manufacturer / Part #
1	2	C1,C3	CAP, X7R 4700pF 50V 10% 0402	AVX 04025C472KAT1A
2	1	C2	CAP, NPO 470pF 25V 10% 0402	AVX 04023A471KAT1A
3	1	C4	CAP, X5R 10uF 16V 20% 1210	TAIYO YUDEN EMK325BJ106MN
4	3	C5,C6,C7	CAP, X5R 22uF 6.3V 20% 1206	AVX 12066D226MAT
5	3	C8,C9,C10	CAP, ELEC 220uF 6.3V 20% SVP	SANYO 6SVP220MX
6	3	E1,E2,E3	TURRET	MILL-MAX 2501-2
7	2	JP2,JP1	HEADER, 3 PINS 2mm	COMM 2802S-03G2
8	2	JP2,JP1	SHUNT, 2PIN 2mm	COMM CON CCIJ2MM-138G
9	1	J1	CONN, BNC 5 PINS	CONNEX 112404
10	2	J3,J2	JACK, BANANA	KEYSTONE 575-4
11	8	J5-J12	CONN, BNC, RIGHT ANGLE	CANARE BCJ-BPLH
12	3	R1,R2,R3	RES, 75 OHM 1% 1/16W 0402	AAC CR05-75R0FM
13	3	R4,R5,R6	RES, 80.6 OHM 1% 1/16W 0402	AAC CR05-80R6FM
14	3	R7,R9,R11	RES, 6.8K OHMS 5% 1/16W 0402	AAC CR05-682JM
15	3	R8,R10,R12	RES, 2.2K OHMS 5% 1/16W 0402	AAC CR05-222JM
16	1	R13	RES, 0402 30K OHM 5% 1/16W	AAC CR05-303JM
17	1	U1	IC, LT6553CGN	LINEAR TECH LT6553CGN

Figure 4. DC743 Bill of Material

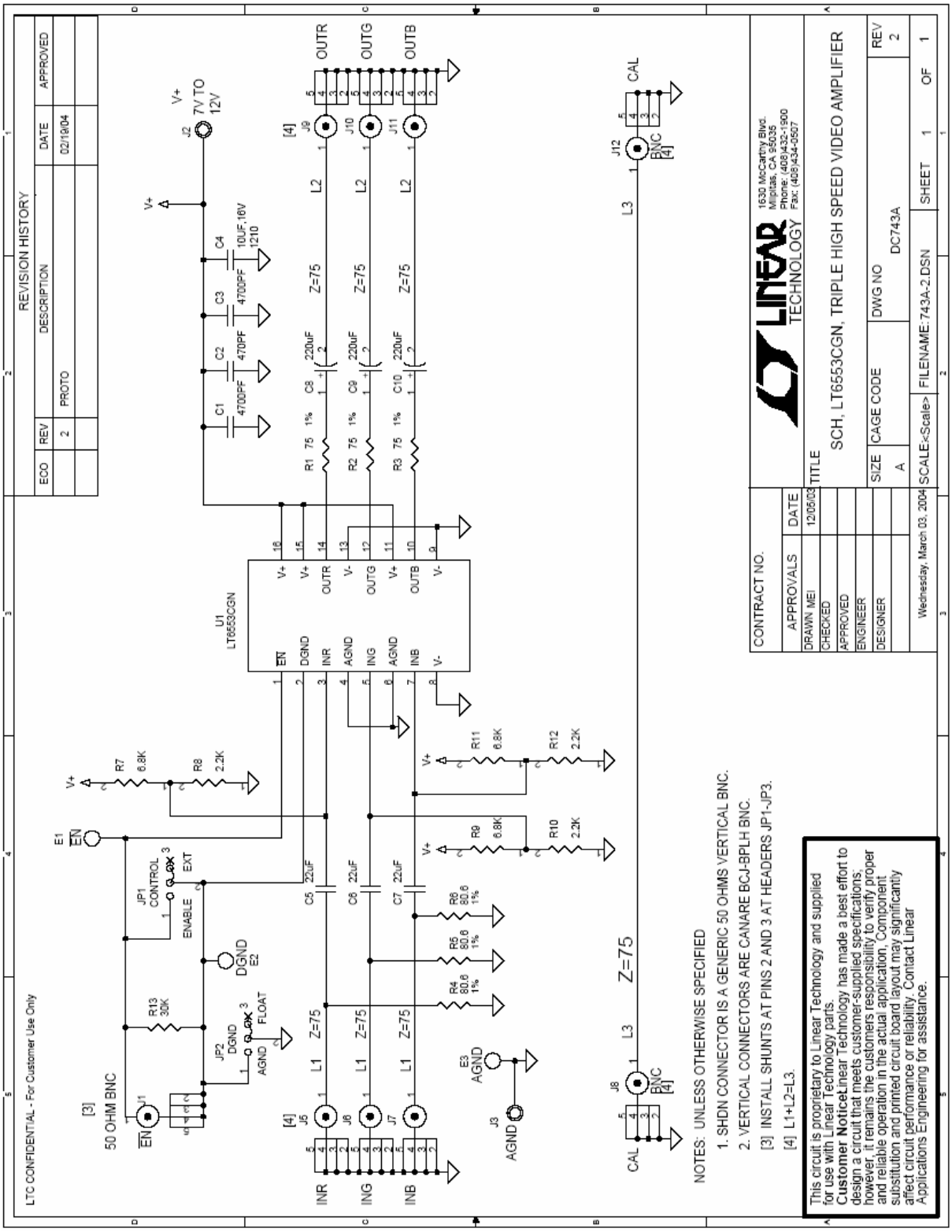

Figure 5. DC743 Electrical Schematic Diagram