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NTE4017B & NTE4022B
Integrated Circuit
CMOS, Counter/Divider

Description:

The NTE4017B and NTE4022B are 5–stage and 4–stage Johnson counters in 16–Lead DIP type packages having 10 and 8 decoded outputs, respectively. Inputs include a CLOCK, a RESET, and a CLOCK INHIBIT signal. Schmitt trigger action in the CLOCK input circuit provides pulse shaping that allows unlimited clock input pulse rise and fall times.

These counters are advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. A high RESET signal clears the counter to its zero count. Use of the Johnson counter configuration permits high–speed operation, 2–input decode–gating, and spike–free decoded outputs. Anti–lock gating is provided, thus assuring proper counting sequence. The decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A CARRY–OUT signal completes one cycle every 10 clock input cycles in the NTE4017B or every 8 clock input cycles in the NTE4022B and is used to ripple–clock the succeeding device in a multi–device counting chain.

Features:

- NTE4017B: Decade Counter with 10 Decoded Outputs
- NTE4022B: Octal Counter with 8 Decoded Outputs
- Fully Static Operation
- Medium Speed Operation: 10MHz (Typ) at V_{DD} = 10V
- Standardized, Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- 5V, 10V, and 15V Parametric Ratings

Applications:

- Decade Counter/Decimal Decode Display (NTE4017B)
- Binary Counter/Decoder
- Frequency Division
- Counter Control/Timers
- Divide–by–N Counting

Absolute Maximum Ratings:

DC Supply−Voltage Range (Voltages referenced to V_{SS}), V_{DD} . . . . . −0.5 to +20V

Input Voltage Range, All Inputs . . . . . −0.5 to V_{DD} +0.5V

DC Input Current, Any One Input . . . . . ±10mA

Power Dissipation, P_D

T_A = −40° to +60°C 500mW

T_A = +60° to +85°C . . . . . Derate Linearly at 12mW/°C to 200mW

Device Dissipation Per Output Transistor (T_A = −40° to +85°C) 100mW

Operating Temperature Range, T_A . . . . . −40° to +85°C

Storage Temperature Range, T_{stg} . . . . . −65° to +150°C

Lead Temperature, T_L

During Soldering, $^1/_{16}$" $\pm^1/_{32}$" (1.59 ± 0.79mm) from case 10s max . . . . . +265°C

Recommended Operating Conditions: (Note 1)

Parameter	Symbol	V_{DD}	Min	Max	Unit
Supply Voltage Range (T_A = −40° to +85°C)			3	18	V
Clock Input Frequency	f_{CL}	5	–	2.5	MHz
		10	–	5.0	MHz
		15	–	5.5	MHz
Colck Pulse Width	t_W	5	200	–	ns
		10	90	–	ns
		15	60	–	ns
Clock Rise & Fall Time	t_{rCL}, t_{fCL}	5, 10, 15	Unlimited		
Clock Inhibit Setup Time	t_s	5	230	–	ns
		10	100	–	ns
		15	70	–	ns
Reset Pulse Width	t_{RW}	5	260	–	ns
		10	110	–	ns
		15	60	–	ns
Reset Removal Time	t_{rem}	5	400	–	ns
		10	280	–	ns
		15	150	–	ns

Note 1. For maximum reliability, nominal operating conditions should be selected so that operation is always within the ranges outlined in the Recommended Operating Conditions.

Static Electrical Characteristics: (T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Device Current	I_{DD}max	V_{IN} = 0.5V, V_{DD} = 5V	–	0.04	5.0	µA
		V_{IN} = 0.10V, V_{DD} = 10V	–	0.04	10.0	µA
		V_{IN} = 0.15V, V_{DD} = 15V	–	0.04	20.0	µA
		V_{IN} = 0.20V, V_{DD} = 20V	–	0.08	100.0	µA

Static Electrical Characteristics (Cont'd): (T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Low (Sink) Current	I_{OH}min	V_O = 0.4V, V_{IN} = 0.5V, V_{DD} = 5V	0.51	1.0	–	mA
		V_O = 0.5V, V_{IN} = 0.10V, V_{DD} = 10V	1.3	2.6	–	mA
		V_O = 1.5V, V_{IN} = 0.15V, V_{DD} = 15V	3.4	6.8	–	mA
Output High (Source) Current	I_{OH}min	V_O = 4.6V, V_{IN} = 0.5V, V_{DD} = 5V	–0.51	–1.0	–	mA
		V_O = 2.5V, V_{IN} = 0.5V, V_{DD} = 5V	–1.6	–3.2	–	mA
		V_O = 9.5V, V_{IN} = 0.10V, V_{DD} = 10V	–1.3	–2.6	–	mA
		V_O = 13.5V, V_{IN} = 0.15V, V_{DD} = 15V	–3.4	–6.8	–	mA
Output Voltage Low–Level	V_{OL}max	V_{IN} = 0.5V, V_{DD} = 5V	–	0	0.05	V
		V_{IN} = 0.10V, V_{DD} = 10V	–	0	0.05	V
		V_{IN} = 0.15V, V_{DD} = 15V	–	0	0.05	V
Output Voltage High–Level	V_{OH}min	V_{IN} = 0.5V, V_{DD} = 5V	4.95	5.0	–	V
		V_{IN} = 0.10V, V_{DD} = 10V	9.95	10.0	–	V
		V_{IN} = 0.15V, V_{DD} = 15V	14.95	15.0	–	V
Input Low Voltage	V_{IL}max	V_O = 0.5V to 4.5V, V_{DD} = 5V	–	–	1.5	V
		V_O = 1.9V, V_{DD} = 10V	–	–	3.0	V
		V_O = 1.5V to 13.5V, V_{DD} = 15V	–	–	4.0	V
Input High Voltage	V_{IH}min	V_O = 0.5V to 4.5V, V_{DD} = 5V	3.5	–	–	V
		V_O = 1.9V, V_{DD} = 10V	7.0	–	–	V
		V_O = 1.5V to 13.5V, V_{DD} = 15V	11.0	–	–	V
Input Current	I_{IN}max	V_{IN} = 0.18V, V_{DD} = 18V	–	$\pm10^{-5}$	±0.1	µA

Dynamic Electrical Characteristics: (T_A = +25°C, Input t_r, t_f = 20ns, C_L = 50pF, R_L = 200kΩ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clocked Operation						
Propagation Delay Time Decode Out	t_{PHL}, t_{PLH}	V_{DD} = 5V	–	325	650	ns
		V_{DD} = 10V	–	135	270	ns
		V_{DD} = 15V	–	85	170	ns
Carry Out		V_{DD} = 5V	–	300	600	ns
		V_{DD} = 10V	–	125	250	ns
		V_{DD} = 15V	–	80	160	ns
Transition Time, Carry Out or Decade Out Line	t_{THL}, t_{TLH}	V_{DD} = 5V	–	100	200	ns
		V_{DD} = 10V	–	50	100	ns
		V_{DD} = 15V	–	40	80	ns
Maximum Clock Input Frequency	f_{CL}	V_{DD} = 5V, Note 2	2.5	5.0	–	MHz
		V_{DD} = 10V, Note 2	5.0	10.0	–	MHz
		V_{DD} = 15V, Note 2	5.5	11.0	–	MHz

Note 2. Measured with respect to carry output line.

Dynamic Electrical Characteristics (Cont'd): (T_A = +25°C, Input t_r, t_f = 20ns, C_L = 50pF, R_L = 200kΩ unless otherwise specified)

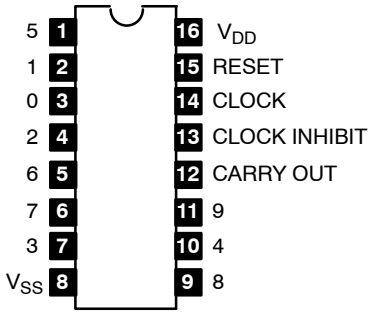
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clocked Operation (Cont'd)						
Minimum Clock Pulse Width	t_W	V_{DD} = 5V	–	100	200	ns
		V_{DD} = 10V	–	45	90	ns
		V_{DD} = 15V	–	30	60	ns
Clock Rise or Fall Time	t_{rCL}, t_{fCL}	V_{DD} = 5V, 10V or 15V	Unlimited			
Minimum Clock Inhibit to Clock Setup Time	t_s	V_{DD} = 5V	–	115	230	ns
		V_{DD} = 10V	–	50	100	ns
		V_{DD} = 15V	–	30	70	ns
Input Capacitance	C_{IN}	Any Input	–	5	–	pF
Reset Operation						
Propagation Delay Time, Carry Out or Decode Out Lines	t_{PHL}, t_{PLH}	V_{DD} = 5V	–	265	530	ns
		V_{DD} = 10V	–	115	230	ns
		V_{DD} = 15V	–	85	170	ns
Minimum Reset Pulse Width	t_W	V_{DD} = 5V	–	130	260	ns
		V_{DD} = 10V	–	55	110	ns
		V_{DD} = 15V	–	30	60	ns
Minimum Reset Removal Time		V_{DD} = 5V	–	200	400	ns
		V_{DD} = 10V	–	140	280	ns
		V_{DD} = 15V	–	75	150	ns

Application Notes:

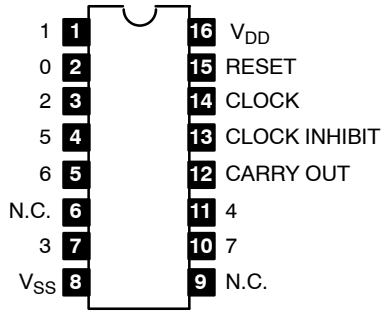
When the N^{th} decoded output is reached (N^{th} clock pulse) the S−R flip−flop (constructed from two NOR gates of the NTE4001B) generates a reset pulse which clears the NTE4017B or NTE4022B to its zero count. At this time, if the N^{th} decoded output is greater than or equal to 6 in the NTE4017B or 5 in the NTE4022B, the C_{OUT} line goes high to clock the next NTE4017B or NTE4022B counter section. The "0" decoded output also goes high at this time. Coincidence of the clock low and decoded "0" output low resets the S−R flip−flop to enable the NTE4017B or NTE4022B. If the N^{th} decoded output is less than 6 (NTE4017B) or 5 (NTE4022B), the C_{OUT} line will not go high and, therefore, cannot be used. In this case "0" decoded output may be used to perform the clocking function for the next counter.

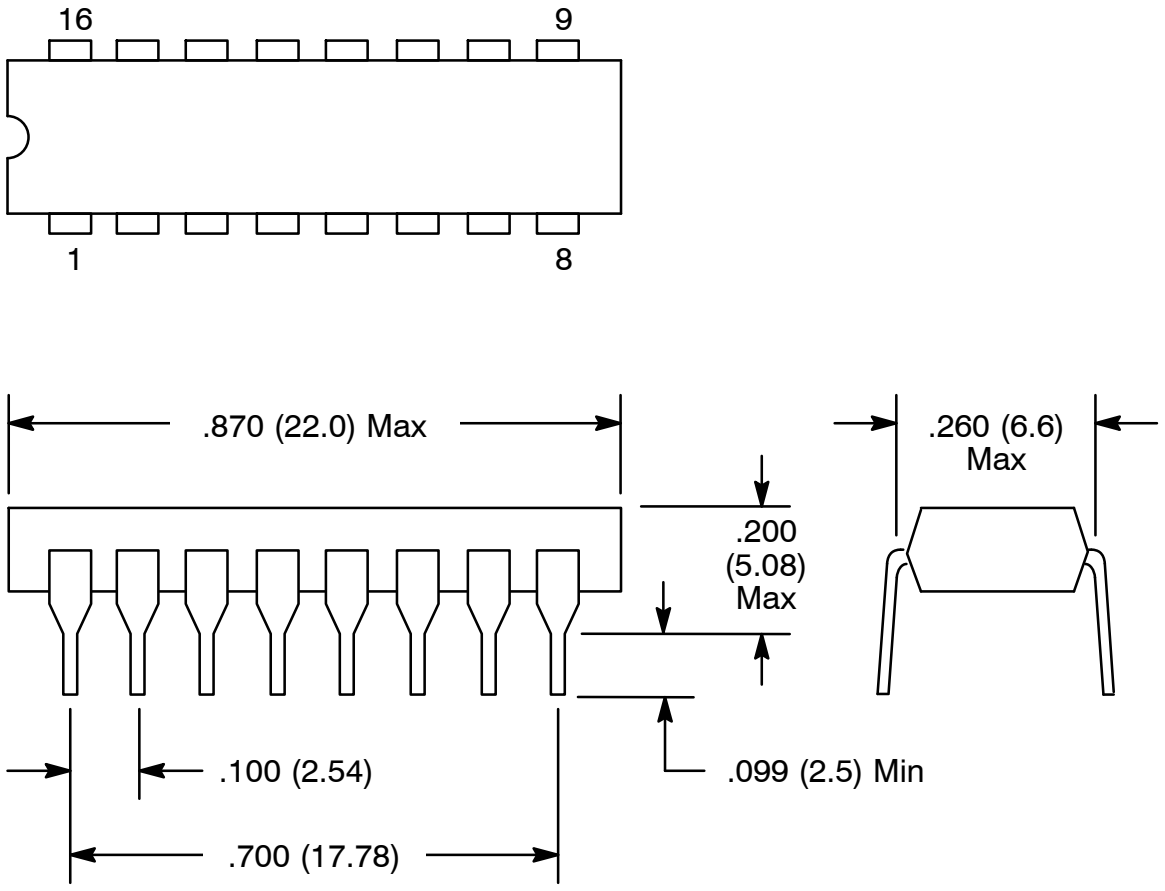
Pin Connection Diagram

NTE4017B



NTE4022B




16
9
1
8
.870 (22.0) Max
.260 (6.6)
Max
.200
(5.08)
Max
.100 (2.54)
.099 (2.5) Min
.700 (17.78)