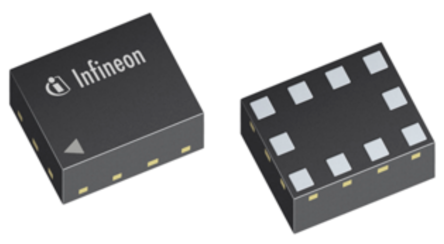
BGSA11GN10

Dual Single Pole Single Throw Antenna Tuning Switch

Features

- Designed for high linearity and high RF voltage tuning applications
- Multiple selectable switch configurations:
  Each throw directly and independently controlled
- Low R_{ON} resistance of 1.0 Ω at each port in ON state,
  0.5 Ω using both SPST in parallel
- Low C_{OFF} capacitance of 250 fF at each port in OFF state
- High bidirectional RF operating voltage of 36 V in OFF state
- Low harmonic generation
- 2 GPIO pins control interface
- Supply voltage range: 1.65 to 3.6 V
- No RF parameter change within supply voltage range
- Small form factor 1.1 mm x 1.5 mm (MSL1, 260°C per JEDEC J-STD-020)
- RoHS and WEEE compliant package



1.1 x 1.5 mm^2

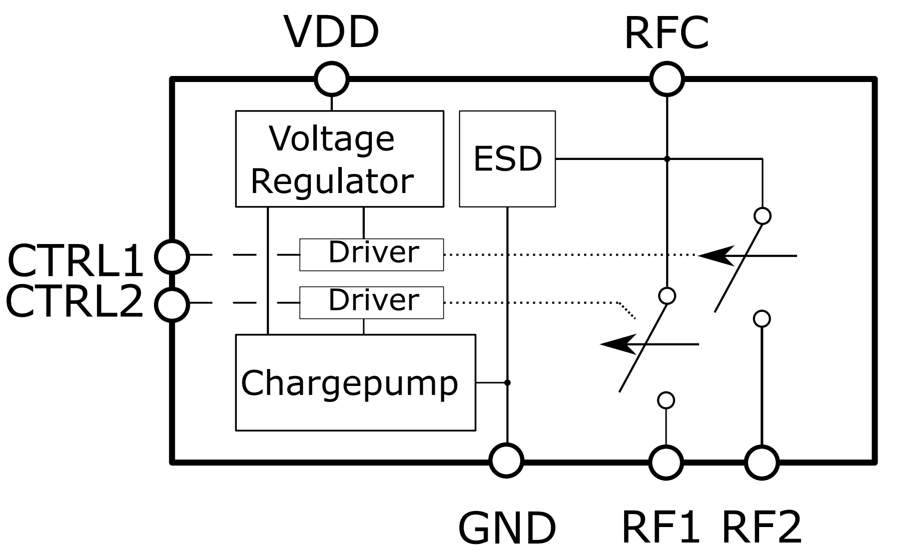
Potential Applications

- Impedance Tuning
- Antenna Tuning
- Inductance Tuning
- Tunable Filters

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Block Diagram



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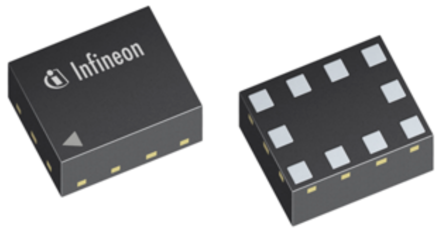
1 Features



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RoHS Halogen-Free Lead-Free Green

Description

The BGSA11GN10 is a Dual Single Pole Single Throw (SPST) RF antenna aperture switch optimized for low C_{OFF} enabling applications up to 6.0 GHz. This single supply chip integrates on-chip CMOS logic driven by a simple, single-pin CMOS or TTL compatible control input signal. Unlike GaAs technology, the 0.1dB compression point exceeds the switch maximum input power level, resulting in linear performance at all signal levels and external DC blocking capacitors at the RF ports are only required if DC voltage is applied externally. Due to its very high RF voltage ruggedness it is suited for switching any reactive devices such as inductors and capacitors in RF matching circuits without significant losses in quality factors.

Product Name	Marking	Package
BGSA11GN10	11	TSNP-10-1

2 Maximum Ratings

Table 1: Maximum Ratings, Table I at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency Range	f	0.1	–	–	GHz	1)
Supply voltage 2)	V_{DD}	-0.5	–	3.6	V	Only for infrequent and short duration time periods
Storage temperature range	T_{STG}	-55	–	150	°C	–
RF input power	P_{RF_max}	–	–	39	dBm	Pulsed RF input power, duty cycle of 25 % with T_period= 4620 μs, ON-state, setup as of Fig. 1
RF voltage	V_{RF_max}	–	–	48	V	Short term peaks (1μs, duty cycle 0.1%), Isolation mode, test setup acc. Fig. 2 / Fig. 3 and exceeding typical linearity, R_{ON} and C_{OFF} parameters
ESD capability, CDM 3)	$V_{ESD_{CDM}}$	-1	–	+1	kV	
ESD capability, HBM 4)	$V_{ESD_{HBM}}$	-1	–	+1	kV	
ESD capability, system level (RF port) 5)	$V_{ESD_{ANT}}$	-8	–	+8	kV	RF vs system GND, with 27 nH shunt inductor
Junction temperature	T_J	–	–	125	°C	–
Thermal resistance junction - soldering point	R_{thJS}	–	–	45	K/W	–
Maximum DC-voltage on RF-Ports and RF-Ground	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF-Ports
Control Voltage Levels	V_{Ctrlx}	-0.7	–	V_{DD}+0.7 (max. 3.6)	V	–
Moisture Sensitivity Level	MSL	–	1	–		–

1) Switch has a low-pass response. For higher frequencies, losses have to be considered for their impact on thermal heating. The DC voltage at RF ports V_{RFDC} has to be 0 V.
2) Note: Consider potential ripple voltages on top of V_{IO}. Including RF ripple, V_{IO} must not exceed the maximum ratings: $V_{Ctrl} = V_{DC} + V_{Ripple}$.
3) Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
4) Human Body Model ANSI/ESDA/JEDEC JS-001 (R = 1,5 kΩ, C = 100 pF).
5) IEC 61000-4-2 (R = 330 Ω, C = 150 pF), contact discharge.

Warning: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

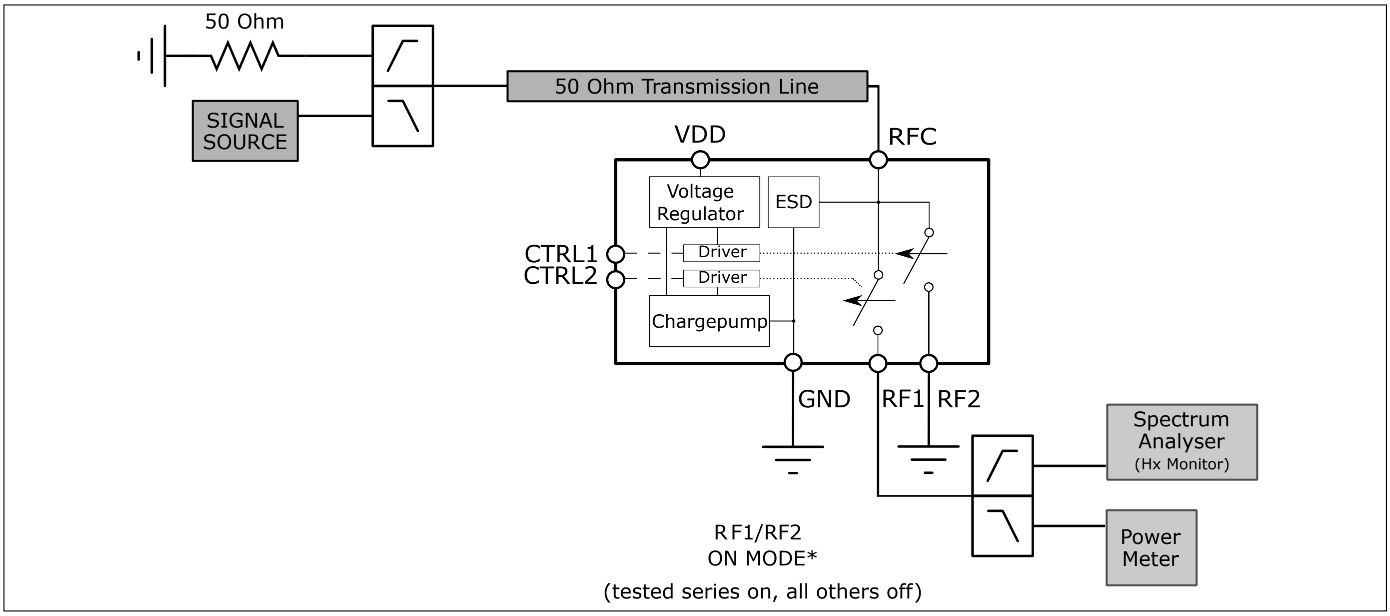

Figure 1: RF operating and Harmonics generation measurement configuration - RFx ON mode

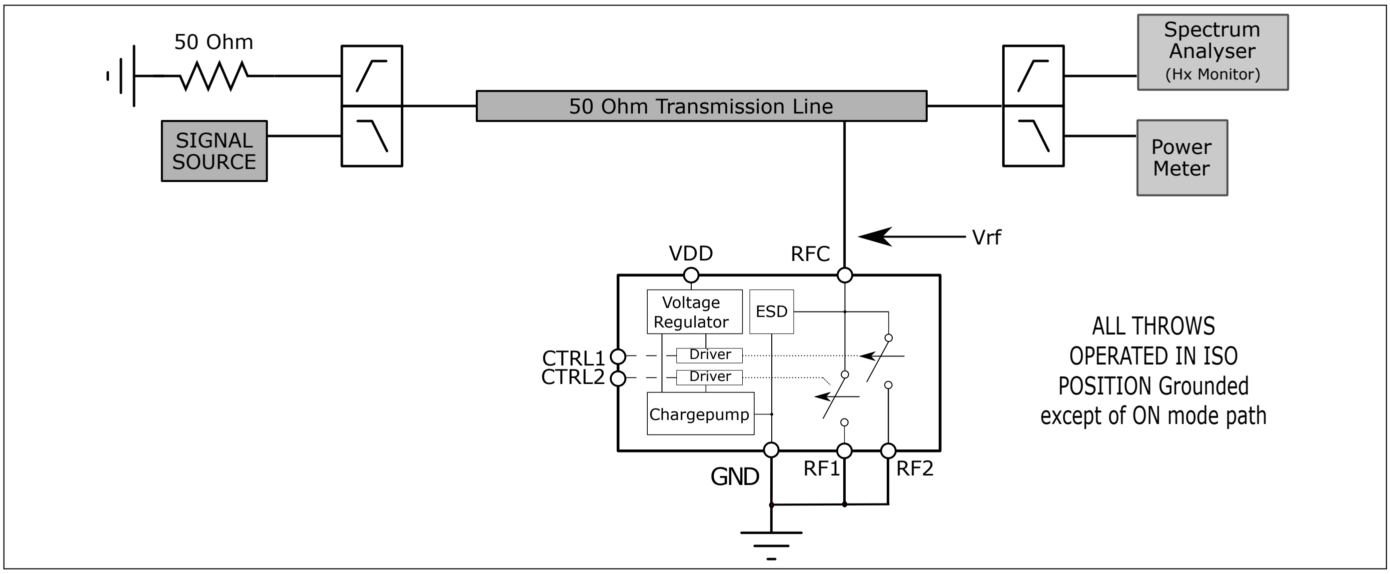

Figure 2: RF operating voltage measurement configuration - OFF mode at RFC

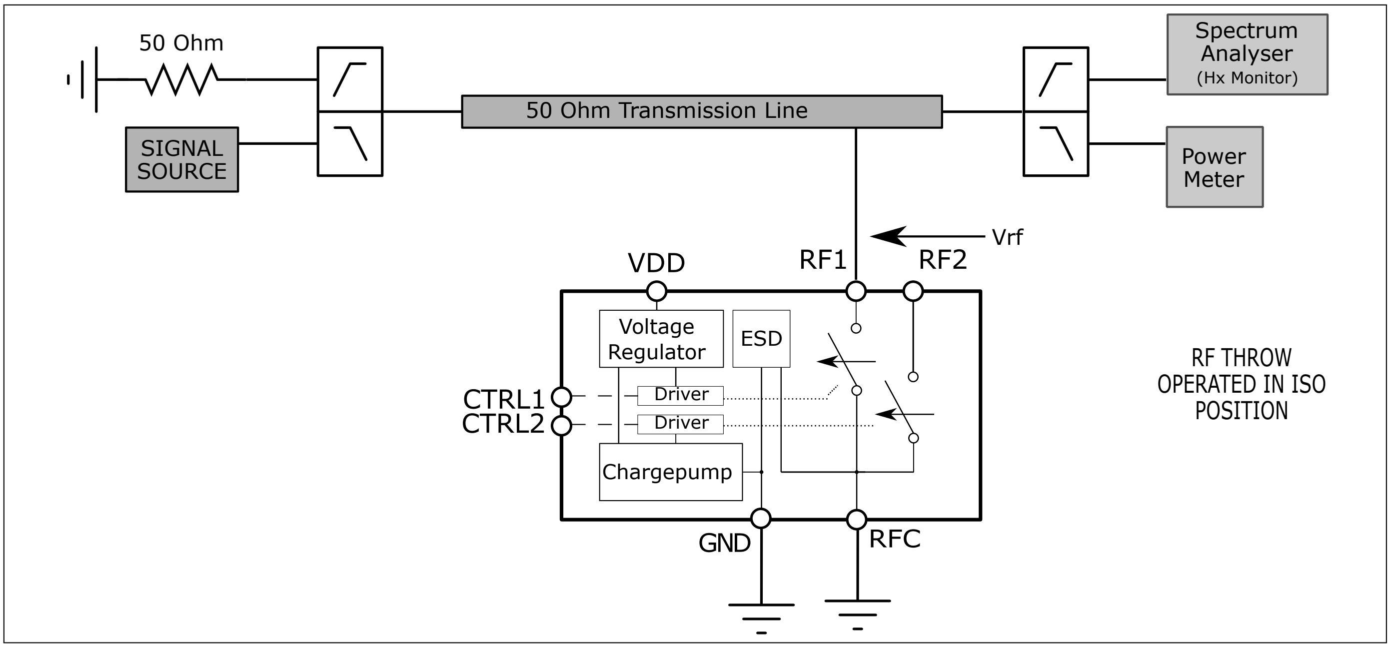

Figure 3: RF operating voltage measurement configuration - OFF mode at RFx

3 DC Characteristics

Table 2: DC Characteristics at $T_A = -40\,°C$ to $85\,°C$

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	1.65	2.8	3.6	V	–
Supply current	I_{DD}	–	80	150	µA	–
Control voltage low	$V_{Ctrl,low}$	0	–	0.45	V	–
Control voltage high	$V_{Ctrl,high}$	1.2	1.8	2.85	V	$V_{Ctrl,high} < V_{DD}$
Control current low	$I_{Ctrl,low}$	-1	0	1	µA	–
Control current high	$I_{Ctrl,high}$	-1	0	1	µA	$V_{Ctrl,high} < V_{DD}$
Ambient temperature	T_A	-40	25	85	°C	–
RF switching time	t_{ST}	2	5	7	µs	P_{IN} = 0 dBm, $Z_0 = 50\,\Omega$, $T_A = -40\,°C... + 85\,°C$ V_{DD} = 1.65 – 3.6 V
Startup time	t_{Pup}	–	20	30	µs	Refering Fig. 4 and Fig. 5

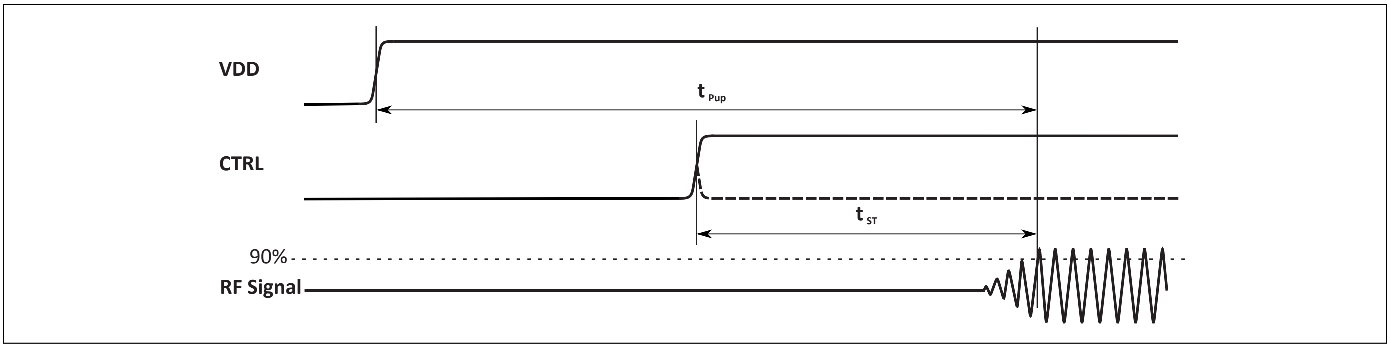

Figure 4: Switching Time Definition

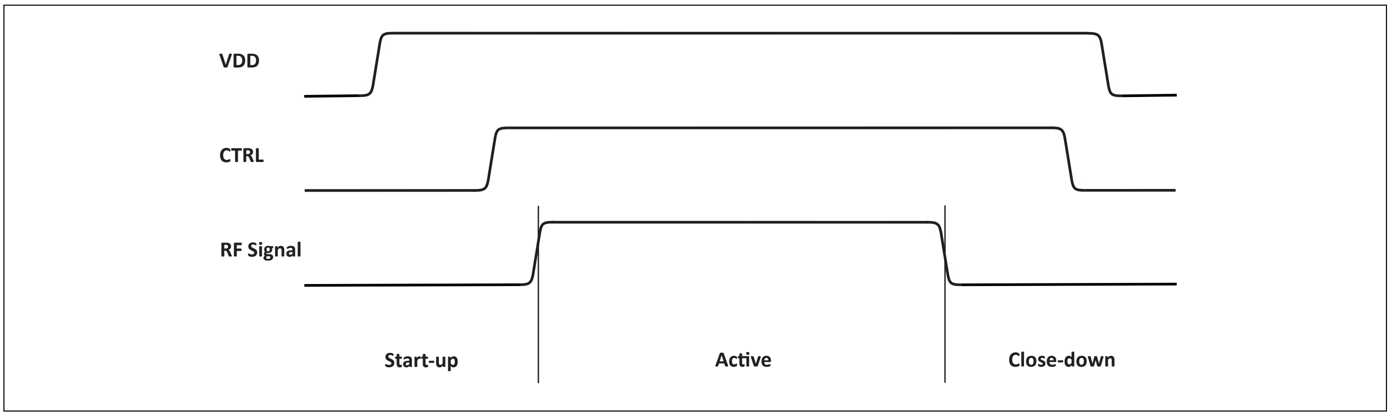

Figure 5: Timing of Control and RF signals for valid operation

4 RF Small Signal Characteristics

Table 3: RF small signal specifications

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency range	f	0.1	–	6.0	GHz	–
Switch ON resistance	R_{ON}	0.7	1.0	1.5	Ω	RFx to RFC
Switch OFF capacitance	C_{OFF}	200	250	350	fF	RFx to RFC
Insertion Loss (1,2,3)						
824 - 960 MHz	IL	0.10	0.19	0.29	dB	V_{DD} = 1.8 − 3.6 V, $T_A = -40\,°C... + 85\,°C$, $Z_0 = 50\,\Omega$, RF1 or RF2 switched to RFC
1710 - 1980 MHz		0.24	0.34	0.43	dB	
1981 - 2169 MHz		0.28	0.36	0.43	dB	
2170 - 2690 MHz		0.29	0.5	0.69	dB	
Return Loss(1,2,3)						
All Ports @ 824 - 915 MHz	RL	20	25	30	dB	V_{DD} = 1.8 − 3.6 V, $T_A = -40\,°C... + 85\,°C$, $Z_0 = 50\,\Omega$
All Ports @ 1710 - 2169 MHz		16	18	20	dB	
All Ports @ 2170 - 2690 MHz		12	15	18	dB	
Isolation RFx to RFC(1,2,3)						
824 - 915 MHz	ISO	16	17	19	dB	V_{DD} = 1.8 − 3.6 V, $T_A = -40\,°C... + 85\,°C$, $Z_0 = 50\,\Omega$
1710 - 1980 MHz		14	12	11	dB	
1981 - 2169 MHz		13	11	11	dB	
2170 - 2690 MHz		9	10	11	dB	
Isolation RFx to RFx(1,2,3)						
824 - 915 MHz	ISO	21	22	24	dB	V_{DD} = 1.8 − 3.6 V, $T_A = -40\,°C... + 85\,°C$, $Z_0 = 50\,\Omega$
1710 - 1980 MHz		16	17	18	dB	
1981 - 2169 MHz		15	16	17	dB	
2170 - 2690 MHz		13	15	17	dB	

1) Valid for all RF power levels, no compression behavior
2) Network analyser input power: $P_{IN} = -20\,dBm$
3) On application board without any matching components

5 RF large signal parameter

Table 4: RF large signal specifications

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RF operating voltage	V_{RF_peak}	–	–	36	V	
Harmonic Generation up to 12.75 GHz(1,2,3)						
All RF Ports - Second Order Harmonics	P_{H2}	–	90	–	dBc	25 dBm, 50Ω, f_0 = 786 MHz
All RF Ports - Third Order Harmonics	P_{H3}	–	115	–	dBc	25 dBm, 50Ω, f_0 = 786 MHz
All RF Ports - Second Order Harmonics	P_{H2}	–	90	–	dBc	33 dBm, 50Ω, f_0 = 824 MHz
All RF Ports - Third Order Harmonics	P_{H3}	–	110	–	dBc	33 dBm, 50Ω, f_0 = 824 MHz
All RF Ports	P_{Hx}	105	–	–	dBc	25 dBm, 50Ω, CW mode
Intermodulation Distortion IMD2 (1,2,3)						
IIP2, low	IIP2,l	–	110	–	dBm	IIP2 conditions table 8
IIP2, high	IIP2,h	–	120	–	dBm	
Intermodulation Distortion IMD3 (1,2,3)						
IIP3	IIP3	–	75	–	dBm	IIP3 conditions table 9
SV LTE Intermodulation (1,2,3)						
IIP3,SVLTE	IIP3,SV	–	75	–	dBm	SV-LTE conditions table 10

1) Terminating Port Impedance: $Z_0 = 50\,\Omega$ 2) Supply Voltage: $V_{DD} = 1.8 - 3.6\,V$ 3) On application board without any matching components

Table 5: IIP2 conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1 Low	2140	1950	20	190	-15
Band 1 High	2140	1950	20	4090	-15
Band 5 Low	881.5	836.5	20	45	-15
Band 5 High	881.5	836.5	20	1718	-15

Table 6: IIP3 conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1	2140	1950	20	1760	-15
Band 5	881.5	836.5	20	791.5	-15

Table 7: SV-LTE conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 5	872	827	23	872	14
Band 13	747	786	23	747	14
Band 20	878	833	23	2544	14

6 Logic Truth Table

Table 8: Logic Table

CTRL 1	CTRL 2	Mode RF1 to RFc	Mode RF2 to RFc2
0	0	OFF	OFF
0	1	OFF	ON
1	0	ON	OFF
1	1	ON	ON

CTRL1 and CTRL 2 can be connected together to control both switches at once. This enables the use of both SPSTs to reduce Ron by parallel switching

7 Application Information

Pin Configuration and Function

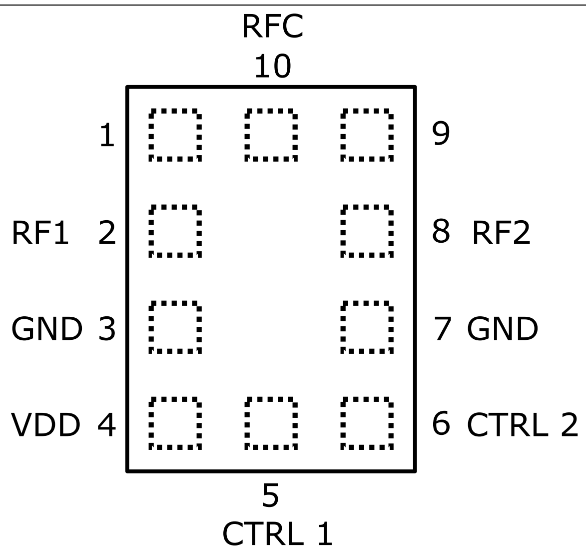

Figure 6: BGSA11GN10 Pin Configuration (top view)

Table 9: Pin Definition and Function

Pin No.	Name	Function
1	N.C.	Not connected
2	RF1	RF1 port
3	GND	Ground
4	VDD	Power Supply
5	CTRL1	GPIO digital control line
6	CTRL2	GPIO digital control line
7	GND	Ground
8	RF2	RF2 port
9	N.C.	Not connected
10	RFC	Common RF

8 Application Examples

The BGSA11GN10 is a dual single pole single throw (SPST) RF switch in a 1.05 mm x 1.55 mm TSNP-10-1 package. Both SPST can be controlled individually by the control placed next to each other. This solution allows the use of the device for several applications shown in Fig. 7:

- Low R_{ON} = 1Ω SPST (a) or ultra low R_{ON} = 0.5Ω SPST (b)
- Tuning with 2 reactive devices such as capacitors or inductors. (c)
- Combinations of above.

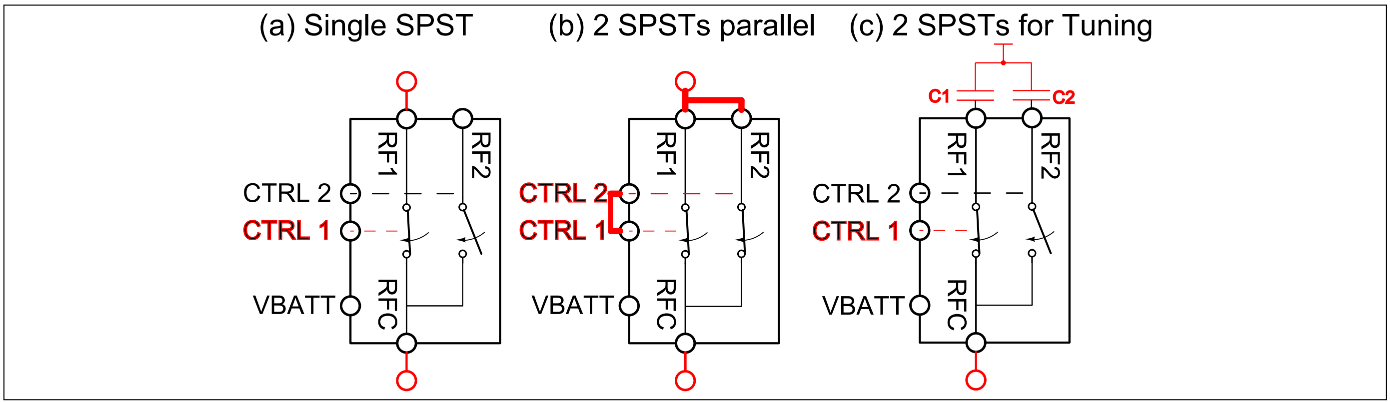

Figure 7: BGSA11GN10 realizable circuit configurations

Single SPST shunt operation

The configuration (a) is used to obtain an R_{ON} = 1Ω and C_{OFF} = 250fF. It can be used for series and shunt configurations. Note, that for single SPST shunt configuration, is is better to connect RFC to GND to avoid additional capacitance contribution of the unused part RF2 to GND as shown in Fig. 8. For simplicity, connecting the unused RF and Control Pin can be connected to ground.

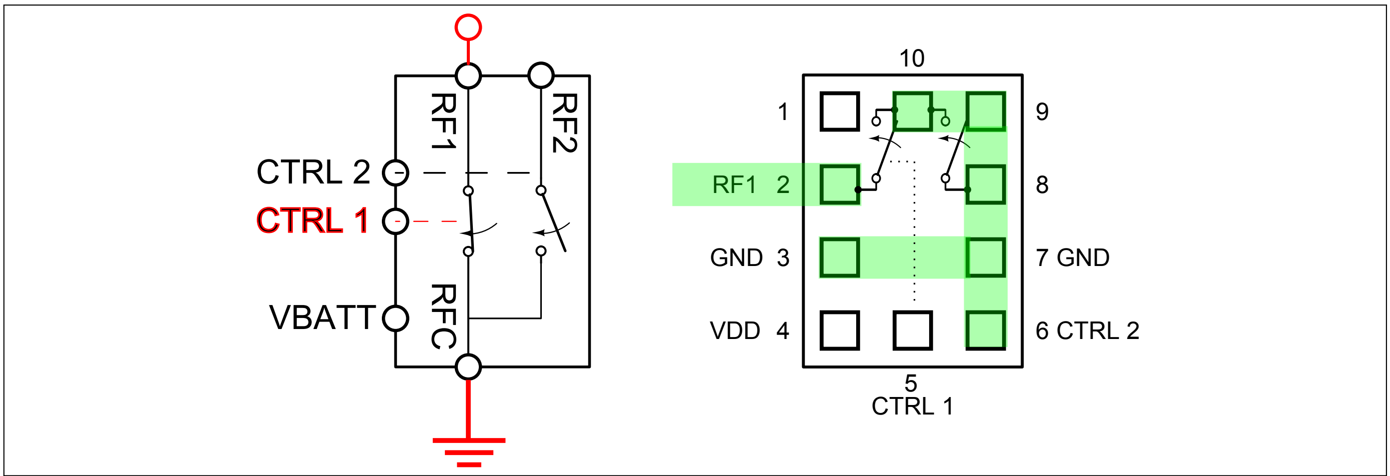

Figure 8: BGSA11GN10 single SPST shunt configuration

Low R_{ON} SPST shunt operation

For lowest possible R_{ON} = 0.5Ω operation, it is required to connect the logic inputs CTRL 1 with CTRL 2 together and same for RF1 and RF2 as shown in Fig. 9

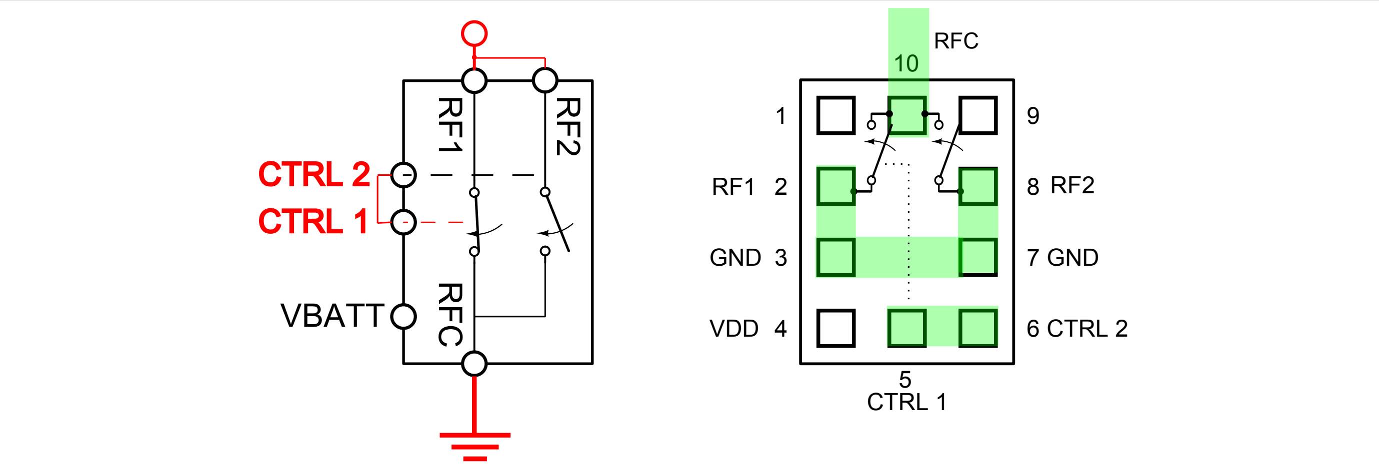

Figure 9: BGSA11GN10 low R_{ON} SPST shunt configuration

Dual SPST for RF tuning

The dual SPST can also be used for tuning applications, for example to tune capacitance or inductance. Fig. 10 shows as example a tunable capacitance with 4 steps by using 2 external MLCC capacitors. Note that the RF voltage should not exceed the specified 36 V over the switch device and also not for the used capacitor.

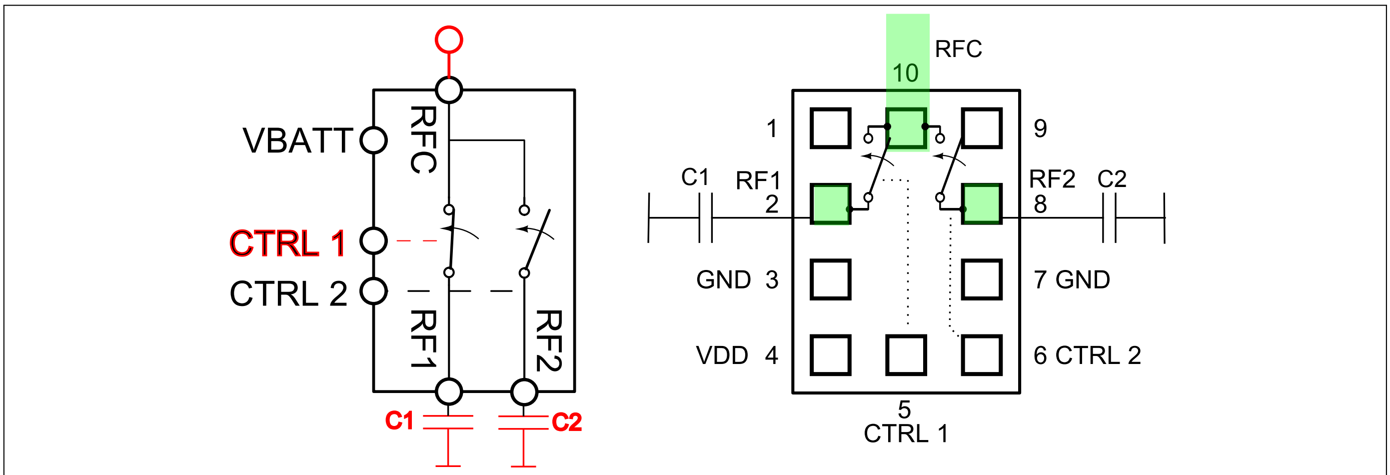

Figure 10: BGSA11GN10 as shunt capacitance tuning device

For example, resulting capacitances using C1 and C2 can be controlled as shown in table 10. Resulting Q factors can be calculated using the R_{ON} values using the equation $Q = \frac{\frac{1}{\omega C}}{R_{ON}}$ with $\omega = 2\pi f$. Same function can be realized also with inductors (Fig. 11) with $Q = \frac{\omega L}{R_{ON}}$ in table 11.

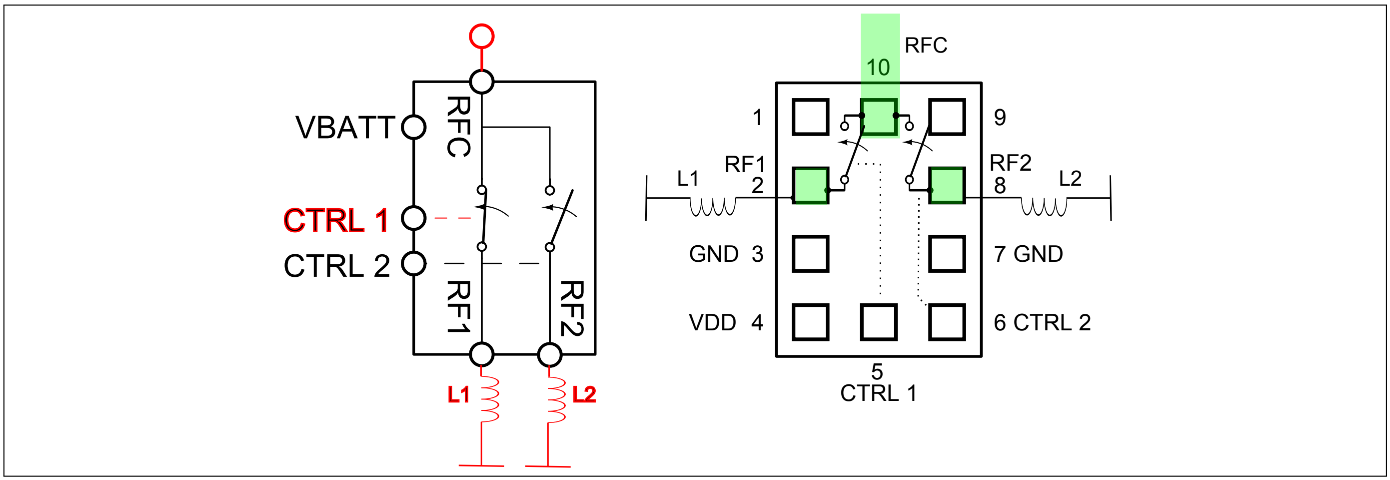

Figure 11: BGSA11GN10 as shunt inductance tuning device

Table 10: Logic Table

CTRL 1	**CTRL 2**	**Mode RF1 to RFc**	**Mode RF2 to RFc**	Capacitance	R_{ON}
0	0	OFF	OFF	500 fF	500 kΩ
0	1	OFF	ON	250 fF + C2	1 Ω
1	0	ON	OFF	250 fF + C1	1 Ω
1	1	ON	ON	C1 + C2	0,5 Ω

Table 11: Logic Table

CTRL 1	**CTRL 2**	**Mode RF1 to RFc**	**Mode RF2 to RFc**	Inductance	R_{ON}
0	0	OFF	OFF	-	500 kΩ
0	1	OFF	ON	L2	1 Ω
1	0	ON	OFF	L1	1 Ω
1	1	ON	ON	L1 || L2	0,5 Ω

9 Package Information

Table 12: Mechanical Data

Parameter	Symbol	Value	Unit
X-Dimension	*X*	1.1 ± 0.05	*mm*
Y-Dimension	*Y*	1.5 ± 0.05	*mm*
Size	*Size*	2.25	mm^2
Height	*H*	0.375 +0.025/−0.015	*mm*

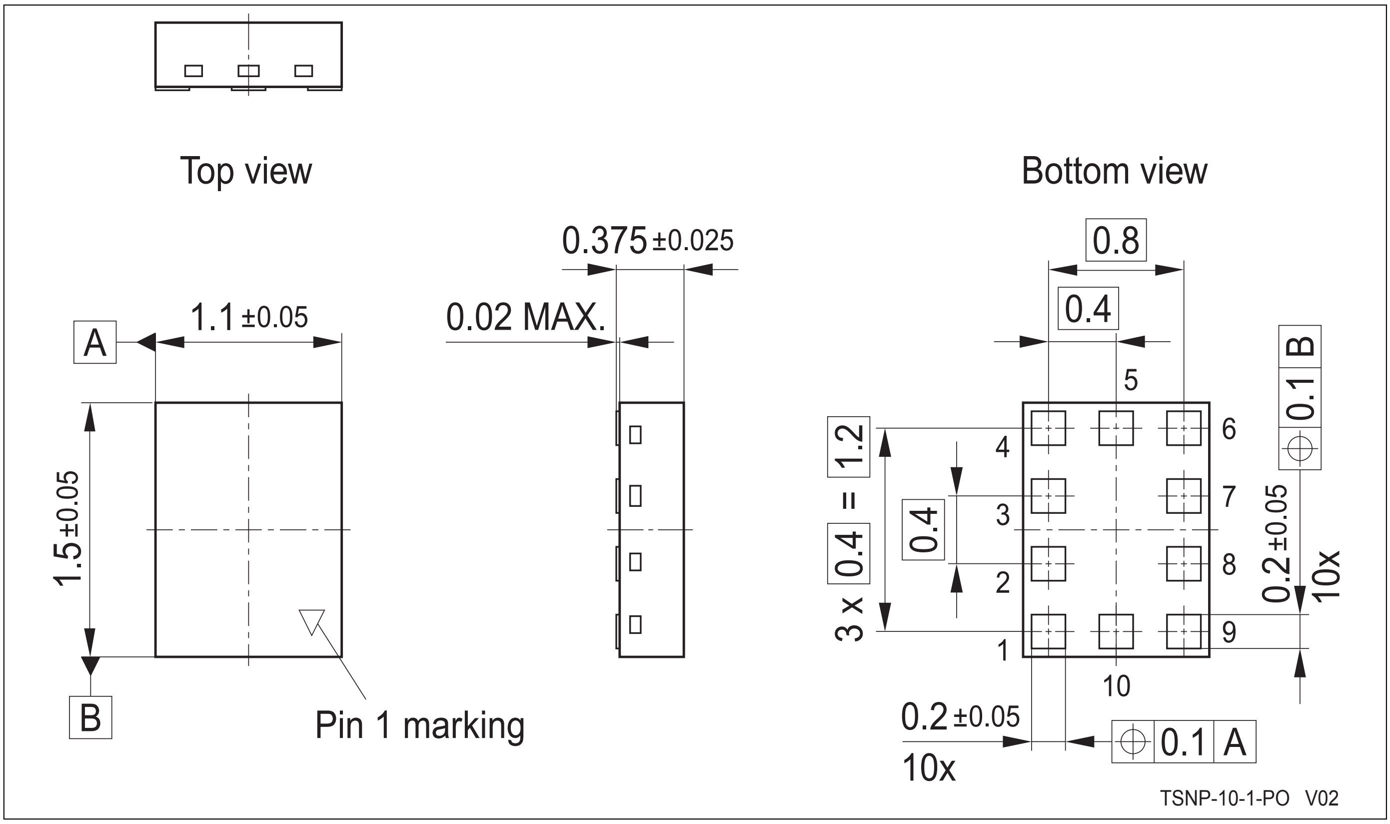

Figure 12: TSNP-10-1 Package Outline (top, side and bottom views)

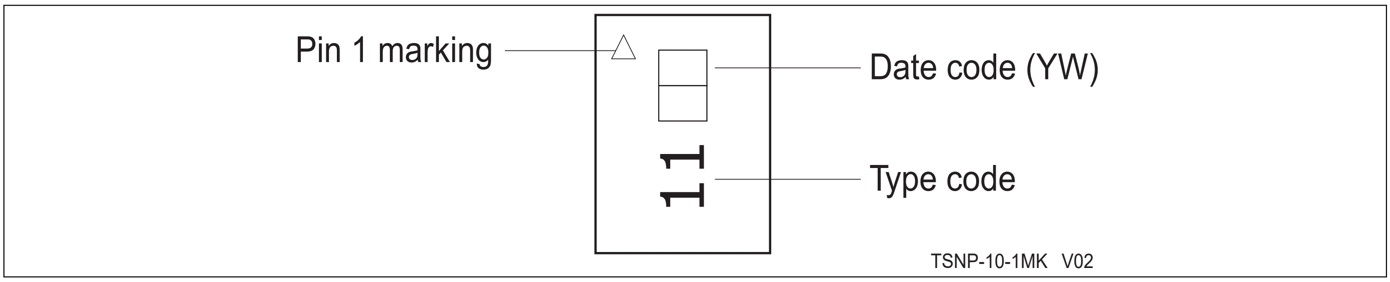

Figure 13: TSNP10-1 Marking Specification (top view): Date code digits Y and W defined in Table 13/14

Table 13: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"	Year	"Y"
2010	0	2020	0	2030	0
2011	1	2021	1	2031	1
2012	2	2022	2	2032	2
2013	3	2023	3	2033	3
2014	4	2024	4	2034	4
2015	5	2025	5	2035	5
2016	6	2026	6	2036	6
2017	7	2027	7	2037	7
2018	8	2028	8	2038	8
2019	9	2029	9	2039	9

Table 14: Week date code marking - digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s	53	M
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

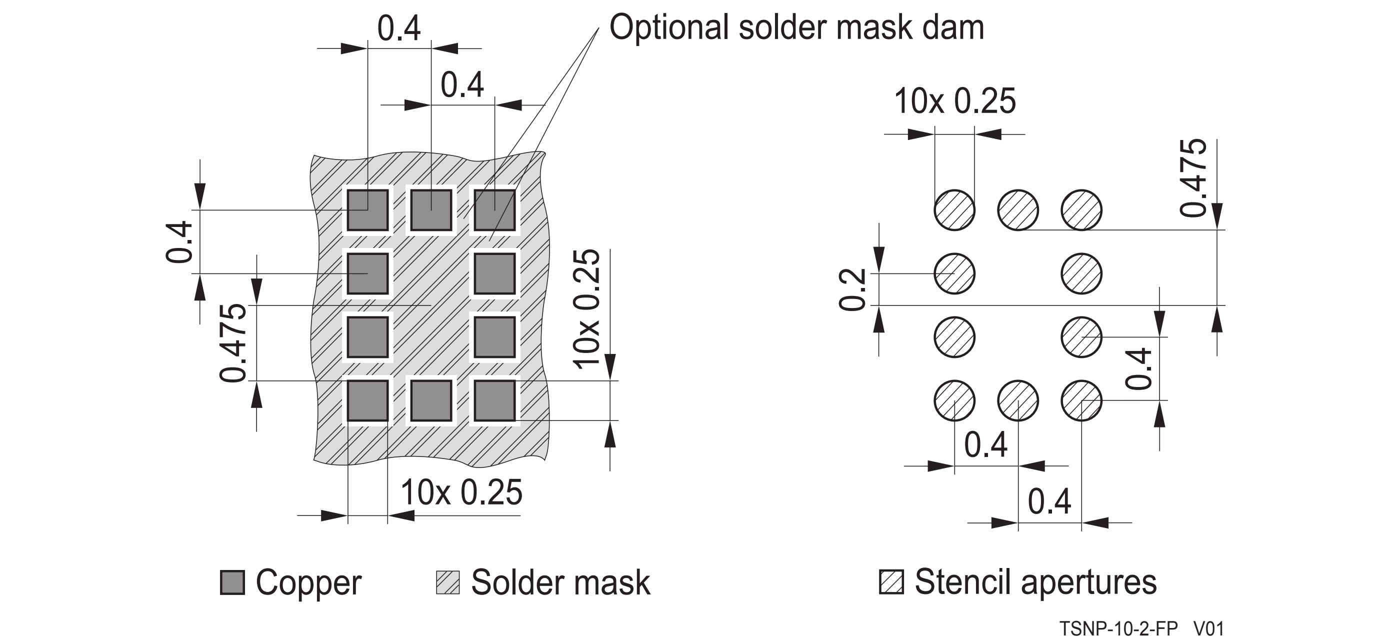

Figure 14: Land pattern and stencil mask (TSNP-10-1)

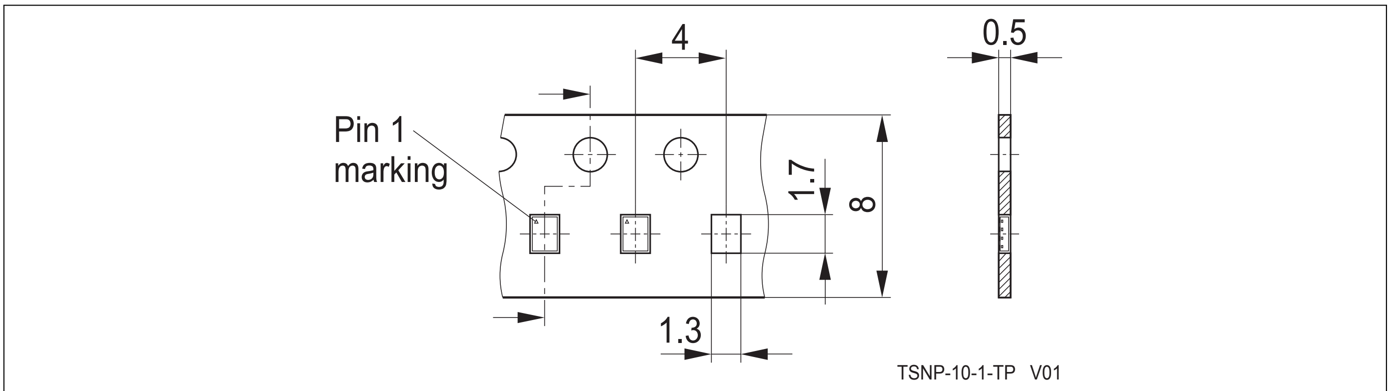

Figure 15: Carrier Tape (TSNP-10-1)

Revision History	
Creation of document Revision 3.2, 2020-07-08	
Page or Item	**Subjects (major changes since previous revision)**
5	Typo at max. control current high corrected

Edition 2020-07-08
Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about any aspect of this document?
Email: erratum@infineon.com

Document reference
Doc_Number