

# MOSFET - Power, Single P-Channel, SO8-FL

**-30 V, 1.8 mΩ, -234 A**

## NVMFS003P03P8Z

### Features

- Ultra Low  $R_{DS(on)}$  to Improve System Efficiency
- Advanced Package Technology in 5x6mm for Space Saving and Excellent Thermal Conduction
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Power Load Switch
- Protection: Reverse Current, Over Voltage, and Reverse Negative Voltage
- Battery Management

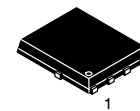
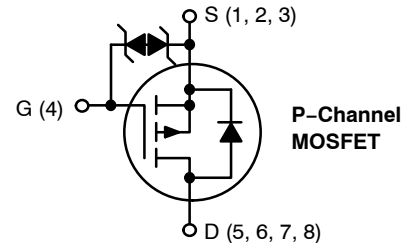
### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DSS}$	-30	V	
Gate-to-Source Voltage		$V_{GS}$	$\pm 25$	V	
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$	-234	A
		$T_C = 100^\circ\text{C}$		-169	
Power Dissipation $R_{\theta JC}$ (Note 2)		$T_C = 25^\circ\text{C}$	$P_D$	168.7	W
		$T_C = 100^\circ\text{C}$		84.4	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	-35.7	A
		$T_A = 100^\circ\text{C}$		-25.7	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		$T_A = 25^\circ\text{C}$	$P_D$	3.9	W
		$T_A = 100^\circ\text{C}$		1.9	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$	-900	A	
Single Pulse Drain-to-Source Avalanche Energy ( $I_{Lpk} = 37.1 \text{ A}$ )		$E_{AS}$	186	mJ	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260	$^\circ\text{C}$	

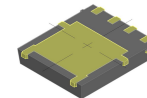
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using a 1 in<sup>2</sup> pad size, 2 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

$V_{(BR)DSS}$	$R_{DS(on)}$	$I_D$
-30 V	1.8 mΩ @ -10 V	-234 A
	2.9 mΩ @ -4.5 V	

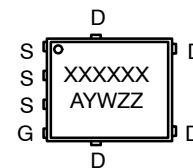


DFN5 5x6, 1.27P (SO-8FL)  
CASE 488AA



DFNW5 5x6 (FULL-CUT SO8FL WF)  
CASE 507BA

### MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

# NVMFS003P03P8Z

## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Drain) (Note 1)	$R_{\theta JC}$	0.9	$^{\circ}C/W$
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	39	$^{\circ}C/W$

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0 V, I_D = -250 \mu A$	-30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250 \mu A, \text{ref to } 25^{\circ}C$		-5		$mV/^{\circ}C$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0 V, V_{DS} = -30 V, T_J = 25^{\circ}C$			-10	$\mu A$
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0 V, V_{GS} = \pm 25 V$			$\pm 10$	$\mu A$

## ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250 \mu A$	-1.0		-3.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = -250 \mu A, \text{ref to } 25^{\circ}C$		5.5		$mV/^{\circ}C$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -10 V, I_D = -23 A$		1.2	1.8	$m\Omega$
		$V_{GS} = -4.5 V, I_D = -20 A$		1.9	2.9	
Forward Transconductance	$g_{FS}$	$V_{DS} = -5 V, I_D = -20 A$		110		S

## CHARGES AND CAPACITANCES

Input Capacitance	$C_{iss}$	$V_{GS} = 0 V, V_{DS} = -15 V, f = 1.0 \text{ MHz}$		12120		$pF$
Output Capacitance	$C_{oss}$			4020		
Reverse Transfer Capacitance	$C_{rss}$			4100		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5 V, V_{DS} = -15 V, I_D = -23 A$		167		$nC$
Threshold Gate Charge	$Q_{G(TH)}$			7		
Gate-to-Source Charge	$Q_{GS}$			21		
Gate-to-Drain Charge	$Q_{GD}$			116		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -10 V, V_{DS} = -15 V, I_D = -23 A$		277		

## SWITCHING CHARACTERISTICS, $V_{GS} = 4.5 V$ (Note 3)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -4.5 V, V_{DS} = -15 V, I_D = -23 A, R_G = 6 \Omega$		81		ns
Rise Time	$t_r$			440		
Turn-Off Delay Time	$t_{d(off)}$			180		
Fall Time	$t_f$			400		

## SWITCHING CHARACTERISTICS, $V_{GS} = 10 V$ (Note 3)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -10 V, V_{DS} = -15 V, I_D = -23 A, R_G = 6 \Omega$		28		ns
Rise Time	$t_r$			116		
Turn-Off Delay Time	$t_{d(off)}$			325		
Fall Time	$t_f$			380		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0 V, I_S = -23 A$	$T_J = 25^{\circ}C$	-0.75	-1.3	V
			$T_J = 125^{\circ}C$	-0.6		

# NVMFS003P03P8Z

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>s</sub> /dt = 100 A/μs, I <sub>s</sub> = -23 A		70		ns
Charge Time	t <sub>a</sub>			43		
Discharge Time	t <sub>b</sub>			28		
Reverse Recovery Charge	Q <sub>RR</sub>			116		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

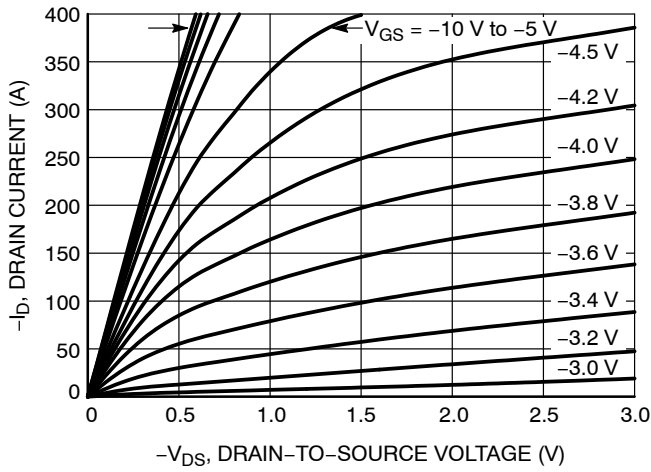


Figure 1. On-Region Characteristics

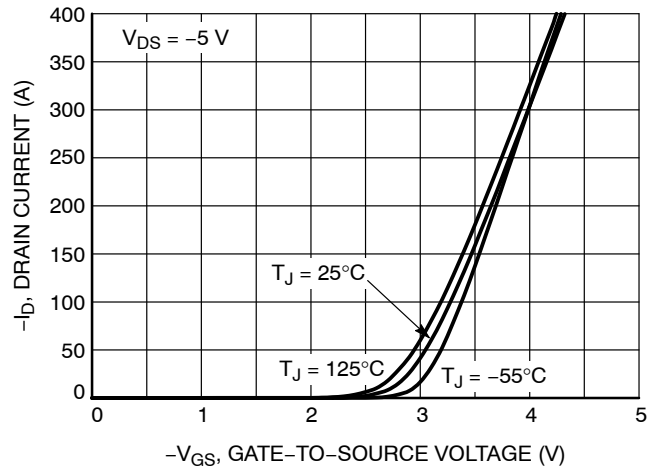


Figure 2. Transfer Characteristics

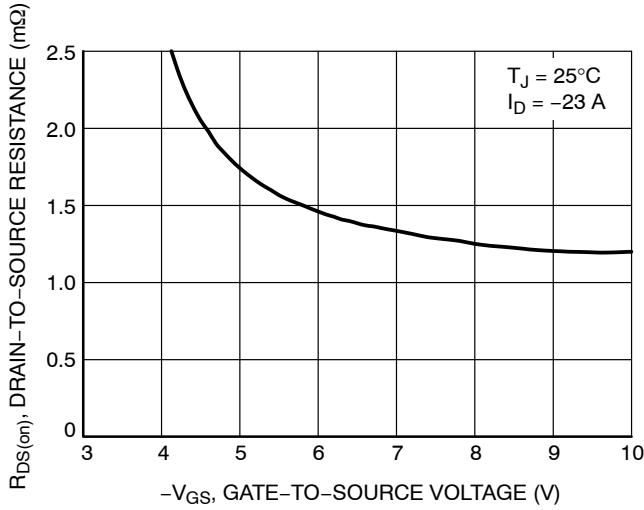


Figure 3. On-Resistance vs. Gate-to-Source Voltage

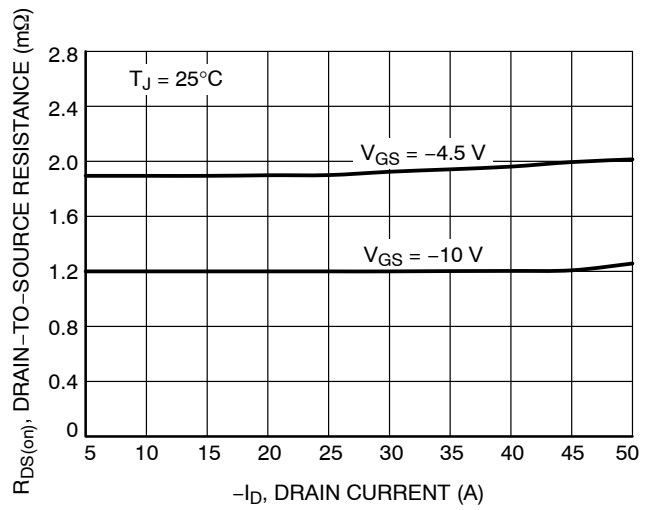


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

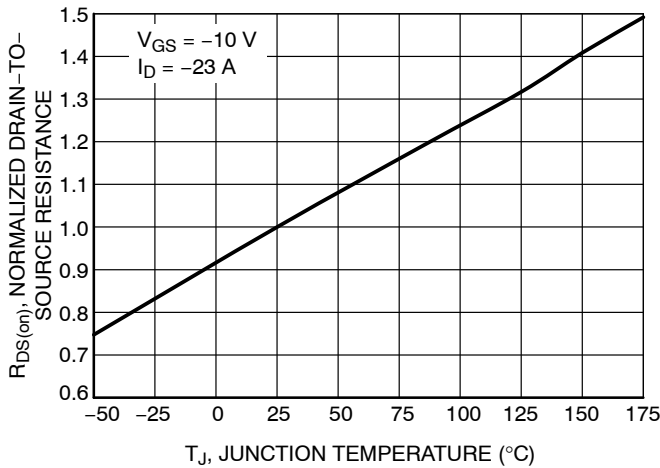


Figure 5. On-Resistance Variation with Temperature

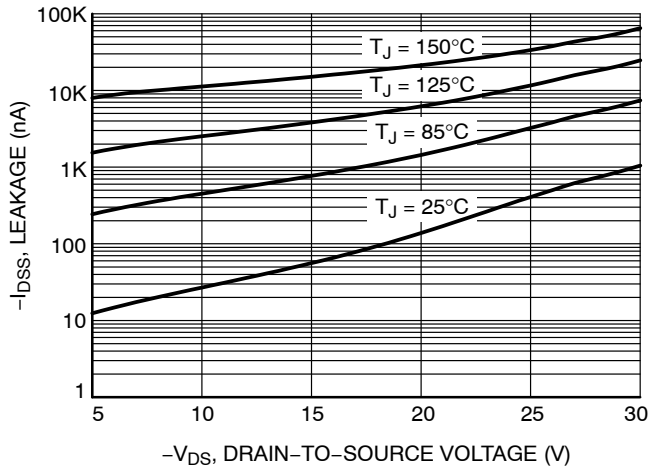


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

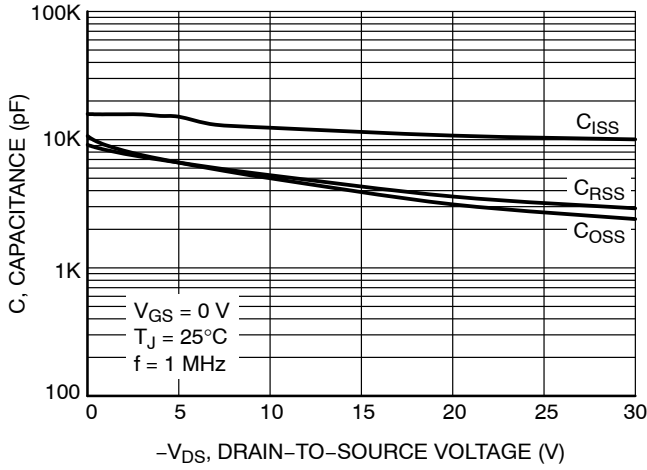


Figure 7. Capacitance Variation

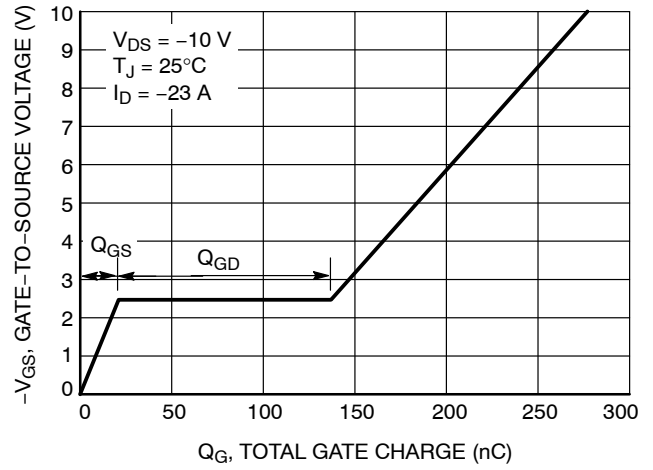


Figure 8. Gate-to-Source Voltage vs. Total Charge

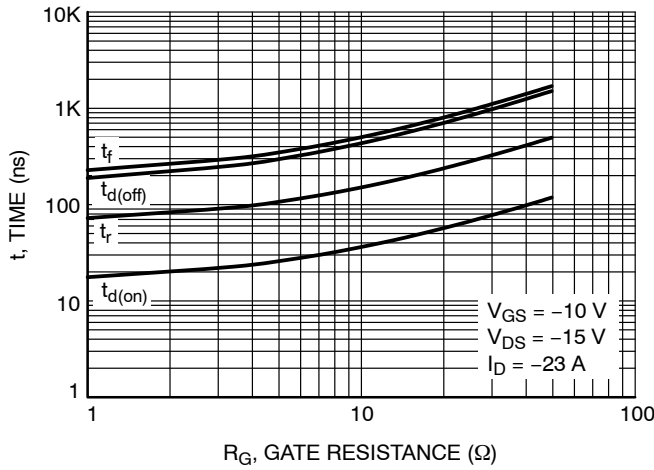


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

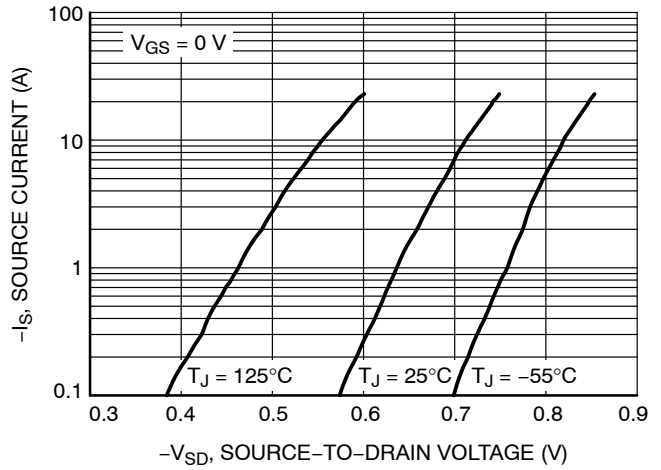


Figure 10. Diode Forward Voltage vs. Current

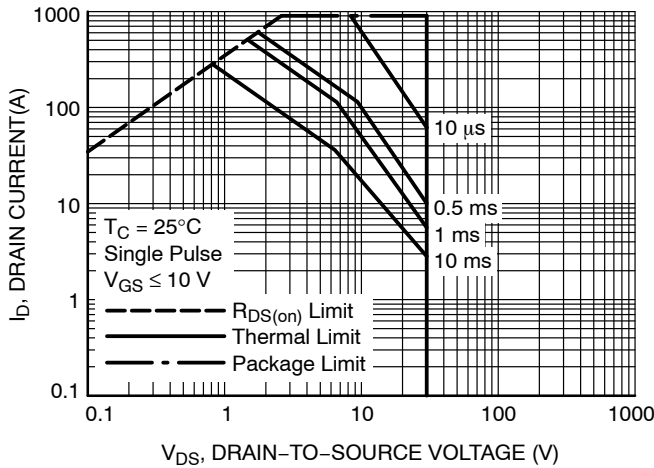


Figure 11. Maximum Rated Forward Biased Safe Operating Area

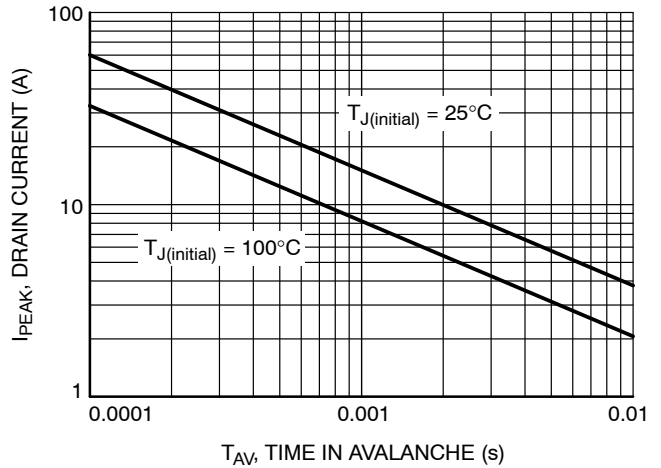


Figure 12.  $I_{PEAK}$  vs. Time in Avalanche

# NVMFS003P03P8Z

## TYPICAL CHARACTERISTICS

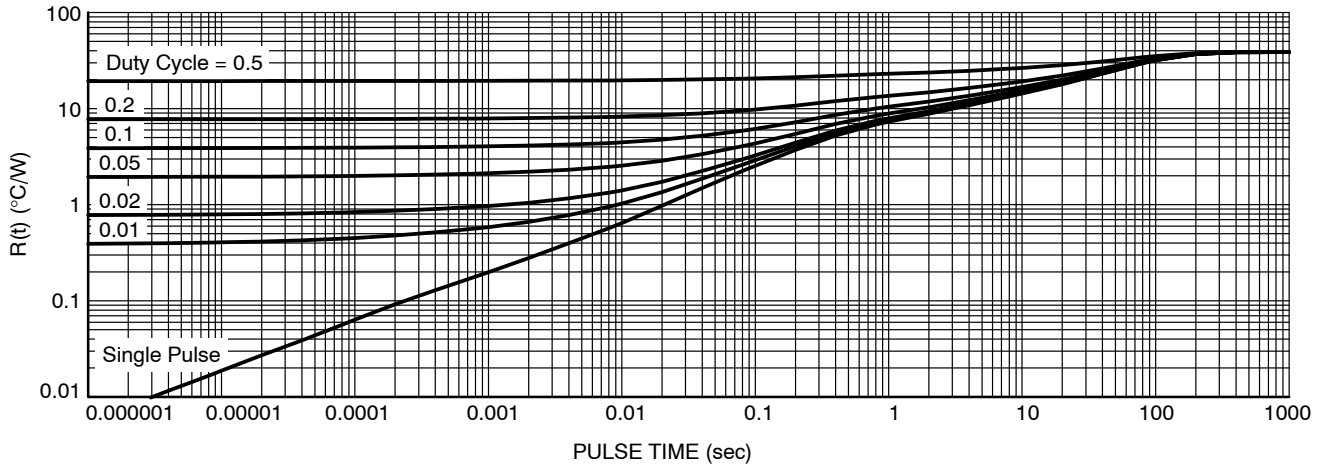


Figure 13. Thermal Characteristics

### PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Shipping <sup>†</sup>
NVMFS003P03P8ZT1G	03P3	DFN5 5x6, 1.27P (Pb-Free)	1500 / Tape & Reel
NVMFWS003P03P8ZT1G	03P3W	DFNW5, 5x6 (FULL-CUT SO8FL WF) (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



1  
SCALE 2:1

DFN5 5x6, 1.27P  
(SO-8FL)  
CASE 488AA  
ISSUE N

DATE 25 JUN 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

### GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



- STYLE 1:  
PIN 1. SOURCE  
2. SOURCE  
3. SOURCE  
4. GATE  
5. DRAIN
- STYLE 2:  
PIN 1. ANODE  
2. ANODE  
3. ANODE  
4. NO CONNECT  
5. CATHODE

DIMENSIONS: MILLIMETERS

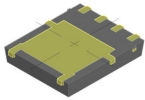
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN5 5x6, 1.27P (SO-8FL)	PAGE 1 OF 1

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

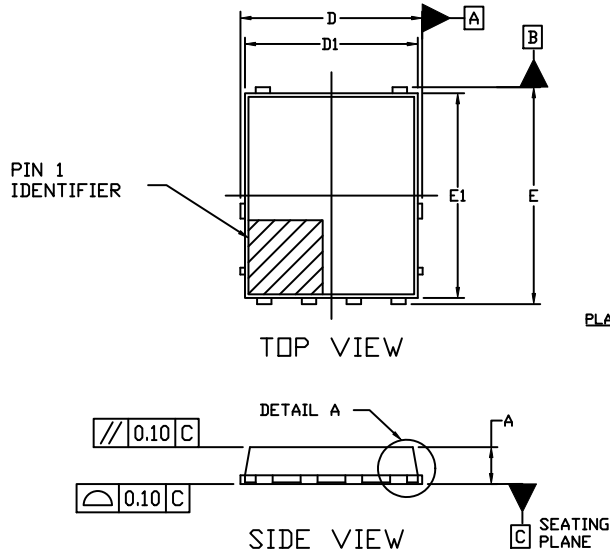


### DFNW5 5x6 (FULL-CUT SO8FL WF)

#### CASE 507BA

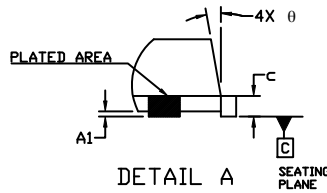
#### ISSUE A

DATE 03 FEB 2021

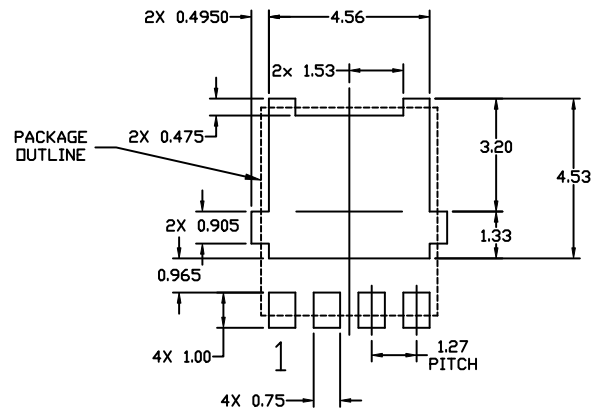
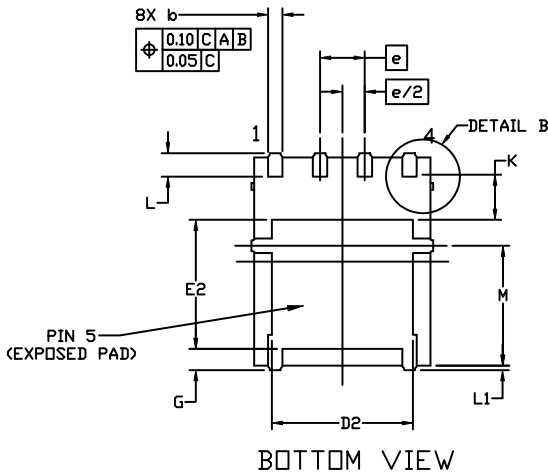
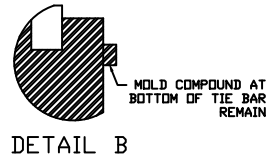


**NOTES:**

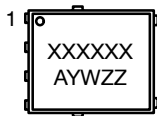
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.150 REF		
M	3.00	3.40	3.80
θ	0°	---	12°



### GENERIC MARKING DIAGRAM\*



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 A = Assembly Location  
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- \*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

**RECOMMENDED MOUNTING FOOTPRINT**

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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