Digital Phase Shifter, 4-Bit, 3.5 - 6.0 GHz

MAPS-010145
Rev. V4

Features

- 4 Bit Digital Phase Shifter
- 360° Coverage with LSB = 22.5°
- Integrated CMOS Driver
- Serial or Parallel Control
- Low DC Power Consumption
- Minimal Attenuation Variation over Phase Shift Range
- 50 Ω Impedance
- EAR99
- Lead-Free 4 mm 24-Lead PQFN Package
- RoHS* Compliant
- Bidirectional

Applications

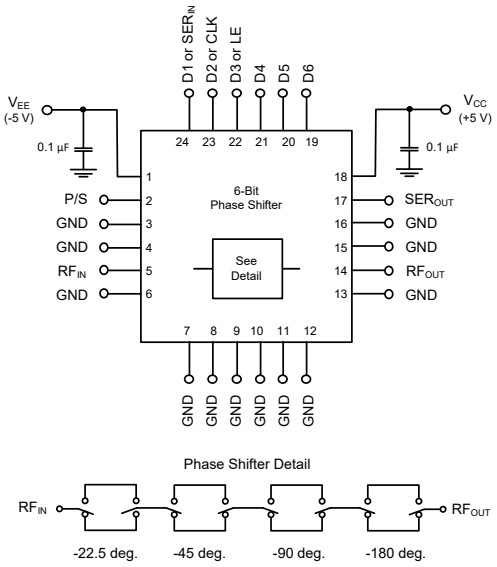
- Aerospace & Defense
- Wireless Networking & Communication...

Description

The MAPS-010145 is a GaAs pHEMT 4-bit digital phase shifter with an integrated CMOS driver in a 4 mm PQFN plastic surface mount package. Step size is 22.5° providing phase shift from 0° to 360° in 22.5° steps. This design has been optimized to minimize variation in attenuation over the phase shift range.

The MAPS-010145 is ideally suited for use where high phase accuracy with minimum loss variation over the phase shift range are required. The 4 mm PQFN package provides a smaller footprint than is typically available for a digital phase shifter with an internal driver. Typical applications include communications antennas and phased array radars.

Functional Schematic



Pin Configuration[2]

Pin #	Function	Pin #	Function
1	V_{EE}	13	GND
2	P/S	14	RF_{OUT}
3	GND	15	GND
4	GND	16	GND
5	RF_{IN}	17	SER_{OUT}
6	GND	18	V_{CC}
7	GND	19	D6
8	GND	20	D5
9	GND	21	D4
10	GND	22	D3 or LE
11	GND	23	D2 or CLK
12	GND	24	D1 or SER_{IN}

2. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

Ordering Information[1]

Part Number	Package
MAPS-010145-TR0500	500 piece reel
MAPS-010145-001SMB	Sample Test Board

1. Reference Application Note M513 for reel size information.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications:

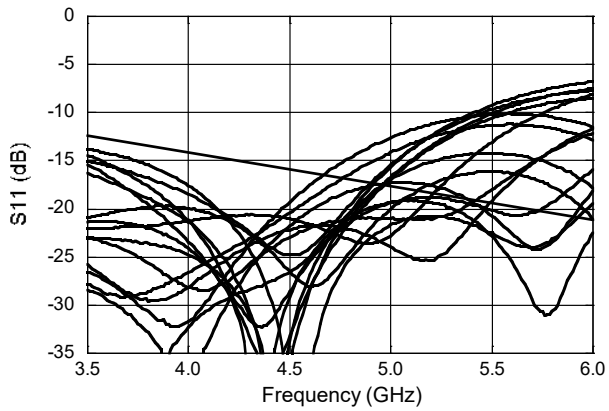
Freq. = 3.5 - 6.0 GHz, T_A = 25°C, Z_0 = 50 Ω, V_{CC} = +5.0 V, V_{EE} = -5.0 V

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Operating Power [3]	3.5 - 6.0 GHz	dBm	—	—	+25
Insertion Loss (Any Phase State)	Any Phase State	dB	—	5.0	6.5
Attenuation Variation	Across All Phase States	dB	—	± 1	—
RMS Attenuation Error [4]	All Values Relative to Insertion Loss at Reference Phase	dB	—	0.4	—
RMS Phase Error [4]	All Values Relative to Reference Phase	deg	—	3	—
Phase Accuracy [5] Relative to Reference Loss State	22.5 Degree Bit 45 Degree Bit 90 Degree Bit 180 Degree Bit Sum of All Bits	deg	—	± 1.7 ± 1.0 ± 2.0 ± 3.5 ± 2.5	—
VSWR	RF Input RF Output	Ratio	—	1.8:1 1.8:1	—
1 dB Compression	Reference State	dBm	—	27	—
Input IP3	Two-tone inputs up to +5 dBm	dBm	—	45	—
T_{RISE}, T_{FALL}	10% to 90% RF, 90% to 10% RF	ns	—	50	—
V_{CC} V_{EE}	—	V	3.0 -5.5	— -5.0	5.5 -3.0
V_{IL} V_{IH}	LOW-level input voltage HIGH-level input voltage	V	0.0 0.7 x V_{CC}	—	0.3 x V_{CC} V_{CC}
I_{IN} (Input Control Current)	V_{IN} = V_{CC} or GND	µA	—	1	—
V_{OH} V_{OL}	For serial out; I_{OH} = -100 µA For serial out; I_{OL} = 100 µA	V	V_{CC} - 0.2 —	—	— 0.2
I_{CC} (Quiescent Supply Current)	$V_{CONTROL}$ = V_{CC} or GND	µA	—	—	2
I_{EE}	V_{EE} min to max V_{IN} = V_{IL} or V_{IH}	mA	-1.0	-0.1	—

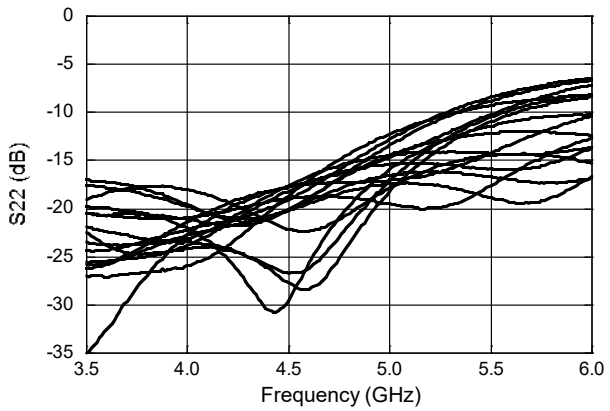
3. Maximum operating power is the maximum power where the specifications are guaranteed.
4. RMS is calculated across all 15 amplitude or phase states. Refer to application section for further discussion of this method.
5. This phase shifter is guaranteed to have monotonic phase shift.

Typical Performance Curves

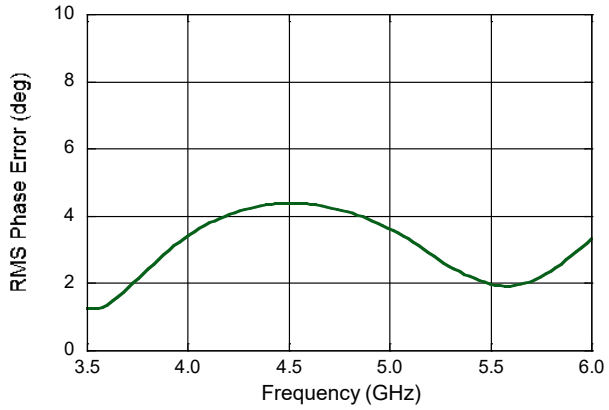
RF_{IN} Return Loss vs. Frequency (All States)



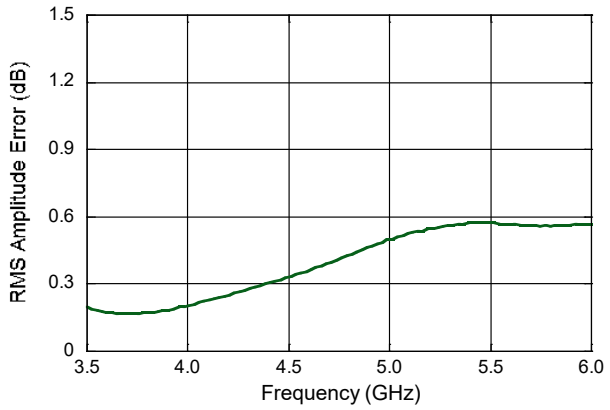
RF_{OUT} Return Loss vs. Frequency (All States)



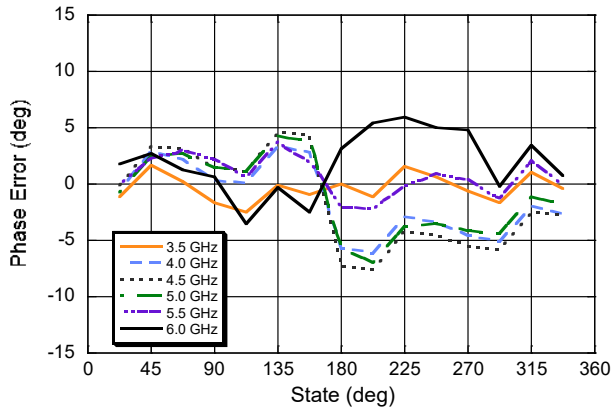
RMS Phase Error vs. Frequency[5]



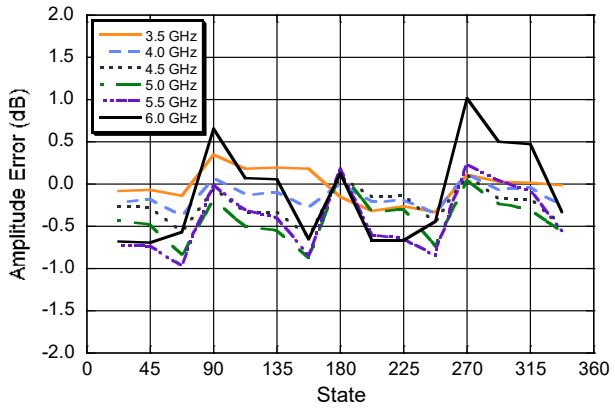
RMS Amplitude Error vs. Frequency (0 degree state reference)[5]



Phase Error (degrees) vs. State

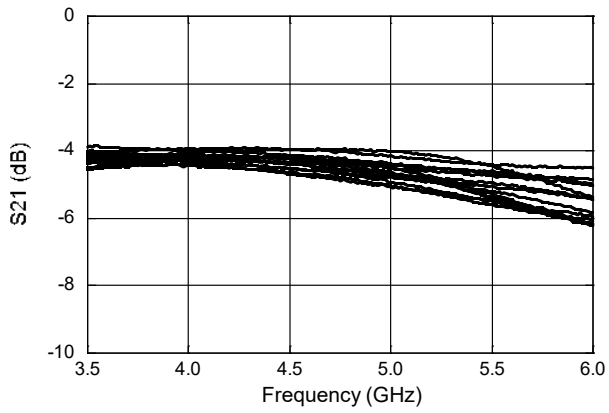


Amplitude Error (dB) vs. State

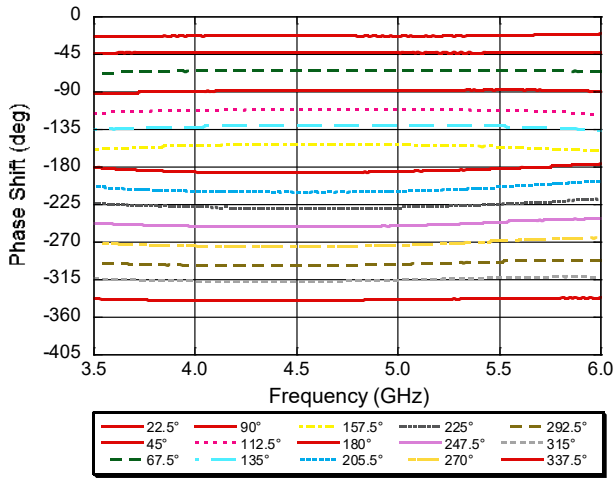


Typical Performance Curves

Amplitude Variation vs. Phase State



Phase Shift vs. Frequency (Major States)

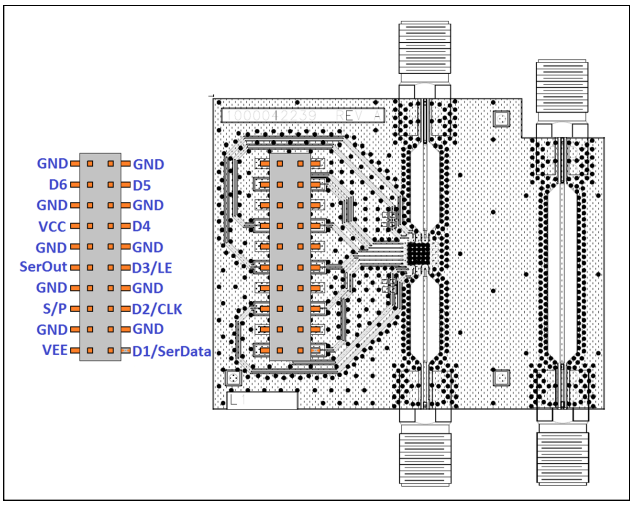


Absolute Maximum Ratings[6,7]

Parameter	Absolute Maximum
Input Power 3.5 - 6.0 GHz	27 dBm
V_{CC}	-0.5 V ≤ V_{CC} ≤ +7.0 V
V_{EE}	-7.0 V ≤ V_{EE} ≤ +0.5 V
D1-D4, P/S, LE, CLK or SER IN	-0.5 V ≤ V_{IN} ≤ V_{CC} + 0.5 V
SER OUT	-0.5 V ≤ V_{OUT} ≤ V_{CC} + 0.5 V
Operating Temperature	-40ºC to +85ºC
Storage Temperature	-65ºC to +150ºC

6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. MACOM does not recommend sustained operation near these survivability limits.

Sample Board Header Pin Labels[8]



8. Sample board CAD files available by request.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide and Silicon Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Modes of Operation: Serial and Direct Parallel

Serial Mode

The serial control interface (SERIN, CLK, LE, SEROUT) is compatible with the SPI protocol. SPI mode is activated when P/S is kept high. The 6-bit serial word must be loaded with the MSB first. After shifting in the 6 bit word, a rising edge on LE will set the phase shifter to the desired state. While LE is high the CLK is masked to protect the data while implementing the change. SEROUT is SERIN delayed by 6 clock cycles.

When P/S is low, the serial control interface is disabled. When P/S is set high, Pins 22, 23, and 24 have the LE, CLK, and SER IN function.

In serial mode operation, the outputs will stay constant while LE is kept low.

Direct Parallel Mode

The parallel mode is enabled when P/S is set low. In the direct parallel mode, the phase shifter is controlled by the parallel control inputs directly. When P/S is set low, Pins 22, 23, and 24 have the D3, D2, and D1 function.

Mode Truth Table[9,10]

P/S	LE	Mode
1	X	Serial
0	N/A	Direct Parallel

9. There are two dummy bits (D1 & D2), that must be sent in the serial mode. This is because the 4 bit phase shifter uses the same driver as the 6 bit phase shifter.
10. In the parallel mode, D1 and D2 should be tied to ground or to V_{CC}.

Truth Table (Digital Phase Shifter)[11]

D6	D5	D4	D3	D2	D1	Phase Shift
0	0	0	0	X	X	Reference Phase
0	0	0	1	X	X	22.5°
0	0	1	0	X	X	45°
0	1	0	0	X	X	90°
1	0	0	0	X	X	180°
1	1	1	1	X	X	337.5°

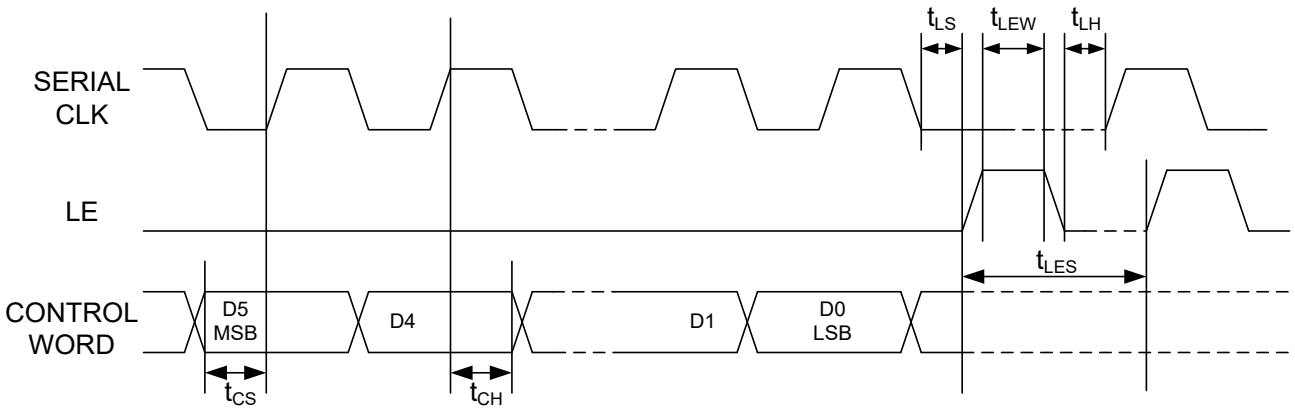
11. 0 = CMOS Low; 1 = CMOS High, X is CMOS Low or High.

Serial Interface Timing Characteristics

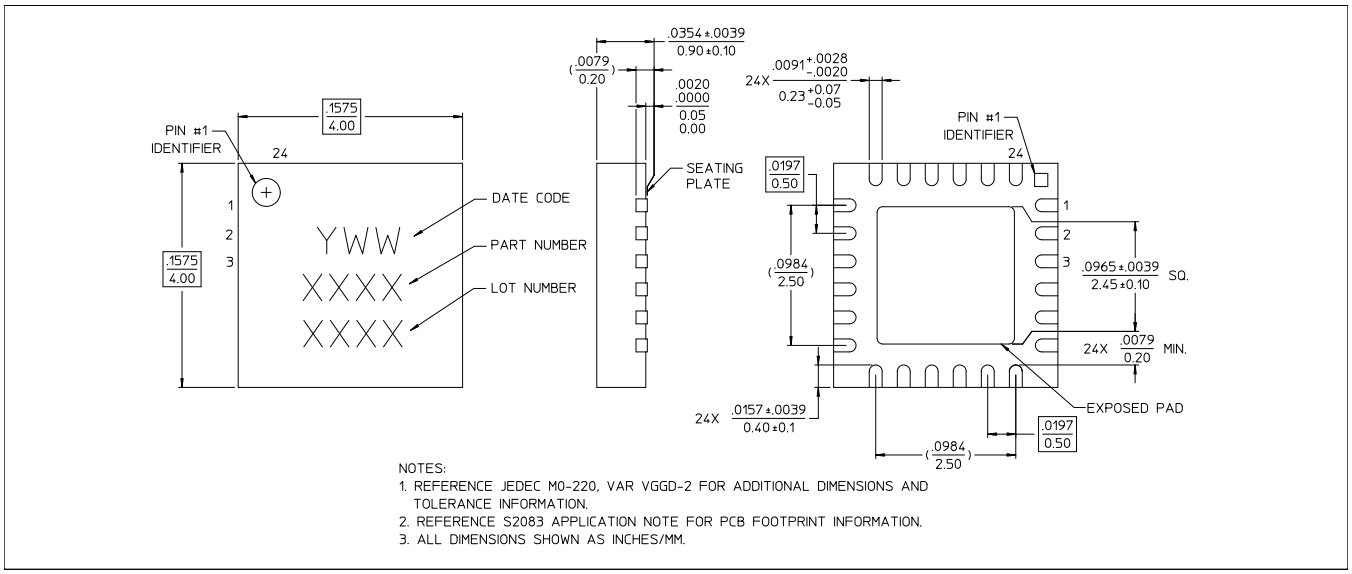
Symbol	Parameter	Typical Performance			Units
		-40°C	25°C	+85°C	
t_{SCK}	Min. Serial Clock Period	100	100	100	ns
t_{CS}	Min. Control Set-up Time	20	20	20	ns
t_{CH}	Min. Control Hold Time	20	20	20	ns
t_{LS}	Min. LE Set-up Time	10	10	10	ns
t_{LEW}	Min. LE Pulse Width	10	10	10	ns
t_{LH}	Min. Serial Clock Hold Time from LE	10	10	10	ns
t_{LES}	Min. LE Pulse Spacing	630	630	630	ns

Functionality
Modes of Operation: Serial and Direct Parallel

Serial Input Interface Timing Diagram



Lead Free 4 mm 24-Lead PQFN †



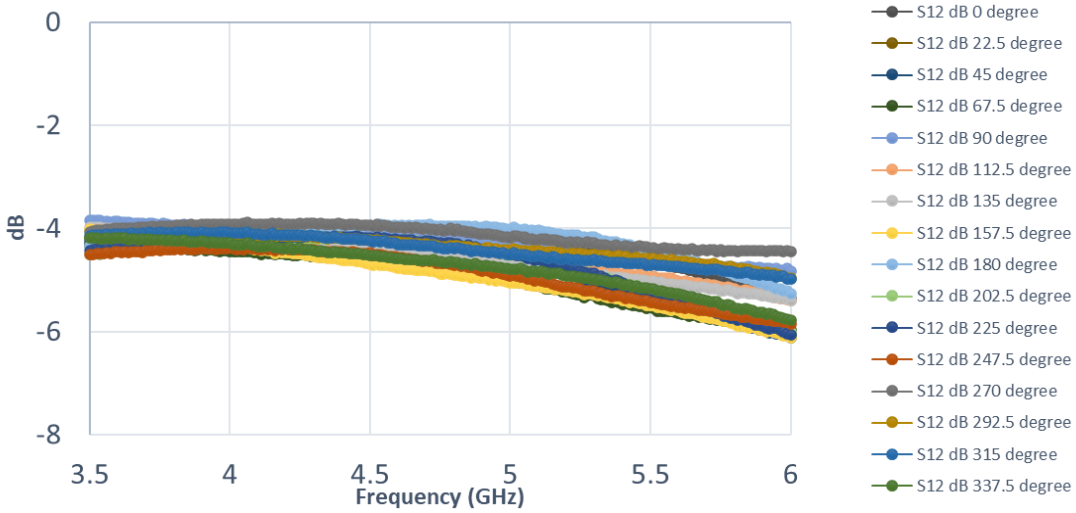
† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.
Plating is 100% matte tin over copper.

Application Section

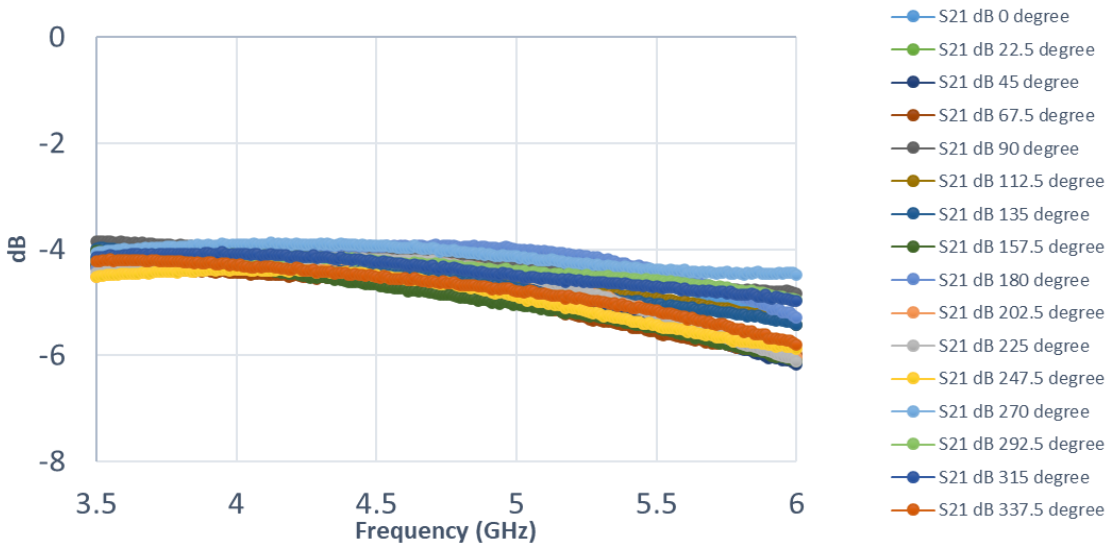
Phase shifters such as this product are bidirectional. All prior data in the datasheet shows S(2,1), but the following pages illustrate typical S(1,2) performance.

By inspection of the posted S-Parameters, one can observe that this device will work bidirectionally. Considering the MMIC topology, this is an expected feature.

Insertion Loss (S12), All States



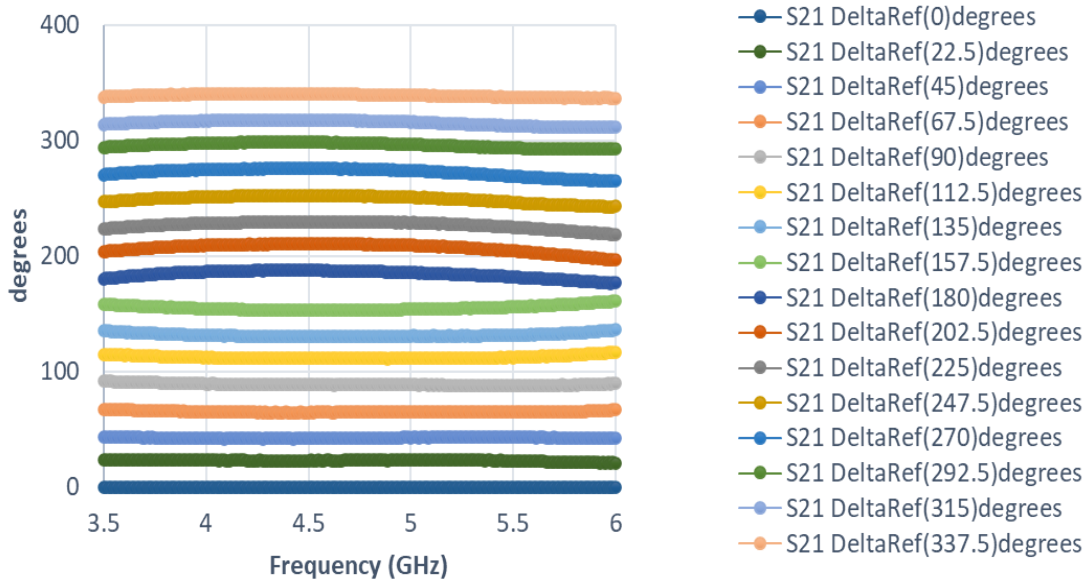
Insertion Loss (S21), All States



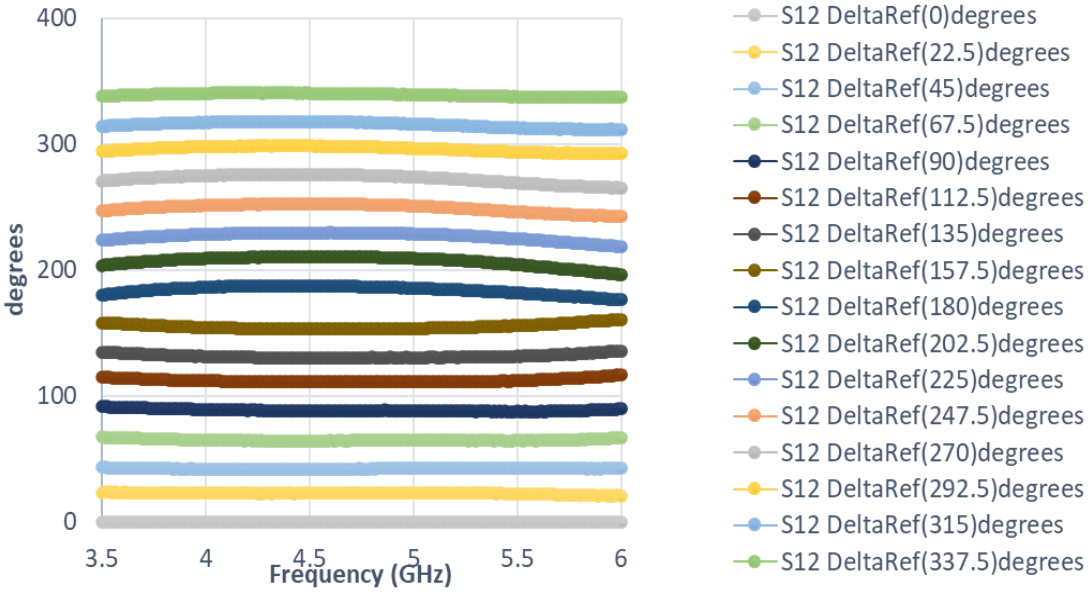
Application Section

Below is a comparison of unwrapped, normalized phase in both directions.

Insertion Phase (S21), All States



Insertion Phase (S12), All State



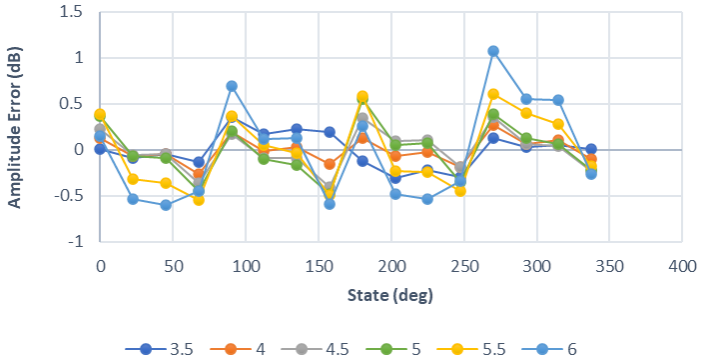
Application Section

To be complete in reviewing phase shifter performance in both directions, error metrics should be discussed.

With phase shifters, both phase and amplitude error are described. Amplitude error describes the state-to-state amplitude variation. Phase error describes the delta-from ideal phase observed in each state.

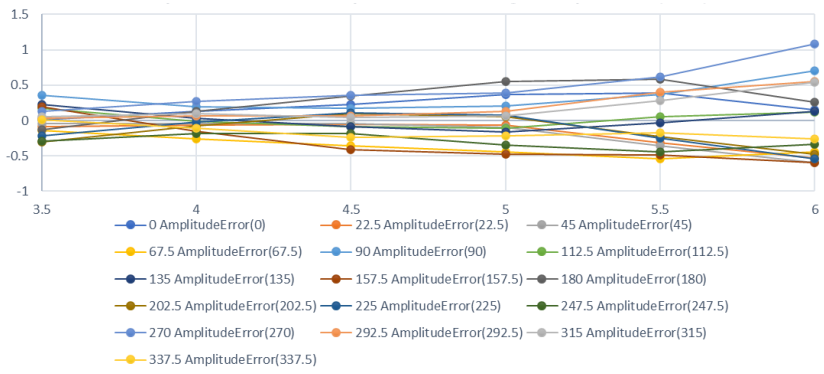
Amplitude error can be calculated in two ways. The first is with respect to the 0° or reference state. This can be called cross-error. Another, and perhaps more widely accepted method for calculating amplitude error, is to compare it by frequency to the mean amplitude of all the states as is calculated here. [1]

Amplitude Error (dB) vs. State (S12)



While the above shows amplitude error at particular frequencies vs phase shifter state, another common way to look at this parameter is error vs frequency.

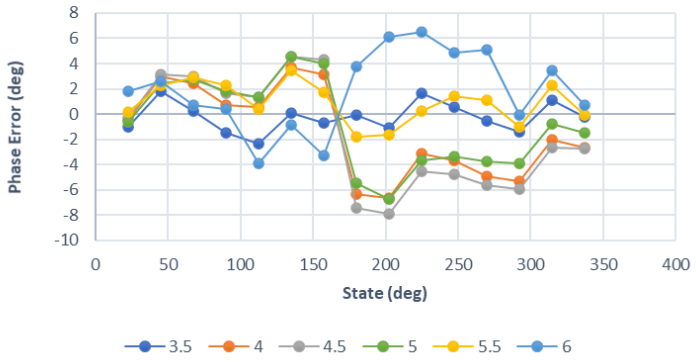
Amplitude Error Compared to Average Amplitude (S12)



Application Section

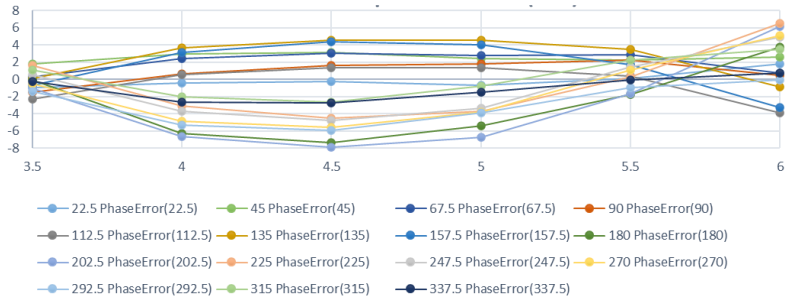
Phase error is calculated as the difference between the requested or ideal phase and actual insertion phase. For example, if 22.5° of shift is desired, and 23.5° is observed, the delta, or error, is 1°.

Phase Error (°) vs. State (S12)



Phase Error (°) vs. Frequency as shown below:

Phase Error compared to ideal (S12)



Following many traces, trying to consider how that will impact a system is difficult. A simpler method is adopted: RMS Error. It is important to use the right convention when applying an RMS calculation to phase shifter insertion phase. We compare the raw errors with the mean (error) below.

If we use only the raw phase errors in an RMS error calculation the result will be pessimistic. This is because the average of the phase errors is not typically zero. Ignoring the mean error would result in an RMS Error that differs depending on chosen reference state. [1]

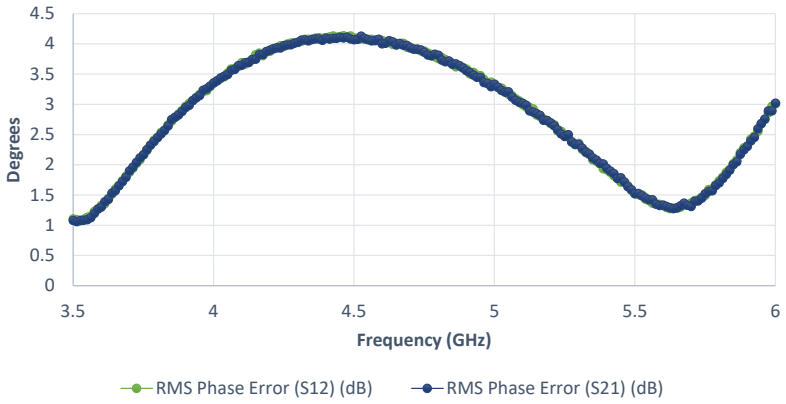
$$\delta_{phase\_rms} = \sqrt{\frac{1}{n}\sum_{m=1}^{n}\varepsilon_{phase}^{2} - \left(\frac{1}{n}\sum_{m=1}^{n}\varepsilon_{phase}\right)^{2}}$$

[1]

Application Section

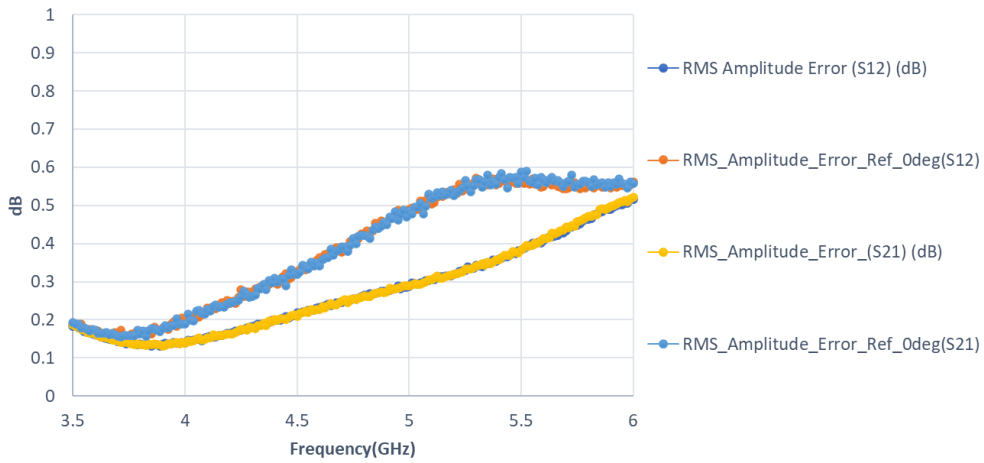
This graph shows RMS Phase Error in both directions. The traces overlay.

RMS Phase Error (S21 & S12)



For RMS Error applied to amplitude, both methods are shown below. One method derives error vs the reference (0°) state, and the other method calculates error vs the mean insertion loss. Forward and reverse conditions overlay.

RMS Amplitude Error Referencing the Average & the 0°States (S21 & S12)



References:

[1] "RMS Phase & Amplitude Calculation for Phase-shifters", 10-12-2008 T.Fattorini, MACOM DesignGuide