User's Guide

SLVU829–August 2014

TPS54122EVM-201, Low Noise 3-A Power Supply Evaluation Module

This User's Guide describes operational use of the TPS54122 Evaluation Module (PWR201) as a reference design for engineering demonstration and evaluation of the TPS54122, a low noise 3-A power supply. Included in this user's guide are setup and operation instructions, a schematic diagram, layout description, a bill of materials, and test results.

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1 Background

The Texas Instruments TPS54122 EVM (PWR201) helps design engineers evaluate the operation and performance of the TPS54122 (Switcher + LDO) for possible use in their own circuit application. This particular EVM configuration contains all of the external components required for a low noise 3A power supply solution in a 3.5mm x 5.5mm thermally enhanced QFN with a PowerPad™ . Both the switcher and the LDO have independent protection and control features such as soft start, internal current limit, thermal shutdown, power good signal, and enable circuitry.

The TPS54122 is capable of delivering a low noise supply of up to 3 A to the load and is designed to operate from an input power supply (VIN) of 2.95 V to 5.5 V when the switcher is used to power the LDO. The TPS54122 EVM provides access to the inputs of both the switcher and LDO, Vin and LDOIN, but this EVM is optimized and tested using DC-DC_Out connected to LDOIN with a minimum input voltage of 2.95V. Rated input voltages and output current ranges for the evaluation module are given in Table 1.

Table 1. EVM Specifications

Configuration	Input Voltage	Bias Voltage	SW Output Voltage	LDO Output Voltage	Output Current
Switcher Independent	2.95 V to 6 V	NA	0.8 V to 4.5 V	NA	0 to 3A
LDO Independent	$V_{(OUT)}$ + $V_{DO(LDOIN)}$ to 5.5 V	$V_{(OUT)}$ + 1.65V to 5.5 V	NA	0.8 V to 3.6 V	0 to 3A
Switcher Powering LDO	2.95 V to 5.5 V	$V_{(OUT)}$ + 1.65V to 5.5 V	$V_{(OUT)}$ + $V_{DO(LDOIN)}$ to 4.5 V	0.8 V to 3.6 V	0 to 3A

This evaluation module is designed to demonstrate the printed-circuit-board space savings that may be achieved when designing with the TPS54122 device compared to stand-alone switcher and LDO topologies. The integrated switcher (SW) and LDO are optimized to allow the TPS54122 to achieve high efficiencies and a low output noise. The compensation components are external to the integrated circuit (IC), and external resistor dividers allow for adjustable output voltages for the switcher and LDO. The switching frequency is externally controlled and these EVMs are set with a nominal switching frequency of 480 kHz.

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, setup and use the TPS54122EVM.

2.1 Input and Output Connections

- **J1 – Vin:** Input power supply connector. The positive input lead and ground return lead from the input power supply should be twisted and kept as short as possible to minimize EMI transmission. Additional bulk capacitance should be added across J1 and J2 if the supply leads are greater than six inches. For example, an additional 47 µF electrolytic capacitor across J1 and J2 can improve the transient response of the TPS54122 by eliminating unwanted voltage drop or ringing on the input due to long connection wires
- **J2 – PGND:** Input power supply ground connector. The positive input lead and ground return lead from the input power supply should be twisted and kept as short as possible to minimize EMI transmission.
- **J3 – LDO VOUT:** The output of the LDO. This is the low noise output from the TPS54122 and the default setting of this EVM is 1.8 V. If the LDO is being loaded using J5, J3 can be used as a kelvin connection to the output capacitors of the LDO.
- **J4 – LDO VOUT GND:** This is the low noise ground connector that is connected to the ground of the LDO (GND).
- **J5 – LDO VOUT SMA:** SMA connector for the output voltage of the LDO. The connector for J5 is not populated on the TPS54122EVM (PWR201). This footprint allows the mounting of an SMA-style connector for more accurate PSRR and noise measurements. If the LDO is being loaded using J3, J5 can be used as a kelvin connection to the output capacitors of the LDO.

- **J6 – DC-DC OUT SMA:** SMA connector for the output voltage of the switching regulator. The connector for J6 is not populated on the TPS54122EVM (PWR201). This footprint allows the mounting of an SMA-style connector for more accurate PSRR and noise measurements. If the switcher is being loaded by the LDO or JP2, J6 can be used as a kelvin connection to JP2. If the switcher is being loaded using J6, the "ON DC_DC OUT" pin on JP1 can be used as a kelvin connection to JP6.
- **JP1 – LDO EN:** LDO enable jumper. This EVM allows for the LDO to be enabled using either the output of the switcher or the power good signal from the switcher. To enable the LDO using the output of the switcher place a shorting jumper on the right side position connecting the center pin ("LDO EN") to "ON DC-DC OUT". To enable the LDO using the power good signal of the switcher place a shorting jumper on the left side position connecting the center pin ("LDO EN") to "ON PWRGD" If the enable signal will be provided by an external source connect that source to the center pin labeled "LDO EN". R10 connects LDOEN to ground through a 100 kΩ resistor so floating the pin labled "LDO EN" will disable the LDO.
- **JP2 – SW TO LDO:** The jumper connection between the output of the switching converter to the LDO input. A shorting jumper is required for normal operation. If you want to disconnect the LDO from the SW, remove the shorting jumper. If the LDO will be powered by an external source (instead of the internal switcher) remove the shorting jumper and connect the input supply for the LDO to the right side pin labeled "LDO IN"
- **JP3 – LDO VBIAS:** The jumper connection between V_{IN} and the LDO Vbias. If Vbias is provided by an external source, connect that source to the pin on the right side labled "LDO VBIAS".
- **JP4 – SW EN:** Switching converter enable jumper. To enable the SWITCHER output, leave this jumper unconnected (there is an internal pull up on this pin). To disable, install a shorting jumper, this will short the enable pin to ground.
- **TP1 – VIN:** Input supply test point. This test point connects to the input supply of the switching regulator.
- **TP2 – GND:** Clean ground test point. This test point connects to the clean ground connected to the LDO ground.
- **TP3 – SW GND:** Power ground test point. This test point connects to the power ground connected to the switching regulator.
- **TP4 – LDO PG:** LDO Power Good test point. This test point connects to the power good open-drain flag of the LDO. Tie this pin through a 10k resistor to a regulated supply ≤ 5.5 V to monitor the status of the LDO output. Note, no test point is provided for the switching regulator power good signal but can be monitored using the "ON PWRGD" pin on JP1.

2.2 Modifications

These evaluation modules are designed to provide access to the features of the TPS54122. However, some modifications can be made to this module.

2.2.1 SW Output Voltage Set Point

The output voltage of the switcher is set by the resistor divider formed by R5 and R6. For simplicity the only component change discussed here will be that of R5, R6 in this document is fixed at 6.2 kΩ since that is the default EVM setup. However, there is no need to keep R6 = 6.2 kΩ in real applications. For a more in depth overview of optimizing the TPS54122 for a specific application refer to Application Report SLVA602, *Design Procedures for the TPS54122*. The value of R5 for a specific output voltage can be calculated using Equation 1. Note that the SW output should be 0.5 V above the LDO output for best PSR and noise performance.

$$R5 = 6.2\ k\Omega \times [(SW_{VOUT} / 0.827\ V) - 1] \quad (1)$$

Table 2 lists the R5 and R4 values for some common output voltages. R4 is the compensation resistor and should be scaled relative to the minimum output resistance which is calculated by dividing V_{OUT} by I_{OUT}. The values given in Table 2 are standard values, not the exact value calculated using Equation 1.

Table 2. Sample 1% Resistor Values for Common SW Output Voltages

SW Output Voltage (V)	R5 Value (kΩ)	R4 Value (kΩ)
1.2	2.7	5.11
1.8	7.5	7.68
2.2	10	9.31
2.5	13	10.7
3	16	12.7
3.3	18	14
4.1	24	17.4

2.2.2 LDO Output Voltage Set Point

The output voltage of the LDO is also set by an external resistor divider formed by R1 and R2. For simplicity the only component change discussed here will be that of R1, R2 in this document is fixed at 2.9 kΩ since that is the default EVM setup. However, there is no need to keep R2 = 2.92 kΩ in real applications. For a more in depth overview of optimizing the TPS54122 for a specific application refer to Application Report SLVA602, *Design Procedures for the TPS54122*. The value of R1 for a specific output voltage can be calculated using Equation 2. Note that the LDO output should be 0.5 V below the SW output for best PSR and noise performance.

$$R1 = 10\ k\Omega\ (LDO\ V_{OUT} - 0.8\ V) / (0.8\ V) \quad (2)$$

Table 3 lists the R1 values for some common output voltages. The values given in Table 3 are standard values, not the exact value calculated using Equation 2.

Table 3. Sample 1% Resistor Values for Common LDO Output Voltages

LDO Output Voltage (V)	R1 Value (kΩ)
0.8	0 (Short)
1	0.75
1.2	1.5
1.5	2.4
1.8	3.6
2.5	6.2
3.3	9.1
3.6	10

2.2.3 Switcher Slow Start Time

The slow start time can be adjusted by changing the value of C17. Use Equation 3 to calculate the required value of C17 for a desired slow start time (t_{ss})

$$C17(nF) = t_{ss}(ms) \times I_{(SS)}(\mu A) / V_{ref}(V) \quad (3)$$

The switcher has an internal current source (I_{ss}) of 2.2 µA (typ) that charges the external slow start capacitor C17. The voltage reference V_{ref}(V) for the switcher is 0.827 V (typ).

2.2.4 LDO Start Up

The start up time of the LDO can be adjusted by changing the value of C7. In addition to start up time, the capacitor on the NR pin is used for noise reduction as well. However, the noise reduction effect is nearly saturated at 0.01 µF. The value of C7 can be calculated using Equation 4

$$C7(nF) = t_{ss}(ms) \times I_{(NR)}(\mu A) / V_{(FB)}(V) \quad (4)$$

The LDO has an internal current source ($I_{(NR)}$) of 0.73 µA (typ) that charges the external slow start capacitor C7. The voltage reference Vref(V) for the LDOis 0.8 V (typ).

2.3 Equipment Interconnect

- Turn off the input power supply after verifying that its output voltage is set to the desired supply voltage (less than 5.5 V) and the current limit is set to approximately 5 A. Connect the positive voltage lead from the input power supply to J1 (VIN) and the ground lead to J2 (PGND).
- Connect a 0-3 A load (I_{Load}) between LDO OUT and GND using J3 and J4.
- Place a shorting jumper on JP3 to connect LDO VBIAS to VIN.
- Place a shorting jumper on JP2 to connect "DC-DC OUT" to "LDO IN"
- Disable the output of the LDO by removing the shorting jumper at JP1, this will pull the LDOEN voltage low through R10.

3 Operation

- Turn on the input power supply. Verify that the switcher output voltage is near 2.2 V and the LDO output is near 0V.
- Enable the LDO output by placing a shorting jumper on JP1.
- Verify that the LDO output voltage is 1.8V.
- Vary the load current and VIN voltage as necessary for test purposes.
- Make any modifications necessary to replicate the desired specifications of the end use application and re-test accordingly.

4 Test Results

This section provides typical performance waveforms for the TPS54122EVM (PWR201) for this EVM design.

4.1 Output Noise

Figure 1 shows the output voltage noise spectrum for the TPS54122EVM with V_{IN} = 5V, LDO OUT = 1.8V, SW OUT = 2.2 V, I_{OUT} = 50 mA, Fswitching = 480 kHz, and various output capacitors

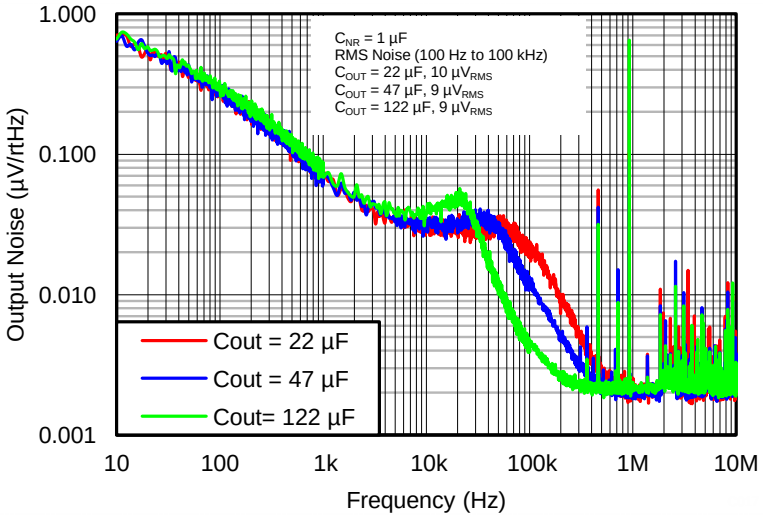

Figure 1. Output Spectrum Noise Density vs. Frequency

4.2 Output Voltage Ripple

Figure 2 shows the output voltage ripple of the LDO and switching converter for the TPS54122EVM with V_{IN} = 5 V, SW OUT = 2.2 V, LDO OUT = 1.8 V, I_{OUT} = 0 mA, and F switching = 480 kHz.

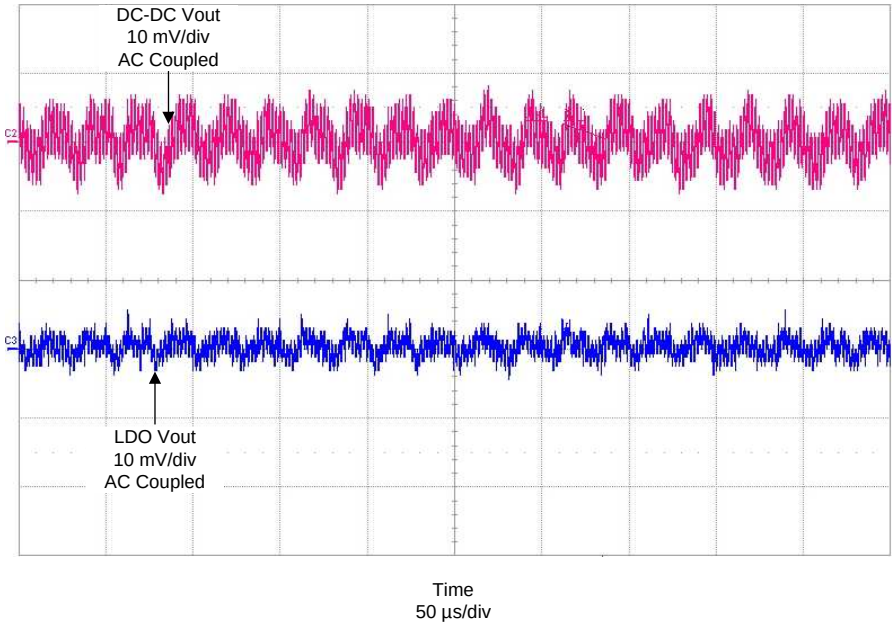

Figure 2. Output Voltage of Both the SW and LDO with no Load

4.3 Output Turn On

Figure 3 shows the SW output voltage during startup of the TPS54122 from SW enable with V_{IN} = 5 V, SW OUT = 2.2 V, LDO OUT = 1.8V, no load, and F switching = 480 kHz.

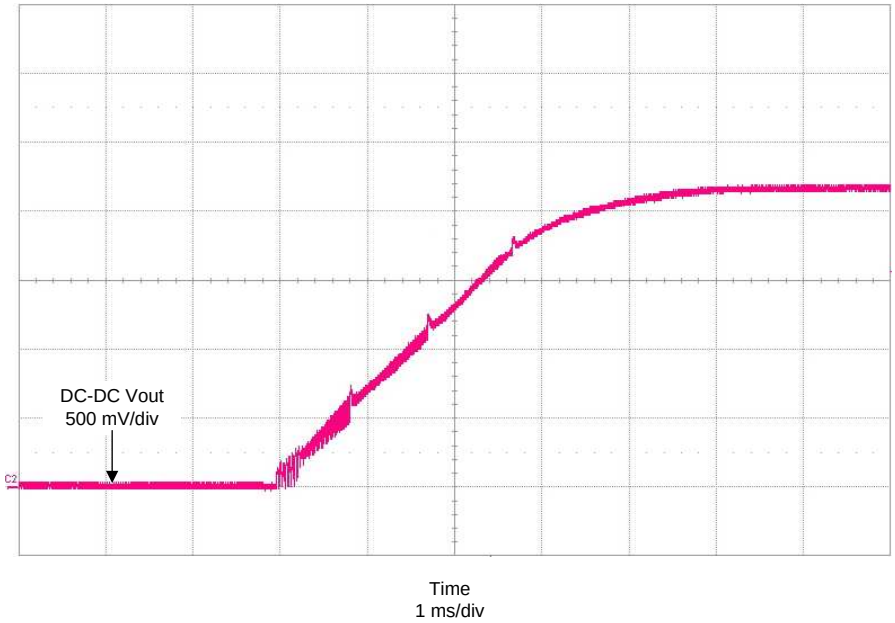

Figure 3. Switcher Converter Output Voltage Turn-on, SW Enable

Figure 4 shows the LDO output voltage during startup of the TPS54122 from LDO enable with V_{IN} = 5 V, SW OUT = 2.2 V, LDO OUT = 1.8 V, no load, F switching = 480 kHz.

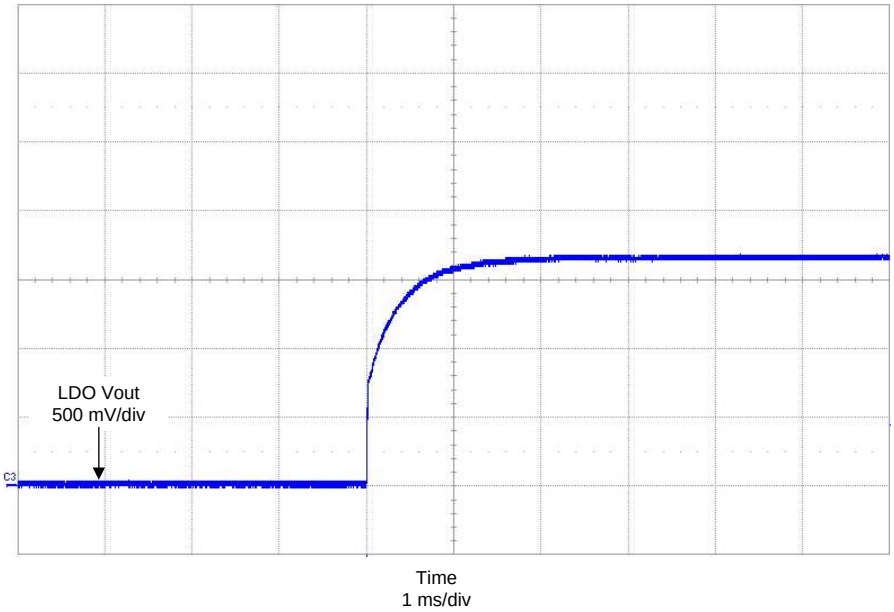

Figure 4. LDO Output Voltage Turn-on, LDO Enable

Figure 5 shows the switcher and LDO output voltage during startup of the TPS54122 from SW enable with V_{IN} = 5 V, SW OUT = 2.2 V, LDO OUT = 1.8 V, no load, F switching = 480 kHz.

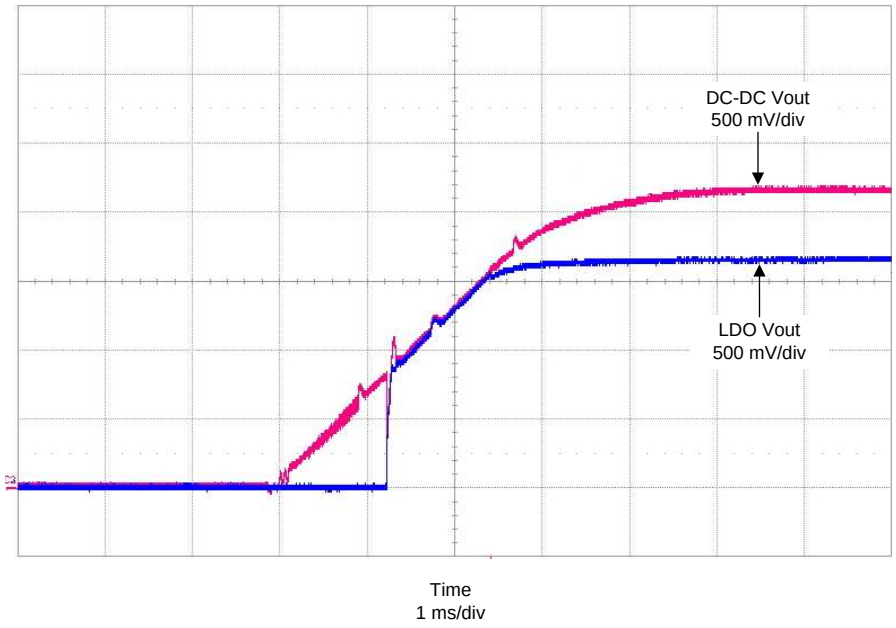

Figure 5. Swiching Converter and LDO Output Voltage Startup, SW Enable

4.4 Load Transient

Figure 6 shows the TPS54122 response to load transients. The current step is from 25% to 75% of the maximum rated load with a 5 V input. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output of both the switcher and the LDO.

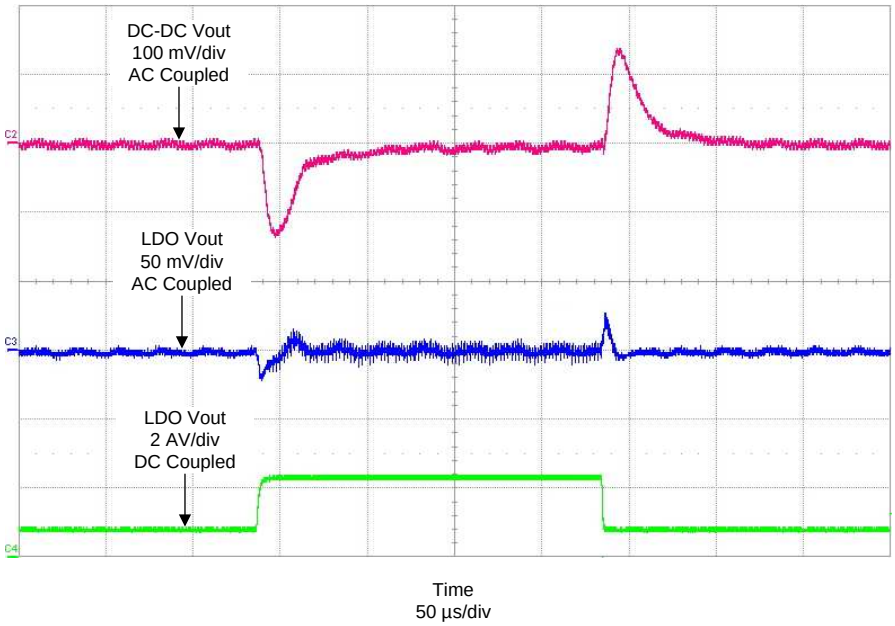

Figure 6. TPS54122 Transient Response

4.5 DC-DC Efficiency

Figure 7 shows the efficiency for the TPS54122 at an ambient temperature of 25°C for V_{IN} = 3.3 V with a switching frequency of 1 MHz.

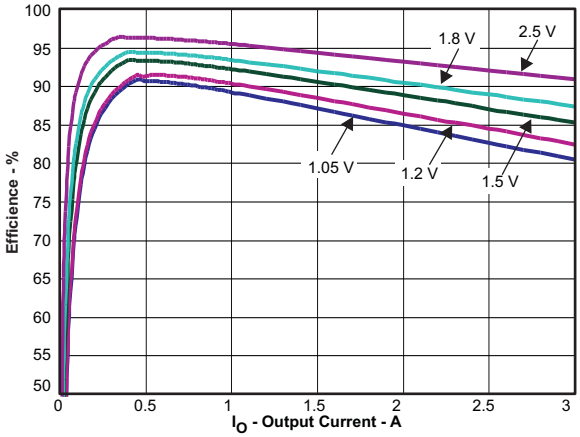

Figure 7. DC-DC Efficiency vs Output Current

5 Board Layout

This section provides a description of the TPS54122, board layout, and layer illustrations.

5.1 Layout Description

The board layout for the TPS54122 evaluation board is shown in Figure 8 through Figure 13. The board consists of 4 layers. It is laid out in such a way that the analog ground of the LDO is shielded as much as possible from the noise of the switcher. Critical analog circuits such as the voltage divider, noise reduction capacitor, input and output capacitors are terminated to the low noise analog ground pour. The topside layer of the EVM is laid out in a manner similar to many user's applications.

The top layer contains the analog ground of the LDO, a portion of the output power ground of the SW side, and the majority of the external components. The first internal layer is connected to the power pad and the analog ground of the IC; mostly this layer is used for power dissipation. This layer also contains the input voltage plane for the switcher. This plane connects the input capacitor and the J1 connector. Only a few separate traces are implemented on this layer such as the LDO enable, and the PWRGD test point trace. The second internal layer is also primarily used for analog ground. To shield the LDO ground from the switch node noise, a small isolated power ground plane is made in the center of this layer to reduce capacitive coupling with the analog ground. The inductor (L1) and the output caps (C9, C10) for the switcher are located close to the center of the bottom layer. The majority of the remaining surface area is connected to the analog ground and connects to the top and internal layers through vias. Some of these vias are directly under the TPS54122 device to provide a thermal path from the top-side ground plane to the internal and bottom-side ground planes. Power ground is also routed on the bottom layer connecting the J2 connector to the input capacitors and compensation components through vias. The only connection between power ground and analog ground is made through a separate set of vias also terminating on the bottom layer.

The input decoupling capacitor of the switcher (C5) is located as close as possible to the IC. connected through vias to the bottom layer power ground. The inductor (L1), the boot cap (C12), and the output caps of the switcher (C9, C10) are placed on the bottom layer of the board to help shield the LDO from the switching noise. The boot cap (C12) and the inductor (L1) are connected through vias that terminate very close to the PH pin of the IC. This connects them as close as possible to the PH pin, reducing parasitic inductance caused by long traces, and still allows the LDO to be shielded from some of the switching noise. The input (C13, C14, C15), output (C2, C3, C4), and noise reduction capacitors (C7) of the LDO are also placed as close as possible to the IC.

The input of the LDO is connected to the output of the switcher using a shorting jumper and the power plane is parallel to the ground plane that connects the ground on the LDO with the ground of the switcher. LDO components that are noise sensitive such as the voltage divider (R1, R2), the LDO input and output caps are terminated to ground using a ground plane separated from the majority of the power ground plane.

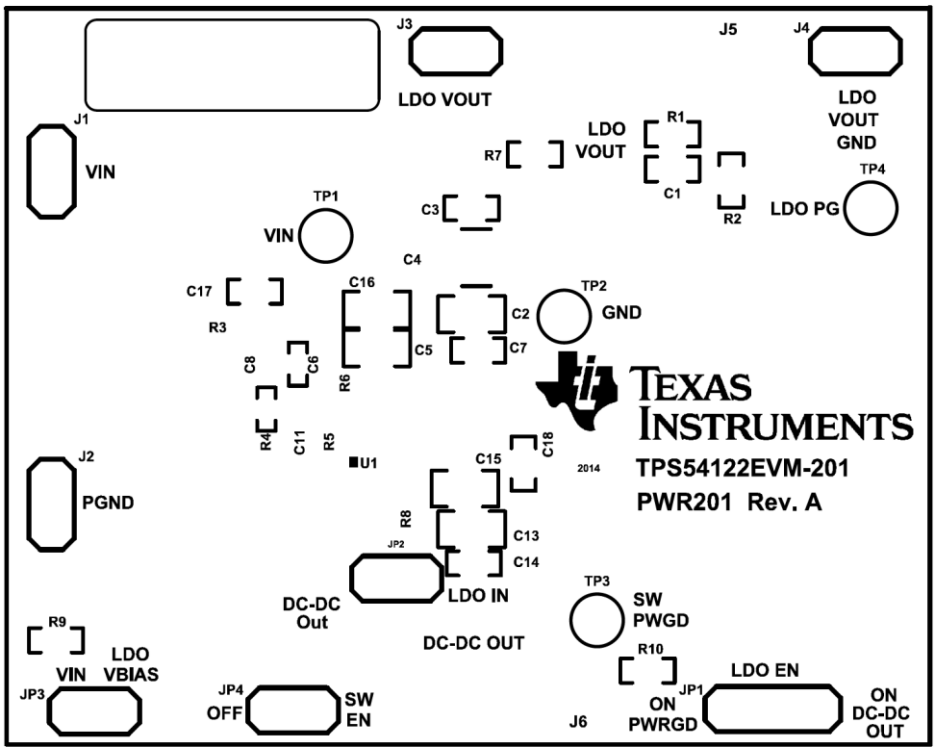

Figure 8. Top Side Silkscreen

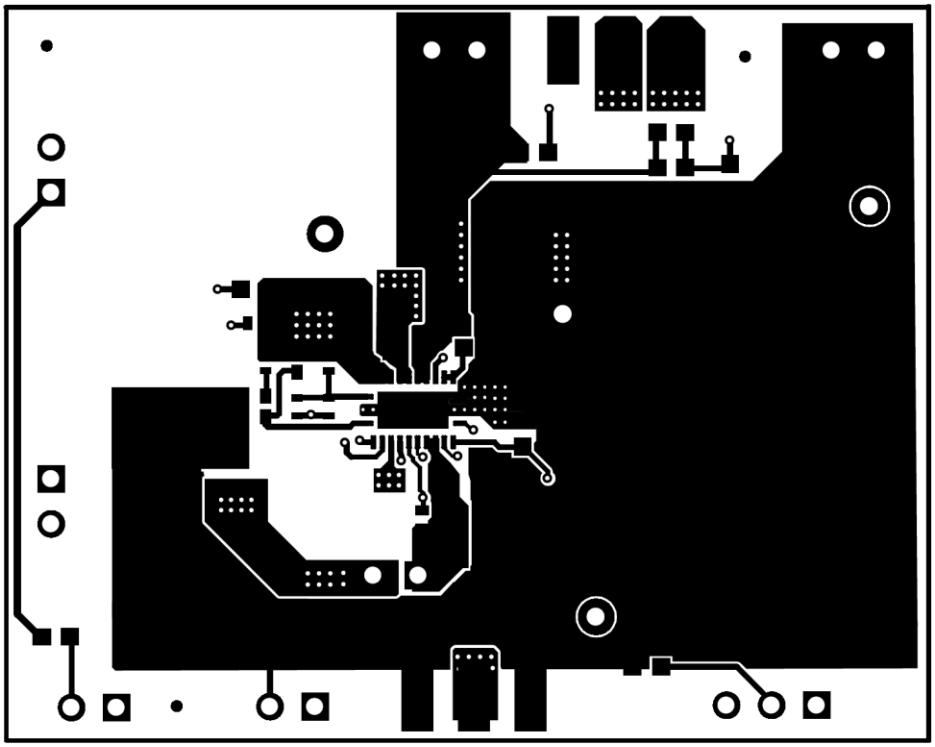

Figure 9. Top Layer Routing

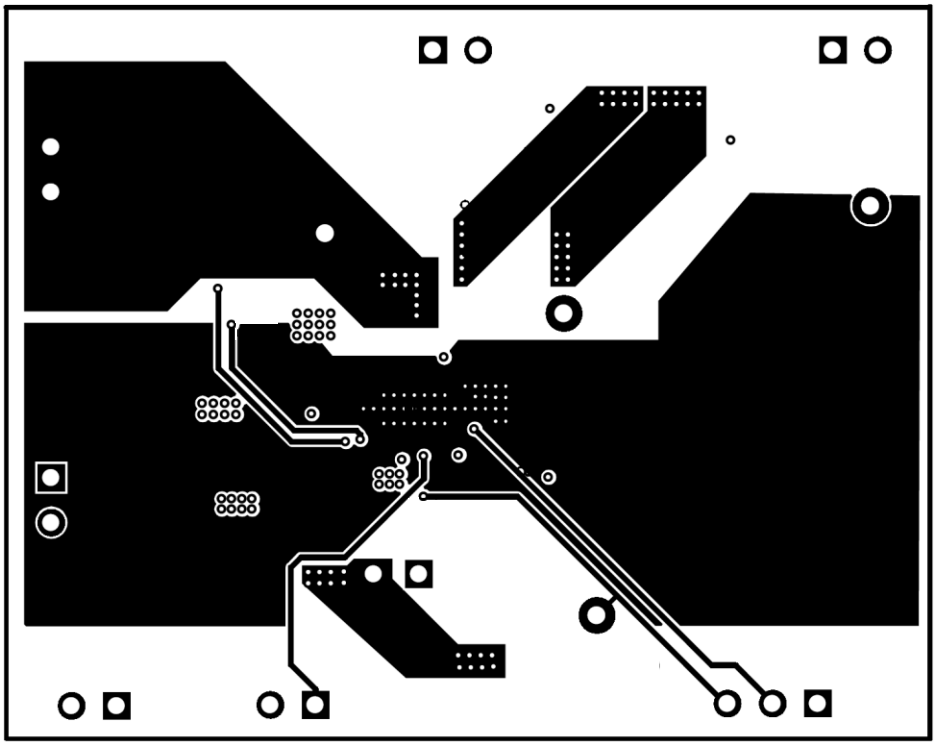

Figure 10. Second Layer (Internal) Routing

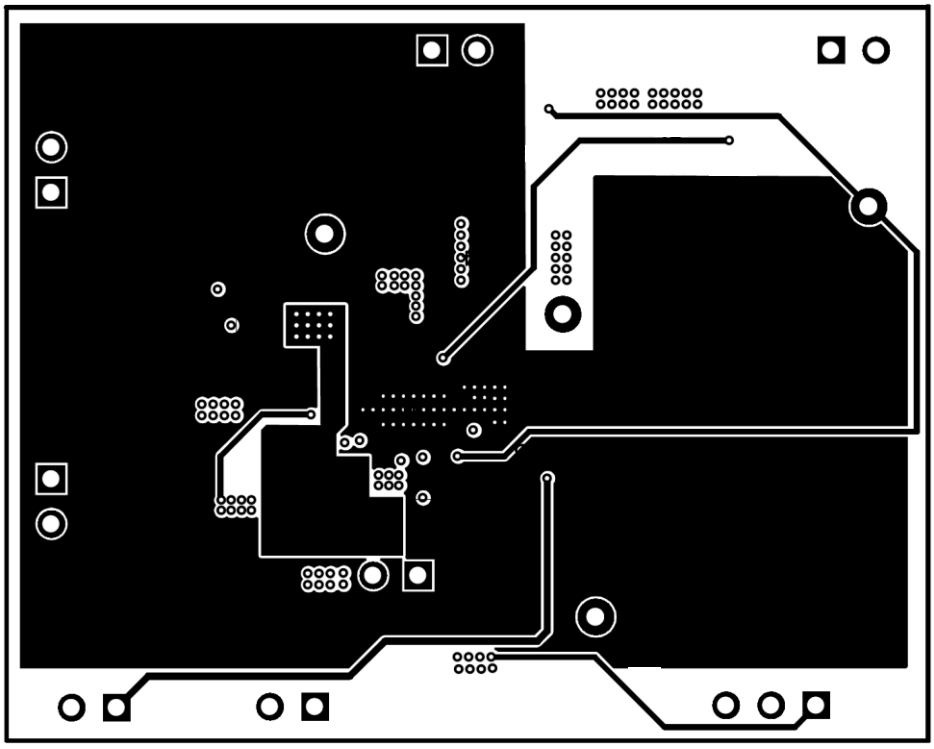

Figure 11. Third Layer (Internal) Routing

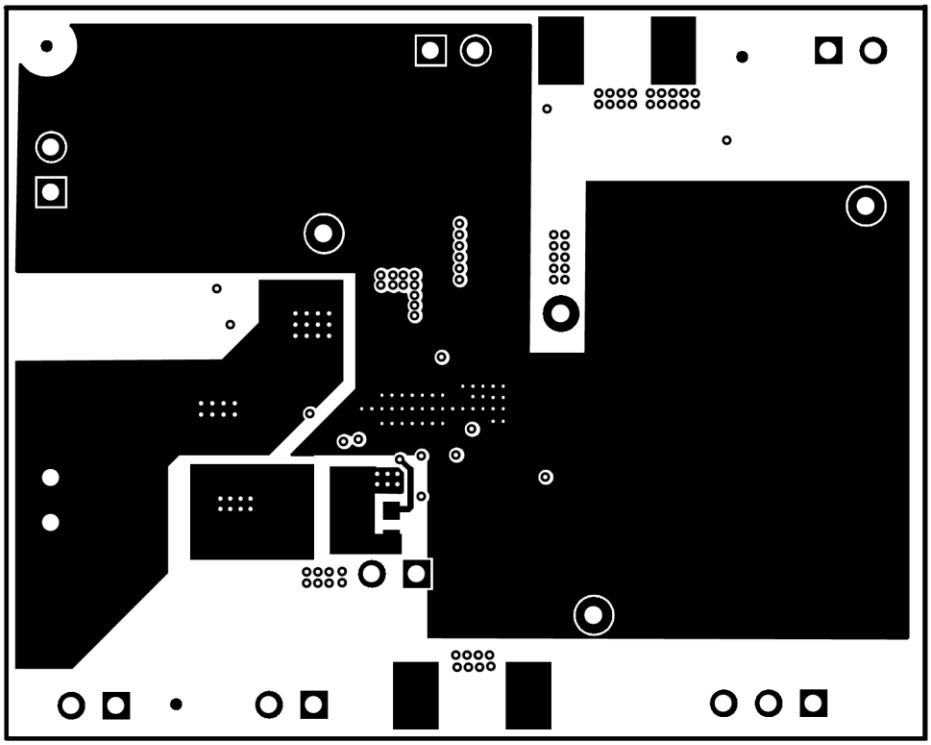

Figure 12. Bottom Layer Routing

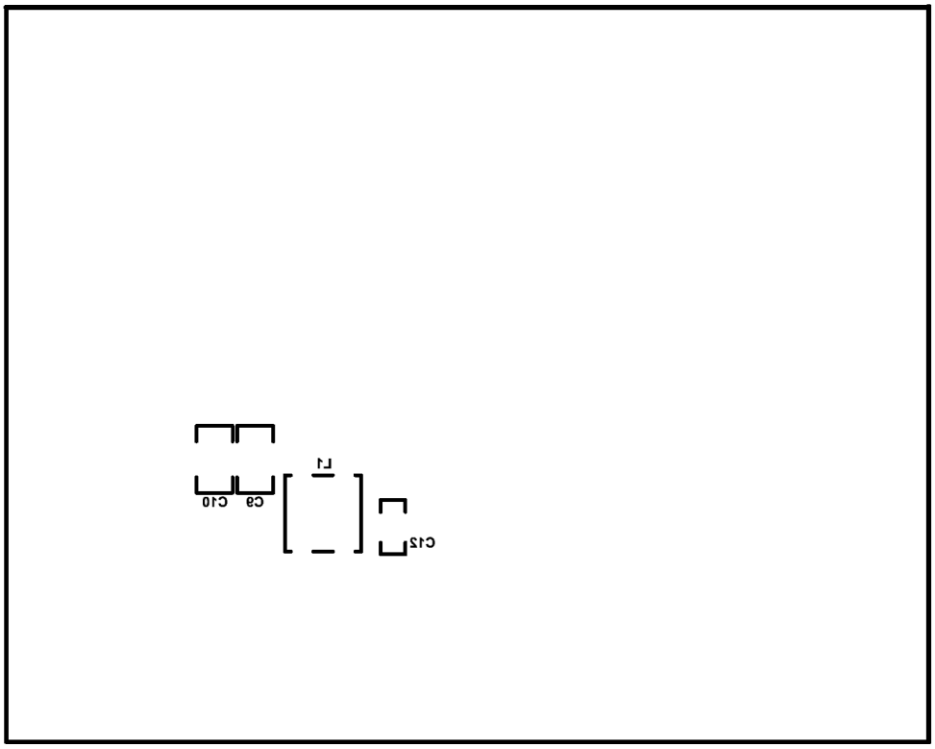

Figure 13. Bottom Side Silkscreen

6 Schematic

Figure 14 is the schematic for the TPS54122 evaluation board.

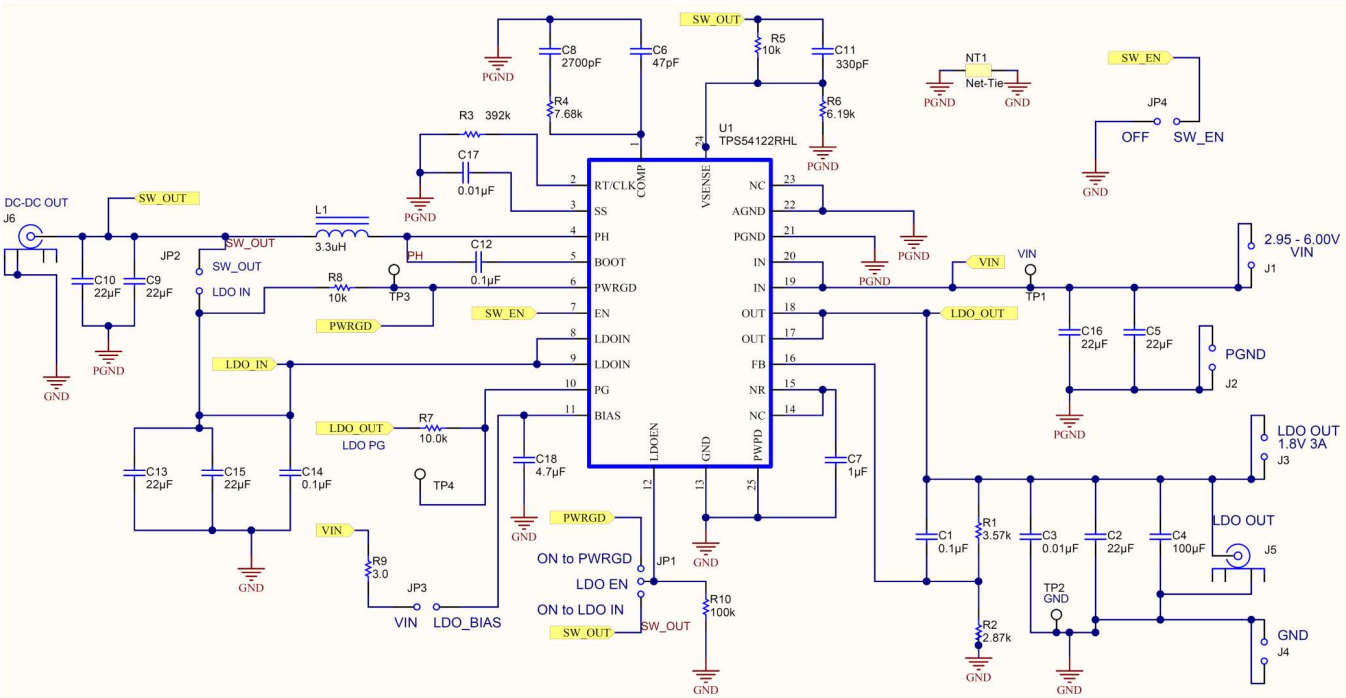

Figure 14. Schematic

7 Bill of Materials

Table 4 presents the bill of materials for the TPS54122 evaluation board.

Table 4. Bill of Materials

Designator	Quantity	Value	Description	Package	Part Number	Manufacturer
C1, C14	2	0.1uF	CAP, CERM, 0.1uF, 100V, +/-10%, X7R, 0603	0603	GRM188R72104KA35J	MuRata
C2, C5, C9, C10, C13, C15, C16	7	22uF	CAP, CERM, 22uF, 35V, +/-20%, JB, 0805	0805	C2012JB1V226M125AC	TDK
C3, C17	2	0.01uF	CAP, CERM, 0.01uF, 16V, +/-10%, X7R, 0603	0603	GRM188R71C103KA01D	MuRata
C4	1	100uF	CAP, CERM, 100uF, 6.3V, +/-20%, X5R, 1812	1812	C4532X5R0J107M	TDK
C6	1	47pF	CAP, CERM, 47pF, 25V, +/-5%, C0G/NP0, 0402	0402	GRM1555C1E470JA01D	MuRata
C7	1	1u	F CAP, CERM, 1uF, 10V, +/-10%, X7R, 0603	0603	GRM188R71A105KA61D	MuRata
C8	1	2700pF	CAP, CERM, 2700pF, 100V, +/-10%, X7R, 0402	0402	GRM155R72A272KA01D	MuRata
C11	1	330pF	CAP, CERM, 330pF, 50V, +/-5%, C0G/NP0, 0402	0402	C1005C0G1H331J	TDK
C12	1	0.1uF	CAP, CERM, 0.1uF, 25V, +/-10%, X8R, 0603	0603	CGA3E2X8R1E104K080AA	TDK
C18	1	4.7uF	CAP, CERM, 4.7uF, 10V, +/-10%, X5R, 0603	0603	CGB3B1X5R1A475K055AC	TDK
J1, J2, J3, J4, JP2, JP3, JP4	7	PEC02SAAN	Header, Male 2-pin, 100mil spacing,	0.100 inch x 2	PEC02SAAN	Sullins
J5, J6	2	142-0711-821	CONNECTOR, SHEILDED, END LAUNCH JACK, GOLD PLATED, FOR 0.062 PCB, EDGE MOUNTED	0.250 SQ	142-0711-821	STD
JP1	1	PEC03SAAN	Header, Male 3-pin, 100mil spacing,	0.100 inch x 3	PEC03SAAN	Sullins
L1	1	3.3uH	Inductor, Shielded, Composite, 3.3uH, 5.5A, 0.026 ohm, SMD	4.0x3.1x4.0mm	XAL4030-332MEB	Coilcraft
R1	1	3.57k	RES, 3.57k ohm, 0.1%, 0.1W, 0603	0603	RG1608P-3571-B-T5	Susumu Co Ltd
R2	1	2.87k	RES, 2.87k ohm, 0.1%, 0.1W, 0603	0603	RG1608P-2871-B-T5	Susumu Co Ltd
R3	1	392k	RES, 392k ohm, 1%, 0.063W, 0402	0402	CRCW0402392KFKED	Vishay-Dale
R4	1	7.68k	RES, 7.68k ohm, 1%, 0.063W, 0402	0402	CRCW04027K68FKED	Vishay-Dale
R5, R8	2	10k	RES, 10k ohm, 5%, 0.063W, 0402	0402	CRCW040210K0JNED	Vishay-Dale
R6	1	6.19k	RES, 6.19k ohm, 1%, 0.063W, 0402	0402	CRCW04026K19FKED	Vishay-Dale
R7	1	10.0k	RES, 10.0k ohm, 0.5%, 0.1W, 0603	0603	RT0603DRE0710KL	Yageo America
R9	1	3.0	RES, 3.0 ohm, 5%, 0.1W, 0603	0603	CRCW06033R00JNEA	Vishay-Dale
R10	1	100k	RES, 100k ohm, 0.1%, 0.1W, 0603	0603	RT0603BRD07100KL	Yageo America
TP1, TP2, TP3, TP4	4	White	Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone
U1	1	TPS54122RHL	IC, Low Noise LDO, 3-A Power Supply with Integrated DC-DC Converter	QFN-24	TPS54122RHL	TI

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2. Unless otherwise indicated, EVMs are not finished products and not intended for consumer use. EVMs are intended solely for use by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.
3. User agrees that EVMs shall not be used as, or incorporated into, all or any part of a finished product.
4. User agrees and acknowledges that certain EVMs may not be designed or manufactured by TI.
5. User must read the user's guide and all other documentation accompanying EVMs, including without limitation any warning or restriction notices, prior to handling and/or using EVMs. Such notices contain important safety information related to, for example, temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit www.ti.com/esh or contact TI.
6. User assumes all responsibility, obligation, and any corresponding liability for proper and safe handling and use of EVMs.
7. Should any EVM not meet the specifications indicated in the user's guide or other documentation accompanying such EVM, the EVM may be returned to TI within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY TI TO USER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. TI SHALL NOT BE LIABLE TO USER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES RELATED TO THE HANDLING OR USE OF ANY EVM.
8. No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which EVMs might be or are used. TI currently deals with a variety of customers, and therefore TI's arrangement with the user is not exclusive. TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services with respect to the handling or use of EVMs.
9. User assumes sole responsibility to determine whether EVMs may be subject to any applicable federal, state, or local laws and regulatory requirements (including but not limited to U.S. Food and Drug Administration regulations, if applicable) related to its handling and use of EVMs and, if applicable, compliance in all respects with such laws and regulations.
10. User has sole responsibility to ensure the safety of any activities to be conducted by it and its employees, affiliates, contractors or designees, with respect to handling and using EVMs. Further, user is responsible to ensure that any interfaces (electronic and/or mechanical) between EVMs and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
11. User shall employ reasonable safeguards to ensure that user's use of EVMs will not result in any property damage, injury or death, even if EVMs should fail to perform as described or expected.
12. User shall be solely responsible for proper disposal and recycling of EVMs consistent with all applicable federal, state, and local requirements.

Certain Instructions. User shall operate EVMs within TI's recommended specifications and environmental considerations per the user's guide, accompanying documentation, and any other applicable requirements. Exceeding the specified ratings (including but not limited to input and output voltage, current, power, and environmental ranges) for EVMs may cause property damage, personal injury or death. If there are questions concerning these ratings, user should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the applicable EVM user's guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using EVMs' schematics located in the applicable EVM user's guide. When placing measurement probes near EVMs during normal operation, please be aware that EVMs may become very warm. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use EVMs.

Agreement to Defend, Indemnify and Hold Harmless. User agrees to defend, indemnify, and hold TI, its directors, officers, employees, agents, representatives, affiliates, licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of, or in connection with, any handling and/or use of EVMs. User's indemnity shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if EVMs fail to perform as described or expected.

Safety-Critical or Life-Critical Applications. If user intends to use EVMs in evaluations of safety critical applications (such as life support), and a failure of a TI product considered for purchase by user for use in user's product would reasonably be expected to cause severe personal injury or death such as devices which are classified as FDA Class III or similar classification, then user must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

RADIO FREQUENCY REGULATORY COMPLIANCE INFORMATION FOR EVALUATION MODULES

Texas Instruments Incorporated (TI) evaluation boards, kits, and/or modules (EVMs) and/or accompanying hardware that is marketed, sold, or loaned to users may or may not be subject to radio frequency regulations in specific countries.

General Statement for EVMs Not Including a Radio

For EVMs not including a radio and not subject to the U.S. Federal Communications Commission (FCC) or Industry Canada (IC) regulations, TI intends EVMs to be used only for engineering development, demonstration, or evaluation purposes. EVMs are not finished products typically fit for general consumer use. EVMs may nonetheless generate, use, or radiate radio frequency energy, but have not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or the ICES-003 rules. Operation of such EVMs may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: For EVMs including a radio, the radio included in such EVMs is intended for development and/or professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability in such EVMs and their development application(s) must comply with local laws governing radio spectrum allocation and power limits for such EVMs. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by TI unless user has obtained appropriate experimental and/or development licenses from local regulatory authorities, which is the sole responsibility of the user, including its acceptable authorization.

U.S. Federal Communications Commission Compliance

For EVMs Annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. Changes or modifications could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at its own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Industry Canada Compliance (English)

For EVMs Annotated as IC – INDUSTRY CANADA Compliant:

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs Including Radio Transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs Including Detachable Antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Canada Industry Canada Compliance (French)

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Important Notice for Users of EVMs Considered "Radio Frequency Products" in Japan

EVMs entering Japan are NOT certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If user uses EVMs in Japan, user is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after user obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after user obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless user gives the same notice above to the transferee. Please note that if user does not follow the instructions above, user will be subject to penalties of Radio Law of Japan.

http://www.tij.co.jp

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In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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