Mercury+ SA2 SoC Module

User Manual

Purpose

The purpose of this document is to present the characteristics of Mercury+ SA2 SoC module to the user, and to provide the user with a comprehensive guide to understanding and using the Mercury+ SA2 SoC module.

Summary

This document first gives an overview of the Mercury+ SA2 SoC module followed by a detailed description of its features and configuration options. In addition, references to other useful documents are included.

Product Information	Code	Name
Product	ME-SA2	Mercury+ SA2 SoC Module

Document Information	Reference	Version	Date
Reference / Version / Date	D-0000-408-002	09	03.12.2021

Approval Information	Name	Position	Date
Written by	DIUN	Design Engineer	11.09.2015
Verified by	GLAC	Design Expert	15.09.2015
Approved by	DIUN	Manager, BU SP	03.12.2021

Copyright Reminder

Document History

Version	Date	Author	Comment
09	03.12.2021	MKON	Removed information on revision 2 modules.
08	16.02.2021	DIUN	Added information on unavailability of R2 modules, corrected information on differential signals shared with FX3, added information on Mercury heatsinks, added Mercury+ ST1 to accesories section, added information on FPGA fuses and warranty, on differential I/Os, on voltage monitoring outputs, other style updates
07	19.08.2019	DIUN	Added information on revision 2 modules, voltage monitoring, power supplies, heat sink, Linux how-to guide, JTAG interface, other style updates
06	21.08.2018	DIUN	Minor corrections and style updates
05	04.05.2017	DIUN	Updated EEPROM map, block diagram and footprint information
04	27.12.2016	DIUN	Added tool support information and updated USB 2.0 information
03	13.09.2016	DIUN	Minor updates and corrections
02	02.06.2016	DIUN	Several corrections
01	21.09.2015	DIUN	Version 01

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1 Overview

1.1 General

1.1.1 Introduction

The Mercury+ SA2 SoC module combines the Altera Cyclone® V ARM® processor-based SoC (System-on-Chip) device with fast DDR3L SDRAM, USB 3.0 controller and PHY, USB 2.0 PHY, PCIe® Gen1/Gen2 ×4, Gigabit Ethernet and dual Fast Ethernet interfaces, multi-gigabit transceivers, high-speed LVDS I/O, and is available in industrial temperature range, forming a complete and powerful embedded processing system.

The use of the Mercury+ SA2 SoC module, in contrast to building a custom SoC hardware, significantly simplifies system design and thus shortens time to market and decreases the development effort of your product.

Together with Mercury+ base boards, the Mercury+ SA2 SoC module allows the user to quickly build a system prototype and start with application development.

The Enclustra Build Environment [14] is available for the Mercury+ SA2 SoC module. This build system allows the user to quickly set up and run Linux on any Enclustra SoC module. It allows the user to choose the desired target, and download all the required binaries, such as bitstream and preloader. It downloads and compiles all required software, such as U-Boot, Linux, and BusyBox based root file system.

1.1.2 Warranty

Please refer to the General Business Conditions, available on the Enclustra website [1].

Warning!

Please note that the warranty of an Enclustra module is voided if the FPGA fuses are blown. This operation is done at own risk, as it is irreversible. Enclustra cannot test the module in case of a warranty product return.

1.1.3 RoHS

The Mercury+ SA2 SoC module is designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2011/65/EC).

1.1.4 Disposal and WEEE

The Mercury+ SA2 SoC module must be properly disposed of at the end of its life.

The Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable for the Mercury+ SA2 SoC module.

1.1.5 Safety Recommendations and Warnings

Mercury+ modules are not designed to be "ready for operation" for the end-user. These can only be used in combination with suitable base boards. Proper configuration of the hardware before usage is required.

Ensure that the power supply is disconnected from the board before inserting or removing the Mercury+ SA2 SoC module, connecting interfaces, or connecting jumpers.

Touching the capacitors of the DC-DC converters can lead to voltage peaks and permanent damage; over-voltage on power or signal lines can also cause permanent damage to the module.

Warning!

It is possible to mount the Mercury+ SA2 SoC module the wrong way round on the base board - always check that the mounting holes on the base board are aligned with the mounting holes of the Mercury+ SA2 SoC module.

The base board and module may be damaged if the module is mounted the wrong way round and powered up.

1.1.6 Electrostatic Discharge

Electronic boards are sensitive to electrostatic discharge (ESD). Please ensure that the product is handled with care and only in an ESD-protected environment.

1.1.7 Electromagnetic Compatibility

The Mercury+ SA2 SoC module is a Class A product (as defined in IEC 61000-3-2 standard) and is not intended for use in domestic environments. The product may cause electromagnetic interference, for which appropriate measures must be taken.

1.2 Features

- Altera Cyclone V SOC 5CSTFD6D5F31I7N
  - ARM dual-core Cortex A9
  - Altera Cyclone V 28 nm FPGA fabric
- 294 user I/Os up to 3.3 V
  - 18 ARM peripheral I/Os (SPI, SDIO, CAN, I2C, UART)
  - 202 FPGA I/Os (single-ended or differential)
  - 32 FPGA I/Os (single-ended or differential) shared with USB 3.0
  - 42 MGT signals (clock and data)
- 9 MGTs @ 6.144 Gbit/sec and 3 reference input clock differential pairs
- PCIe Gen2 ×4 (Altera PCIe hardened IP block)
- 2 GB DDR3L SDRAM
- 64 MB quad SPI flash
- Gigabit Ethernet
- Dual Fast Ethernet
- Cypress EZ-USB FX3 USB 3.0 device controller
- USB 2.0 host/device
- Real-time clock
- CAN, UART, SPI, I2C, SDIO/MMC
- 5 to 15 V supply voltage

1.3 Deliverables

- Mercury+ SA2 SoC module
- Mercury+ SA2 SoC module documentation, available via download:
  - Mercury+ SA2 SoC Module User Manual (this document)
  - Mercury+ SA2 SoC Module Reference Design [2]
  - Mercury+ SA2 SoC Module IO Net Length Excel Sheet [3]

- Mercury+ SA2 SoC Module FPGA Pinout Excel Sheet [4]
- Mercury+ SA2 SoC Module User Schematics (PDF) [5]
- Mercury+ SA2 SoC Module Known Issues and Changes [6]
- Mercury+ SA2 SoC Module Footprint (Altium, Eagle, Orcad and PADS) [7]
- Mercury+ SA2 SoC Module 3D Model (PDF) [8]
- Mercury+ SA2 SoC Module STEP 3D Model [9]
- Mercury Mars Module Pin Connection Guidelines [10]
- Mercury Master Pinout [11]
- Mercury Heatsink Application Note [17]
- Enclustra Build Environment [14] (Linux build environment; refer to Section 1.4.2 for details)
- Enclustra Build Environment How-To Guide [15]

1.4 Accessories

1.4.1 Reference Design

The Mercury+ SA2 SoC module reference design features an example configuration for the Cyclone V SoC device, together with an example top level HDL file for the user logic.

A number of software applications are available for the reference design, that show how to initialize the peripheral controllers and how to access the external devices. Pre-compiled binaries are included in the archive, so that the user can easily check that the hardware is functional.

The reference design can be downloaded from the Enclustra download page [2].

1.4.2 Enclustra Build Environment

The Enclustra Build Environment (EBE) [14] enables the user to quickly set up and run Linux on any Enclustra SoC module or system board. It allows the user to choose the desired target, and download all the required binaries, such as bitstream and preloader/bootloader. It downloads and compiles all required software, such as U-Boot, Linux, and BusyBox based root file system.

The Enclustra Build Environment features a graphical user interface (GUI) and a command line interface (CLI) that facilitates the automatic build flow.

The Enclustra Build Environment How-To Guide [15] describes in more detail how to use the EBE to customize the provided software for the user application. The document provides information on the configuration options for U-boot, Linux kernel and Buildroot, debugging possibilities for Linux applications, customization of device trees and integration of existing or new kernel drivers.

1.4.3 Enclustra Heat Sink

For Mercury modules an Enclustra heat sink is available for purchase along with the product. Please refer to section 2.11.6 for further information on the available cooling options.

1.4.4 Mercury+ PE1 Base Board

- 168-pin Hirose FX10 module connectors (PE1-200: 2 connectors; PE1-300/400: 3 connectors)
- System controller
- Power control
- System monitor (PE1-300/400)
- Current sense (PE1-300/400)
- Low-jitter clock generator (PE1-300/400)
- microSD card holder
- User EEPROM
- eMMC managed NAND flash (PE1-300/400)

- PCIe ×4 interface
- USB 3.0 device connector
- USB 2.0 host connector (PE1-200: 1 connector; PE1-300/400: 4 connectors)
- Micro USB 2.0 device (UART, SPI, I2C, JTAG) connector
- 2 × RJ45 Gigabit Ethernet connectors
- mPCIe/mSATA card holder (USB only) (PE1-300/400)
- SIM card holder (optional, PE1-300/400 only)
- SMA clock and data in/out (optional, PE1-300/400 only)
- 1 × FMC LPC connector (PE1-200)
- 1 × FMC HPC connector (PE1-300)
- 2 × FMC LPC connector (PE1-400)
- 2 × 40-pin Anios pin header
- 3 × 12-pin IO headers
- 5 to 15 V DC supply voltage
- USB bus power (with restrictions)

Please note that the available features depend on the equipped Mercury module type and on the selected base board variant.

1.4.5 Mercury+ ST1 Base Board

- 168-pin Hirose FX10 module connectors (3 connectors)
- 2 × MIPI D-PHY connectors: CSI and CSI/DSI (requires FPGA support)
- Mini DisplayPort connector (requires FPGA support)
- HDMI connector (requires FPGA support)
- SFP+ connector
- Low-jitter clock generator
- USB 3.0 device connector
- USB 3.0 host connector
- FTDI USB 2.0 device controller with micro USB device connector (UART, SPI, I2C, JTAG)
- 2 × RJ45 Gigabit Ethernet connectors
- 1 × FMC HPC connector (note: not all pins are available)
- 2 × 40-pin Anios pin header
- 3 × 12-pin IO headers
- microSD card holder
- 5 to 15 V DC supply voltage
- Form factor: 100 × 120 mm

Please note that the available features depend on the equipped Mercury module type.

1.5 Intel Tool Support

The SoC devices equipped on the Mercury+ SA2 SoC module are supported by the Quartus Prime Lite Edition (or Quartus II Web Edition, for older software versions), which is available free of charge. Please contact Intel for further information.

2 Module Description

2.1 Block Diagram

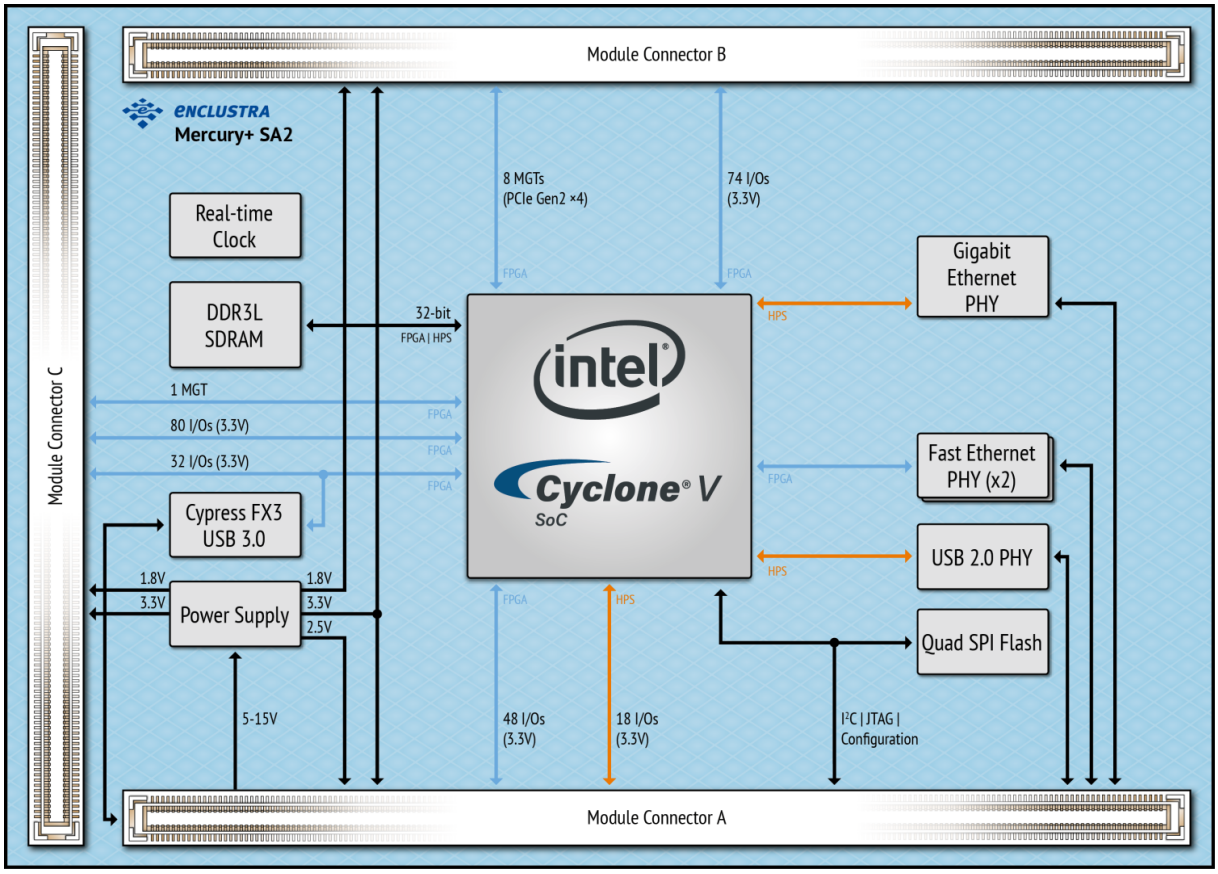

Figure 1: Hardware Block Diagram

The main component of the Mercury+ SA2 SoC module is the Intel Cyclone V SoC device. Most of its I/O pins are connected to the Mercury module connectors, making up to 252 regular user I/Os available to the user. Further, nine multi-gigabit transceivers with support for PCIe Gen2 ×4 are available on the module connectors.

The SoC device can boot from the on-board QSPI flash or from an external SD card. For development purposes, a JTAG interface is connected to Mercury module connector.

The memory subsystem is built from a 64 MB QSPI flash and 2 GB DDR3L SDRAM in the standard configuration.

Further, the module is equipped with a Gigabit Ethernet PHY, two Fast Ethernet PHYs for dual Fast Ethernet implementation and a USB 2.0 PHY, making it ideal for communication applications.

A Cypress FX3 USB 3.0 controller is fitted on the module to easily implement a communication link to a host PC.

A real-time clock is available on the module and is connected to the global I2C bus.

On-board clock generation is based on a 50 MHz crystal oscillator.

The module's internal supply voltages are generated from a single input supply of 5 - 15 V DC. Some of these voltages are available on the Mercury module connectors to supply circuits on the base board.

Four LEDs are connected to the SoC pins for status signaling.

2.2 Module Configuration and Product Models

Table 1 describes the available standard module configurations. Custom configurations are available; please contact Enclustra for further information.

Product Model	SoC	DDR3L SDRAM	PCI Express	Temperature Range
ME-SA2-D6-7I-D11	5CSTFD6D5F31I7N	2 GB	✓	-40 to +85° C

Table 1: Standard Module Configurations

The product model indicates the module type and main features. Figure 2 describes the fields within the product model.

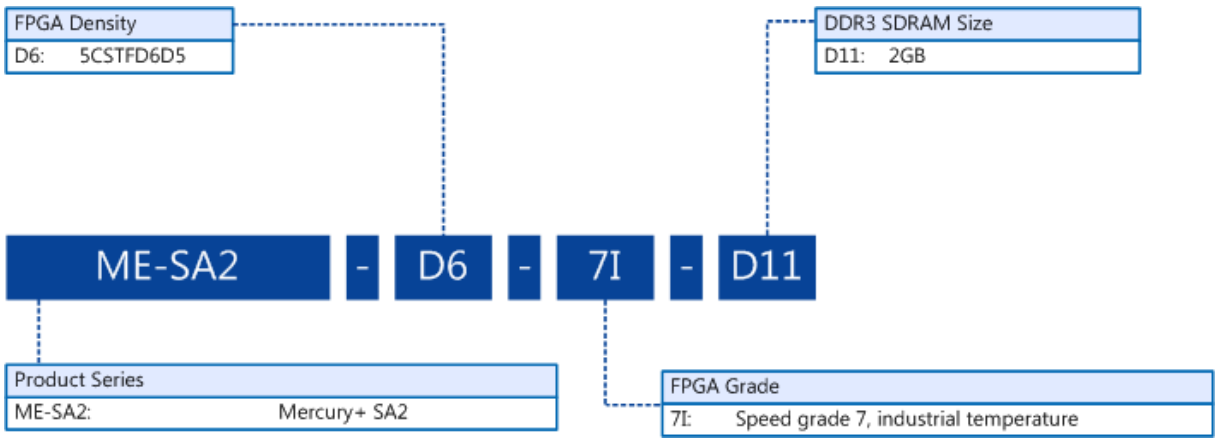

Figure 2: Product Model Fields

Please note that for the first revision modules or early access modules, the product model may not respect entirely this naming convention. Please contact Enclustra for details on this aspect.

2.3 EN-Numbers and Part Names

Every module is uniquely labeled, showing the EN-number and serial number. An example is presented in Figure 3.

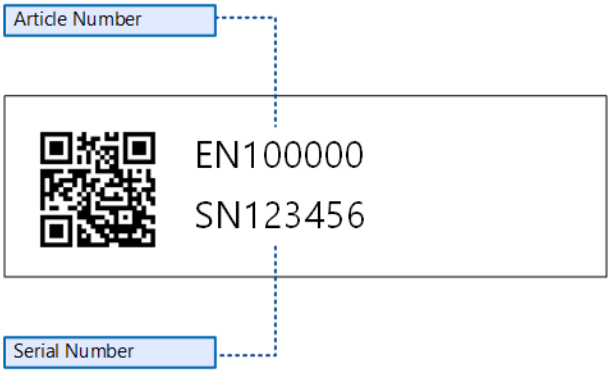

Figure 3: Module Label

The correspondence between EN-number and part name is shown in Table 2. The part name represents the product model, followed by the revision; the R suffix and number represent the revision number.

The revision changes and product known issues are described in the Mercury+ SA2 SoC Module Known Issues and Changes document [6].

EN-Number	Part Name
EN101010	ME-SA2-D6-7I-D11-R1

Table 2: EN-Numbers and Part Names

2.4 Top and Bottom Views

2.4.1 Top View

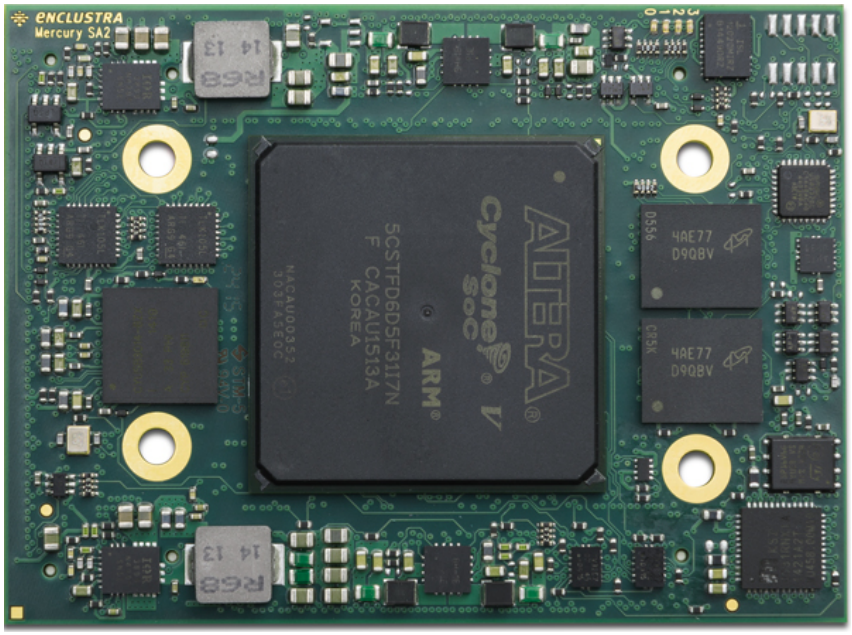

Figure 4: Module Top View

2.4.2 Bottom View

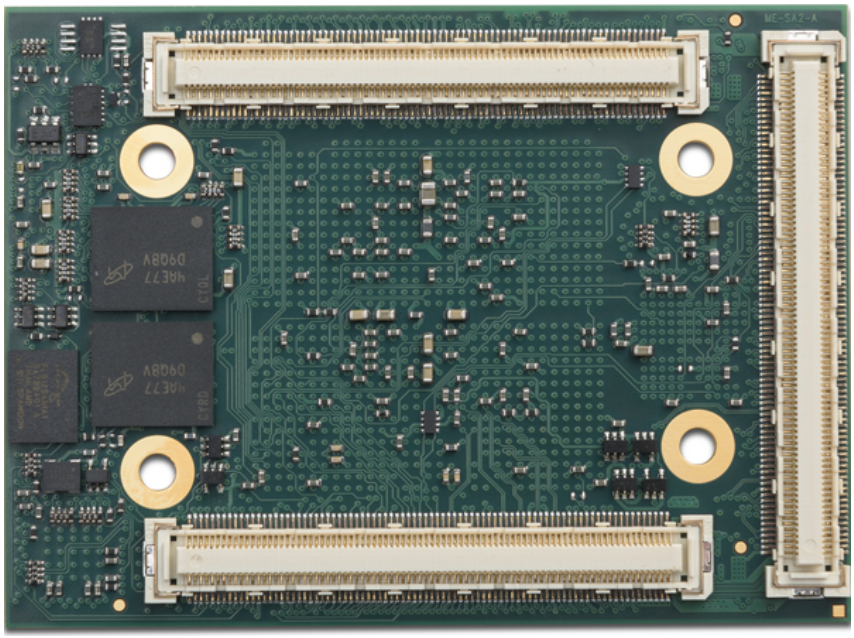

Figure 5: Module Bottom View

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.5 Top and Bottom Assembly Drawings

2.5.1 Top Assembly Drawing

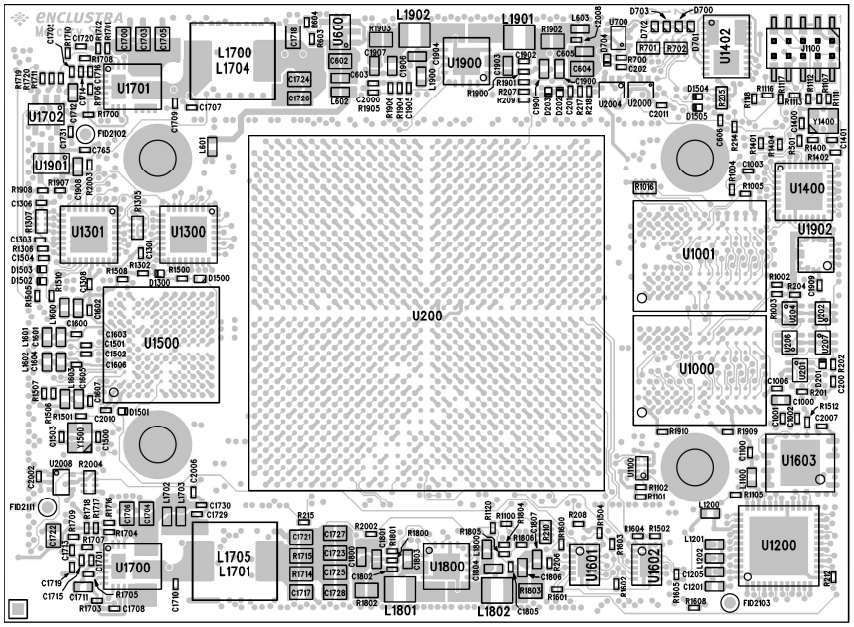

Figure 6: Module Top Assembly Drawing

2.5.2 Bottom Assembly Drawing

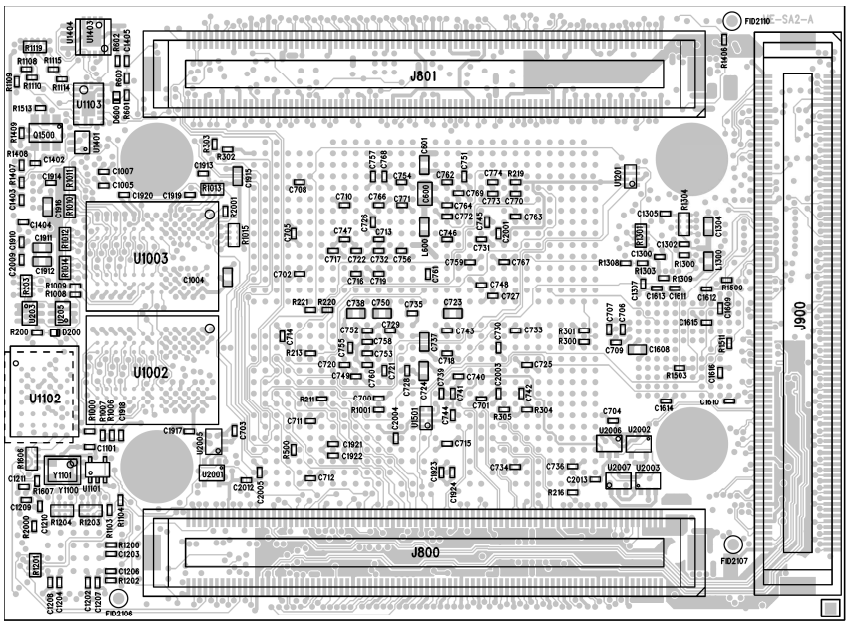

Figure 7: Module Bottom Assembly Drawing

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.6 Module Footprint

Figure 8 shows the dimensions of the module footprint on the base board.

Enclustra offers Mercury and Mercury+ modules of various geometries having widths of 56, 64, 65, 72 or 74 mm and having different topologies for the mounting holes. If different module types shall be fixed on the base board by screws, additional mounting holes may be required to accommodate different modules. The footprints of the module connectors for the base board design are available for different PCB design tools (Altium, PADS, Eagle, Orcad) [7] and include the required information on the module sizes and holes.

The maximum component height on the base board under the module is dependent on the connector type. Please refer to the Hirose FX10 series product website for detailed connector information [12].
The three connectors are called A (J800), B (J801) and C (J900).

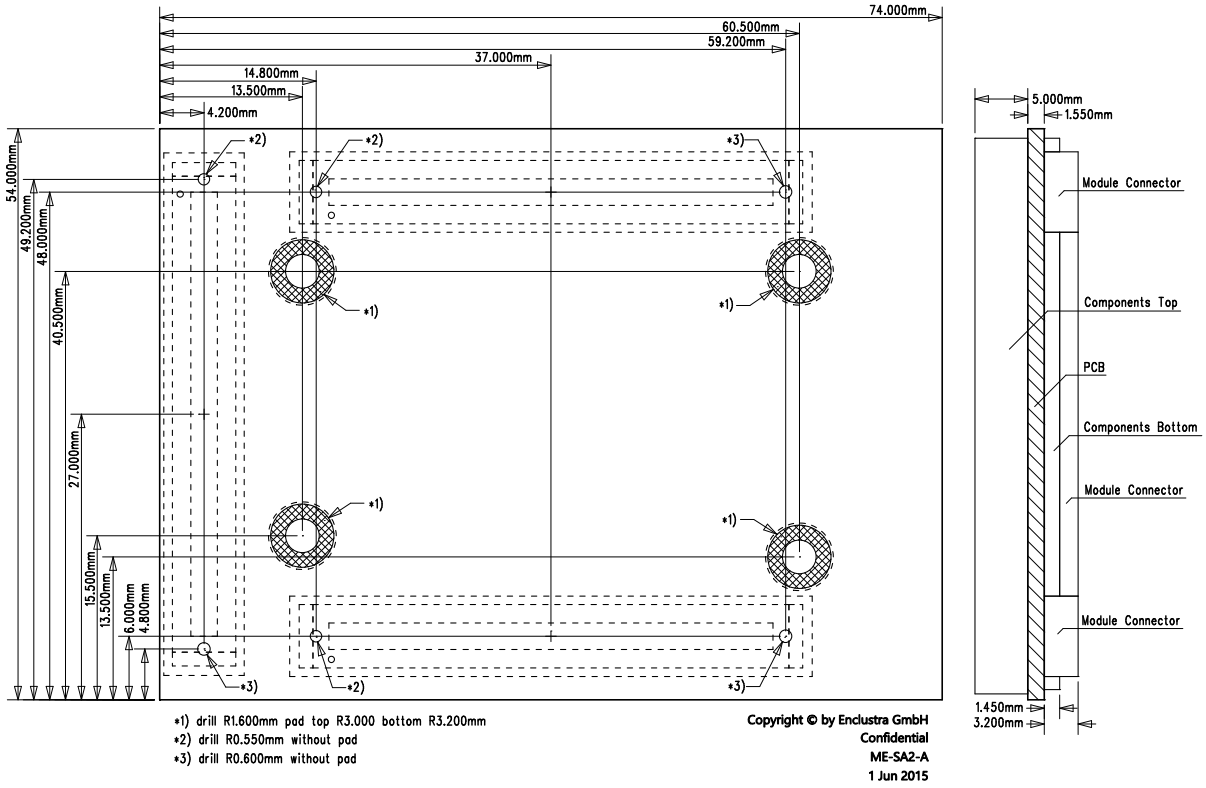

Figure 8: Module Footprint - Top View

Warning!

It is possible to mount the Mercury+ SA2 SoC module the wrong way round on the base board - always check that the mounting holes on the base board are aligned with the mounting holes of the Mercury+ SA2 SoC module.

2.7 Mechanical Data

Table 3 describes the mechanical characteristics of the Mercury+ SA2 SoC module. A 3D model (PDF) and a STEP 3D model are available [8], [9].

Symbol	Value
Size	74 × 54 mm
Component height top	5.0 mm
Component height bottom	1.45 mm
Weight	29 g

Table 3: Mechanical Data

2.8 Module Connector

Three Hirose FX10 168-pin 0.5 mm pitch headers with a total of 504 pins have to be integrated on the base board. Up to four M3 screws may be used to mechanically fasten the module to the base board. Do not use excessive force to tighten the screws, as this could damage the module.

The pinout of the module connector is found in the Mercury Master Pinout Excel Sheet [11]. The connector is available in different packaging options and different stacking heights. Some examples are presented in Table 4. Please refer to the connector datasheet for more information.

Reference	Type	Description
Mercury module connector	FX10A-168S-SV	Hirose FX10, 168-pin, 0.5 mm pitch
Base board connector	FX10A-168P-SV(71)	Hirose FX10, 168-pin, 0.5 mm pitch, 4 mm stacking height
Base board connector	FX10A-168P-SV1(71)	Hirose FX10, 168-pin, 0.5 mm pitch, 5 mm stacking height

Table 4: Module Connector Types

Figure 9 indicates the pin numbering for the Mercury module connectors from the top view of the base board. The connector pins are numbered as follows:

- Connector A: from J800-1 to J800-168
- Connector B: from J801-1 to J801-168
- Connector C: from J900-1 to J900-168

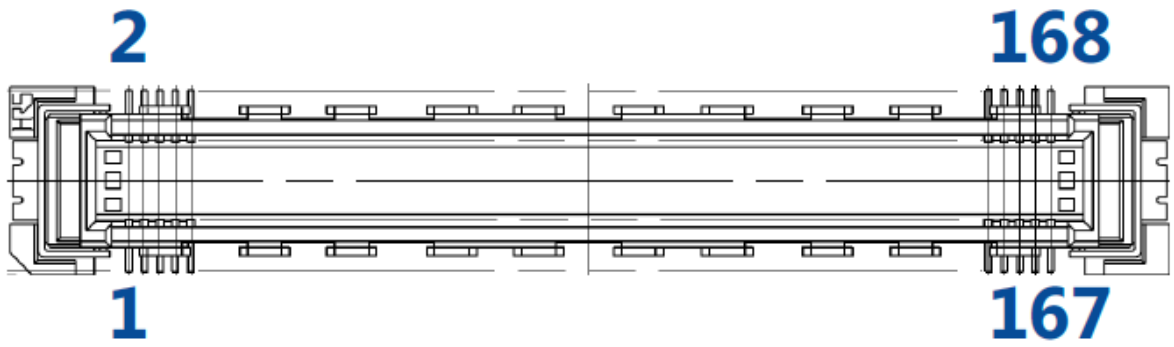

Figure 9: Pin Numbering for the Module Connector

Warning!

Do not use excessive force to latch a Mercury module into the Mercury connectors on the base board, as this could damage the module and the base board; always make sure that the module is correctly oriented before mounting it into the base board.

2.9 User I/O

2.9.1 Pinout

Information on the Mercury+ SA2 SoC module pinout can be found in the Enclustra Mercury Master Pinout [11], and in the additional document Enclustra Module Pin Connection Guidelines [10].

Warning!

Please note that the pin types on the schematics symbol of the module connector and in the Master Pinout document are for reference only. On the Mercury+ SA2 SoC module it may be possible that the connected pins do not have the targeted functions (such as primary clocks, differential pins, MGT signals, etc).

The naming convention for the user I/Os is:
IO_B<BANK>_<FUNCTION>_<PIN_NAME>_<PACKAGE_PIN>_<POLARITY>

For example, IO_B4A_RX_B42_AE17_P is located on pin AE17 of I/O bank 4A, and when used in a differential pair it is a receive pin and has positive polarity.

The naming convention for the user I/Os shared with the FX3 device is:
FX3_<FX3_FUNCTION>_B<BANK>_<_FUNCTION>_<PACKAGE_PIN>.

The clock capable pins are marked with "CLK" in the signal name. For details on their function and usage, please refer to the Intel documentation.

Table 5 includes information related to the total number of I/Os available in each I/O bank and possible limitations.

Please note that Cyclone V devices can only use I/O pins marked with "RX" in the signal name as differential inputs and only pins marked with "TX" as differential outputs. The I/O pins marked with "CLK" are receive-only differential signals and can be used as dedicated clock differential inputs. All pins can be used as single-ended inputs or outputs.

Signal Name	Signals	Pairs	Differential	Single-ended	I/O Bank
IO_B5A_RX<...>	16	8	In	In/Out	5A
IO_B5A_TX<...>	16	8	Out	In/Out	5A
IO_B5B_RX<...>	4	2	In	In/Out	5B
IO_B5B_CLK<...>	4	2	In	In/Out	5B
IO_B5B_TX<...>	8	4	Out	In/Out	5B
IO_B4A_RX<...>	36	18	In	In/Out	4A
IO_B4A_CLK<...>	4	2	In	In/Out	4A
IO_B4A_TX<...>	40	20	Out	In/Out	4A
IO_B8A_RX<...>	36	18	In	In/Out	8A
IO_B8A_CLK<...>	4	2	In	In/Out	8A
IO_B8A_TX<...>	34	17	Out	In/Out	8A
FX3_<...>	32	-	Pins not routed differentially Shared with the FX3 pins	In/Out	3B
Total	**234**	**117**	-	-	-

Table 5: User I/Os

Warning!

The FX3 signals must be left unconnected on the module connector C when using the USB 3.0 on the Mercury+ SA2 SoC module.

Warning!

When using the signals on FPGA bank 3B as regular FPGA I/Os, the FX3 must be kept by driving the FX3_RESET#_LS signal (pin AK2) low.

2.9.2 I/O Pin Exceptions

The I/O pin exceptions are pins with special functions or restrictions (for example, when used in combination with certain Mercury boards they may have a specific role).

Table 6 lists the I/O pin exceptions on the Mercury+ SA2 SoC module.

I/O Name	Module Connector Pin	Description
HPS_GPIO59_MISO	A-104	Connected via a 47 kΩ resistor to IO_B5A_RX_R6_PERST#_W22_N pin (A-36) for PCIe PERST# connection implementation
HPS_GPIO57_CLK	A-98	Can optionally be connected via a 47 kΩ resistor to IO_B5A_TX_R3_CVP_AH29_N pin (A-21) for Configuration via Protocol (CVP) implementation (CVP pin can be connected to PCIe WAKE# pin)

Table 6: I/O Pin Exceptions

When the Mercury+ SA2 SoC module is used in combination with a Mercury+ PE1 base board as a PCIe device, the PERST# signal coming from the PCIe edge connector on the module connector pin A-104 (HPS_GPIO59_MISO) is driven further to IO_B5A_RX_R6_PERST#_W22_N.

Because the PCIe block inside the FPGA logic side requires this reset signal, the PERST# signal is connected to the FPGA pin IO_B5A_RX_R6_PERST#_W22_N via a 47 kΩ resistor. In situations in which a custom board is used or PCIe functionality is not required, this FPGA pin can be used in the same manner as a regular I/O pin.

The connection of the CVP pin to the PCIe WAKE# pin on the Mercury+ PE1 base board is made in a similar manner - note that the connection is not available in the standard configuration, as not all PCIe cards support the wake function. Details on the CVP implementation can be found in the Altera CVP documentation [23] and details on the WAKE# pin are available in the PCIe specification.

2.9.3 Differential I/Os

When using differential pairs, a differential impedance of 100 Ω must be matched on the base board, and the two nets of a differential pair must have the same length.

The information regarding the length of the signal lines from the SoC device to the module connector is available in Mercury+ SA2 SoC Module IO Net Length Excel Sheet [3]. This enables the user to match the total length of the differential pairs on the base board if required by the application.

Warning!

Please note that the trace length of various signals may change between revisions of the Mercury+ SA2 SoC module. Please use the information provided in the Mercury+ SA2 SoC Module IO Net Length Excel Sheet [3] to check which signals are affected. The differential signals will still be routed differentially in subsequent product revisions.

Please note that Cyclone V devices can only use I/O pins marked with "RX" in the signal name as differential inputs and only pins marked with "TX" as differential outputs. All pins can be used as single-ended inputs or outputs.

Warning!

Check Mercury+ SA2 SoC module pinout with Quartus before producing your own base board hardware, to make sure that all pins are used according to the correct direction.

2.9.4 I/O Banks

Table 7 describes the main attributes of the FPGA and Hard Processing System (HPS) I/O banks, and indicates which peripherals are connected to each I/O bank. All I/O pins within a particular I/O bank must use the same I/O (VCC_IO) and reference (VREF) voltages.

Bank	Connectivity	VCC_IO	VREF
MGT Bank L0	Module connector	1.1 V	-
MGT Bank L1	Module connector	1.1 V	-
MGT Bank L2	Module connector	1.1 V	-
Bank 3A	Configuration, Fast Ethernet PHYs	1.8 V	0 V
Bank 3B	Module connector	User selectable VCC_IO_B3B_B4A	0.5 × VCC_IO_B3B_B4A
Bank 4A	Module connector	User selectable VCC_IO_B3B_B4A	0.5 × VCC_IO_B3B_B4A
Bank 5A	Module connector	User selectable VCC_IO_B5A_B5B	0.5 × VCC_IO_B5A_B5B
Bank 5B	Module connector	User selectable VCC_IO_B5A_B5B	0.5 × VCC_IO_B5A_B5B
Bank 8A	Module connector, LEDs	User selectable VCC_IO_B8A	0.5 × VCC_IO_B8A
HPS Bank 6A	DDR3L SDRAM	1.35 V	0.68 V
HPS Bank 6B	DDR3L SDRAM	1.35 V	0.68 V
HPS Bank 7A	Module connector, I2C, LEDs	VCC_CFG_HPS	0 V
HPS Bank 7B	Gigabit Ethernet PHY, QSPI flash	VCC_CFG_HPS	0 V
HPS Bank 7C	Module connector	VCC_CFG_HPS	0 V
HPS Bank 7D	USB PHY	VCC_CFG_HPS	0 V

Table 7: I/O Banks

2.9.5 VCC_IO Usage

The VCC_IO voltages for the I/O banks located on the module connector are configurable by applying the required voltage to the VCC_IO_B[x] or VCC_CFG_[x] pins. All VCC_IO_B[x] or VCC_CFG_[x] pins of the same bank must be connected to the same voltage.

For compatibility with other Enclustra Mercury modules, it is recommended to use a single I/O voltage per module connector.

Signal Name	SoC Pins	Supported Voltages	Connector A Pins	Connector B Pins	Connector C Pins
VCC_IO_B3B_B4A	VCCIO3B, VCCIO4A	1.8 V - 3.3 V ±5%	-	-	76, 116, 158
VCC_IO_B5A_B5B	VCCIO5A, VCCIO5B	1.2 V - 3.3 V ±5%	38, 41	-	-
VCC_IO_B8A	VCCIO8A	1.8 V - 3.3 V ±5%	-	64, 67, 88, 95, 140, 143	-
VCC_CFG_HPS	VCCIO7A-D	1.8 V, 2.5 V - 3.3 V ±5%	74, 77	-	-

Table 8: VCC_IO Pins

If the Mercury+ SA2 SoC module is used in combination with a base board having only two module connectors, the VCC_IO_B3B_B4A pin that powers I/O banks 3B and 4A is connected to the on-board generated 1.8 V supply voltage.

Note that the VCCPD (I/O pre-driver power supply) for each bank is set automatically to 2.5 V (if the corresponding VCCIO is less than or equal to 2.5 V) or to VCCIO (if the corresponding VCCIO is higher or equal to 3.0 V).

Warning!

Use only VCC_IO voltages compliant with the equipped SoC device; any other voltages may damage the equipped SoC device, as well as other devices on the Mercury+ SA2 SoC module.

Do not leave a VCC_IO pin floating, as this may damage the equipped SoC device, as well as other devices on the Mercury+ SA2 SoC module.

Warning!

Do not power the VCC_IO pins when PWR_GOOD and PWR_EN signals are not active. If the module is not powered, you need to make sure that the VCC_IO voltages are disabled (for example, by using a switch on the base board, which uses PWR_GOOD as enable signal). Figure 10 illustrates the VCC_IO power requirements.

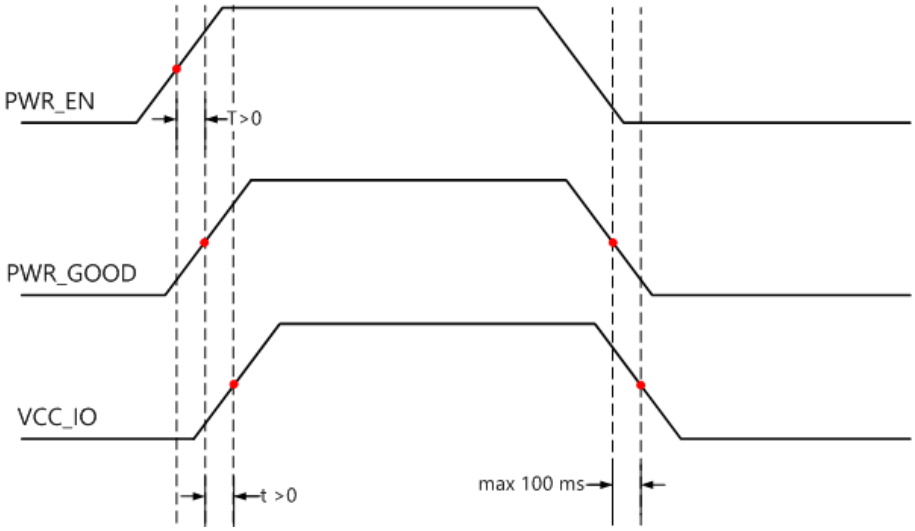

Figure 10: Power-Up Sequence - VCC_IO in Relation with PWR_GOOD and PWR_EN Signals

2.9.6 Signal Terminations

Differential Inputs

There are no external differential termination resistors on the Mercury+ SA2 SoC module for differential inputs. Differential input pairs on the module connector may be terminated either by external termination resistors on the base board (close to the module pins), or by the SoC device's internal termination resistors.

Please note that Cyclone V devices can only use I/O pins marked with "RX" in the name as differential inputs.

Single-Ended Outputs

There are no series termination resistors on the Mercury+ SA2 SoC module for single-ended outputs. If required, series termination resistors may be equipped on the base board (close to the module pins).

2.9.7 HPS I/O Pins

Table 9 gives an overview over the HPS pin connections on the Mercury+ SA2 SoC module. Only the pins marked with "user functionality" are available on the module connector.

The suggested functions below are for reference only - always verify your HPS pinout with the Intel device handbook.

HPS_GPIO	Function	Connection
0-8, 10-13, 53	USB 2.0	USB 2.0 PHY
9	RTC interrupt	Real-time clock
14-27	Gigabit Ethernet	Gigabit Ethernet PHY (RGMII)
28	HPS boot select 2	Boot mode selection
29-34	QSPI flash	QSPI flash
35	Fast Ethernet PHY reset (output, active-low)	Fast Ethernet PHY A and PHY B

Continued on next page...

HPS_GPIO	Function	Connection
36, 38-39, 45-47	SD card/user functionality	Module connector
37	Gigabit Ethernet interrupt (input, active-low)	Gigabit Ethernet PHY
40	Boot mode 0	BOOT_MODE0
41	Gigabit Ethernet link status (ETH_LED2#, input, active-low)	Gigabit Ethernet PHY
42	Boot mode 1	BOOT_MODE1
43	Power good (input, active-high)	PWR_GOOD
44	Gigabit Ethernet PHY reset (output, active-low)	Gigabit Ethernet PHY
48-50	LEDs (connected in parallel with FPGA I/Os)	On-board LEDs
51-52	I2C/user functionality	Module connector
54-56	I2C	On-board I2C bus and module connector via level shifter
57-60	SPI/user functionality	Module connector
61-62	CAN/user functionality	Module connector
63 64	UART1 RX[1]/user functionality UART1 TX[1]/user functionality	Module connector
65 66	UART0 RX[1]/user functionality UART0 TX[1]/user functionality	Module connector

Table 9: HPS Pin Connections

2.10 Multi-Gigabit Transceiver (MGT)

There are nine Multi-Gigabit transceivers and three reference input clock differential pairs on the Mercury+ SA2 SoC module routed directly to the module connectors. Eight transceiver pairs are routed to module connector B and one pair to the module connector C.

The transceivers on the SoC device support a data rate of 6.144 Gbit/sec.

Warning!

The maximum data rate on the MGT lines on the Mercury+ SA2 SoC module depends on the routing path for these signals. Adequate signal integrity over the full signal path must be ensured when using MGTs at high performance rates.

[1]UART RX is an SoC input; UART TX is an SoC output.

Warning!

No AC coupling capacitors are placed on the Mercury+ SA2 SoC module on the MGT lines - make sure capacitors are mounted, if required, on the base board (close to the module pins), to prevent MGT lines from being damaged.

2.11 Power

2.11.1 Power Generation Overview

The Mercury+ SA2 SoC module uses a 5 - 15 V DC power input for generating the on-board supply voltages (1.1 V, 1.2 V, 1.35 V, 1.55 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V). Some of these voltages (1.8 V, 2.5 V, 3.3 V) are accessible on the module connector.

Table 10 describes the power supplies generated on the module.

Voltage Supply Name	Voltage Value	Rated Current	Voltage Source	Shut down via PWR_EN	Influences PWR_GOOD
VCC_1V1	1.1 V	9 A	VCC_MOD	Yes	Yes
VCC_1V2	1.2 V	1 A	VCC_3V3	Yes	Yes
VCC_1V35	1.35 V	1.5 A	VCC_3V3	Yes	Yes
VCC_1V55	1.55 V	0.15 A	VCC_1V8	Yes	No
VCC_1V8	1.8 V	1 A	VCC_3V3	Yes	Yes
VCC_2V5	2.5 V	1.5 A	VCC_3V3	Yes	Yes
VCC_3V3	3.3 V	9 A	VCC_MOD	No	Yes
VCC_5V0	5.0 V	0.15 A	VCC_MOD	No	No

Table 10: Generated Power Supplies

Please refer to the Enclustra Module Pin Connection Guidelines for general rules on the power pins [10].

2.11.2 Power Enable/Power Good

The Mercury+ SA2 SoC module provides a power enable input on the module connector. This input may be used to shut down the DC/DC converters for 1.1 V, 1.2 V, 1.5 V, 1.8 V, and 2.5 V. The 3.3 V supply is always active.

The PWR_EN input is pulled to VCC_3V3 on the Mercury+ SA2 SoC module with a 10 kΩ resistor. The PWR_GOOD signal is pulled to VCC_3V3 on the Mercury+ SA2 SoC module with a 10 kΩ resistor.

PWR_GOOD is an open collector signal and must not be used to drive a load directly. This signal is pulled to GND if the on-board regulators fail or if the module is disabled via PWR_EN. The list of regulators that influence the state of PWR_GOOD signal is provided in Section 2.11.1.

Pin Name	Module Connector Pin	Remarks
PWR_EN	A-10	Floating/3.3 V: Module power enabled Driven low: Module power disabled
PWR_GOOD	A-12	0 V: Module supply not ok 3.3 V: Module supply ok

Table 11: Module Power Status and Control Pins

Warning!

Do not apply any other voltages to the PWR_EN pin than 3.3 V or GND, as this may damage the Mercury+ SA2 SoC module. PWR_EN pin can be left unconnected.

Do not power the VCC_IO pins (for example by connecting VCC_3V3 to VCC_IO directly) when PWR_EN is driven low to disable the module. In this case, VCC_IO needs to be switched off in the manner indicated in Figure 10.

2.11.3 Voltage Supply Inputs

Table 12 describes the power supply inputs on the Mercury+ SA2 SoC module. The VCC voltages used as supplies for the I/O banks are described in Section 2.9.5.

Pin Name	Module Connector Pins	Voltage	Description
VCC_MOD	A-1, 2, 3, 4, 5, 6, 7, 8, 9, 11	5 - 15 V ±5%	Supply for the 1.1 V and 3.3 V voltage regulators. All other supplies are generated from the 3.3 V supply. The input current is rated at 3 A (0.3 A per connector pin).
VCC_BAT	A-168	2.0 - 3.6 V	Battery for the RTC and SoC encryption key storage

Table 12: Voltage Supply Inputs

2.11.4 Voltage Supply Outputs

Table 13 presents the supply voltages generated on the Mercury+ SA2 SoC module, that are available on the module connector.

Pin Name	Module Connector Pins	Voltage	Maximum Current[2]	Comment
VCC_3V3	A-26, 29, 50, 86 B-55, 79, 115, 127, 152, 155 C-96, 103, 136, 143	3.3 V ±5%	4 A (and max 0.3 A per pin)	Always active
VCC_2V5	A-53, 62, 65, 89 C-83, 123, 165	2.5 V ±5%	0.5 A	Controlled by PWR_EN
VCC_1V8	B-52, 76, 108, 128	1.8 V ±5%	0.5 A	Controlled by PWR_EN

Table 13: Voltage Supply Outputs

Warning!

Do not connect any power supply to the voltage supply outputs nor short circuit them to GND, as this may damage the Mercury+ SA2 SoC module.

2.11.5 Power Consumption

Please note that the power consumption of any SoC device strongly depends on the application (on the configured bitstream and I/O activity).

To estimate the power consumption of your design, please use the Intel PowerPlay Early Power Estimators (EPE) and Power Analyzer available on the Intel website.

2.11.6 Heat Dissipation

High performance devices like the Intel Cyclone V SoC need cooling in most applications; always make sure the SoC is adequately cooled.

For Mercury modules an Enclustra heat sink kit is available for purchase along with the product. It represents an optimal solution to cool the Mercury+ SA2 SoC module - the heat sink body is low profile and usually covers the whole module surface. The kit comes with a gap pad for the SoC device, a fan and required mounting material to attach the heat sink to the module PCB and baseboard PCB. With additional user configured gap pads, it is possible to cool other components on board as well.

Alternatively, if the Enclustra heat sink does not match the application requirements, a third-party heat sink body (ATS) and an additional gap pad (t-Global) may be used. Please note that the Enclustra heat sink kit already contains all necessary items for cooling the module (heat sink body, gap pad, fan, mounting material).

Table 14 lists the heat sink and thermal pad part numbers that are compatible with the Mercury+ SA2 SoC module. Details on the Mercury heatsink kit can be found in the Mercury Heatsink Application Note [17].

[2] The maximum available output current depends on your design. See sections 2.11.1 and 2.11.5 for details.

Product Name	Package Name	Enclustra Heat Sink	ATS Heat Sink	t-Global Thermal Pad
Mercury+ SA2	896-pin FBGA [24]	ACC-HS3-Set	ATS-52310G-C1-R0	TG-A6200-30-30-1

Table 14: Heat Sink Type

Please note that the adhesive heat sink part is recommended only for prototyping purposes. In cases where the module is used in environments subject to vibrations, additional mechanical fixation is recommended.

Warning!

Depending on the user application, the Mercury+ SA2 SoC module may consume more power than can be dissipated without additional cooling measures; always make sure the SoC is adequately cooled by installing a heat sink and/or providing air flow.

2.11.7 Voltage Monitoring

Several pins on the module connector on the Mercury+ SA2 SoC module are marked as VMON. These are voltage monitoring outputs that are used in the production test for measuring some of the on-board voltages.

It is not allowed to draw power from the voltage monitoring outputs.

Table 15 presents the VMON pins on the Mercury+ SA2 SoC module.

Pin Name	Module Connector Pin	Connection	Description
VMON_1V1	A-102	VCC_1V1	FPGA and HPS core voltages
VMON_1V2	B-167	VCC_1V2	1.2 V on-board voltage (default)/SoC battery voltage (assembly option)
VMON_1V55	B-168	VCC_1V55	Fast Ethernet PHYs supply voltage
VMON_1V35	B-8	VCC_1V35	DDR3 voltage

Table 15: Voltage Monitoring Outputs

Warning!

The voltage monitoring outputs are for Enclustra-use only. Pinout changes may be applied between revisions.

2.12 Clock Generation

A 50 MHz oscillator is used for the Mercury+ SA2 SoC module clock generation. The 50 MHz clock is fed to the HPS. A clock divider generates a 25 MHz clock for Ethernet and the second HPS clock.

Signal Name	Frequency	Destination	Remark
CLK_HPS1	50 MHz	HPS_CLK1	HPS clock 1
CLK_HPS2	25 MHz	HPS_CLK2	HPS clock 2
CLK_ETH0	25 MHz	Gigabit Ethernet PHY	-

Table 16: Module Clock Resources

2.13 Reset

The cold reset signal (POR) and the HPS warm reset signal (RST) of the SoC device are available on the module connector.

Pulling HPS_POR# low resets the SoC device and the QSPI flash. Further, the CONFIG# pin is pulled low to re-trigger the FPGA configuration. Please refer to the Enclustra Module Pin Connection Guidelines [10] for general rules regarding the connection of reset pins.

Pulling HPS_RST# low resets the SoC device. For details on the functions of the HPS_NPOR and HPS_NRST signals refer to the Intel documentation.

Table 17 presents the available reset signals. Both signals, HPS_POR# and HPS_RST#, have on-board 4.7 kΩ pull-up resistors to VCC_CFG_HPS.

Signal Name	Connector Pin	FPGA Pin Type	Description
HPS_POR#	A-132	HPS_NPOR	Cold reset
HPS_RST#	A-124	HPS_NRST	Warm reset

Table 17: Reset Resources

Please note that HPS_POR# is automatically asserted if PWR_GOOD is low.

2.14 LEDs

Three LEDs on the Mercury+ SA2 SoC module are connected to the FPGA logic and the HPS in parallel; it is recommended to drive the FPGA pins to a high impedance state before driving the HPS pins and vice versa. The fourth LED, LED3#, is connected only to the FPGA logic.

Signal Name	HPS GPIO	FPGA Pin	Remarks
LED0#	48	F6	User function/active-low
LED1#	49	G7	User function/active-low
LED2#	50	E6	User function/active-low
LED3#	-	E7	User function/active-low

Table 18: LEDs

2.15 DDR3L SDRAM

There is a single DDR3 SDRAM channel on the Mercury+ SA2 SoC module attached directly to the HPS side and is available only as a shared resource to the FPGA side.

The DDR3L SDRAM is connected to HPS I/O banks 6A and 6B, and it is always operated at 1.35 V (low power mode). Four 8-bit memory chips are used to build a 32-bit wide memory.

The maximum memory bandwidth on the Mercury+ SA2 SoC module is:
800 Mbit/sec × 32 bit = 3200 MB/sec

2.15.1 DDR3L SDRAM Type

Table 19 describes the memory availability and configuration on the Mercury+ SA2 SoC module.

Module	SDRAM Type	Density	Configuration	Manufacturer
ME-SA2-D11 (industrial)	K4B4G0846D-BMK0	4 Gbit	512 M × 8 bit	Samsung
ME-SA2-D11 (industrial)	K4B4G0846E-BMMA	4 Gbit	512 M × 8 bit	Samsung
ME-SA2-D11 (industrial)	NT5CC512M8CN-DII	4 Gbit	512 M × 8 bit	Nanya
ME-SA2-D11 (industrial)	NT5CC512M8DN-DII	4 Gbit	512 M × 8 bit	Nanya
ME-SA2-D11 (industrial)	NT5CC512M8EN-DII	4 Gbit	512 M × 8 bit	Nanya
ME-SA2-D11 (industrial)	NT5CC512M8EQ-EKI	4 Gbit	512 M × 8 bit	Nanya
ME-SA2-D11 (industrial)	MT41K512M8RH-125IT:E	4 Gbit	512 M × 8 bit	Micron

Table 19: DDR3L SDRAM Types

Warning!

Other DDR3L memory devices may be equipped in future revisions of the Mercury+ SA2 SoC module. Please check the user manual regularly for updates. Any parts with different speed bins or temperature ranges that fulfill the requirements for the module variant may be used.

2.15.2 Signal Description

Please refer to the Mercury+ SA2 SoC Module FPGA Pinout Excel Sheet [4] for detailed information on the DDR3L SDRAM connections.

2.15.3 Termination

Warning!

No external termination is implemented for the data signals on the Mercury+ SA2 SoC module. Therefore, it is strongly recommended to enable the on-die termination (ODT) feature of the DDR3 SDRAM device.

2.15.4 Parameters

Please refer to the Mercury+ SA2 SoC module reference design [2] for DDR3 settings guidelines. The DDR3L SDRAM parameters and the DDR3L board timing information to be set in Quartus project are presented in Tables 20 and 21.

The values given in Table 20 are for reference only. Depending on the equipped memory device on the Mercury+ SA2 SoC module and on the DDR3L SDRAM frequency, the configuration may be different to the one in the reference design. Please refer to the memory device datasheet for details.

Parameter	Value
SDRAM protocol	DDR3
PHY settings - supply voltage	1.35 V DDR3L
Memory device speed grade	400 MHz
Total interface width	32 bit
Row bits	16
Column bits	10
Bank bits	3
tRAS	37.5 ns
tRCD	15 ns
tRP	15 ns
tREFI	7.8 us
tRFC	260.0 ns
tWR	15.0 ns
tWTR	4 cycles
tFAW	40.0 ns
tRRD	10 ns
tRTP	10 ns

Table 20: DDR3L SDRAM Parameters

Parameter	Value
Maximum CK delay to DIMM/device	0.4 ns
Maximum DQS delay to DIMM/device	0.4 ns
Maximum skew within DQS group	0.05 ns
Maximum skew between DQS groups	0.05 ns

Table 21: DDR3L Board Timing

2.16 QSPI Flash

The QSPI flash can be used to boot the HPS, and to store the FPGA bitstream, ARM application code and other user data.

2.16.1 QSPI Flash Type

Table 22 describes the memory availability and configuration on the Mercury+ SA2 SoC module.

Flash Type	Size	Manufacturer
S25FL512S	512 Mbit	Cypress (Spansion)

Table 22: QSPI Flash Type

Warning!

Other flash memory devices may be equipped in future revisions of the Mercury+ SA2 SoC module. Please check the user manual regularly for updates. Any parts with different speeds and temperature ranges that fulfill the requirements for the module variant may be used.

2.16.2 Signal Description

The QSPI flash is connected to the HPS pins 29-34 and to the FPGA SPI configuration port. Some of the signals are available on the module connector, allowing the user to program the QSPI flash from an external master.

Please refer to Section 3 for details on programming the flash memory.

Warning!

Special care must be taken when connecting the QSPI flash signals on the base board. Long traces or high capacitance may disturb the data communication between the SoC and the flash device.

2.16.3 QSPI Flash Corruption Risk

There have been cases in which it was observed that the content of the flash device got corrupted. According to Cypress, this issue is caused by power loss during the Write Register (WRR) command. The most common reason to use the WRR command is to turn the QUAD bit ON or OFF - this operation takes place usually at the beginning of the boot process. If required, the bootloader code can be adjusted to set the QUAD bit to a fixed value, without invoking this command during boot.

For additional information on this issue, please refer to the Cypress documentation and forum discussions [25], [26].

2.17 SD Card

An SD card can be connected to the HPS_GPIOs available on the module connector. This allows the Mercury+ SA2 SoC module to boot from the SD card, as well as data access after booting. Information on SD card boot is available in Section 3.7.

Please note that external pull-ups are needed for SD card operation. Depending on the selected voltage for VCC_CFG_HPS, a level shifter to 3.3 V may be required (some level shifters also have built-in pull-ups).

2.17.1 Signal Description

HPS Pin	SD Card Signal	Connector Pin
36	CMD	A-93
38	D0	A-95
39	D1	A-97
45	CLK	A-91
46	D2	A-101
47	D3	A-103

Table 23: SD Card Signals

2.18 Gigabit Ethernet

A 10/100/1000 Mbit Ethernet PHY is available on the Mercury+ SA2 SoC module, connected to the HPS via RGMII interface.

2.18.1 Ethernet PHY Type

Table 24 describes the equipped Ethernet PHY device type on the Mercury+ SA2 SoC module.

PHY Type	Manufacturer	Type
KSZ9031RNX	Microchip (Micrel)	10/100/1000 Mbit

Table 24: Gigabit Ethernet PHY Type

2.18.2 Signal Description

The RGMII interface is connected to HPS pins for use with the hard macro MAC. The reset pin has a pull-down resistor and needs to be driven high to release the PHY from reset. A detailed list of the HPS connections is found in Section 2.9.7.

2.18.3 External Connectivity

The Ethernet signal lines can be connected directly to the magnetics. Please refer to the Enclustra Module Pin Connection Guidelines [10] for details regarding the connection of Ethernet signals.

2.18.4 MDIO Address

The MDIO address assigned to the Gigabit Ethernet PHY is 3. The MDIO interface is connected to the HPS pins 20-21.

2.18.5 PHY Configuration

The configuration of the Ethernet PHY is bootstrapped when the PHY is released from reset. Make sure all I/Os on the RGMII interface are initialized and all pull-up or pull-down resistors are disabled at that moment.

The bootstrap options of the Ethernet PHY are set as indicated in Table 25.

Please note that the RGMII delays in the Ethernet PHY need to be configured before the Ethernet interface can be used. This is done in the patch for the Preloader (SPL) provided in the Mercury+ SA2 SoC module reference design [2].

Pin	Signal Value	Description
MODE[3-0]	1110	RGMII mode: advertise all capabilities (10/100/1000, half/full duplex) except 1000Base-T half duplex.
PHYAD[2-0]	011	MDIO address 3
Clk125_EN	0	125 MHz clock output disabled
LED_MODE	1	Single LED mode
LED1/LED2	1	Active-low LEDs

Table 25: Gigabit Ethernet PHY Configuration

For the Ethernet PHY configuration via the MDIO interface, the MDC clock frequency must not exceed 1 MHz.

2.19 Dual Fast Ethernet

There are two 10/100 Mbit Ethernet PHYs equipped on the Mercury+ SA2 SoC module, connected to FPGA I/Os via MII interface.

2.19.1 Ethernet PHY Type

Table 26 describes the equipped Ethernet PHY device type on the Mercury+ SA2 SoC module.

PHY Type	Manufacturer	Type
TLK105LRHBR	Texas Instruments	10/100 Mbit

Table 26: Fast Ethernet PHY Type

2.19.2 Signal Description

The MII interfaces are connected to the FPGA pins in bank 3A for use with soft Ethernet MAC IP cores. The two Fast Ethernet PHYs have a shared MDIO interface and a shared interrupt line. Details on connections are available in the Mercury+ SA2 SoC Module User Schematics [5] and in the FPGA Pinout Excel Sheet [4].

The 25 MHz clock for the Fast Ethernet must be supplied via FPGA pin AD11.

Some of the MII signals have pull-up or pull-down resistors for bootstrapping. Make sure all FPGA internal resistors are disabled.

The reset signal of the Fast Ethernet PHYs has a pull-down resistor and is connected to HPS GPIO 35. It needs to be driven high to release the PHYs from reset.

2.19.3 External Connectivity

The Ethernet signal lines can be connected directly to the magnetics. Please refer to the Enclustra Module Pin Connection Guidelines [10] for details regarding the connection of Ethernet signals.

2.19.4 MDIO Address

The MDIO address assigned to the Fast Ethernet PHY A is 1, while the address assigned to PHY B is 2.

The MDIO interface is shared between the Gigabit Ethernet PHY and the two Fast Ethernet PHYs; the PHYs can be configured individually by using the corresponding addresses.

2.19.5 PHY Configuration

The configuration of the Ethernet PHY is bootstrapped when the PHY is released from reset. Make sure all I/Os on the MII interface are initialized and all pull-up or pull-down resistors are disabled at that moment.

The bootstrap options of the Ethernet PHY are set as indicated in Table 27.

Pin	Signal Value	Description
MII_MODE	0	MII mode
PHYAD[4-0]	00001 00010	PHY0: MDIO address 1 PHY1: MDIO address 2
LED_CFG	1	LED mode 1 (Link LED)
AMDIX_EN	1	Auto MDI-X enabled
AN_0	1	Auto-negotiation enabled

Table 27: Fast Ethernet PHY Configuration

For the Ethernet PHY configuration via the MDIO interface, the MDC clock frequency must not exceed 1 MHz.

2.20 Cypress FX3 USB 3.0 Controller

The Mercury+ SA2 SoC module features a USB 3.0 controller from Cypress, which allows data transfers to a host computer using speeds of over 300 MB/s.

The USB controller is connected to the FPGA module using a slave FIFO interface that can be configured for 16-bit or 32-bit mode using an interface clock of 100 MHz. The USB 3.0 controller includes a 32-bit ARM926 core operating at 200 MHz using a 19.2 MHz crystal oscillator. It can access the I2C bus and the QSPI flash.

The Cypress FX3 JTAG interface can be routed to the optional JTAG connector J1100. Please refer to Section 3.4.2 for details.

2.20.1 Cypress FX3 Type

Table 28 describes the equipped Cypress FX3 controller type on the Mercury+ SA2 SoC module.

Type	Manufacturer	Description
CYUSB3014	Cypress	USB 3.0 device controller (Cypress FX3) including USB 3.0 and USB 2.0 PHYs

Table 28: USB 3.0 Controller Type

2.20.2 Cypress FX3 Pinout

For details on FX3 interface pinout, please refer to the Mercury+ SA2 SoC Module FPGA Pinout Excel Sheet [4] and Mercury+ SA2 SoC Module User Schematics [5].

2.20.3 Functional Description

The FX3 controller is configured to boot from the FX3 SPI flash boot by default. The flash is factory programmed with a booloader that sets up all configuration pins of the FPGA correctly - if the FX3 bootloader is deleted or overwritten, the FPGA may not work correctly anymore.

Please make sure all configuration pins are properly setup if you load a custom FX3 firmware - in case a wrong firmware has been programmed to the FX3 SPI flash, the SPI flash boot can be prevented by shorting R1608 (see Figure 11).

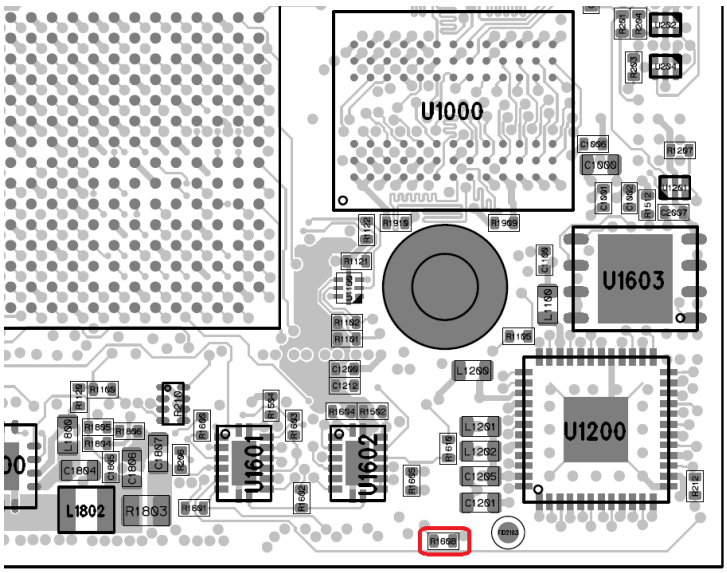

Figure 11: FX3 SPI Flash Boot Bypass

For more information on the FPGA configuration pins, refer to Section 3.

2.21 USB 2.0

The Mercury+ SA2 SoC module has an on-board USB 2.0 PHY connected to the SoC device. The USB interface can be configured for USB host or for USB device.

Please note that simultaneous usage of the USB 3.0 device interface (FX3) and USB 2.0 in device mode is not USB compliant; the Mercury pinout does not support voltage detection for each USB interface.

2.21.1 USB PHY Type

Table 29 describes the equipped USB PHY device type on the Mercury+ SA2 SoC module.

PHY Type	Manufacturer	Type
USB3320C	Microchip	USB 2.0 PHY

Table 29: USB 2.0 PHY Type

2.21.2 Signal Description

The ULPI interface is connected to HPS pins for use with the integrated USB controller. The USB reset has a pull-down resistor and needs to be driven high to release the PHY from reset.

A detailed list of the HPS connections is found in Section 2.9.7.

2.22 Real-Time Clock (RTC)

A real-time clock is connected to the I2C bus. The RTC features a battery-buffered 128 bytes user SRAM and a temperature sensor. See Section 4 for details on the I2C bus on the Mercury+ SA2 SoC module.

VBAT pin of the RTC is connected to VCC_BAT on the module connector, and can be connected directly to a 3 V battery. Please refer to the Enclustra Module Pin Connection Guidelines [10] for details.

2.22.1 RTC Type

Table 30 describes the equipped RTC device type on the Mercury+ SA2 SoC module.

Type	Manufacturer
ISL12020MIRZ	Intersil

Table 30: RTC Type

An example demonstrating how to use the RTC is included in the Mercury+ SA2 SoC module reference design [2].

2.23 Secure EEPROM

The secure EEPROM is used to store the module type and serial number, as well as the Ethernet MAC address and other information. It is connected to the I2C bus.

The secure EEPROM must not be used to store user data.

Please refer to Section 4.4 for details on the content of the EEPROM.

2.23.1 EEPROM Type

Table 31 describes the equipped EEPROM device type on the Mercury+ SA2 SoC module.

Type	Manufacturer
ATSHA204A-MAHDA-T (default)	Atmel
DS28CN01 (assembly option)	Maxim

Table 31: EEPROM Type

An example demonstrating how to read data from the EEPROM is included in the Mercury+ SA2 SoC module reference design [2].

3 Device Configuration

3.1 Configuration Signals

Table 32 describes the most important configuration pins.

Signal Name	FPGA Pin	HPS Pin	QSPI Flash Pin	Module Connector Pin	Comments
FLASH_CLK	DCLK	GPIO 34	CLK	A-118	4.7 kΩ pull-up to VCC_CFG_HPS
FLASH_CS#	CSO#	GPIO 33	CS#	A-116	Depending on the boot mode
FLASH_DI	ASDATA0_ASDO	GPIO 29	SI/IO0	A-114	4.7 kΩ pull-up to VCC_CFG_HPS
FLASH_DO	ASDATA1	GPIO 30	SO/IO1	A-122	9.4 kΩ pull-up to VCC_CFG_HPS
FLASH_IO2	ASDATA2	GPIO 31	IO2	-	-
FLASH_IO3	ASDATA3	GPIO 32	IO3	-	-
HPS_RST#	-	HPS_RST#	-	A-124	4.7 kΩ pull-up to VCC_CFG_HPS
HPS_POR#	CONFIG#	HPS_POR#	RESET#	A-132	4.7 kΩ pull-up to VCC_CFG_HPS
FPGA_CONFDONE	CONFDONE	-	-	A-130	1 kΩ pull-up to VCC_CFG_HPS
BOOT_MODE0	-	GPIO 40	-	A-126	4.7 kΩ pull-up to VCC_CFG_HPS
BOOT_MODE1	-	GPIO 42	-	A-112	4.7 kΩ pull-up to VCC_CFG_HPS

Table 32: FPGA and HPS Configuration Pins

Warning!

All configuration signals except for BOOT_MODE must be high impedance as soon as the device is released from reset. Violating this rule may damage the equipped SoC device, as well as other devices on the Mercury+ SA2 SoC module.

HPS and FPGA Configuration Pins

The BSEL and CSEL pins determine in which memory interface is the boot loader stored and how to clock the interface; details on BSEL and CSEL pins when using the HPS boot are available in the Booting and Configuration Introduction document [20]. The MSEL pins, which are used to select an FPGA configuration scheme, are described in the Cyclone V Device Handbook [19].

3.2 Module Connector C Detection

Signal C_PRSNT# (pin C-167) must be connected to GND on the base board if the designed base board has three connectors. Depending on the value of this pin, the FPGA banks routed to module connector C are supplied with the voltages provided by the user (when C_PRSNT# is low) or with a default voltage of 1.8 V (when C_PRSNT# is unconnected).

C_PRSNT# is equipped with a 4.7 kΩ pull-up resistor on the module.

3.3 Boot Mode

The BOOT_MODE signals determine whether the SoC device boots from the QSPI flash or from an SD card connected to the SD pins on the HPS bank.

Table 33 describes the available boot modes and the corresponding boot mode signals.

BOOT_MODE1	BOOT_MODE0	HPS boot	FPGA boot	MSEL[4:0]	CSEL[1:0]	BSEL[2:0]
0	0	from FPGA	passive serial	10000	00	001
0	1	reserved	reserved	10010	00	10X[3]
1	0	QSPI	from HPS	00010	00	11X[3]
1	1	SDIO	from HPS	00010	00	10X[3]

Table 33: Boot Modes

Please note that the passive serial mode is not supported on the Mercury+ SA2 SoC module nor has it been tested on Enclustra side.

3.4 JTAG

The FPGA and the HPS JTAG interfaces are connected into one single chain available on the module connector. If required for a third-party ARM debugger, the HPS JTAG interface may be routed to an optional JTAG connector (J1100) on the Mercury+ SA2 SoC module.

The SoC device and the QSPI flash can be configured via JTAG using Intel tools.

The Mercury+ SA2 SoC module is compatible with Intel FPGA download cable (Blaster) I and II. Terasic USB Blaster is compatible with the module, provided that the VCC_CFG_HPS is in the 2.5 V - 3.3 V voltage range.

When the VCC_CFG_HPS is set to 1.8 V, the JTAG interface is functional only if the JTAG clock frequency is lowered. This is an intermittent timing issue that affects revision 1 modules and which is planned to be fixed

[3] BSEL[0] depends on the VCC_CFG_HPS voltage: it is set to 0 for 1.8 V and 1 for 2.5-3.3 V

in future revisions.

By default, the JTAG clock frequency is set to 24 MHz; to lower the frequency (for example to 16 MHz), the following command can be used in the SoCEDS console:

```
jtagconfig --setparam 1 JtagClock 16M
```

3.4.1 JTAG on Module Connector

Signal Name	Module Connector Pin	Resistor
JTAG_TCK	A-123	4.7 kΩ pull-down
JTAG_TMS	A-119	4.7 kΩ pull-up to VCC_CFG_HPS
JTAG_TDI	A-117	4.7 kΩ pull-up to VCC_CFG_HPS
JTAG_TDO	A-121	-

Table 34: JTAG Interface

3.4.2 HPS JTAG Connector

Figure 12 presents the pinout of the HPS JTAG connector. To enable the HPS JTAG port on J1100, JTAG_PRESENT# (pin 9) must be pulled low. J1100 connector is not equipped in the standard configuration. If needed, a 10-pin 1.27 mm pinheader (e.g. Sullins GRPB052VWQS-RC) can be mounted.

In order to enable the return clock path for the HPS JTAG debug connector, pins 4 and 7 of J1000 must be connected together, by mounting the R1107 resistor as displayed in the Figure 12.

Cypress FX3 is also connected to the HPS JTAG connector. Note that the FX3 JTAG connection is not equipped in the standard configuration (the resistors are marked with DNE - Do Not Equip). In order to use the FX3 JTAG, some of the resistors present on the module need to be removed, while the resistors on the JTAG lines must be mounted. Figure 13 indicates the location of the resistors on the module PCB - upper right part on the top view drawing, respectively upper left part on the bottom view drawing.

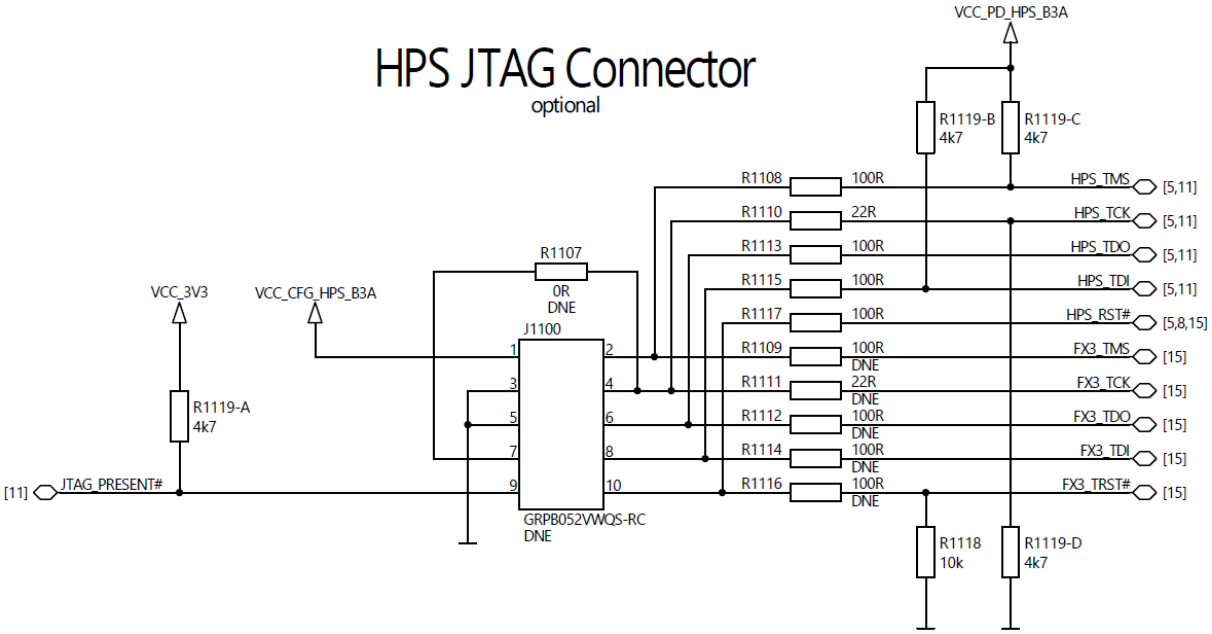

Figure 12: HPS JTAG Connector

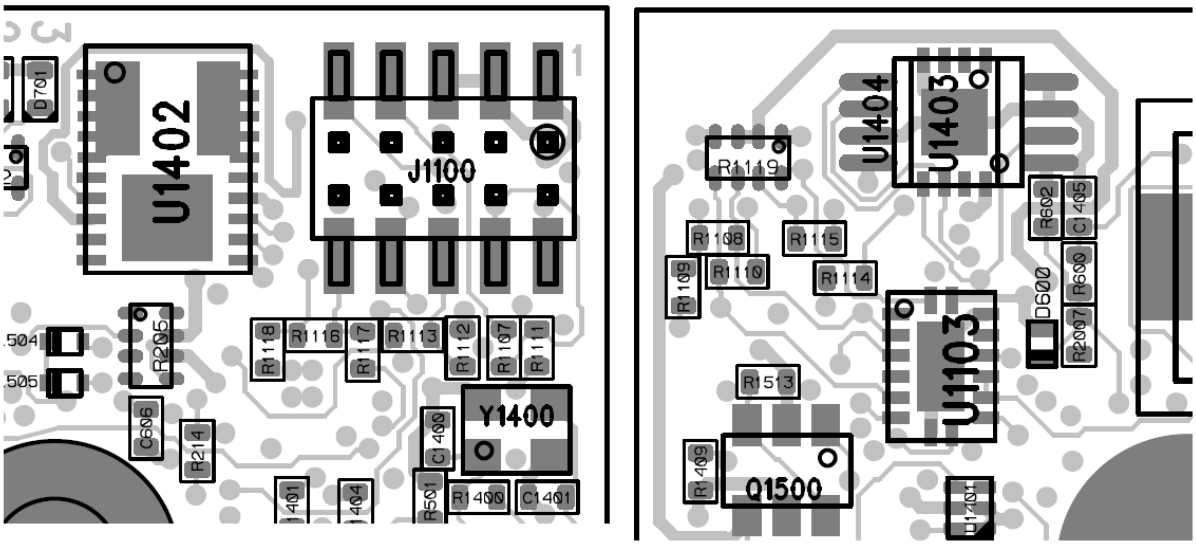

Figure 13: HPS JTAG Connector Resistors - Assembly Drawing Top and Bottom Views

3.4.3 External Connectivity

JTAG signals can be connected directly on the base board to a JTAG connector. No pull-up/pull-down resistors are necessary. The VCC pin of the programmer must be connected to VCC_CFG_HPS.

It is recommended to add 22 Ω series termination resistors between the module and the JTAG header, close to the source. Please refer to the Enclustra Module Pin Connection Guidelines for details on JTAG interface.

3.5 Passive Serial Configuration

In the passive serial configuration mode the FPGA bitstream is programmed from an external source into the SPI port of the FPGA. The HPS is configured afterwards via HPS2FPGA bridge. For more information, please refer to the Cyclone V datasheet [18].

3.6 QSPI Boot Mode

In the QSPI boot mode, the HPS boots from the QSPI flash and configures the FPGA logic from the HPS. The HPS configuration and the FPGA bitstream need to be stored in a boot image. For more information, please refer to the Cyclone V datasheet [18].

3.7 SD Card Boot Mode

In the SD card boot mode, the HPS boots from the SD card located on the base board and configures the FPGA logic from the HPS. The HPS configuration and the FPGA bitstream need to be stored in a boot image. For more information, please refer to the Cyclone V datasheet [18].

3.8 QSPI Flash Programming via JTAG

The Intel Quartus software offers QSPI flash programming support via JTAG. For more information, please refer to the Quartus user manual [22].

The process of programming the QSPI flash via JTAG using "quartus_hps" tool can take up to 30 minutes.

3.9 QSPI Flash Programming from an External SPI Master

The signals of the QSPI flash are directly connected to the module connector for flash access. As the flash signals are connected to the SoC device as well, the SoC device pins must be tri-stated while accessing the QSPI flash directly from an external device.

This is ensured by pulling the HPS_RST# signal to GND followed by a pulse on HPS_POR#, which puts the SoC device into reset state and tri-states all I/O pins. HPS_RST# must be low when HPS_POR# is released and kept low until the flash programming has finished. Afterwards, all SPI lines and HPS_RST# must be tri-stated and another reset impulse must be applied to HPS_POR#.

Figure 14 shows the signal diagrams corresponding to flash programming from an external master.

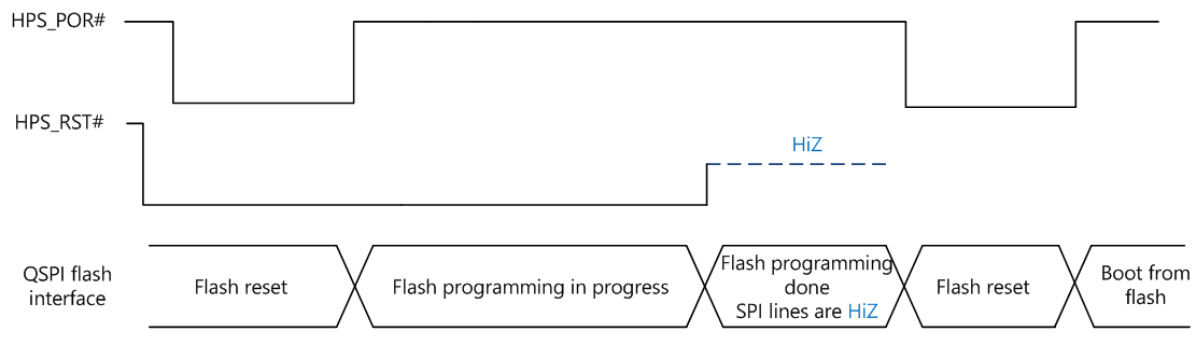

Figure 14: QSPI Flash Programming from an External SPI Master - Signal Diagrams

Warning!

Accessing the QSPI flash directly without putting the SoC device into reset may damage the equipped SoC device, as well as other devices on the Mercury+ SA2 SoC module.

3.10 Enclustra Module Configuration Tool

The QSPI flash on the Mercury+ SA2 SoC module can be programmed via Cypress FX3 using the Enclustra Module Configuration Tool (MCT) [16].

4 I2C Communication

4.1 Overview

The I2C bus on the Mercury+ SA2 SoC module is connected to the SoC device, EEPROM, RTC and FX3 USB 3.0 controller, and is available on the module connector. This allows external devices to read the module type and to connect more devices to the I2C bus.

The I2C clock frequency should not exceed 400 kHz.

Warning!

Maximum I2C speed may be limited by the routing path and additional loads on the base board.

Warning!

If the I2C traces on the base board are very long, 100 Ω series resistors should be added between module and I2C device on the base board.

4.2 Signal Description

Table 35 describes the signals of the I2C interface. All signals have on-board pull-up resistors to VCC_3V3.

All signals must be connected to open collector outputs and must not be driven high from any source. I2C_INT# is an input to the SoC and must not be driven from the SoC device.

Level shifters are used between the I2C bus and the HPS pins, to allow I/O voltages lower than 3.3 V.

Signal Name	SoC Pin	Connector Pin	Resistor
I2C_SDA	HPS_GPIO55	A-113	2.2 kΩ pull-up
I2C_SCL	HPS_GPIO56	A-111	2.2 kΩ pull-up
I2C_INT#	HPS_GPIO54	A-115	4.7 kΩ pull-up

Table 35: I2C Signal Description

4.3 I2C Address Map

Table 36 describes the addresses for several devices connected on I2C bus.

Address (7-bit)	Description
0x64	Secure EEPROM
0x5C	Secure EEPROM (assembly option, refer to Section 2.23)
0x57	RTC user SRAM
0x6F	RTC registers

Table 36: I2C Addresses

4.4 Secure EEPROM

The secure EEPROM is used to store the module serial number and configuration. In the future, the EEPROM will be used for copy protection and licensing features. Please contact us for further information.

An example demonstrating how to read the module information from the EEPROM memory is included in the Mercury+ SA2 SoC module reference design.

Warning!

The secure EEPROM is for Enclustra use only. Any attempt to write data to the secure EEPROM causes the warranty to be rendered void.

4.4.1 Memory Map

Address	Length (bits)	Description
0x00	32	Module serial number
0x04	32	Module product information
0x08	32	Module configuration
0x0C	32	Reserved
0x10	48	Ethernet MAC address
0x16	48	Reserved
0x1C	32	Checksum (only for DS28CN01 EEPROM type)

Table 37: EEPROM Sector 0 Memory Map

Module Serial Number

The module serial number is a unique 32-bit number that identifies the module. It is stored using big-endian byte order (MSB on the lowest address).

Module Product Information

This field indicates the type of module and hardware revision.

Module	Product Family	Reserved	Revision	Product Information
Mercury+ SA2 SoC module	0x032A	0x[XX]	0x[YY]	0x032A [XX][YY]

Table 38: Product Information

Module Configuration

Addr.	Bits	Comment	Min. Value	Max. Value	Comment
0x08	7-4	SoC Type	0	0	See SoC type table (Table 40)
	3-0	SoC device speed grade	6	8	
0x09	7	Temperature range	0 (Commercial)	1 (Industrial)	
	6	Power grade	0 (Normal)	1 (Low Power)	
	5-4	Fast Ethernet port count	0	2	
	3	Gigabit Ethernet port count	0	1	
	2	RTC equipped	0	1	
	1-0	Reserved	-	-	
0x0A	7-2	Reserved	-	-	
	1	USB 2.0 port count	0	1	
	0	USB 3.0 device port count	0	1	
0x0B	7-4	DDR3L RAM size (MB)	0 (0 MB)	10 (4 GB)	Resolution = 8 MB
	3-0	QSPI flash memory size (MB)	0 (0 MB)	7 (64 MB)	Resolution = 1 MB

Table 39: Module Configuration

The memory sizes are defined as Resolution$\times 2^{(Value-1)}$ (e.g. DRAM=0: not equipped, DRAM=1: 8 MB, DRAM=2: 16 MB, DRAM=3: 32 MB, etc).

Table 40 shows the available SoC types.

Value	SoC Device Type
0	5CSTFD6D5F31

Table 40: SoC Device Types

Ethernet MAC Address

The Ethernet MAC address is stored using big-endian byte order (MSB on the lowest address). Each module is assigned two sequential MAC addresses; only the lower one is stored in the EEPROM.

5 Operating Conditions

5.1 Absolute Maximum Ratings

Table 41 indicates the absolute maximum ratings for Mercury+ SA2 SoC module. The values given are for reference only; for details please refer to the Cyclone V Datasheet [18].

Symbol	Description	Rating	Unit
VCC_MOD	Supply voltage relative to GND	-0.5 to 16	V
VCC_BAT	Supply voltage for the RTC and encryption key storage	-0.3 to 3.6	V
VCC_IO_[x] VCC_CFG_[x]	Output drivers supply voltage relative to GND	-0.5 to 3.6	V
V_IO	I/O input voltage relative to GND	-0.5 to V_{CCIO}+0.5	V
Temperature	Temperature range for commercial modules (C)* Temperature range for industrial modules (I)*	0 to +70 -40 to +85	°C °C

Table 41: Absolute Maximum Ratings

5.2 Recommended Operating Conditions

Table 42 indicates the recommended operating conditions for Mercury+ SA2 SoC module. The values given are for reference only; for details please refer to the Cyclone V Datasheet [18].

Symbol	Description	Rating	Unit
VCC_MOD	Supply voltage relative to GND	4.75 to 15.75	V
VCC_BAT	Supply voltage for the RTC and encryption key storage	2.0 to 3.45	V
VCC_IO_[x] VCC_CFG_[x]	Output drivers supply voltage relative to GND	Refer to Section 2.9.5	V
V_IO	I/O input voltage relative to GND	-0.2 to V_{CCIO}+0.2	V
Temperature	Temperature range for commercial modules (C)* Temperature range for industrial modules (I)*	0 to +70 -40 to +85	°C °C

Table 42: Recommended Operating Conditions

Warning!

** The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.*

6 Ordering and Support

6.1 Ordering

Please use the Enclustra online request/order form for ordering or requesting information:
`http://www.enclustra.com/en/order/`

6.2 Support

Please follow the instructions on the Enclustra online support site:
`http://www.enclustra.com/en/support/`

List of Figures

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References

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