Product Document

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TMG49037

Gesture, Color and Proximity Sensor Module

General Description

The TMG49037 features gesture, ambient light and color (RGB) sensing and proximity. In addition, the device integrates an IR LED and advanced LED driver, all within a low-profile and small footprint, 2.0mm x 5.0mm x 1.0mm package.

The Gesture and Proximity sensing function synchronizes IR emission and detection to sense gesture and proximity events. The architecture of the engine features automatic high sample rate activation, self-maximizing dynamic range, ambient light subtraction, advanced crosstalk cancelation, 14-bit data output, 32-dataset FIFO, and interrupt-driven I^2C communication. Sensitivity, power consumption, and noise can be optimized with adjustable IR LED timing and power. The gesture engine is capable of 3D detection of motion and position. Gesture interrupts are configurable to reduce I^2C communication load.The proximity engine recognizes detect/release events and produces a configurable interrupt whenever proximity result crosses upper or lower threshold settings.

The Ambient Light and Color Sensing function provides Red, Green, and Blue (RGB) ambient light sensing with a Clear reference (C). The color diode array has a UV/IR blocking filter and parallel ADCs to produce simultaneous 16-bit results. This architecture accurately measures ambient light and enables the calculation of illuminance, chromaticity, and color temperature to manage display appearance.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TMG49037, Gesture, Color and Proximity Sensor Module are listed below:

Figure 1:
Added Value of Using TMG49037

Benefit	Feature
• 2D and 3D gesture and proximity detection	• Automatic sample rate adjustment (1) • Self-maximizing dynamic range (2) • 2D and 3D gesture detect • Ambient light rejection • Advanced crosstalk compensation • AFE saturation flag • Programmable LED driver • Interrupt-driven I^2C communication
• Ambient light and color sensing	• Variable sensitivity • Designed to operate behind inked glass • UV/IR blocking filter • Programmable gain and integration time • 6.7M:1 dynamic range by gain adjustment only • Interrupt-driven I^2C communication
• Integrated LED and driver	• Calibrated emission and response • Invisible 950nm emission
• Low supply voltage	• 1.8V operation

Note(s):

1. While an object is detected, the sample rate increases automatically to improve response.
2. Device sensitivity is automatically adjusted based on reflected response to support a wide detection distance.

Applications

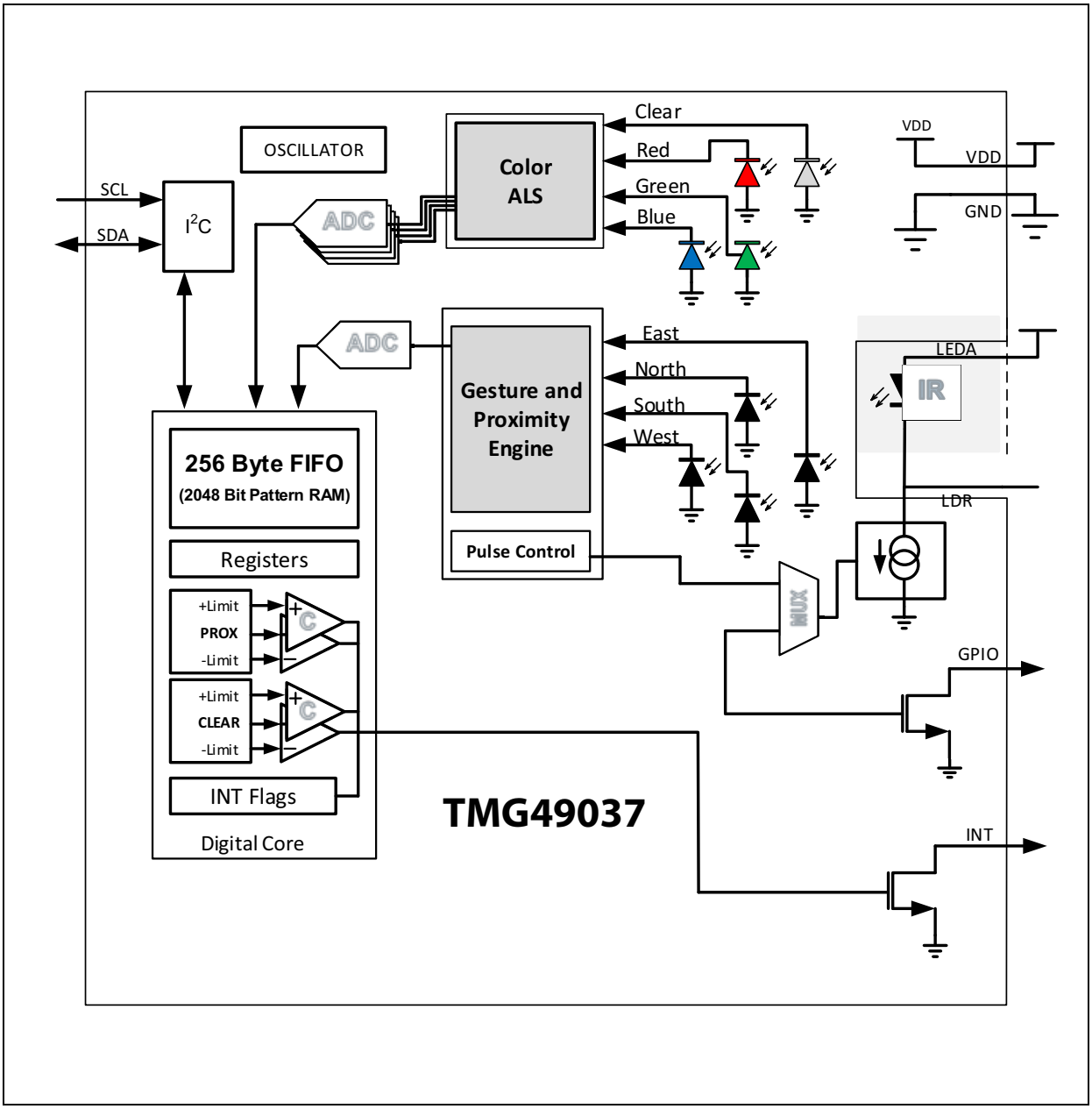
The TMG49037 applications include:

- Gesture detection
- Color sensing
- Ambient light sensing
- Cell phone touch screen disable
- Mechanical switch replacement

Block Diagram

The functional blocks of this device are shown below:

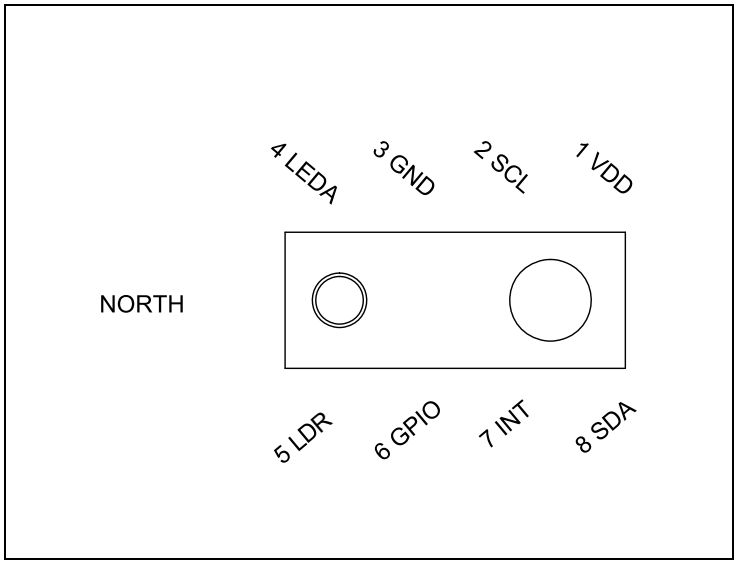
Figure 2:
TMG49037 Block Diagram



Pin Assignment

The device pin assignments are described below.

Figure 3:
Pin Diagram



Pin Description

Figure 4:
Pin Description

Pin Number	Pin Name	Description
1	V_{DD}	Supply voltage (1.8V)
2	SCL	I^2C serial clock terminal
3	GND	Ground. All voltages are referenced to GND
4	LEDA	LED anode
5	LDR	LED driver (sinks current) and LED cathode (for direct access to LED)
6	GPIO	Open drain output or alternate interrupt
7	INT	Interrupt. Open drain output and logic level output for external IR LED circuit
8	SDA	I^2C serial data I/O terminal

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
V_{DD}	Supply voltage	-0.3	2.2	V	
V_{LEDA}	LED anode supply	-0.3	3.6	V	
V_{IO}	Digital I/O terminal voltage	-0.3	3.6	V	
V_{LDR}	Terminal voltage	-0.3	3.6	V	See note (2)
I_{IO}	Output terminal current	-1	20	mA	
T_{strg}	Storage temperature range	-40	85	°C	
ESD_{HBM}	ESD tolerance, human body model	±2000		V	

Note(s):

1. All voltages with respect to GND
2. Measured with LDR = OFF or LDR = ON and LDRIVE = 310mA.

Electrical Characteristics

The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Supply voltage	1.7	1.8	2.0	V
T_A	Operating free-air temperature (1)	-30		85	°C

Note(s):

1. While the device is operational across the temperature range, functionality will vary with temperature. Specifications are stated at 25°C, unless otherwise noted.

Figure 7:
Operating Characteristics, VDD = 1.8 V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{OSC}	Oscillator frequency			8.1		MHz
I_{DD}	Supply current (1)	Active ALS state (PON=AEN=1, PEN=0) (2)		150	200	µA
		Idle state (PON=1, AEN=PEN=0) (3)		30	60	
		Sleep state (4)		0.4	5	
V_{OL}	INT, SDA, GPIO output low voltage	6 mA sink current			0.6	V
I_{LEAK}	Leakage current, SDA, SCL, INT, GPIO, LDR pins		-5		5	µA
V_{IH}	SCL, SDA input high voltage		1.26			V
V_{IL}	SCL, SDA input low voltage				0.54	V

Note(s):

1. Values are shown at the VDD pin and do not include current through the IR LED.
2. This parameter indicates the supply current during periods of ALS integration. If Wait is enabled (WEN=1), the supply current is lower during the Wait period.
3. Idle state occurs when PON=1 and all functions are not enabled.
4. Sleep state occurs when PON = 0 and I^2C bus is idle. If Sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.

Figure 8:
ALS/Color Operating Characteristics, VDD = 1.8 V, T_A = 25°C, AGAIN = 16x, ATIME = 0xF6 (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Integration time step size (1), (2)		2.68	2.78	2.90	ms
Dark ADC count value (2)	E_e = 0 µW/ cm^2 AGAIN: 64x ATIME: 100ms (0xDC)	0	1	3	counts
Gain scaling, relative to 16x gain setting	AGAIN: 1/4x	0.0135		0.0175	x
	AGAIN: 1x	0.058		0.067	
	AGAIN: 4x	0.237		0.263	
	AGAIN: 64x	3.75		4.37	
Clear channel irradiance responsivity	White LED, 2700K	8.94	10.28	11.62	counts/ (µW/ cm^2)
Lux accuracy (3)	White LED, 2700K	90	100	110	%
ADC Noise (4)	AGAIN: 16x		0.005		% Full Scale

Note(s):

1. Integration time is configured from 1 step (0xFF) to 256 steps (0x00) for a typical range of 2.78ms to 711.11ms. An ATIME setting of 0xFF results in a full-scale count value of 1024. Each additional integration step adds 1024 counts to full scale. To enable 16-bit ADC range, 64 or more integration steps (177.8ms or more) are required (ATIME <= 0xC0).
2. The typical 3-sigma distribution is between 0 and 1 count for an AGAIN setting of 16x.
3. Lux accuracy is function of red, green, blue and clear channels, and not 100% production tested.
4. ADC noise is calculated as the standard deviation of 1000 data samples.

Figure 9:
Color Ratio Characteristics, VDD = 1.8V, T_A = 25°C

Parameter	Test Conditions	Ratio of Color to Clear Channel					
		Red Channel		Green Channel		Blue Channel	
		Min	Max	Min	Max	Min	Max
Color ADC count value ratio: Color/Clear	White LED, 2700 K	45%	65%	19%	39%	15%	40%
	λ_D = 465 nm (1)	0%	15%	10%	42%	70%	90%
	λ_D = 525 nm (2)	4%	25%	60%	85%	10%	45%
	λ_D = 615 nm (3)	80%	110%	0%	14%	5%	24%

Note(s):

1. The 465 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 465 nm, spectral halfwidth $\Delta\lambda_{½}$ = 22 nm.
2. The 525 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 525 nm, spectral halfwidth $\Delta\lambda_{½}$ = 35 nm.
3. The 615 nm input irradiance is supplied by an AlInGaP light-emitting diode with the following characteristics: dominant wavelength λ_D = 615 nm, spectral halfwidth $\Delta\lambda_{½}$ = 15 nm.

Figure 10:
Gesture and Proximity Operating Characteristics, VDD = 1.8 V, T_A = 25°C (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Unit
ADC conversion time step size			20		µs
Offset (no target response) (1)	PGAIN = 2 (4x) PGLDRIVE = 7 (150mA) PGPULSE_LEN = 1 (8µs) No target present After electrical calibration		16	36	counts
Part to part variation (2)	PGAIN = 2 (4x) PGLDRIVE = 1 (30mA) PGPULSE_LEN = 1 (8µs) d=23mm round target 30mm target distance After electrical calibration	75	100	125	%
Response, absolute (3)	PGAIN = 2 (4x) PGLDRIVE = 7 (150mA) PGPULSE_LEN = 1 (8µs) 100x100mm, 90% reflective Kodak gray card 100mm target distance After electrical calibration	670	840	1010	counts
Photodiode relative deviation, north and south channels (4)		-25		25	%
Photodiode relative deviation, east and west channels (4)		-25		25	
Noise/Signal (5)	PGAIN = 2 (4x) PGLDRIVE = 2 (50mA) PGPULSE_LEN = 1 (8µs) PGPULSE = 7 (8 pulses)			2	%

Note(s):

1. Offset varies with power supply characteristics and system noise.
2. Production tested result is the average of 5 readings expressed relative to a calibrated response.
3. Representative result by characterization. Device settings can vary from 1 to 64 pulse count, 4µs to 32µs pulse width, 10mA to 310mA current setting, and 1x to 8x electrical gain. Refer to Figure 21 for device performance with different settings.
4. Relative mismatch in the response between opposing channels.
5. Production tested result is the standard deviation of 20 readings as a percentage of full scale response.

Figure 11:
Proximity Test Circuit

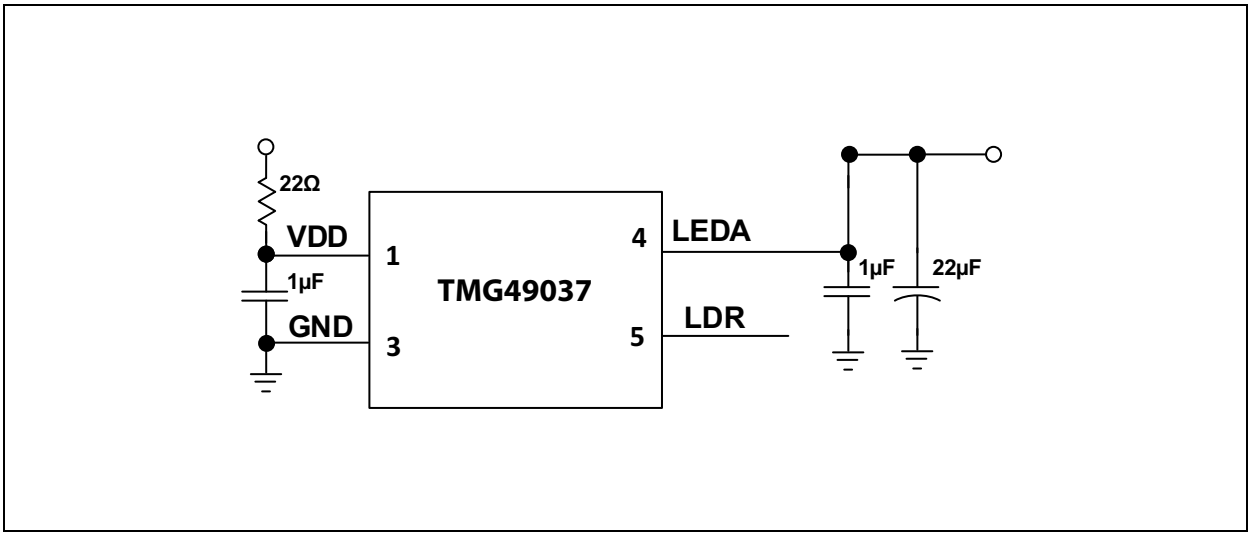


Figure 12:
Wait Characteristics, VDD = 1.8 V, T_A = 25°C, WEN = 1 (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Wait step size		2.68	2.78	2.90	ms
Long wait step size			33.3		ms

Timing Characteristics

Figure 13:
AC Electrical Characteristics, VDD = 1.8 V, T_A = 25°C (unless otherwise noted)

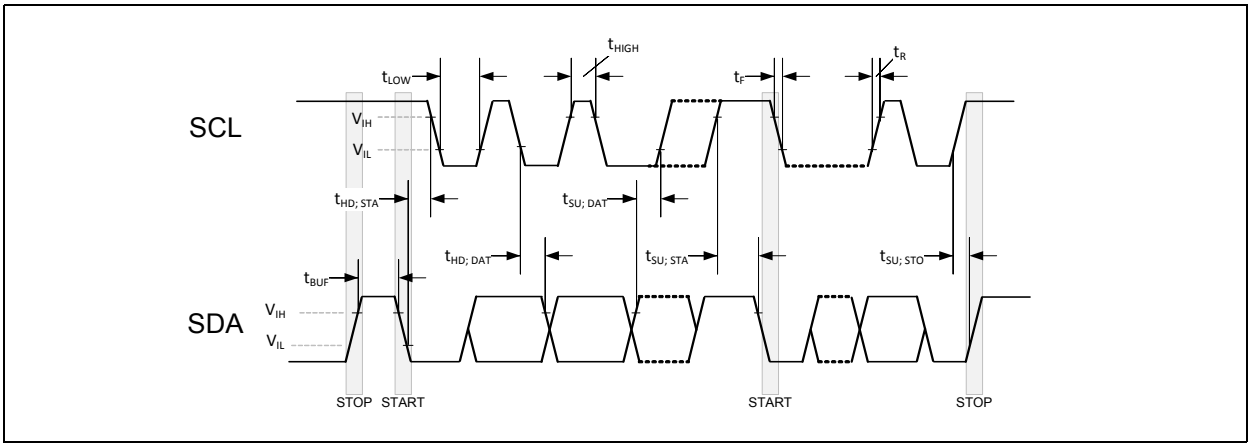
Parameter	Description	Min	Typ	Max	Unit
f_{SCL} (1)	Clock frequency (I^2C only)	0		400	kHz
t_{BUF} (1)	Bus free time between start and stop condition	1.3			µs
$t_{HS;STA}$ (1)	Hold time after (repeated) start condition. After this period, the first clock is generated.	0.6			µs
$t_{SU;STA}$ (1)	Repeated start condition setup time	0.6			µs
$t_{SU;STO}$ (1)	Stop condition setup time	0.6			µs
$t_{HD;DAT}$ (1)	Data hold time	0			ns
$t_{SU;DAT}$ (1)	Data setup time	100			ns
t_{LOW} (1)	SCL clock low period	1.3			µs
t_{HIGH} (1)	SCL clock high period	0.6			µs
t_F (1)	Clock/data fall time			300	ns
t_R (1)	Clock/data rise time			300	ns
C_i (1)	Input pin capacitance			10	pF

Note(s):

1. Specified by design and characterization; not production tested.

Timing Diagram

Figure 14:
Timing Parameter Measurement Drawing



Typical Operating Characteristics

Figure 15:
Spectral Responsivity

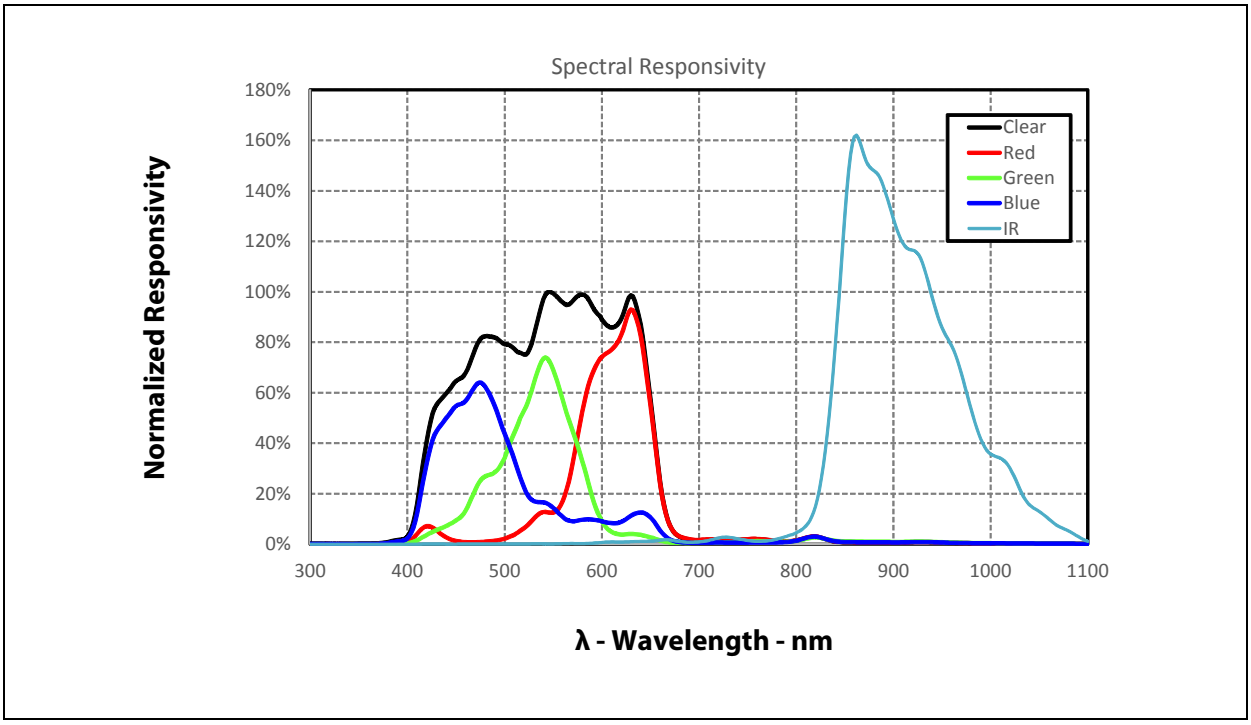


Figure 16:
CRGB Responsivity vs. Angular Displacement

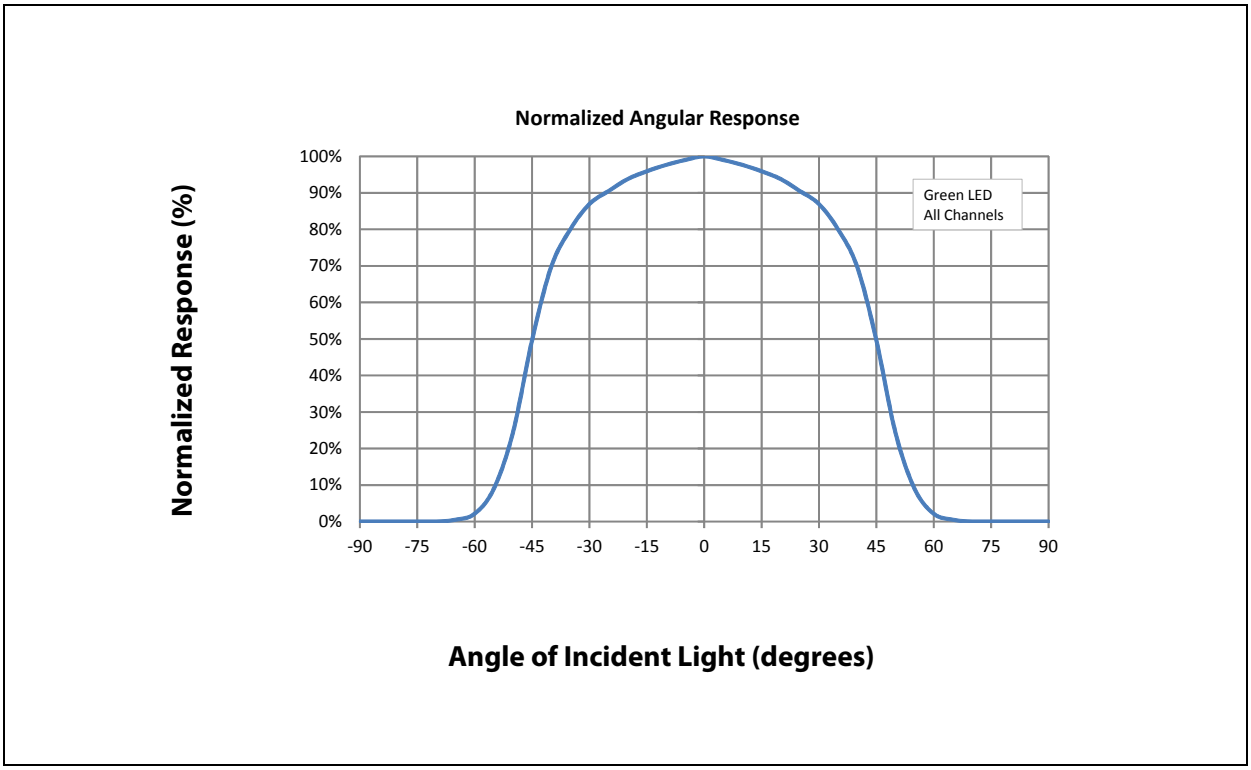


Figure 17:
Typical LDR Current vs. Voltage

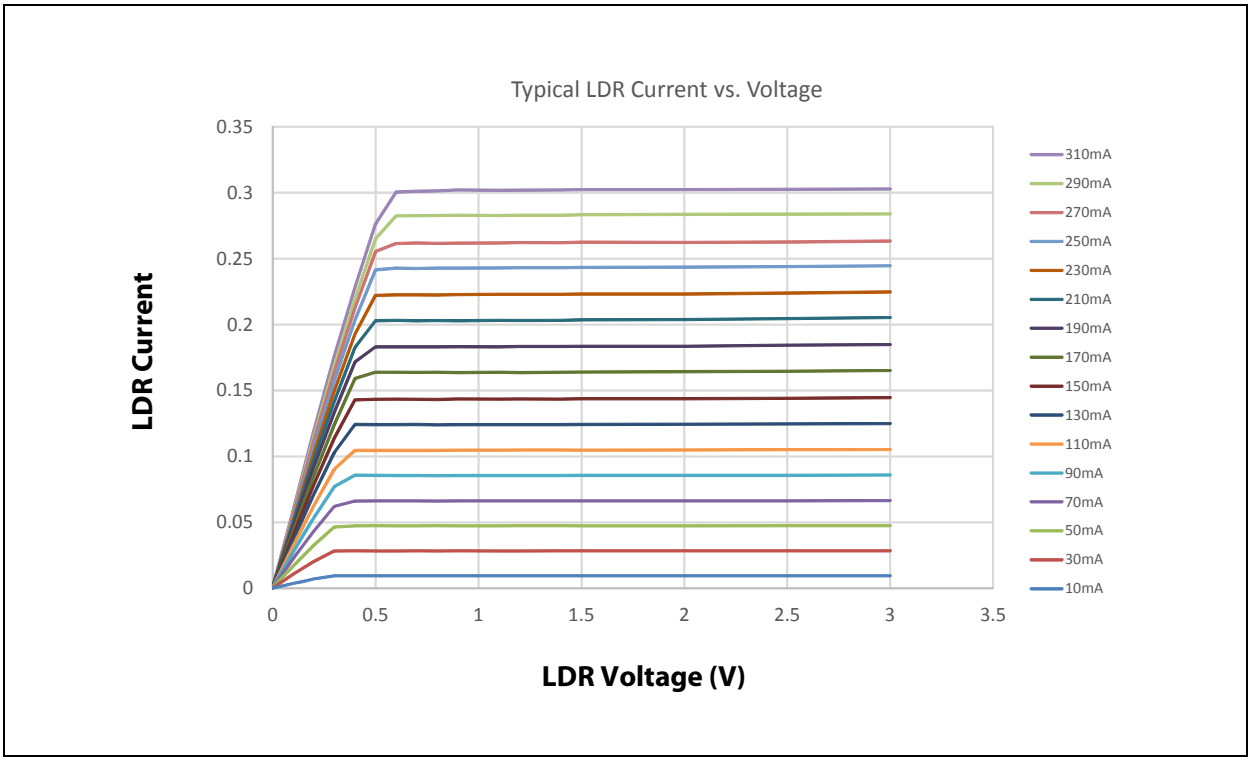


Figure 18:
Responsivity Temperature Coefficient

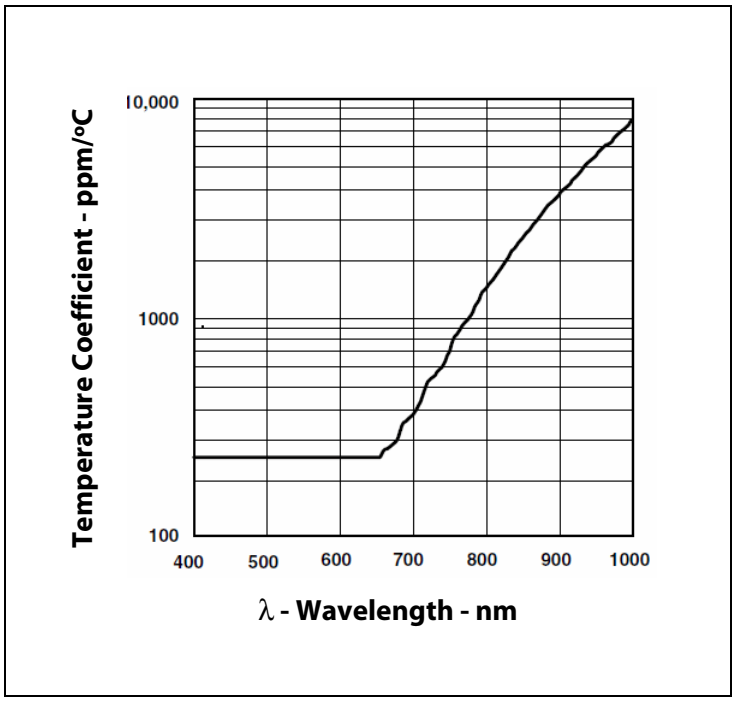


Figure 19:
Illuminance (Lux) vs. Counts (Clear Channel)

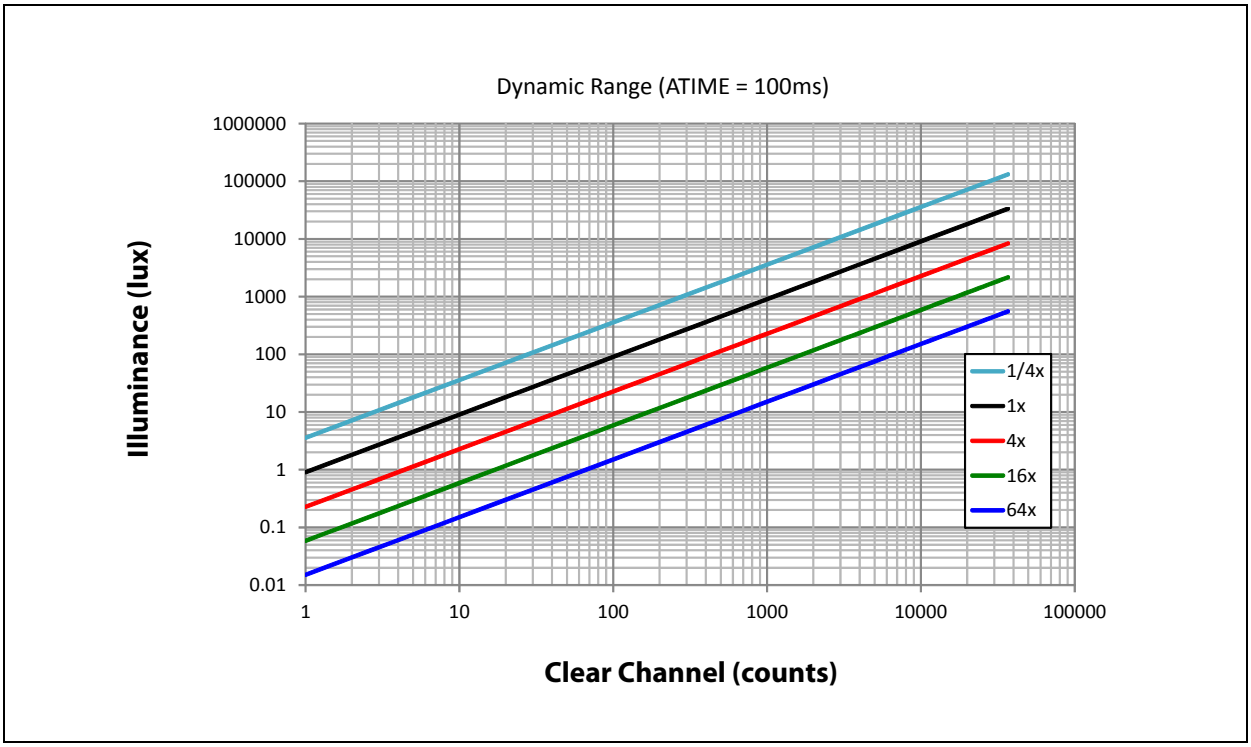
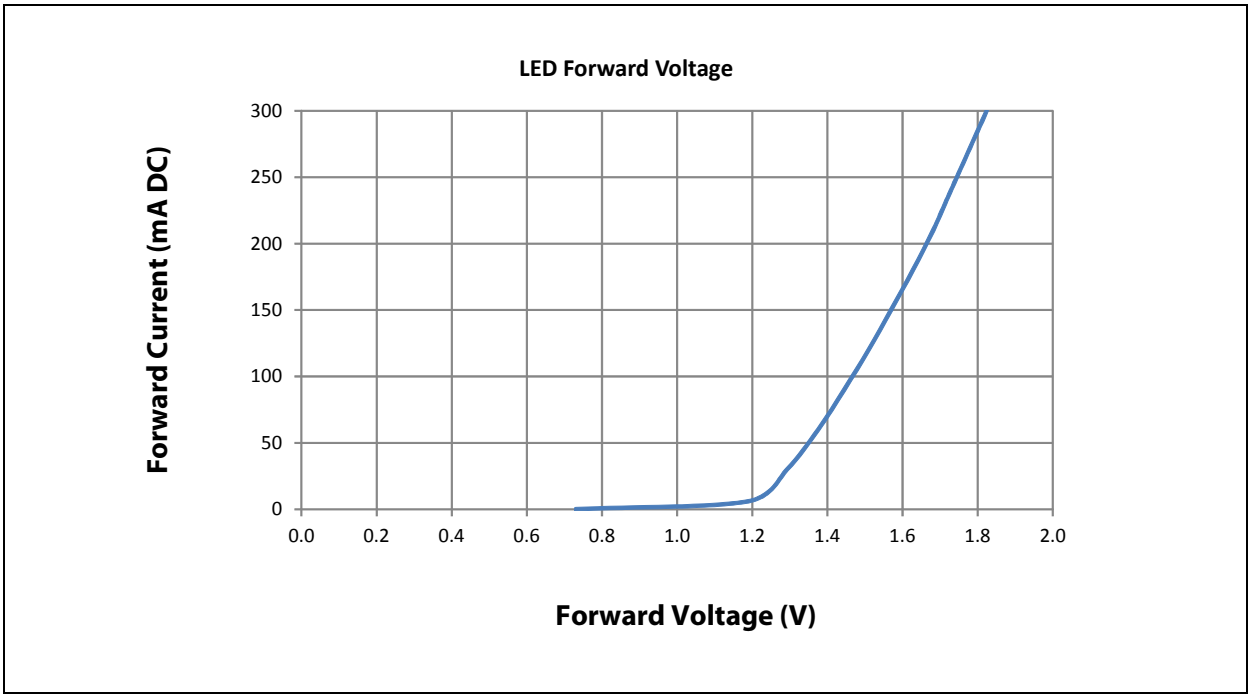


Figure 20:
950nm LED Forward Voltage vs. Current



Note(s):

1. The voltage on the LDR pin (VLEDA – VLED FORWARD) must be sufficiently large to guarantee proper operation of the regulated current sink.

Figure 21:
Gesture and Proximity Response vs. Target Distance

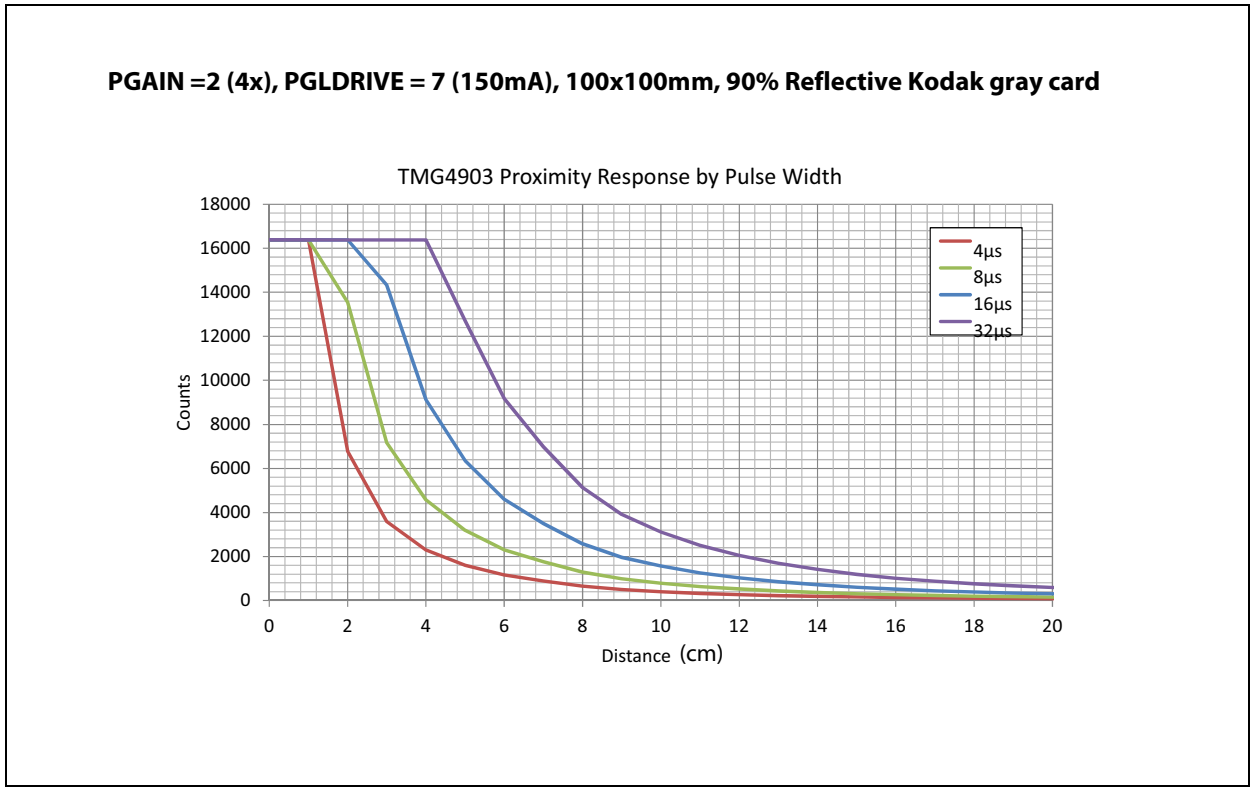


Figure 22:
Gesture Angle Response

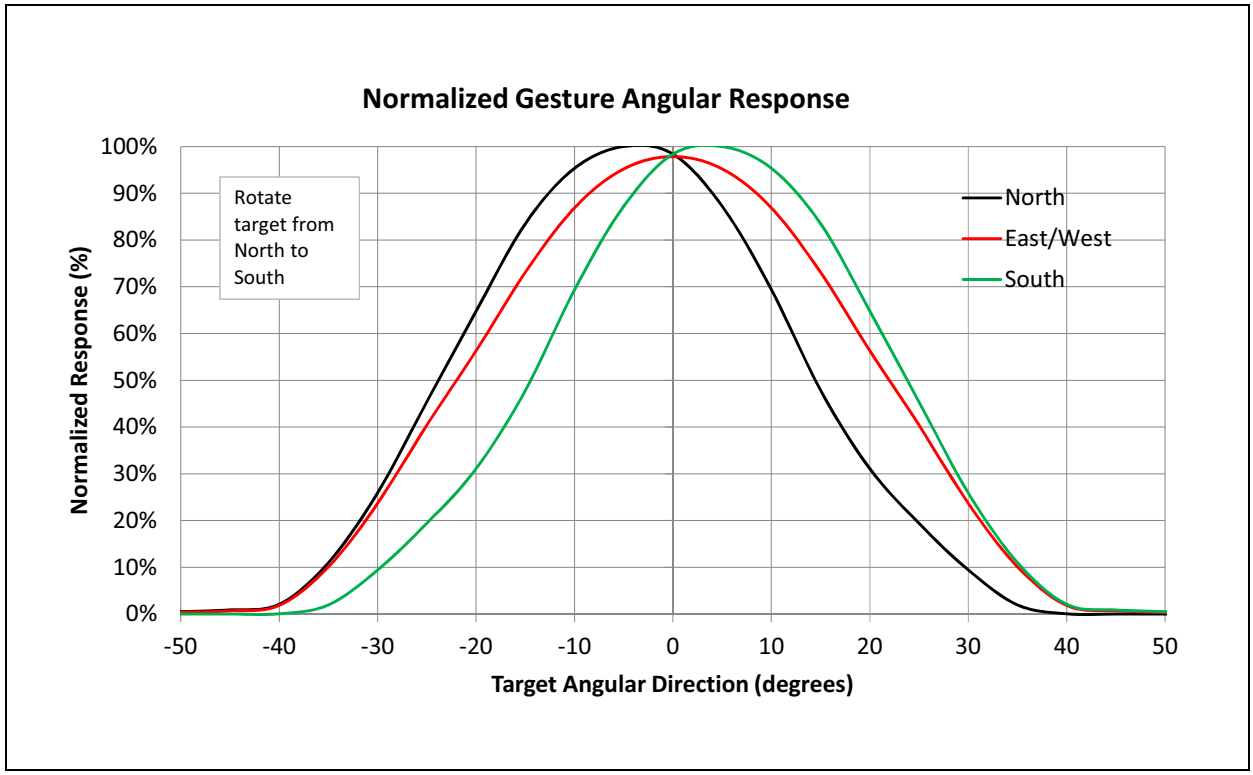
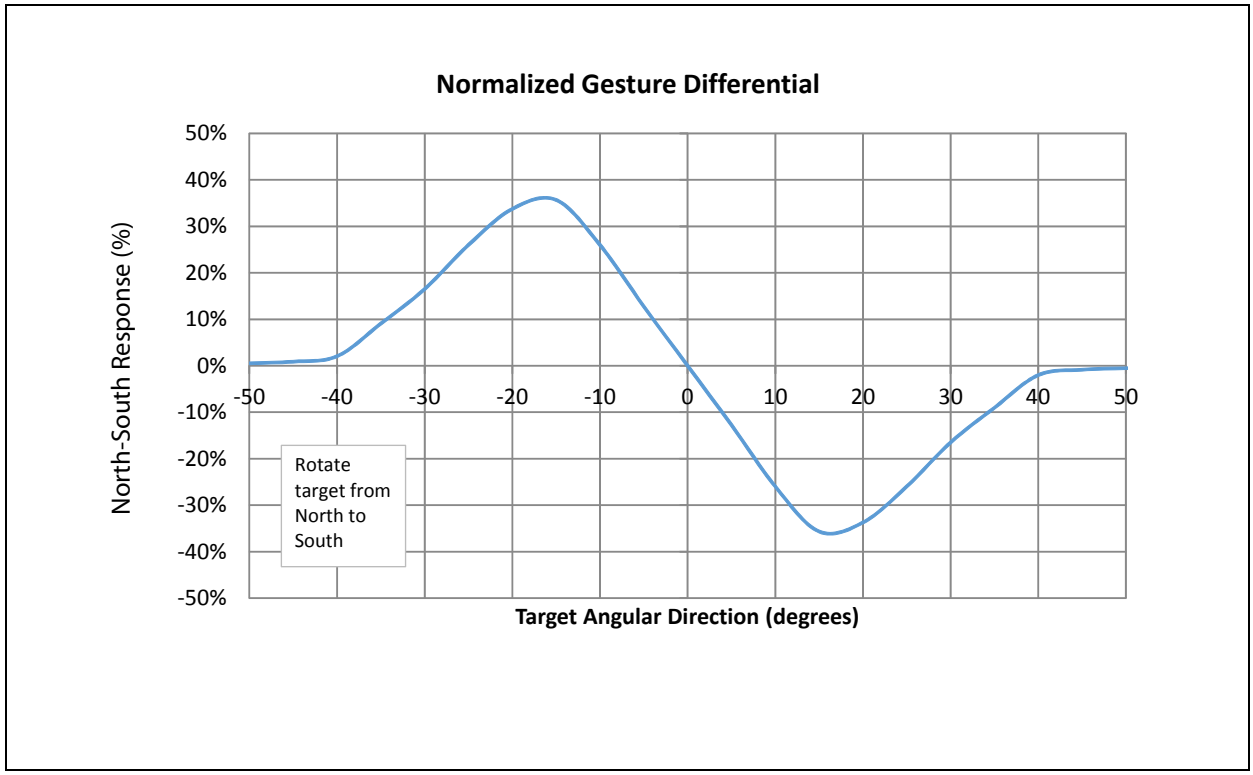


Figure 23:
Gesture Differential



Note(s):

1. The East-West Response (%) is the same vs Target Angular Direction when the target is rotated from East to West.

I²C Protocol

The device uses I²C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and full-speed clock frequency modes. Read and Write transactions comply with the standard set by Philips (now NXP).

Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (I.e. valid even after the master issues a STOP command and the I²C bus is released). During consecutive Read transactions, the future/repeated I²C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address +1.

All 16-bit fields have a latching scheme for reading and writing. In general it is recommended to use I²C bursts whenever possible, especially in this case when accessing two bytes of one logical entity. When reading these fields, the low byte must be read first, and it triggers a 16-bit latch that stores the 16-bit field. The high byte must be read immediately afterwards. When writing to these fields, the low byte must be written first, immediately followed by the high byte. Reading or writing to these registers without following these requirements will cause errors.

I²C Write Transaction

A Write transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS WRITE, DATA BYTE(S), and STOP. Following each byte (9TH clock pulse) the slave places an ACKNOWLEDGE/NOT- ACKNOWLEDGE (ACK/NACK) on the bus. If NACK is transmitted by the slave, the master may issue a STOP.

I²C Read Transaction

A Read transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS, RESTART, CHIP-ADDRESSREAD, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9TH clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification.

Figure 24:
Simplified State Diagram

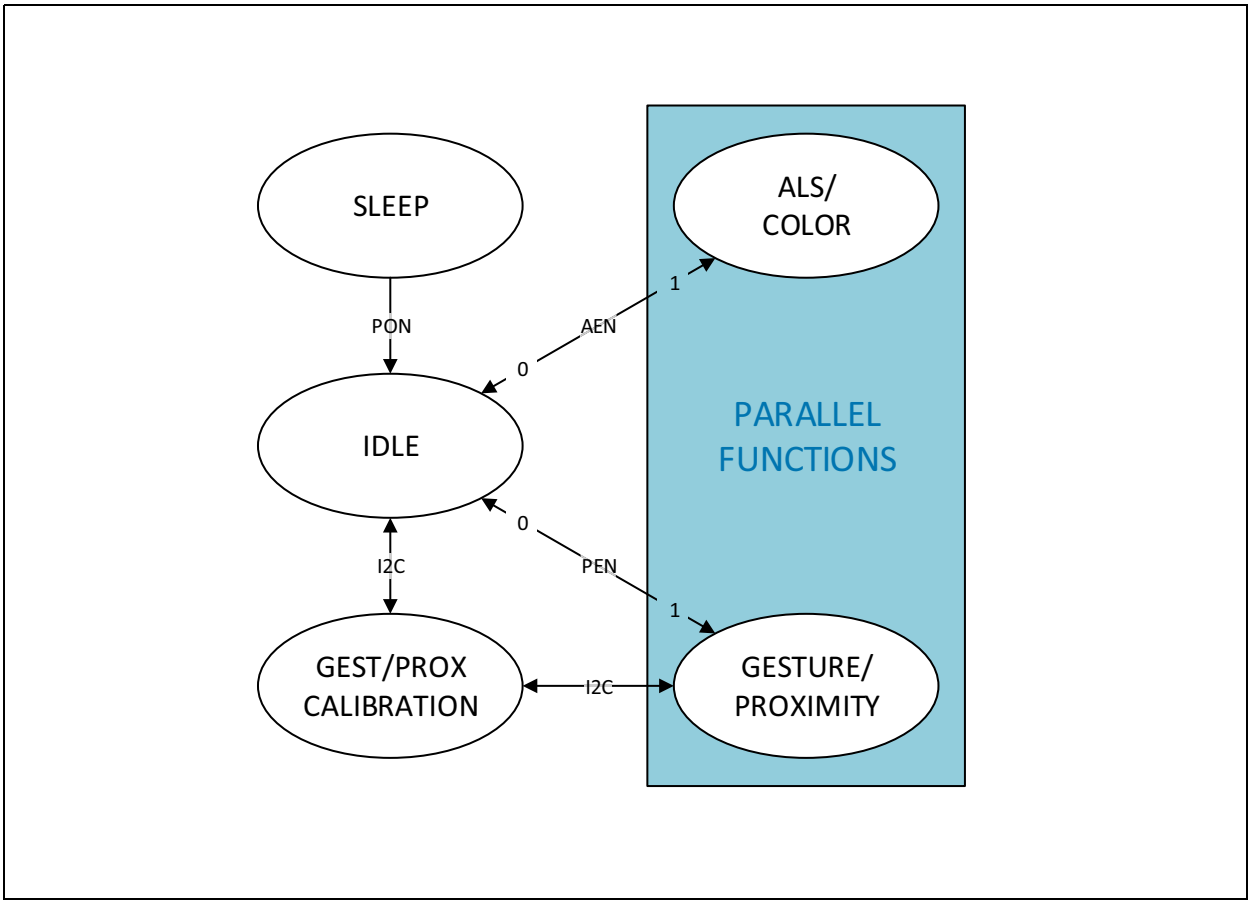
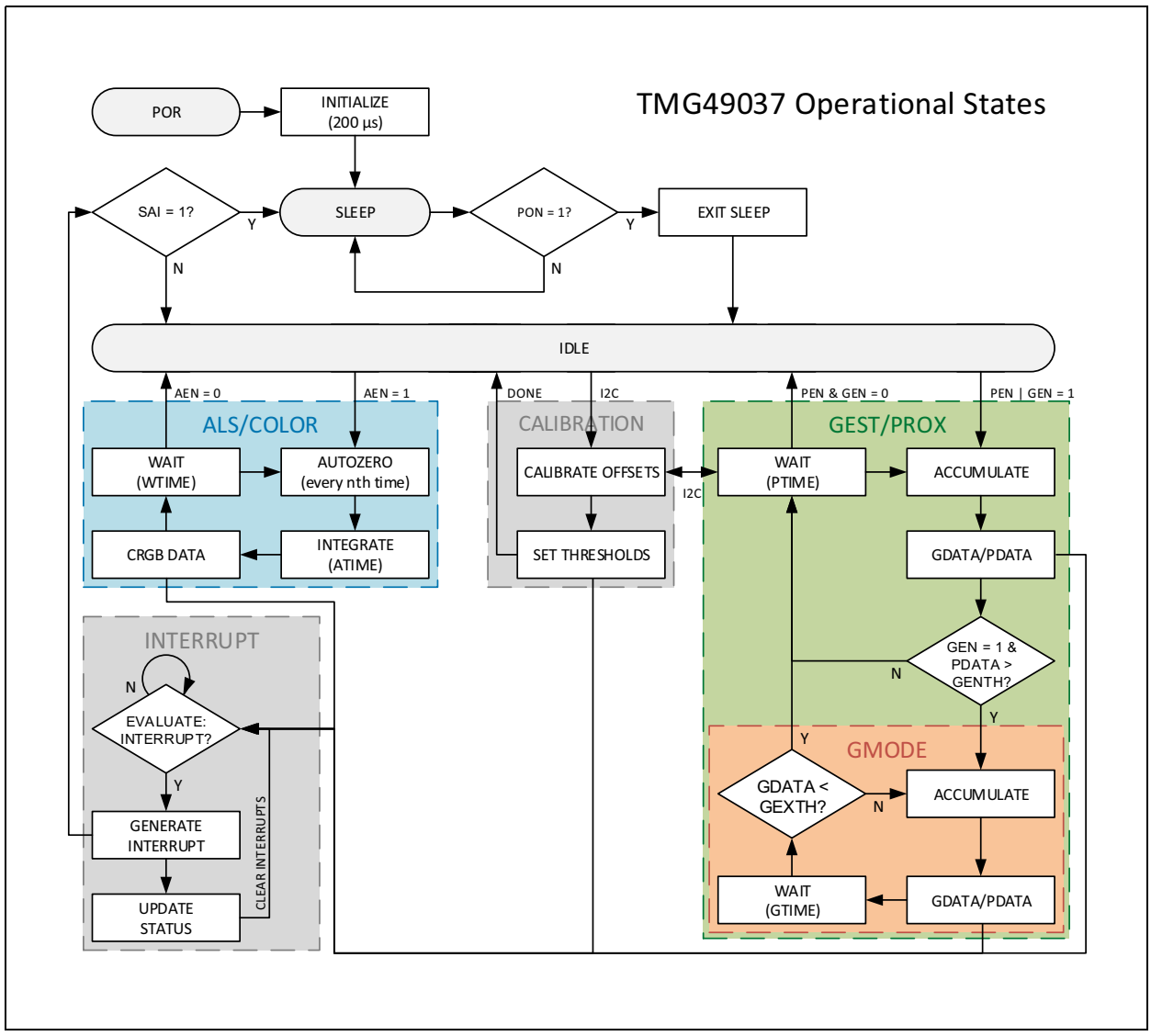


Figure 25:
Detailed State Diagram



Detailed Description

Upon power-up, POR, the device initializes. During initialization (typically 200µs), the device will deterministically send NAK on I^2C and cannot accept I^2C transactions. All communication with the device must be delayed, and all outputs from the device must be ignored including interrupts. After initialization, the device enters the SLEEP state. In this operational state the internal oscillator and other circuitry are not active, resulting in ultra-low power consumption. If I^2C transaction occurs during this state, the I^2C core wake up temporarily to service the communication. Once the Power ON bit, PON, is enabled, the device enters the IDLE state in which the internal oscillator and attendant circuitry are active, but power consumption remains low. The first time the SLEEP state is exited and any functions are enabled (PEN | GEN | AEN = 1) an EXIT SLEEP pause occurs followed by an immediate entry into the selected engines. If all functions are disabled
(PEN = 0 & AEN = 0), the device returns to the IDLE state.

As depicted in Figure 24 and Figure 25, the gesture/proximity and CRGB color sensing functions operate in parallel when enabled (PEN | GEN | AEN = 1). A simplified state diagram for each function is depicted in Figure 25. Each function is individually configured (e.g. Gain, ADC integration time, wait time, persistence, thresholds, etc.).

Sleep After Interrupt Operation

If Sleep After Interrupt is enabled (SAI = 1), the state machine will enter SLEEP when non-gesture interrupts occur. However, for gesture, the state machine remains in these active modes to continue to support these functions. Entering SLEEP does not automatically change any of the register settings (e.g. PON bit is still high, but the normal operational state is over-ridden by SLEEP state). SLEEP state is terminated when the SAI bit is cleared.

Register Description

The device is controlled and monitored by registers accessed through the I^2C serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in Figure 26.

Figure 26:
Control Register Map

Address	Register Name	R/W	Register Function	Reset Value
0x80	ENABLE	R/W	Enables states and interrupts	0x00
0x81	ATIME	R/W	ADC integration time	0xFF
0x82	PTIME	R/W	Proximity sample time	0x00
0x83	WTIME	R/W	ALS wait time	0xFF
0x84	AILTL	R/W	ALS interrupt low threshold low byte	0x00
0x85	AILTH	R/W	ALS interrupt low threshold high byte	0x00
0x86	AIHTL	R/W	ALS interrupt high threshold low byte	0x00
0x87	AIHTH	R/W	ALS interrupt high threshold high byte	0x00
0x88	PILTL	R/W	Proximity interrupt low threshold low byte	0x00
0x89	PILTH	R/W	Proximity interrupt high threshold high byte	0x00
0x8A	PIHTL	R/W	Proximity interrupt low threshold low byte	0x00
0x8B	PIHTH	R/W	Proximity interrupt high threshold high byte	0x00
0x8C	PERS	R/W	ALS & Proximity interrupt persistence filters	0x00
0x8D	CFG0	R/W	Configuration register zero	0xA0
0x8E	PGCFG0	R/W	Proximity pulse width and count	0x4F
0x8F	PGCFG1	R/W	Proximity gain and LED current	0x80
0x90	CFG1	R/W	Configuration register one	0x00
0x91	REVID	R	Revision ID	0x12
0x92	ID	R	Device ID	0xB8
0x93	STATUS	R	Device status register one	0x00
0x94	CDATAL	R	Clear ADC low data register	0x00
0x95	CDATAH	R	Clear ADC high data register	0x00
0x96	RDATAL	R	Red ADC low data register	0x00
0x97	RDATAH	R	Red ADC high data register	0x00

Address	Register Name	R/W	Register Function	Reset Value
0x98	GDATAL	R	Green ADC low data register	0x00
0x99	GDATAH	R	Green ADC high data register	0x00
0x9A	BDATAL	R	Blue ADC low data register	0x00
0x9B	BDATAH	R	Blue ADC high data register	0x00
0x9C	PDATAL	R	Proximity ADC low data register	0x00
0x9D	PDATAH	R	Proximity ADC high data register	0x00
0x9E	STATUS2	R	Additional device status	0x00
0x9F	CFG2	R/W	Configuration register two	0x04
0xAB	CFG3	R/W	Configuration register three	0x00
0xAC	CFG4	R/W	Configuration register four	0x07
0xAD	CFG5	R/W	Configuration register five	0x08
0xB0	GCFG0	R/W	Gesture configuration register zero	0x00
0xB1	GCFG1	R/W	Gesture configuration register one	0x8F
0xB2	GCFG2	R/W	Gesture configuration register two	0x80
0xB3	STATUS3	R	Status register three	0x00
0xB4	GTIME	R/W	Gesture time	0x0A
0xB5	GST_CTRL	R/W	Gesture control	0x00
0xB6	GTHR_INL	R/W	Gesture entry threshold low byte	0x00
0xB7	GTHR_INH	R/W	Gesture entry threshold high byte	0x00
0xB8	GTHR_OUTL	R/W	Gesture exit threshold low byte	0x00
0xB9	GTHR_OUTH	R/W	Gesture exit threshold high byte	0x00
0xBA	GFIFO_LVL	R	Gesture FIFO entries waiting for readout	0x00
0xBB	GSTATUS	R	Gesture status	0x00
0xBC	CONTROL	R/W	Control register	0x00
0xBD	AUXID	R	Auxiliary ID	0x00
0xC0	OFFSETNL	R/W	North channel offset low byte	0x00
0xC1	OFFSETNH	R/W	North channel offset high byte	0x00
0xC2	OFFSETSL	R/W	South channel offset low byte	0x00
0xC3	OFFSETSH	R/W	South channel offset high byte	0x00
0xC4	OFFSETWL	R/W	West channel offset low byte	0x00

Address	Register Name	R/W	Register Function	Reset Value
0xC5	OFFSETWH	R/W	West channel offset high byte	0x00
0xC6	OFFSETEL	R/W	East channel offset low byte	0x00
0xC7	OFFSETEH	R/W	East channel offset high byte	0x00
0xD0	PBSLN_MEASL	R	Measured baseline low byte	0x00
0xD1	PBSLN_MEASH	R	Measured baseline high byte	0x00
0xD2	PBSLNL	R	Stored baseline low byte	0x00
0xD3	PBSLNH	R	Stored baseline high byte	0x00
0xD6	AZ_CONFIG	R/W	Configure CRGB autozero frequency	0xFF
0xD7	CALIB	R/W	Start offset calibration	0x00
0xD8	CALIBCFG0	R/W	Calibration configuration register zero	0x44
0xD9	CALIBCFG1	R/W	Calibration configuration register one	0x0C
0xDA	CALIBCFG2	R/W	Calibration configuration register two	0x20
0xDB	CALIBCFG3	R/W	Calibration configuration register three	0x10
0xDC	CALIBSTAT	R/W	Calibration status	0x00
0xDD	INTENAB	R/W	Interrupt enable	0x00
0xDE	INCLEAR	R/W	Interrupt clear	0x00
0xF8	GFIFO0L	R	Gesture FIFO North low byte	0x00
0xF9	GFIFO0H	R	Gesture FIFO North high byte	0x00
0xFA	GFIFO1L	R	Gesture FIFO South low byte	0x00
0xFB	GFIFO1H	R	Gesture FIFO South high byte	0x00
0xFC	GFIFO2L	R	Gesture FIFO West low byte	0x00
0xFD	GFIFO2H	R	Gesture FIFO West high byte	0x00
0xFE	GFIFO3L	R	Gesture FIFO East low byte	0x00
0xFF	GFIFO3H	R	Gesture FIFO East high byte	0x00

Enable Register (ENABLE 0x80)

Enable has fields that power on the device and enable the functions. Before enabling any functions, all of the bits associated with each function must be set. Changing control register values while operating may result in invalid results.

Figure 27:
Enable Register

7	6	5	4	3	2	1	0
Reserved	GEN	PIEN	AIEN	WEN	PEN	AEN	PON

Field	Bits	Description
Reserved	7	**Reserved.**
GEN	6	**Gesture Enable.** When asserted, the gesture state machine can be activated by setting GMODE = 1 or when a proximity value is above the gesture entry threshold.
PIEN	5	**Proximity Interrupt Enable.** When asserted permits proximity interrupts to be generated, subject to the proximity thresholds and persistence filter.
AIEN	4	**ALS Interrupt Enable.** When asserted permits ALS interrupts to be generated, subject to the ALS thresholds and persistence filter.
WEN	3	**Wait Enable.** This bit activates the wait feature. Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.
PEN	2	**Proximity Enable.** This bit activates the proximity function. Writing a 1 enables proximity. Writing a 0 disables proximity.
AEN	1	**ALS Enable.** This bit activates the ALS/Color functionality. Writing a 1 enables ALS/Color. Writing a 0 disables ALS/Color.
PON	0	**Power ON.** This bit activates the internal oscillator to permit the timers and ADC channels to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator and clears, PEN, and AEN. Only set this bit after all other registers have been initialized by the host.

ALS Integration Time Register (ATIME 0x81)

Figure 28:
ALS Integration Time Register

7	6	5	4	3	2	1	0
ATIME							

Field	Bits	Description		
ATIME	7:0	**ALS Integration Time.** Sets the internal integration time of ALS/Color analog to digital converters in increments of 2.78ms. The power on reset value is 0xFF. The ADC maximum count (or saturation) value depends on the integration time. It is the lesser of either: 65535 (16-bit saturation) or The result of equation: $Count_{MAX} = 1024 \; X \; CYCLES$		
		VALUE	**INTEGRATION TIME**	**MAX COUNTS**
		0xFF	2.78ms	1024
		0xF6	27.8ms	10240
		0xDC	100ms	36864
		…	*2.78ms X (256 - ATIME)*	…
		0xC0	178ms	65535
		0x00	711ms	65535

Proximity Sample Time Register (PTIME 0x82)

Figure 29:
Proximity Sample Time Register

7	6	5	4	3	2	1	0
PTIME							

Field	Bits	Description		
PTIME	7:0	**Proximity Sample Time.** Sets the proximity sample rate. The power on reset value is 0x00. Proximity is executed once for each sample time.		
		VALUE	**SAMPLE TIME**	**FREQUENCY**
		0x00	2.78ms	360Hz
		0x01	5.56ms	180Hz
		0x03	11.1ms	90Hz
		0x23	100ms	10Hz
		…	*2.78ms X (PTIME +1)*	*1/Proximity Sample Time*
		0xFF	711ms	1.41Hz

Wait Time Register (WTIME 0x83)

Figure 30:
Wait Time Register

7	6	5	4	3	2	1	0
WTIME							

Field	Bits	Description		
WTIME	7:0	**Wait Time.** Sets the wait time between ALS cycles. Wait mode reduces current consumption. It is set in 2.78ms increments unless the WLONG bit is asserted in which case the wait times are 12x longer. The power on reset value is 0xFF. Wait time should be configured before AEN is asserted.		
		VALUE	**WAIT TIME (WLONG=0)**	**WAIT TIME (WLONG=1)**
		0xFF	2.78ms	0.03s
		0xDC	100ms	1.20s
		…	*2.78ms X (256 - WTIME)*	*33.3ms X (256 - WTIME)*
		0x6A	417ms	5.00s
		0x00	711ms	8.53s

ALS Interrupt Threshold Registers (0x84 – 0x87)

ALS level detection uses data generated by the Clear Channel. The ALS Interrupt Threshold registers provide 16-bit values to be used as the high and low thresholds for comparison to the 16-bit CDATA values. If AIEN is enabled and CDATA is not between AILT and AIHT for the number of consecutive samples specified in APERS an interrupt is asserted on the interrupt pin.

Figure 31:
ALS Interrupt Threshold Registers

Field	Register	Bits	Description
AILT	0x84	7:0	ALS low threshold low byte
	0x85	15:8	ALS low threshold high byte
AIHT	0x86	7:0	ALS high threshold low byte
	0x87	15:8	ALS high threshold high byte

Proximity Interrupt Threshold Registers (0x88 – 0x8B)

The Proximity Interrupt Threshold Registers set the high and low trigger points for the comparison function which generates an interrupt. If PDATA, the value generated by proximity channel, crosses from above to below the lower threshold or from below to above the upper threshold, an interrupt may be signaled to the host processor. Interrupt generation is subject to the value set in persistence filter (PPERS).

Figure 32:
Proximity Interrupt Threshold Registers

Field	Register	Bits	Description
PILT	0x88	7:0	Proximity low threshold low byte
	0x89	15:8	Proximity low threshold high byte
PIHT	0x8A	7:0	Proximity high threshold low byte
	0x8B	15:8	Proximity high threshold high byte

Interrupt Persistence Register (PERS 0x8C)

Figure 33:
Interrupt Persistence Register

7	6	5	4	3	2	1	0
PPERS				APERS			

Field	Bits	Description	
PPERS	7:4	**Proximity Interrupt Persistence.** Defines a filter for the number of consecutive occurrences that PDATA must remain outside the threshold range between PILT and PIHT before an interrupt is generated. Any sample that is inside the threshold range resets the counter to 0.	
		VALUE	**CONSECUTIVE OCCURENCES OUT OF RANGE**
		0	Every proximity cycle generates an interrupt
		1	Generate interrupt after every occurrence.
		2	Generate interrupt after 2 occurrences.
		...	Generate interrupt after *PPERS* occurrences.
		15	Generate interrupt after 15 occurrences.
APERS	3:0	**ALS Interrupt Persistence.** Defines a filter for the number of consecutive occurrences that CDATA must remain outside the threshold range between AILT and AIHT before an interrupt is generated. Any sample that is inside the threshold range resets the counter to 0.	
		VALUE	**CONSECUTIVE OCCURENCES OUT OF RANGE**
		0	Every ALS cycle generates an interrupt
		1	Generate interrupt after every occurrence.
		2	Generate interrupt after 2 occurrences.
		3	Generate interrupt after 3 occurrences.
		4	Generate interrupt after 5 occurrences.
		5	Generate interrupt after 10 occurrences.
		…	Generate interrupt after *5 X (APERS -3)* occurrences.
		14	Generate interrupt after 55 occurrences.
		15	Generate interrupt after 60 occurrences.

Configuration Register Zero (CFG0 0x8D)

Figure 34:
Configuration Register Zero

7	6	5	4	3	2	1	0
Reserved		LOWPOWER_IDLE	Reserved		WLONG	Reserved	

Field	Bits	Description
Reserved	7:6	**Reserved.**
LOWPOWER_IDLE	5	**Low Power Idle.** When asserted, the device will run in a low power mode if all functions are in wait states or disabled.
Reserved	4:3	**Reserved.**
WLONG	2	**Wait Long Enable.** When asserted, the wait cycles are increased by a factor 12x.
Reserved	1:0	**Reserved.**

Proximity/Gesture Configuration Register Zero (PGCFG0 0x8E)

PGCFG0 has fields that set the amount of time the LED driver is sinking current during a proximity pulse and set the maximum number of pulses for each proximity sample.

Figure 35:
Proximity Configuration Register Zero

7	6	5	4	3	2	1	0
PGPULSE_LEN		PPULSE					

Field	Bits	Description	
PGPULSE_LEN	7:6	**Proximity Pulse Length.** Sets the LED-ON pulse width during a Proximity pulse.	
		VALUE	**LED ON**
		0	4µs
		1	8µs
		2	16µs
		3	32µs
PPULSE	5:0	**Proximity Pulse Count.** Specifies the maximum number of Proximity pulses to be generated on LDR. The pulse count can be set between 1 and 64 pulses. The number of pulses is equal to the PPULSE value plus 1.	

Proximity/Gesture Configuration Register One (PGCFG1 0x8F)

PGCFG1 has fields that set the electrical gain of the proximity response and set the LED drive current during pulses.

Figure 36:
Proximity Configuration Register One

7	6	5	4	3	2	1	0
PGGAIN		Reserved	PGLDRIVE				Reserved

Field	Bits	Description	
PGGAIN	7:6	**Proximity Gain Control.**	
		VALUE	**GAIN VALUE**
		0	1x Gain
		1	2x Gain
		2	4x Gain
		3	8x Gain
Reserved	5	**Reserved.** Bit must be set to 0.	
PGLDRIVE	4:1	**Proximity LED Drive Strength.** Configures nominal LED current linearly in steps of 20mA (actual current depends on factory-configuration of LED drive strength).	
		VALUE	**LED STRENGTH**
		0	10mA
		1	30mA
		2	50mA
		…	*10mA + (20mA * PGLDRIVE)*
		14	290mA
		15	310mA
Reserved	0	**Reserved.** Bit must be set to 0.	

Configuration Register One (CFG1 0x90)

CFG1 has fields that enable or disable the saturation interrupts for Proximity and ALS and set the electrical gain of the ALS response.

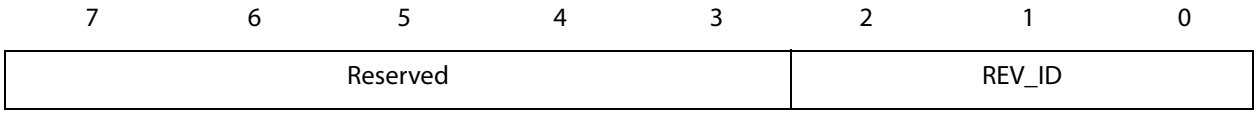
Figure 37:
Configuration Register One

7	6	5	4	3	2	1	0
PGSIEN	ASIEN	Reserved				AGAIN	

Field	Bits	Description	
PGSIEN	7	**Proximity Saturation Interrupt Enable.** When asserted permits proximity saturation interrupts to be generated.	
ASIEN	6	**ALS Saturation Interrupt Enable.** When asserted permits ALS saturation interrupts to be generated.	
Reserved	5:2	**Reserved.** Bits must be set to 0.	
AGAIN	1:0	ALS and Color Gain Control.	
		FIELD VALUE	**CRGB GAIN VALUE**
		0	1x Gain
		1	4x Gain
		2	16x Gain
		3	64x Gain

Revision ID Register (REVID 0x91)

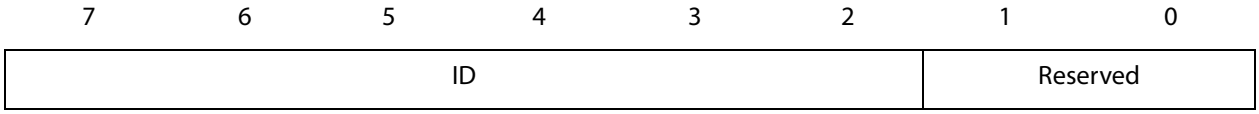
Figure 38:
Revision ID Register



Field	Bits	Description
Reserved	7:3	**Reserved.** Default value is 00010.
REV_ID	2:0	Wafer die revision level. Default value is 010.

ID Register (ID 0x92)

Figure 39:
ID Register



Field	Bits	Description
ID	7:2	Device Identification = 101110
Reserved	1:0	**Reserved.** Default value is 00.

Status Register (STATUS 0x93)

The read-only Status Register provides the status of the device.

Figure 40:
Status Register

7	6	5	4	3	2	1	0
ASAT	PGSAT	PINT	AINT	Reserved	GINT	CINT	Reserved

Field	Bits	Description
ASAT	7	**ALS Saturation.** If ASIEN is set, indicates ALS saturation. Check the STATUS2 register to differentiate between analog or digital saturation.
PGSAT	6	**Proximity/Gesture Saturation.** If PGSIEN is set, indicates analog saturation during a previous proximity cycle. Check the STATUS2 register to differentiate between ambient or reflected light saturation.
PINT	5	**Proximity Interrupt.** If PIEN is set, indicates that a proximity detect or release event that met the programmed proximity thresholds (PILT or PIHT) and persistence (PPERS) occurred.
AINT	4	**ALS Interrupt.** If ASIEN is set, indicates that an ALS event that met the programmed ALS thresholds (AILT or AIHT) and persistence (APERS) occurred.
Reserved	3	**Reserved.**
GINT	2	**Gesture Interrupt.** If GIEN is set, indicates that one or more gesture event conditions have been met. GINT indicates that there is data available in the FIFO buffer for readout and GFIFO_LVL is greater than GFIFOTHR or that GVALID has become asserted when GMODE transitioned to zero. The bit is reset whenever the FIFO buffer is completely emptied (read).
CINT	1	**Calibration Interrupt.** Indicates that either calibration is finished or that one of certain events have occurred during normal operation. If each function is enabled, CINT will be asserted if too many zeroes occur too often in a period of samples, if the proximity baseline has decreased, or if at least one offset register has been adjusted. Check the CALIBSTAT register to identify the triggering event(s).
Reserved	0	**Reserved.**

CRGB Data Registers (0x94 – 0x9B)

Red, green, blue, and clear data are stored as 16-bit values. The read sequence must read byte pairs (low followed by high) starting on an even address boundary (0x94, 0x96, 0x98, or 0x9A) inside the CRGB Data Register block. In addition, reading the Clear channel data low byte (0x94) latches all 8 data bytes. Reading these 8 bytes consecutively (0x94 - 0x9A) ensures that the data is concurrent.

Figure 41:
CRGB Data Registers

Field	Register	Bits	Description
CDATA	0x94	7:0	Clear channel data low byte
	0x95	15:8	Clear channel data high byte
RDATA	0x96	7:0	Red channel data low byte
	0x97	15:8	Red channel data high byte
GDATA	0x98	7:0	Green channel data low byte
	0x99	15:8	Green channel data high byte
BDATA	0x9A	7:0	Blue channel data low byte
	0x9B	15:8	Blue channel data high byte

Proximity Data Registers (0x9C – 0x9D)

Proximity data is stored as a 14-bit value (two bytes).

Proximity detection uses an Automatic Pulse Control (APC) mechanism that adjusts the number of pulses per measurement based on the magnitude of the reflected IR signal. As the magnitude of the signal increases, the number of pulses decreases. Proximity detection uses a 10-bit ADC that is extended to a 14-bit dynamic range for PDATA using the following formula:

$PDATA = ADC_{value} \times (16 / proximity\ pulses)$

PDATA is the average response of the non-masked proximity photodiodes. If one or more photodiodes are masked (CFG2 register 0x9F), the proximity response will remain the same since it is an average of the active photodiodes. PDATA is therefore proportional to the reflected energy per pulse, independent of the number of pulses used.

Figure 42:
Proximity Data Register

Field	Register	Bits	Description
PDATA	0x9C	7:0	Proximity data low byte
	0x9D	13:8	Proximity data high byte

Status Register Two (STATUS2 0x9E)

Figure 43:
Status Register Two

7	6	5	4	3	2	1	0
PVALID	AVALID	Reserved	ASAT_ DIGITAL	ASAT_ ANALOG	PGSAT_ ADC	PGSAT_ REFLECTIVE	PGSAT_ AMBIENT

Field	Bits	Description
PVALID	7	**Proximity Valid.** Indicates that the ALS state has completed a cycle since either an assertion of PEN or the last readout of PDATA.
AVALID	6	**ALS Valid.** Indicates that the proximity state has completed a cycle since either an assertion of AEN or the last readout of the CDATAL data register.
Reserved	5	**Reserved.**
ASAT_DIGITAL	4	**ALS Digital Saturation.** Indicates that the maximum counter value has been reached. Maximum counter value depends on integration time set in the ATIME register.
ASAT_ANALOG	3	**ALS Analog Saturation.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS analog circuit.
PGSAT_ADC	2	**Proximity/Gesture ADC Saturation.** Indicates that the maximum ADC value has occurred.
PGSAT_REFLECTIVE	1	**Proximity/Gesture Reflective Saturation.** Indicates that the intensity of reflected light has exceeded the maximum integration level for the proximity analog circuit.
PGSAT_AMBIENT	0	**Proximity/Gesture Ambient Saturation.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the proximity analog circuit.

Configuration Register Two (CFG2 0x9F)

Figure 44:
Configuration Register Two

7	6	5	4	3	2	1	0
PMASK_E	PMASK_W	PMASK_S	PMASK_N	AMASK	Reserved		

Field	Bits	Description
PMASK_E	7	**Proximity Mask East.** Writing a 1 disables the East photodiode.
PMASK_W	6	**Proximity Mask West.** Writing a 1 disables the West photodiode.
PMASK_S	5	**Proximity Mask South.** Writing a 1 disables the South photodiode.
PMASK_N	4	**Proximity Mask North.** Writing a 1 disables the North photodiode.
AMASK	3	**ALS Mask.** Writing a 1 reduces the ALS gain by a factor of the ALS photodiode pixels. Only the center 2x2 array of pixels remains enabled out of the 4x4 array. Reduces ALS sensitivity for measurement of maximum ambient light levels.
Reserved	2:0	**Reserved.**

Configuration Register Three (CFG3 0xAB)

Figure 45:
Configuration Register Three

7	6	5	4	3	2	1	0
Reserved	LTF_USEPROX	Reserved	SAI	Reserved			

Field	Bits	Description			
Reserved	7	**Reserved.**			
LTF_USEPROX	6	**Use Proximity Photodiodes for ALS Measurement.** Connects the IR-sensitive proximity/gesture photodiodes to the ALS engine in order to collect ALS data in the IR band. The data registers contain the following channel data depending on the LTF_USEPROX setting.			
		16-bit Output Registers		**LTF_USEPROX**	
		High	**Low**	**0**	**1**
		0x95	0x94	Clear	North
		0x97	0x96	Red	South
		0x99	0x98	Green	West
		0x9B	0x9A	Blue	East
Reserved	5	**Reserved.**			
SAI	4	**Sleep After Interrupt.** Powers down the device at the end of a proximity/ALS cycle if an interrupt has been generated. Note that SAI does not modify any register bits directly, it rather uses the interrupt signal to turn off the oscillator. The only way to "wake up" the device from SAI-sleep is by clearing the SAI_ACTIVE flag.			
		PON	**SAI**	**INT (Low Active)**	**Oscillator**
		0			Off
		1	0		On
		1	1	1	On
		1	1	0	Off (sleep after interrupt)
Reserved	3:0	**Reserved.**			

Configuration Register Four (CFG4 0xAC)

Figure 46:
Configuration Register Four

7	6	5	4	3	2	1	0
ALS_INT_ DIRECT	ALS_INT_ DIRECT_GPIO	PROX_INT_ DIRECT	PROX_INT_ DIRECT_GPIO	Reserved			

Field	Bits	Description
ALS_INT_DIRECT	7	**ALS Interrupt Direct.** If asserted, then the INT pin shows the ALS state directly and it is not necessary to clear the interrupt. If the CLEAR data exits the threshold range from within, the INT pin is asserted. The interrupt pin is de-asserted when the CLEAR data re-enters the threshold range. As long as the CLEAR data is within the thresholds, the INT pin is not asserted.
ALS_INT_DIRECT_GPIO	6	**ALS Interrupt Direct on GPIO Pin.** If asserted, the GPIO pin shows the ALS interrupt state directly instead of the INT pin. This function operates in the same manner otherwise as ALS_INT_DIRECT.
PROX_INT_DIRECT	5	**Proximity Interrupt Direct.** If asserted, then the INT pin shows the proximity state directly and it is not necessary to clear the interrupt. If PDATA crosses the upper threshold from below, the INT pin is asserted. The interrupt pin is only de-asserted when PDATA crosses the lower threshold from above. As long as PDATA is below the lower threshold, the INT pin is not asserted.
PROX_INT_DIRECT_GPIO	4	**Proximity Interrupt Direct on GPIO Pin.** If asserted, the GPIO pin shows the proximity interrupt state directly instead of the INT pin. This function operates in the same manner otherwise as PROX_INT_DIRECT.
Reserved	3:0	**Reserved.**

Configuration Register Five (CFG5 0xAD)

Figure 47:
Configuration Register Five

7	6	5	4	3	2	1	0
Reserved		LONG_LTFSTOP_ DISCARD_ALS	Reserved	DISABLE_IR_ CORRECTION	PROX_FILTER_ DOWNSAMPLE	PROX_FILTER_ SIZE	PROX_ FILTER

Field	Bits	Description
Reserved	7:6	**Reserved.**
LONG_LTFSTOP_DISCARD_ ALS	5	**Long Disruption Discard ALS.** Aborts ALS integration that is disrupted if the gesture state is entered (sensor field of view is obstructed). Immediately after gesture mode is exited, a new ALS integration is started. When restarting ALS, this function ignores wait configuration, which may cause more ALS measurements to occur than expected.
Reserved	4	**Reserved.**
DISABLE_IR_CORRECTION	3	**Disable IR Correction.** Default is 1. If bit is 0, then calculate IR=(R+G+B-C)/2 and store R'=R-IR, G', B', and C' in the color DATA registers.
PROX_FILTER_ DOWNSAMPLE	2	**Proximity Filter Downsample.** If PROX_FILTER = 1, then, if asserted, PDATA and proximity interrupt check are performed only every n proximity samples. If not asserted, then proximity filtering uses a moving window: PDATA is updated every cycle and proximity interrupt is checked every cycle.
PROX_FILTER_SIZE	1	**Proximity Filter Size.** Determines the number of consecutive proximity samples to average to filter out noise. **VALUE** / **FILTER** 0 / 2 samples
PROX_FILTER	0	**Proximity Filter.** If asserted, enables proximity filter functionality. Depending on PROX_FILTER_SIZE, 2 or 4 consecutive proximity samples are averaged.

Gesture Configuration Register Zero (GCFG0 0xB0)

GCFG0 has fields that affect the exit of gesture mode, GMODE.

Figure 48:
Gesture Configuration Register Zero

7	6	5	4	3	2	1	0
Reserved		GTHR_MASK				GTHR_OUT_NR	

Field	Bits	Description	
Reserved	7:6	**Reserved.**	
GTHR_MASK	5:2	**Gesture Exit Mask.** Controls which gesture channels will be compared to GTHR_OUT to exit gesture mode, GMODE.	
		BIT	**EXIT MASK**
		5	Ignore E when exiting GMODE.
		4	Ignore W when exiting GMODE.
		3	Ignore S when exiting GMODE.
		2	Ignore N when exiting GMODE.
GTHR_OUT_NR	1:0	**Gesture Exit Persistence.** Defines how many consecutive times the gesture channel data must be below the gesture exit threshold, GTHR_OUT, for the device to exit gesture mode, GMODE.	
		VALUE	**PERSISTENCE**
		0	Exit after first occurrence.
		1	Exit after 2 consecutive occurrences.
		2	Exit after 4 consecutive occurrences.
		3	Exit after 8 consecutive occurrences.

Gesture Configuration Register One (GCFG1 0xB1)

Figure 49:
Gesture Configuration Register One

7	6	5	4	3	2	1	0
GFIFOTHR		GPULSE					

Field	Bits	Description	
GFIFOTHR	7:6	**Gesture FIFO Threshold.** Defines the FIFO Level, the number of NSWE datasets, required to generate an interrupt (if enabled).	
		VALUE	**FIFO LEVEL FOR INTERRUPT**
		0	1
		1	4
		2	8
		3	16
GPULSE	5:0	**Maximum Gesture Pulse Count**. Specifies the maximum number of pulses to be generated for each gesture dataset. The maximum number of pulses is calculated as follows: $n_{Pulses} = GPULSE + 1$	

Gesture Configuration Register Two (GCFG2 0xB2)

Figure 50:
Gesture Configuration Register Two

7	6	5	4	3	2	1	0
Reserved		GEST_FILTER_SIZE	GEST_FILTER	Reserved			

Field	Bits	Description	
Reserved	7:6	**Reserved.**	
GEST_FILTER_SIZE	5	**Proximity Filter Size.** Determines the number of consecutive gesture samples to average to filter out noise.	
		VALUE	**FILTER**
		0	2 samples
		1	4 samples
GEST_FILTER	4	**Gesture Filter.** If asserted, enables gesture filter functionality. Depending on GEST_FILTER_SIZE, 2 or 4 consecutive gesture samples are averaged. A moving window is used and gesture data is added to the buffer at every cycle.	
Reserved	3:0	**Reserved.**	

Status Register Three (STATUS3 0xB3)

Figure 51:
Status Register Three

7	6	5	4	3	2	1	0
Reserved						SAI_ACTIVE	Reserved

Field	Bits	Description
Reserved	7:2	**Reserved.**
SAI_ACTIVE	1	**Sleep-After-Interrupt Active.** If SAI is set, indicates that the oscillator has been stopped and the device is in sleep after an interrupt. SAI_ACTIVE must be cleared (CONTROL 0xBC[0]: CLEAR_SAI_ACTIVE) to clear SAI and resume chip operation.
Reserved	0	**Reserved.**

Gesture Sample Time Register (GTIME 0xB4)

Figure 52:
Gesture Sample Time Register

7	6	5	4	3	2	1	0
GTIME							

<table>
<tr><th>Field</th><th>Bits</th><th colspan="2">Description</th></tr>
<tr><td rowspan="8">GTIME</td><td rowspan="8">7:0</td><td colspan="2">Gesture Sample Time. Sets the gesture sample rate while in gesture mode, GMODE. The power on reset value is 0x0A. Gesture data is collected once for each sample time. There is a minimum GTIME that must be configured that depends on the GPULSE and PGPULSE_LEN settings. The maximum GPULSE and PGPULSE_LEN settings for the default GTIME (0x0A) are GPULSE = 15 (16 pulses) and PGPULSE_LEN = 1 (8µs). Contact technical support for more information.</td></tr>
<tr><td>VALUE</td><td>SAMPLE</td></tr>
<tr><td>0x00</td><td>88µs</td></tr>
<tr><td>0x01</td><td>176µs</td></tr>
<tr><td>0x0A</td><td>968µs</td></tr>
<tr><td>0x70</td><td>9.9ms</td></tr>
<tr><td>…</td><td>88µs X (GTIME +1)</td></tr>
<tr><td>0xFF</td><td>22.5ms</td></tr>
</table>

Gesture Control Register (GST_CTRL 0xB5)

Figure 53:
Gesture Control Register

7	6	5	4	3	2	1	0
Reserved						GIEN	GMODE

Field	Bits	Description
Reserved	7:2	**Reserved.**
GIEN	1	**Gesture Interrupt Enable.** When asserted permits all gesture-related interrupts to occur. The first gesture interrupt is subject to GFIFOTHR.
GMODE	0	**Gesture Mode.** Reports if the device is in gesture mode. In gesture mode, GTIME sets the sample rate of the proximity/gesture state machine, and datasets are added to the FIFO buffer. Writing 1 to this bit forces the device to enter gesture mode (as if GTHR_IN has been exceeded). Writing a 0 to this bit causes exit of gesture when current analog conversion has finished (as if all gesture data is below GTHR_OUT).

Gesture Threshold Registers (0xB6 – 0xB9)

PDATA is compared to GTHR_IN if GEN = 1. If PDATA is greater than GTHR_IN, the device enters gesture mode (GMODE). Once in GMODE, the gesture data from each channel is compared to GTHR_OUT to determine when the device should exit GMODE. The criteria for exiting GMODE are user-configured. The proximity persistence filter, PPERS, is not used to determine gesture state machine entry.

Figure 54:
Gesture Threshold Registers

Field	Register	Bits	Description
GTHR_IN	0xB6	7:0	Gesture entry threshold low byte
	0xB7	15:8	Gesture entry threshold high byte
GTHR_OUT	0xB8	7:0	Gesture exit threshold low byte
	0xB9	15:8	Gesture exit threshold high byte

Gesture FIFO Buffer Level Register (GFIFO_LVL 0xBA)

Figure 55:
Gesture FIFO Buffer Level Register

7	6	5	4	3	2	1	0
GFLVL							

Field	Bits	Description
GFIFO_LVL	7:0	**Gesture FIFO Buffer Level.** Indicates the number of unread NSWE datasets in the FIFO buffer.

Gesture Status Register (GSTATUS 0xBB)

Figure 56:
Gesture Status Register

7	6	5	4	3	2	1	0
Reserved						GFIFO_OV	GVALID

Field	Bits	Description
Reserved	7:2	**Reserved.**
GFIFO_OV	1	**Gesture FIFO Overflow**. Indicates that the FIFO buffer has been filled to capacity and data may be lost.
GVALID	0	**Gesture FIFO Data.** Indicates when GFIFO_LVL has exceeded GFIFOTHR. If enabled, a gesture interrupt (GINT) is asserted at this time. GINT clears as soon GFIFO_LVL = 0, but GVALID only clears after the gesture event is over when GFIFO_LVL = 0 and GMODE = 0.

Control Register (CONTROL 0xBC)

Figure 57:
Control Register

7	6	5	4	3	2	1	0
Reserved							SAI_ACTIVE_CLEAR

Field	Bits	Description
Reserved	7:1	**Reserved.**
SAI_ACTIVE_CLEAR	0	**Sleep-After-Interrupt Active Clear.** If SAI is set and SAI_ACTIVE is true (an Interrupt has occurred), asserting this pin clears the SAI_ACTIVE flag and restarts the device oscillator to resume chip operation if functions are enabled.

Auxiliary ID Register (AUXID 0xBD)

Figure 58:
Auxiliary ID Register

7	6	5	4	3	2	1	0
Reserved				AUXID			

Field	Bits	Description
Reserved	7:4	**Reserved.**
AUXID	3:0	**Auxiliary ID.** Value is 0000.

Proximity/Gesture Offset Registers (0xC0 – 0xC7)

Proximity/gesture offset values have a range of ±255 and are expressed as 9-bit two's-complement values. Do not program values outside of this range. Only the lower 9 bits are significant, but the high byte must only be programmed with values of 0x00 (indicates that the low byte has a positive value) or 0xFF (indicates that the low byte has a negative value).

Figure 59:
Proximity/Gesture Offset Registers

Field	Register	Bits	Description
OFFSETN	0xC0	7:0	North channel offset low byte
	0xC1	15:8	North channel offset high byte
OFFSETS	0xC2	7:0	South channel offset low byte
	0xC3	15:8	South channel offset high byte
OFFSETW	0xC4	7:0	West channel offset low byte
	0xC5	15:8	West channel offset high byte
OFFSETE	0xC6	7:0	East channel offset low byte
	0xC7	15:8	East channel offset high byte

Proximity/Gesture Baseline Registers (0xD0 – 0xD3)

After proximity/gesture calibration is complete, the user may define a number of consecutive proximity cycles for which PDATA is averaged. The number of consecutive PDATA cycles to be averaged is defined by PXDCAVG_BASELINE_WINDOW (0xD9[2:0]). Averaging will repeat after every window of PDATA cycles. The latest averaged result is stored in the PBSLN_MEAS field.

The second proximity baseline field, PBSLN, is first updated at the end of proximity/gesture calibration. This value does not change unless the user sets. PXDCAVG_AUTO_BASELINE (0xD9[3]) to 1. If asserted, PBSLN will be updated with the value of PBSLN_MEAS whenever PBSLN_MEAS is less than PBSLN. In addition, a multiple of PBSLN is used at the end of the calibration routine to set the gesture entry and exit thresholds if the user sets. PXDCAVG_AUTO_GTHR field (0xD9[7]) to 1. The multiplication factor for setting the entry and exit thresholds is user-defined in the AUTO_GTHR_IN_MULT (0xDA[3:0]).

Figure 60:
Proximity/Gesture Baseline Registers

Field	Register	Bits	Description
PBSLN_MEAS	0xD0	7:0	Measured baseline low byte
	0xD1	15:8	Measured baseline high byte
PBSLN	0xD2	7:0	Stored baseline low byte
	0xD3	15:8	Stored baseline high byte

Autozero Configuration Register (AZ_CONFIG 0xD6)

Figure 61:
Autozero Configuration Register

7	6	5	4	3	2	1	0
AZ_NTH_ITERATION							

Field	Bits	Description	
AZ_NTH_ITERATION	7:0	**ALS Autozero Frequency.** Sets the frequency at which the device performs autozero of the ALS pulse counter.	
		VALUE	**AUTOZERO FREQUENCY**
		0	Never
		1	Every cycle
		2	Every 2 cycles
		…	Every *(AZ_NTH_ITERATION)* cycles
		253	Every 253 cycles
		254	Every 254 cycles
		255	Only once (before 1st cycle)

Calibration Register (CALIB 0xD7)

Figure 62:
Calibration Register

7	6	5	4	3	2	1	0
Reserved							START_OFFSET_CALIB

Field	Bits	Description
Reserved	7:1	**Reserved.**
START_OFFSET_ CALIB	0	**Start Offset Calibration.** Starts the proximity/gesture offset register calibration routine. Results are stored in the Proximity/Gesture Offset Registers (0xC0 – 0xC7). The CALIB_FINISHED flag is asserted when calibration is complete and an interrupt (CINT) is asserted if CIEN is set. Calibration can be stopped by writing a 0 to this field.

Calibration Configuration Register Zero (CALIBCFG0 0xD8)

Figure 63:
Calibration Configuration Register Zero

7	6	5	4	3	2	1	0
Reserved	DCAVG_ AUTO_OFFSET_ ADJUST	Reserved	ELECTRICAL_ CALIBRATION	BINSRCH_ SKIP	DCAVG_ITERATIONS		

Field	Bits	Description
Reserved	7	**Reserved.**
DCAVG_AUTO_OFFSET_ADJUST	6	**DC Averaging Auto Offset Adjust.** If set, then during DC averaging, whenever an ADC measurement is zero, the appropriate offset register will be decreased and the OFFSET_ADJUSTED flag is set. Note also that DC averaging is not automatically restarted when this happens, so the calculated baseline might be wrong. Software could restart averaging in this case.
Reserved	5	**Reserved.**
ELECTRICAL_CALIBRATION	4	**Enable Electrical Calibration.** When asserted the calibration routine will perform an internal electrical calibration to adjust the proximity offset registers to remove electrical crosstalk – there is no optical response at all for this routine. When not asserted, calibration will measure both optical and electrical crosstalk during calibration.
BINSRCH_SKIP	3	**Binary Search Skip.** When asserted the calibration routine will skip the binary search step. It is useful if zeroes are detected during the DC averaging process to manually reset the baseline and reduce the likelihood of zero counts.

<table>
<tr><th>Field</th><th>Bits</th><th colspan="2">Description</th></tr>
<tr><td rowspan="8">DCAVG_ITERATIONS</td><td rowspan="8">2:0</td><td colspan="2">DC Averaging Iterations. Sets the number of proximity results during calibration that are averaged after the binary search is complete. During this period, whenever a result is zero, the appropriate offset register is automatically decremented. The default value is 4 (16 iterations).</td></tr>
<tr><td>VALUE</td><td>SAMPLES</td></tr>
<tr><td>0</td><td>Skip</td></tr>
<tr><td>1</td><td>2</td></tr>
<tr><td>2</td><td>4</td></tr>
<tr><td>…</td><td>$n_{Iterations} = 2^{DCAVG\_ITERATIONS}$</td></tr>
<tr><td>6</td><td>64</td></tr>
<tr><td>7</td><td>128</td></tr>
</table>

Calibration Configuration Register One (CALIBCFG1 0xD9)

Figure 64:
Calibration Configuration Register One

7	6	5	4	3	2	1	0
PXDCAVG_ AUTO_ GTHR	PROX_ AUTO_OFFSET_ ADJUST	Reserved		PXDCAVG_ AUTO_ BASELINE	PXDCAVG_BASELINE_WINDOW		

Field	Bits	Description
PXDCAVG_AUTO_GTHR	7	**Proximity Automatic Thresholds.** When asserted, GTHR_IN and GTHR_OUT are automatically written with a multiple of the PBSLN every time PBSLN changes. The multiplication factor is set in AUTO_GTHR_IN_MULT. PBSLN can only change if PXDCAVG_AUTO_BASELINE is asserted and PBSLN_MEAS is less than PBSLN.
PROX_AUTO_OFFSET_ADJUST	6	**Proximity Auto Offset Adjust.** If set, then during proximity/gesture mode, whenever an ADC measurement is zero, the appropriate offset register will be decreased. Will set the OFFSET_ADJUSTED flag if it happens.
Reserved	5:4	**Reserved.**
PXDCAVG_AUTO_BASELINE	3	**Proximity Automatic Baseline.** When asserted, PBSLN_MEAS is written to PBSLN whenever PBSLN_MEAS is less than PBSLN. When this happens, the BASELINE_ ADJUSTED flag is raised. The default value is 1.
PXDCAVG_BASELINE_WINDOW	2:0	**Prox Baseline Averaging Window.** Sets the number of proximity samples averaged to calculate PBSLN_MEAS, which is updated at the end of each window. The default value is 16 samples.

VALUE	SAMPLES
0	Skip
1	2
2	4
…	$n_{Iterations} = 2^{PXDCAVG\_BASELINE\_WINDOW}$
6	64
7	128

Calibration Configuration Register Two (CALIBCFG2 0xDA)

Figure 65:
Calibration Configuration Register Two

7	6	5	4	3	2	1	0
DCAVG_ AUTO_GTHR	BINSRCH_TARGET			AUTO_GTHR_IN_MULT			

Field	Bits	Description
DCAVG_AUTO_GTHR	7	**DC Averaging Automatic Thresholds.** When asserted, GTHR_IN and GTHR_OUT are automatically written with a multiple of the PBSLN at the end of the calibration routine. The multiplication factor is set in AUTO_GTHR_IN_MULT.
BINSRCH_TARGET	6:4	**Binary Search Target.** Sets the ADC target for proximity/gesture calibration. The default value is 2.

VALUE	SEARCH TARGET
0	0
1	1
2	3
…	$Target_{BINSRCH} = 2^{BINSRCH\_TARGET} - 1$
6	63
7	127

Field	Bits	Description
AUTO_GTHR_IN_MULT	3:0	**Automatic Gesture Threshold Multiplier.** Sets the multiplication factor used if the gesture entry and exit thresholds are automatically calculated as a multiple of PBSLN. The default value is 0, but the recommended value is 8 (3x factor).

VALUE	MULTIPLIER
0	1.00
1	1.25
2	1.50
…	$factor = \frac{(AUTO\_GTHR\_IN\_MULT + 4)}{4}$
14	4.50
15	4.75

Calibration Configuration Register Three (CALIBCFG3 0xDB)

Figure 66:
Calibration Configuration Register Three

7	6	5	4	3	2	1	0
Reserved				ZERO_WEIGHT			

Field	Bits	Description
ZERO_WEIGHT	3:0	**Zero Detection Weighting Filter.** Sets the frequency of detection of zeroes necessary to raise the ZERO_DETECTED flag. ZERO_WEIGHT should only be used if DCAVG_AUTO_OFFSET_ADJUST and PROX_AUTO_OFFSET_ADJUST are NOT used, in other words, when offset adjustments are handled only by software. If the automatic on-chip adjustments are made, ZERO_WEIGHT has no purpose. ZERO_DETECTED is raised when an internal counter reaches a value of 15. During normal proximity/gesture operation, if any of the ADC values on the four channels is zero, the counter increments by ZERO_WEIGHT. Every time there are no zeroes, it decrements by 1. At each weight, there is an equilibrium frequency that will rarely raise the ZERO_DETECTED flag. For example, if ZERO_WEIGHT is set to 3, zero detection will be at equilibrium if there are 3 non-zero cycles for every 1 zero cycle, a 25% frequency of zeroes. Even at equilibrium, there is a chance that enough zeroes will occur in a short period of time to raise the ZERO_DETECTED flag. For each weighting, there is a never flag frequency below which it is exceedingly unlikely that the flag will be raised.

VALUE	WEIGHT	EQUILIBRIUM FREQUENCY	NEVER FLAG FREQUENCY
0	0	Never (Ignored)	Never (Ignored)
1	1	50%	35%
2	2	33%	16%
3	3	25%	8%
4	4	20%	4%
5	5	17%	2%

Calibration Status Register (CALIBSTAT 0xDC)

Figure 67:
Calibration Status Register

7	6	5	4	3	2	1	0
Reserved				ZERO_ DETECTED	BASELINE_ ADJUSTED	OFFSET_ ADJUSTED	CALIB_ FINISHED

Field	Bits	Description
Reserved	7:4	**Reserved.**
ZERO_DETECTED	3	**Zero Detected.** Indicates that zeroes are being detected in proximity or gesture often enough to exceed the ZERO_WEIGHT conditions. Recalibration is recommended. Bit generates interrupt if CIEN is asserted. To prevent interrupt, set ZERO_WEIGHT to zero. Clear this bit by writing '1' to it.
BASELINE_ADJUSTED	2	**Proximity/Gesture Baseline Adjusted.** Indicates that the proximity baseline, PBSLN, has changed. This may occur in two ways: During DC averaging at calibration, if DCAVG_AUTO_BASELINE is asserted (independent of actual value). During regular proximity/gesture operation if DCAVG_AUTO_BASELINE is set and a new PBSLN_MEAS value is collected that is lower than previous PBSLN). Bit generates interrupt if CIEN is asserted. To prevent interrupt, set DCAVG_AUTO_BASELINE and PXDCAVG_AUTO_BASELINE to zero. Clear bit by writing '1' to it or by writing '1' to INTCLEAR_CINT.
OFFSET_ADJUSTED	1	**Proximity/Gesture Offset Adjusted.** Indicates that one or more proximity/gesture offset register values were automatically adjusted. Bit generates interrupt if CIEN is asserted. To prevent interrupt, set DCAVG_AUTO_OFFSET_ADJUST and PROX_AUTO_OFFSET_ADJUST to zero. Clear bit by writing '1' to it.
CALIB_FINISHED	0	**Calibration Finished.** Indicates that calibration is complete. Bit generates interrupt if CIEN is asserted. Clear bit by writing '1' to it.

Interrupt Enable Register (INTENAB 0xDD)

Figure 68:
Interrupt Enable Register

7	6	5	4	3	2	1	0
ASIEN	PGSIEN	PIEN	AIEN	Reserved	GIEN	CIEN	Reserved

Field	Bits	Description
ASIEN	7	**ALS Saturation Interrupt Enable.** When asserted permits ALS saturation interrupts to be generated. Bit is mirrored in the CFG1 register.
PGSIEN	6	**Proximity Saturation Interrupt Enable.** When asserted permits proximity saturation interrupts to be generated. Bit is mirrored in the CFG1 register.
PIEN	5	**Proximity Interrupt Enable.** When asserted permits proximity interrupts to be generated, subject to the proximity thresholds and persistence filter. Bit is mirrored in the ENABLE register.
AIEN	4	**ALS Interrupt Enable.** When asserted permits ALS interrupts to be generated, subject to the ALS thresholds and persistence filter. Bit is mirrored in the ENABLE register.
Reserved	3	**Reserved.**
GIEN	2	**Gesture Interrupt Enable.** When asserted permits all gesture-related interrupts to occur. The first gesture interrupt is subject to GFIFOTHR. Bit is mirrored in the GST_CTRL register.
CIEN	1	**Calibration Interrupt Enable.** When asserted permits calibration interrupts to be generated.
Reserved	0	**Reserved.**

Interrupt Clear Register (INTCLEAR 0xDE)

Figure 69:
Interrupt Clear Register

7	6	5	4	3	2	1	0
INTCLEAR_ ASAT	INTCLEAR_ PGSAT	INTCLEAR_ PINT	INTCLEAR_ AINT	Reserved	INTCLEAR_ GINT	INTCLEAR_ CINT	Reserved

Field	Bits	Description
INTCLEAR_ASAT	7	**Clear Interrupt: Analog Saturation.** Clears the analog saturation interrupt.
INTCLEAR_PGSAT	6	**Clear Interrupt: Proximity Saturation.** Clears the proximity saturation interrupt.
INTCLEAR_PINT	5	**Clear Interrupt: Proximity.** Clears the proximity interrupt.
INTCLEAR_AINT	4	**Clear Interrupt: ALS.** Clears the ALS interrupt.
Reserved	3	**Reserved.**
INTCLEAR_GINT	2	**Clear Interrupt: Gesture.** Must be used to clear the gesture interrupt after device exits GMODE and GVALID is asserted. If there is a gesture interrupt because the gesture FIFO level (GFIFO_LVL) is above the gesture FIFO threshold (GFIFOTHR), INTCLEAR_GINT will not clear the interrupt. To clear the gesture interrupt in this case, the data in the FIFO must be read.
INTCLEAR_CINT	1	**Clear Interrupt: Calibration.** Clears the calibration interrupt.
Reserved	0	**Reserved.**

Gesture FIFO Access Registers (0xF8 – 0xFF)

Gesture data is stored in a 256 byte FIFO buffer containing 32 eight byte datasets. Each dataset contains one sample each of North, South, West, & East gesture data. If the FIFO overflows (i.e. 33 datasets before host/system reads data from the FIFO buffer), an overflow flag will be set and new data will be lost.

Host/Systems acquire gesture data by reading addresses: 0xF8 – 0xFF, which directly correspond to North, South, West, and East data points. The register address pointer automatically wraps from 0xFF to 0xF8. Data can be read one byte at a time (eight consecutive I^2C transactions) or in blocks (there is no block-read length limit). When reading single bytes, the internal FIFO read pointer and the Gesture FIFO Buffer Level, GFIFO_LVL, are updated each time register 0xFF is read. For block-reads, the internal FIFO read pointer and the Gesture FIFO Buffer Level, GFIFO_LVL update for each eight byte dataset. If the FIFO continues to be accessed after GFIFO_LVL = 0, the device will return 0 for all data.

Gesture interrupts and the gesture valid (GVALID) flag indicate when there is valid data in the FIFO buffer. When the Gesture FIFO Buffer Level exceeds the Gesture Entry Threshold (GFIFO_LVL > GTHR_IN), a gesture interrupt is generated, and the GVALID flag is raised. Reading any data will clear the gesture interrupt, but GVALID will remain raised. A second interrupt is generated when the gesture is complete (GTHR_OUT conditions are met). The GVALID flag will remain raised until all data has been read, clearing the FIFO buffer. Once the FIFO buffer is empty, GVALID will be cleared to indicate that the gesture is complete and all data is read. The amount of unread data is indicated by the GFIFO_LVL.

Figure 70:
Gesture FIFO Access Registers

Field	Register	Bits	Description
GFIFO_N	0xF8	7:0	Gesture North FIFO low byte
	0xF9	15:8	Gesture North FIFO high byte
GFIFO_S	0xFA	7:0	Gesture South FIFO low byte
	0xFB	15:8	Gesture South FIFO high byte
GFIFO_W	0xFC	7:0	Gesture West FIFO low byte
	0xFD	15:8	Gesture West FIFO high byte
GFIFO_E	0xFE	7:0	Gesture East FIFO low byte
	0xFF	15:8	Gesture East FIFO high byte

Application Information

The typical application hardware circuit of this device is shown below.

Figure 71:
TMG49037 Typical Application Circuit

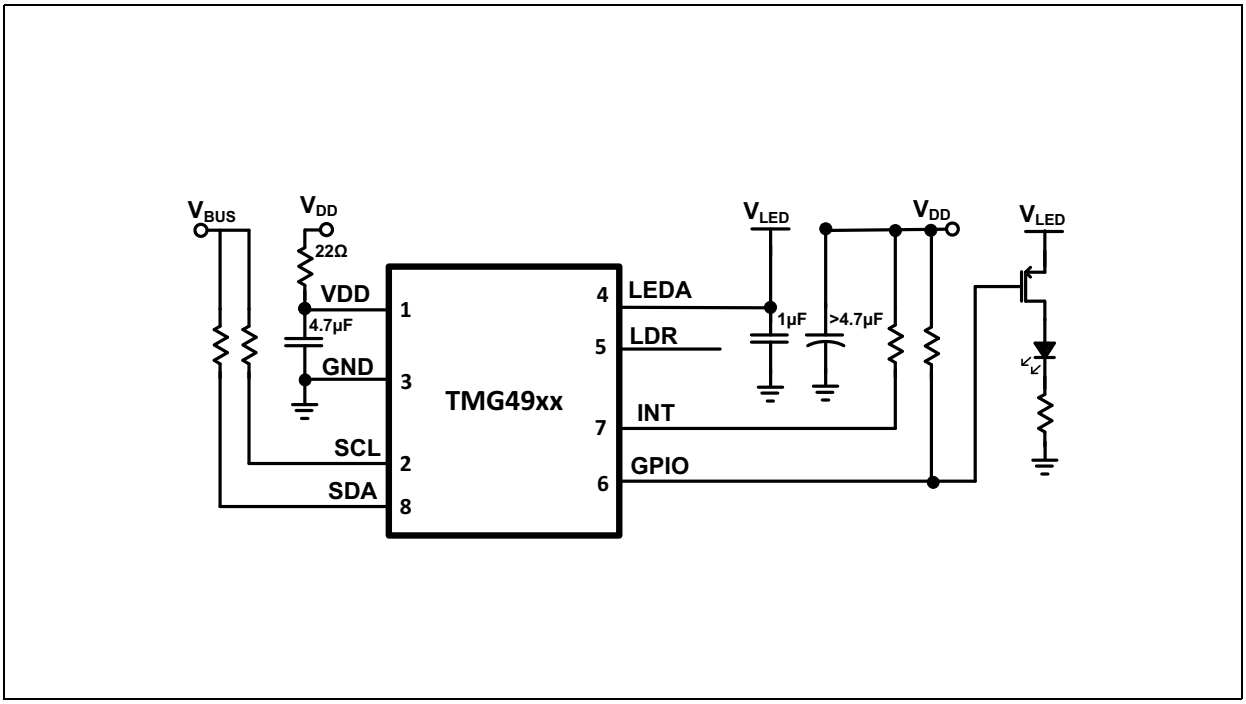
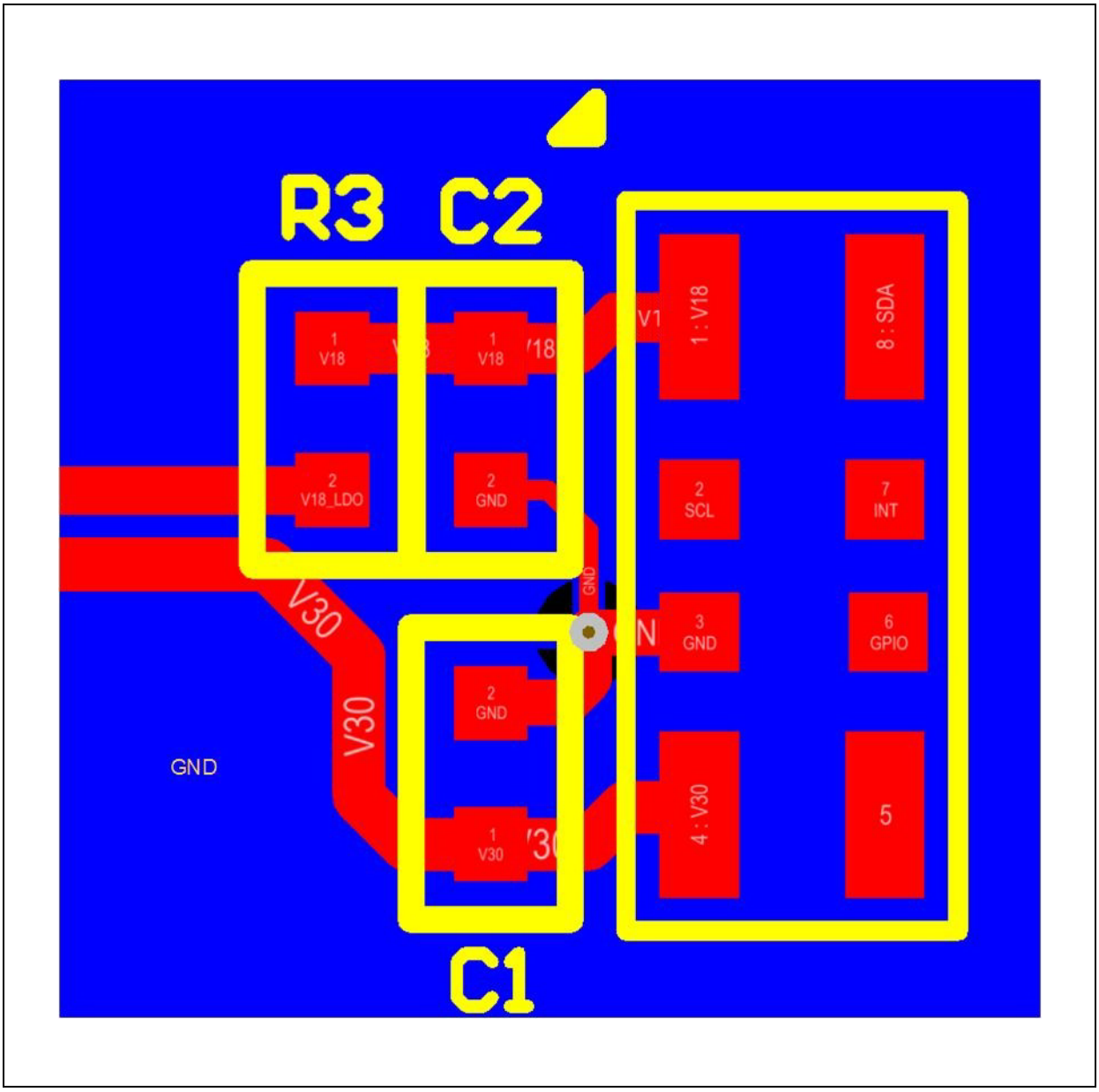
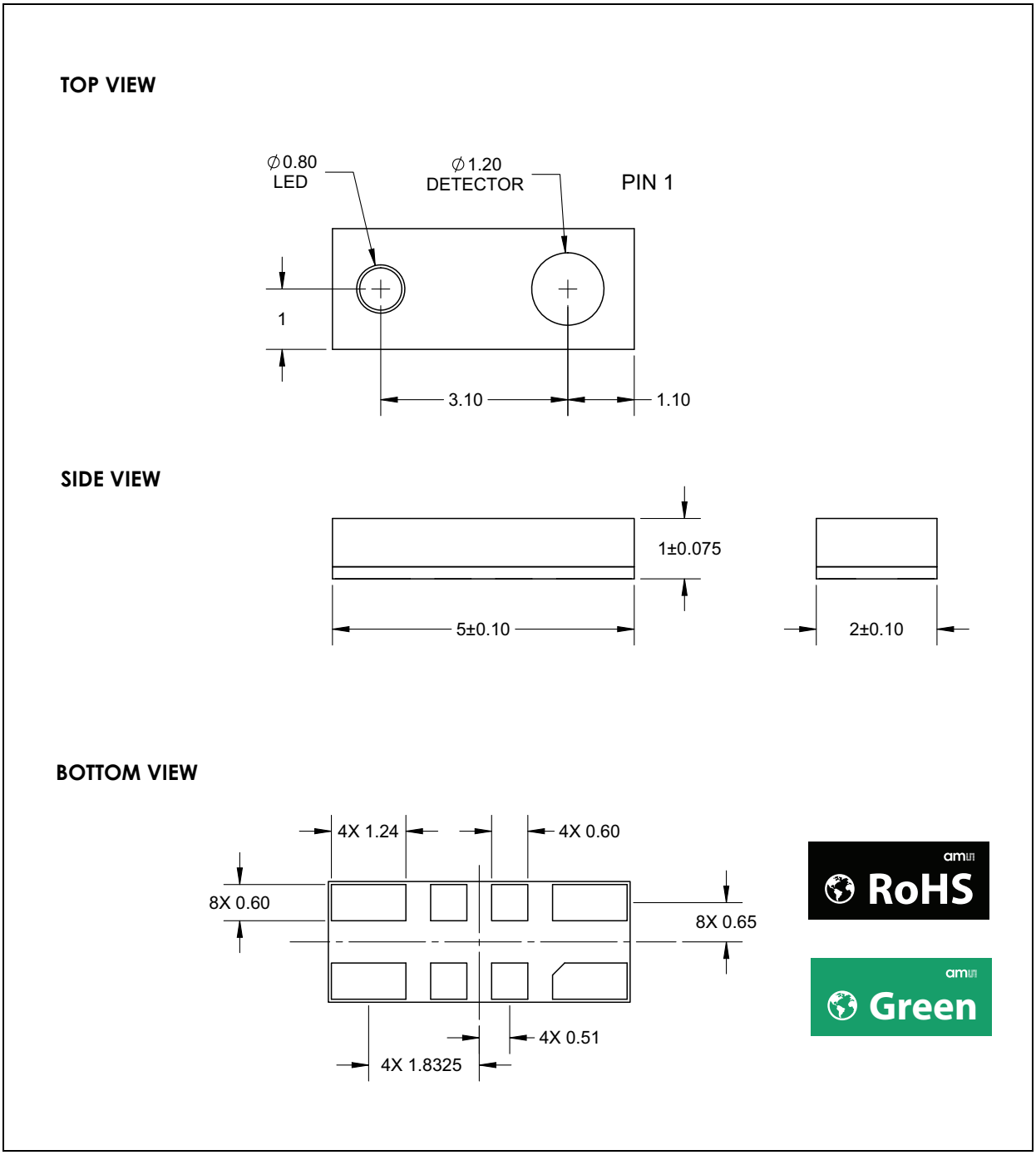


Figure 72:
TMG49037 Recommended Circuit Layout



Package Drawings & Markings

Figure 73:
TMG49037 Module Dimensions



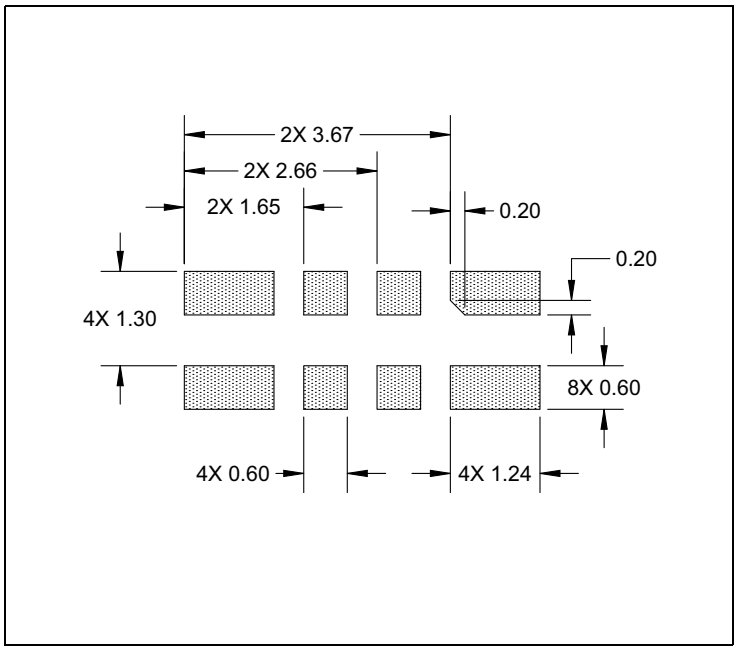
Note(s):

1. Package type: oLGA8
2. All linear dimensions are in millimeters.
3. Dimension tolerances are ±0.05mm unless otherwise noted.
4. Contacts are copper with NiPdAu plating.
5. This package contains no lead (Pb).
6. This drawing is subject to change without notice.
7. Measurement guarantee by lot acceptance testing using 20 units.

PCB Pad Layout

Suggested PCB pad layout guidelines for the surface mount module are shown. Flash Gold is recommended as a surface finish for the landing pads.

Figure 74:
Recommended PCB Pad Layout

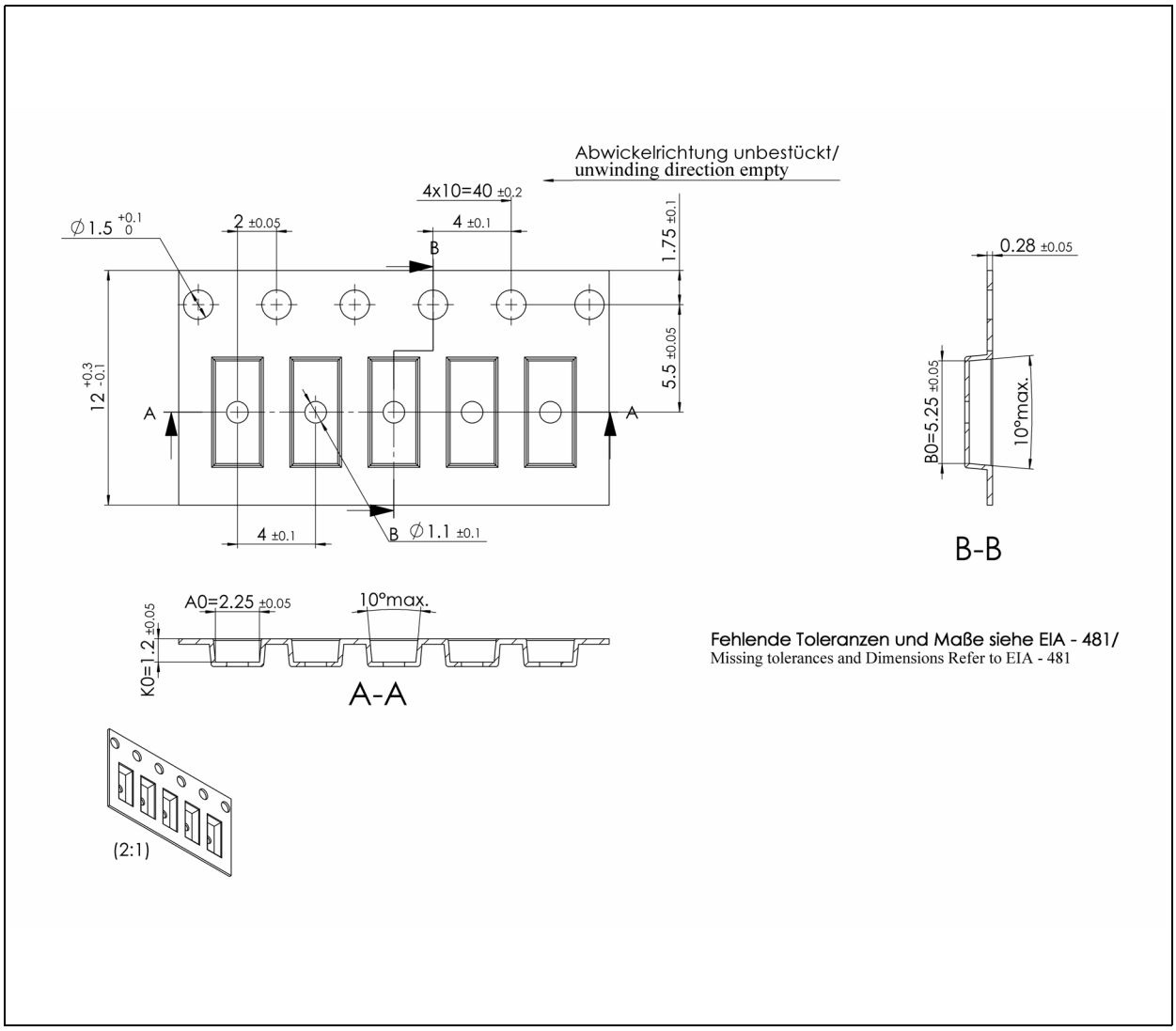


Note(s):

1. All linear dimensions are in millimeters.
2. Dimension tolerances are ±0.05mm unless otherwise noted.
3. This drawing is subject to change without notice.

Mechanical Data

Figure 75:
Tape and Reel Mechanical Drawing



Note(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ± 0.10 mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing Ao, Bo, and Ko are defined in ANSI EIA Standard 481−B 2001.
4. Each reel is 330 millimeters in diameter and contains 5000 parts.
5. **ams** packaging tape and reel conform to the requirements of EIA Standard 481−B.
6. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.

Soldering and Storage Information

Soldering Information

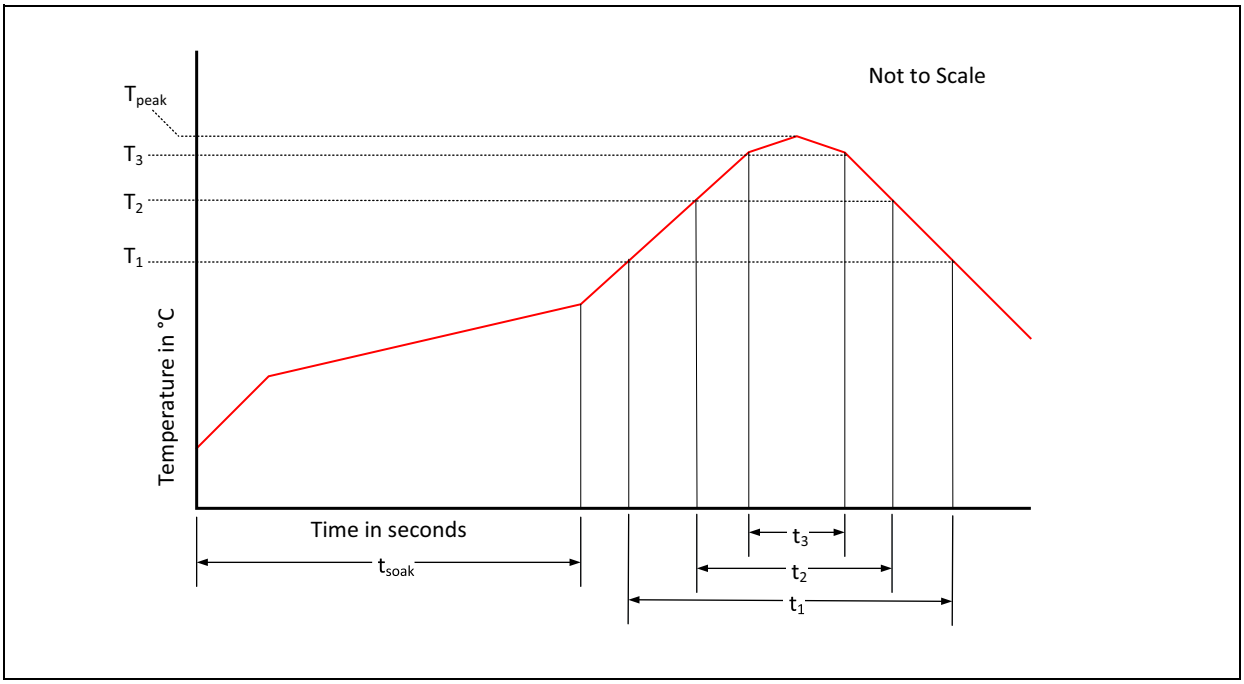
The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 76:
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5 °C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217 °C (T1)	t_1	Max 60s
Time above 230 °C (T2)	t_2	Max 50s
Time above T_{peak} – 10 °C (T3)	t_3	Max 10s
Peak temperature in reflow	T_{peak}	260 °C
Temperature gradient in cooling		Max -5 °C/s

Figure 77:
Solder Reflow Profile Graph



Storage Information

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping.

Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: <40°C
- Relative Humidity: <90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: <30°C
- Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

Ordering & Contact Information

Figure 78:
Ordering Information

Ordering Code	Address	Interface	Delivery Form
TMG49037	0x29	I^2C bus = 1.8V Interface	Tape & Reel

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ams Green (RoHS compliant and no Sb/Br): ams Green defines that in addition to RoHS compliance, our products are free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

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Revision Information

Changes from 1-00 (2019-Aug-15) to current revision 1-01 (2019-Aug-20)	Page
Updated figure 26	21
Updated Revision ID Register	35

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide