LM5112, LM5112-Q1 Tiny 7-A MOSFET Gate Driver

1 Features

- LM5112-Q1 is Qualified for Automotive Applications
- AEC-Q100 Grade 1 Qualified
- Manufactured on an Automotive Grade Flow
- Compound CMOS and Bipolar Outputs Reduce Output Current Variation
- 7-A Sink and 3-A Source Current
- Fast Propagation Times: 25 ns (Typical)
- Fast Rise and Fall Times: 14 ns or 12 ns Rise or Fall With 2-nF Load
- Inverting and Non-Inverting Inputs Provide Either Configuration With a Single Device
- Supply Rail Undervoltage Lockout Protection
- Dedicated Input Ground (IN_REF) for Split Supply or Single Supply Operation
- Power Enhanced 6-Pin WSON Package (3 mm × 3 mm) or Thermally Enhanced MSOP-PowerPAD Package
- Output Swings From V_{CC} to V_{EE} Which Are Negative Relative to Input Ground

2 Applications

- DC to DC Switch-Mode Power Supplies
- AC to DC Switch-Mode Power Supplies
- Solar Microinverters
- Solenoid and Motor Drives

3 Description

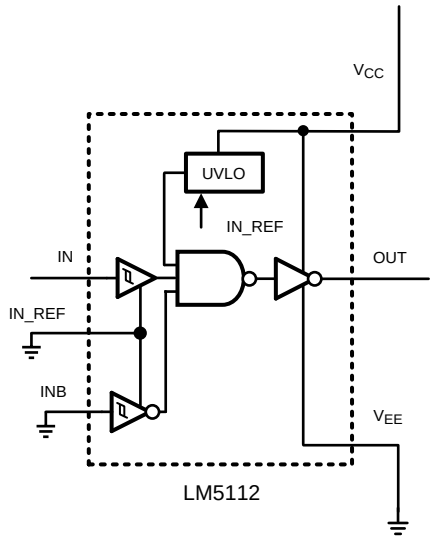
The LM5112 device MOSFET gate driver provides high peak gate drive current in the tiny 6-pin WSON package (SOT-23 equivalent footprint) or an 8-pin exposed-pad MSOP package with improved power dissipation required for high frequency operation. The compound output driver stage includes MOS and bipolar transistors operating in parallel that together sink more than 7 A peak from capacitive loads. Combining the unique characteristics of MOS and bipolar devices reduces drive current variation with voltage and temperature. Undervoltage lockout protection is provided to prevent damage to the MOSFET due to insufficient gate turnon voltage. The LM5112 device provides both inverting and non-inverting inputs to satisfy requirements for inverting and non-inverting gate drive with a single device type.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5112, LM5112-Q1	WSON (6)	3.00 mm × 3.00 mm
	MSOP PowerPAD (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram



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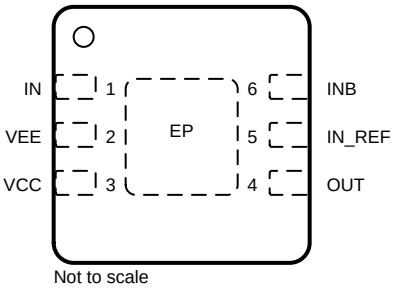
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2006) to Revision C	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Changed values in the *Thermal Information* table to align with JEDEC standards	4

5 Pin Configuration and Functions

NGG Package
6-Pin WSON
Top View



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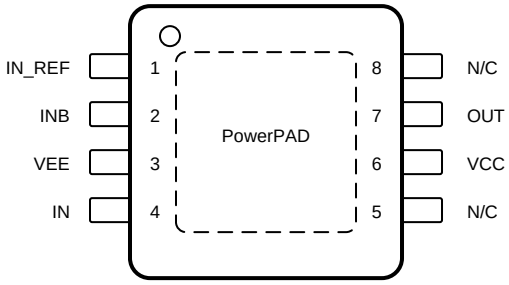
DGN Package
8-Pin MSOP PowerPAD
Top View



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Pin Functions

PIN			I/O	DESCRIPTION
NAME	WSON	MSOP		
Exposed Pad	—	—	—	Exposed pad, underside of package: Internally bonded to the die substrate. Connect to V_{EE} ground pin for low thermal impedance.
IN	1	4	I	Non-inverting input pin: TTL compatible thresholds. Pull up to V_{CC} when not used.
INB	6	2	I	Inverting input pin: TTL compatible thresholds. Connect to IN_REF when not used.
IN_REF	5	1	—	Ground reference for control inputs: Connect to power ground (V_{EE}) for standard positive only output voltage swing. Connect to system logic ground when V_{EE} is connected to a negative gate drive supply.
N/C	—	5, 8	—	Not internally connected
OUT	4	7	O	Gate drive output: Capable of sourcing 3 A and sinking 7 A. Voltage swing of this output is from V_{EE} to V_{CC}.
V_{CC}	3	6	I	Positive supply voltage input: Locally decouple to V_{EE}. The decoupling capacitor must be placed close to the chip.
V_{EE}	2	3	—	Power ground for driver outputs: Connect to either power ground or a negative gate drive supply for positive or negative voltage swing.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
V_{CC} to V_{EE}	–0.3	15	V
V_{CC} to IN_REF	–0.3	15	V
IN/INB to IN_REF	–0.3	15	V
IN_REF to V_{EE}	–0.3	5	V
Maximum junction temperature		150	°C
Operating junction temperature	–40	125	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Operating voltage, V_{CC} – IN_REF and V_{CC} – V_{EE}	3.5	14	V
	Operating junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM5112, LM5112-Q1		UNIT
		NGG (WSON)	DGN (MSOP PowerPAD)	
		6 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40	53.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.8	61.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.3	37.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	7.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.5	36.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.5	4.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{CC} = 12 V, INB = IN_REF = V_{EE} = 0 V, and no Load on output (unless otherwise noted).

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{CC}	Operating voltage	V_{CC} – IN_REF and V_{CC} – V_{EE}	3.5		14	V
UVLO	Undervoltage lockout (rising)	V_{CC} – IN_REF	2.4	3	3.5	V
V_{CCH}	Undervoltage hysteresis			230		mV
I_{CC}	Supply current			1	2	mA
CONTROL INPUTS						
V_{IH}	Logic high		2.3			V
V_{IL}	Logic low				0.8	V
V_{thH}	High threshold		1.3	1.75	2.3	V
V_{thL}	Low threshold		0.8	1.35	2	V
HYS	Input hysteresis			400		mV
I_{IL}	Input current low	IN = INB = 0 V	–1	0.1	1	µA
I_{IH}	Input current high	IN = INB = V_{CC}	–1	0.1	1	µA
OUTPUT DRIVER						
R_{OH}	Output resistance high	I_{OUT} = –10 mA(1)		30	50	Ω
R_{OL}	Output resistance low	I_{OUT} = 10 mA(1)		1.4	2.5	Ω
I_{SOURCE}	Peak source current	OUT = V_{CC} / 2,200 ns pulsed current		3		A
I_{SINK}	Peak sink current	OUT = V_{CC} / 2,200 ns pulsed current		7		A
LATCHUP PROTECTION						
	AEC–Q100, METHOD 004	T_J = 150°C		500		mA

(1) The output resistance specification applies to the MOS device only. The total output current capability is the sum of the MOS and bipolar devices.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
td1	Propagation delay time low to high, IN or INB rising (IN to OUT)	C_{LOAD} = 2 nF, see Figure 13		25	40	ns
td2	Propagation delay time high to low, IN or INB falling (IN to OUT)	C_{LOAD} = 2 nF, see Figure 13		25	40	ns
tr	Rise time	C_{LOAD} = 2 nF, see Figure 13		14		ns
tf	Fall time	C_{LOAD} = 2 nF, see Figure 13		12		ns

6.7 Typical Characteristics

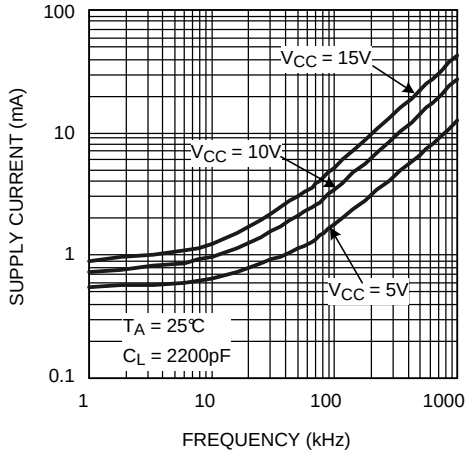


Figure 1. Supply Current vs Frequency

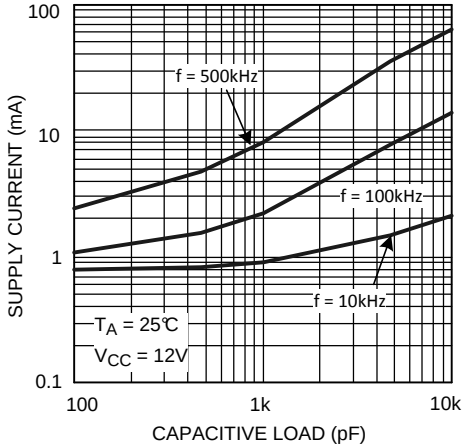


Figure 2. Supply Current vs Capacitive Load

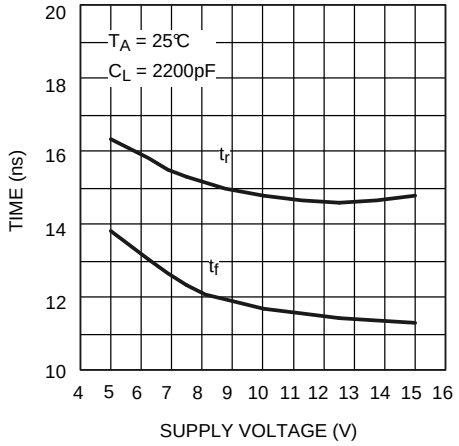


Figure 3. Rise and Fall Time vs Supply Voltage

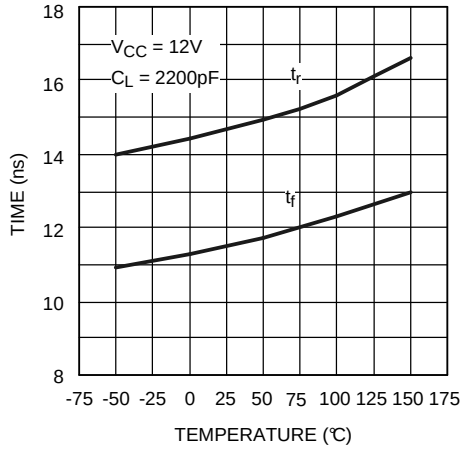


Figure 4. Rise and Fall Time vs Temperature

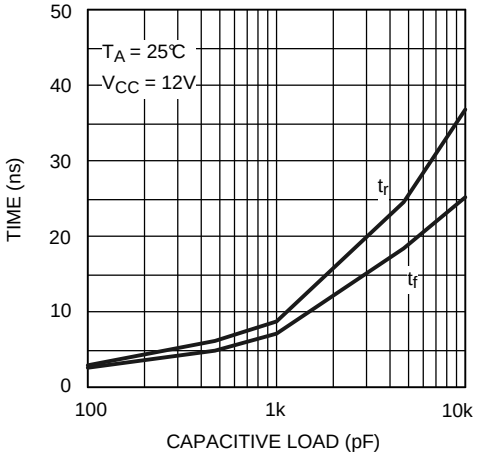


Figure 5. Rise and Fall Time vs Capacitive Load

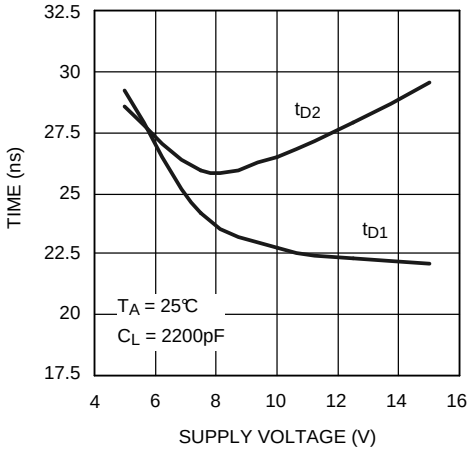


Figure 6. Delay Time vs Supply Voltage

Typical Characteristics (continued)

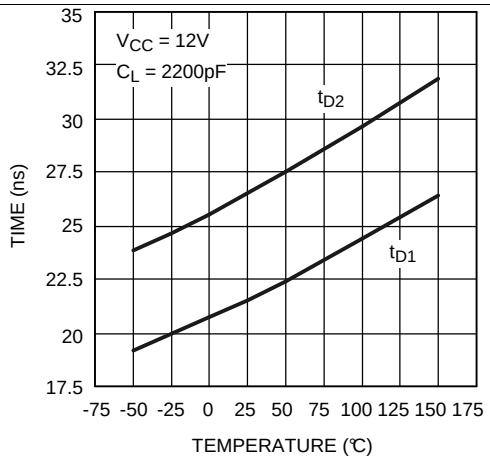


Figure 7. Delay Time vs Temperature

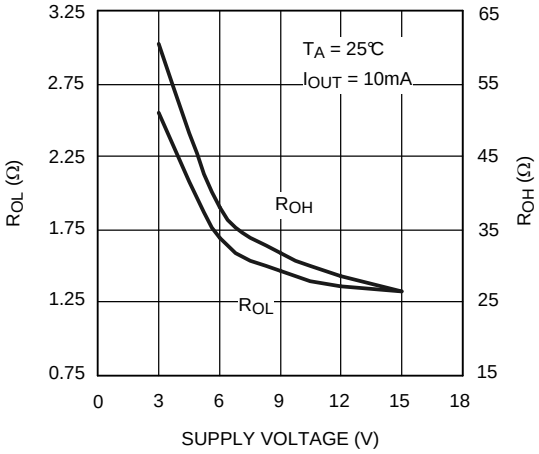


Figure 8. Rds(on) vs Supply Voltage

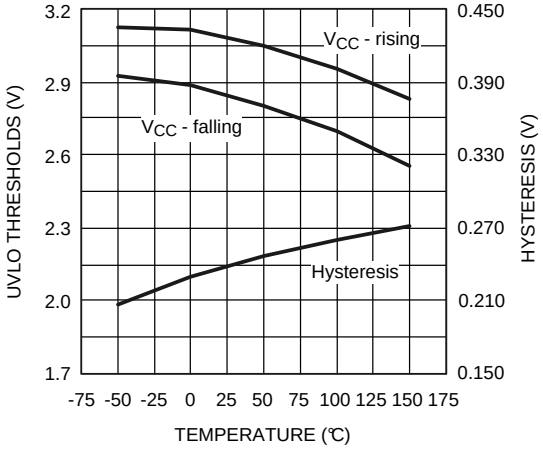


Figure 9. UVLO Thresholds and Hysteresis vs Temperature

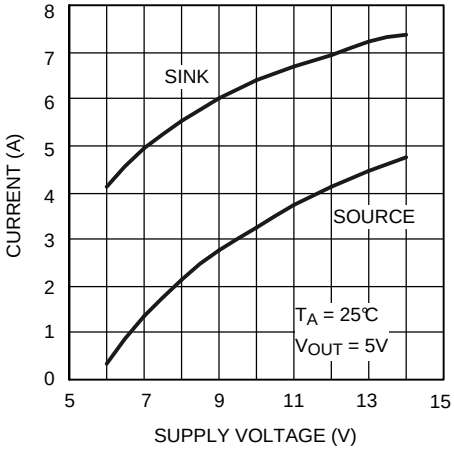


Figure 10. Peak Current vs Supply Voltage

7 Detailed Description

7.1 Overview

The LM5112 device is a high-speed, high-peak current (7 A) single-channel MOSFET driver. The high-peak output current of the LM5112 device switches power MOSFETs on and off with short rise and fall times, thereby reducing switching losses considerably. The LM5112 device includes both inverting and non-inverting inputs that give the user flexibility to drive the MOSFET with either active low or active high logic signals. The driver output stage consists of a compound structure with MOS and bipolar transistor operating in parallel to optimize current capability over a wide output voltage and operating temperature range. The bipolar device provides high peak current at the critical Miller plateau region of the MOSFET V_{GS}, while the MOS device provides rail-to-rail output swing. The totem pole output drives the MOSFET gate between the gate drive supply voltage V_{CC} and the power ground potential at the V_{EE} pin.

7.2 Functional Block Diagram

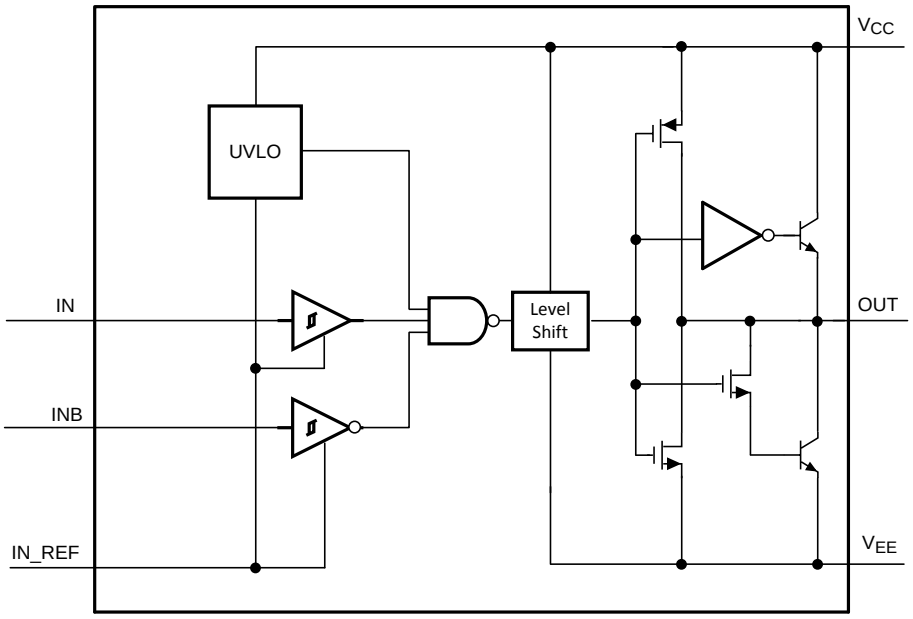


Figure 11. LM5112 Functional Block Diagram

7.3 Feature Description

The control inputs of the driver are high impedance CMOS buffers with TTL compatible threshold voltages. The negative supply of the input buffer is connected to the input ground pin IN_REF. An internal level shifting circuit connects the logic input buffers to the totem pole output drivers. The level shift circuit and the separate input or output ground pins provide the option of single supply or split supply configurations. When driving the MOSFET gate from a single positive supply, the IN_REF and V_{EE} pins are both connected to the power ground.

The isolated input and output stage grounds provide the capability to drive the MOSFET to a negative V_{GS} voltage for a more robust and reliable off state. In split supply configuration, the IN_REF pin is connected to the ground of the controller which drives the LM5112 inputs. The V_{EE} pin is connected to a negative bias supply that can range from the IN_REF potential to as low as 14 V below the V_{CC} gate drive supply. For reliable operation, the maximum voltage difference between V_{CC} and IN_REF or between V_{CC} and V_{EE} is 14 V.

The minimum recommended operating voltage between V_{CC} and IN_REF is 3.5 V. An undervoltage lockout (UVLO) circuit is included in the LM5112 which senses the voltage difference between V_{CC} and the input ground pin, IN_REF. When the V_{CC} to IN_REF voltage difference falls below 2.8 V the driver is disabled and the output pin is held in the low state. The UVLO hysteresis prevents chattering during brown-out conditions; the driver resumes normal operation when the V_{CC} to IN_REF differential voltage exceeds 3 V.

7.4 Device Functional Modes

The device output state is dependent on states of the IN and INB pins. Table 1 lists the output states for different input pin combinations.

Table 1. Device Logic Table

IN PIN	INB PIN	OUT PIN
L	L	L
L	H	L
H	L	H
H	H	L

7.4.1 Inverting Mode

During the inverting mode of operation, INB is used as the control input and the polarity of OUT is reversed with respect to INB. Figure 12 shows a timing diagram of this mode. The IN pin is not used in this mode of operation and must be pulled up to V_{CC}.

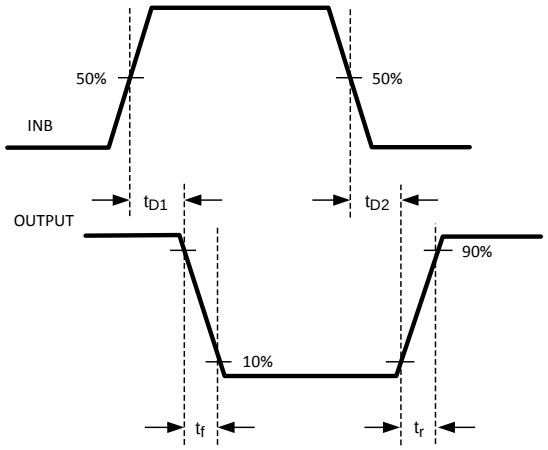


Figure 12. Inverting

7.4.2 Non-Inverting Mode

During the non-inverting mode of operation, IN is used as the control input and the polarity of OUT is the same with respect to IN. Figure 13 shows a timing diagram of this mode. The INB pin is not used in this mode of operation and must be connected to IN_REF.

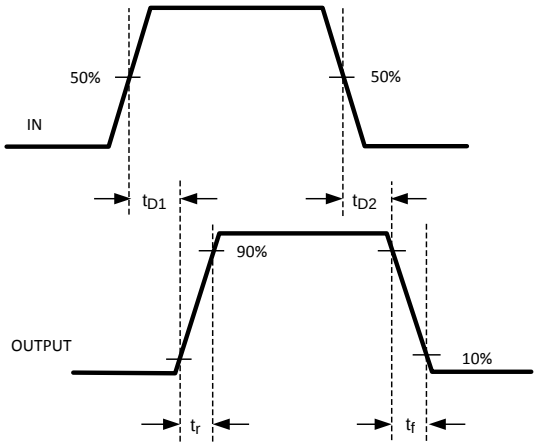


Figure 13. Non-Inverting

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

A leading application for gate drivers such as the LM5112 is providing a high power buffer stage between the PWM output of a control IC and the gates of the primary power switching devices. In other cases, the driver IC is used to drive the power device gates through a drive transformer. Driver ICs are used when it is not feasible to have the primary PWM regulator IC directly drive the switching devices for one or more reasons. The PWM IC may not have the brute drive capability required for the intended switching MOSFET, limiting the switching performance in the application.

The LM5112 is used to drive a low side MOSFET with low switching losses. Either one of the control input pins, IN or INB, are used to control the gate drive to the MOSFET. The choice of the control input pin used depends on the polarity of operation.

8.2 Typical Application

Typical application diagrams for the LM5112 device are shown below, illustrating use in non-inverting and inverting driver configurations. The high peak gate drive current of the LM5112 allows for short rise and fall times on the low-side MOSFET, thereby improving overall efficiency of the system and reducing switching losses.

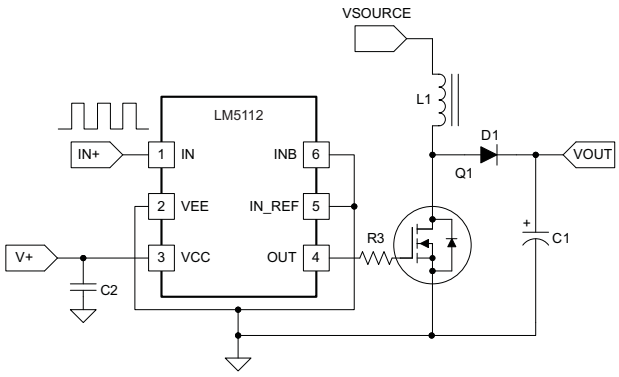


Figure 14. Typical Application Diagram (Using Non-Inverting Control Input)

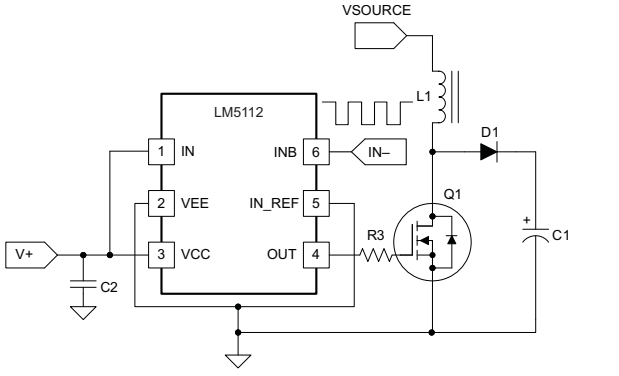


Figure 15. Typical Application Diagram (Using Inverting Control Input)

Typical Application (continued)

8.2.1 Design Requirements

When selecting the proper gate driver device for an end application, some design considerations must be evaluated first to make the most appropriate selection. Among these considerations are input-to-output configuration, the input threshold type, bias supply voltage levels, peak source and sink currents, capacitive load, and switching frequency. Table 2 shows some sample values for a typical application.

Table 2. Design Parameters

PARAMETER	VALUE
Input-to-output logic	Non-inverting
V_{CC} bias supply voltage (measured with respect to V_{EE})	12 V
Supply configuration	Split supply
Peak source current	3 A
Peak sink current	7 A
Output load (MOSFET gate capacitance)	2 nF
Gate drive resistor	1 Ω
Switching frequency	300 kHz

8.2.2 Detailed Design Procedure

See *Power Supply Recommendations* , *Layout*, and *Thermal Considerations* for key design considerations regarding the input supply, grounding, and thermal calculations specific to the LM5112.

8.2.3 Application Curves

The rise and fall times of the OUT signal depends on the capacitance of the MOSFET gate. Therefore, an appropriate MOSFET must be selected to meet the switching speed and efficiency requirements of the system. Figure 16 shows the rise and fall time curves as a function of capacitive load. Figure 17 shows output rise and fall time measured on an application board, showing actual device performance. The testing conditions for this figure are C_{load}= 2.2 nF, R_{drive} = 1 Ω, and f_s = 300 kHz.

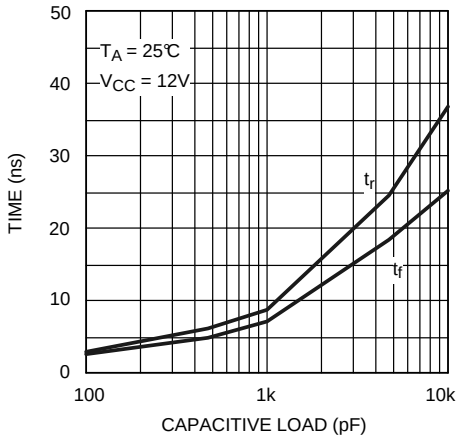
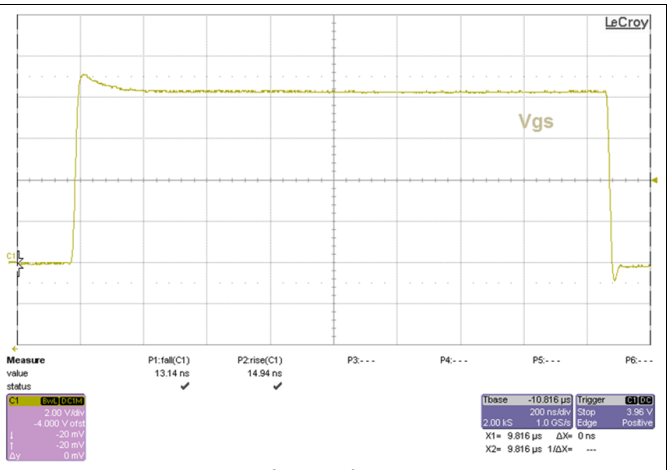


Figure 16. Rise and Fall Time vs Capacitive Load



C_{load}= 2.2 nF, R_{drive} = 1 Ω, f_s = 300 kHz

Figure 17. Measured Rise and Fall Time

9 Power Supply Recommendations

The recommended bias supply voltage range for LM5112 is from 3.5 V to 14 V. The lower end of this range is governed by the internal UVLO protection feature of the V_{CC} supply circuit. The upper end of this range is driven by the 14 V maximum recommended operating voltage rating of the V_{CC} supply. It is recommended to keep proper margin to allow for transient voltage spikes. The dedicated input ground pin (IN_REF) allows split output supply operation. For such applications, ensure V_{EE} is not connected to IN_REF.

The UVLO protection feature also involves a hysteresis function. This means that once the device is operating in normal mode, if the V_{CC} voltage drops, the device continues to operate in normal mode as long as the voltage drop does not exceed the hysteresis specification, V_{CCH}. If the voltage drop is greater than the hysteresis specification, the device shuts down. Therefore, while operating at or near the 3.5 V range, the voltage ripple on the auxiliary power supply output must be smaller than the hysteresis specification of LM5112 to avoid triggering device-shutdown.

A low-ESR or low-ESL capacitor must be connected close to the IC and between the V_{CC} and V_{EE} pins to support high peak currents being drawn from V_{CC} during turnon of the MOSFET. Also, if input pin (IN or INB) is not being used, it must be connected to V_{CC} or IN_REF, respectively, to avoid spurious output signals.

10 Layout

10.1 Layout Guidelines

Attention must be given to board layout when using the LM5112 device. Some important considerations include:

Proper grounding is crucial. The driver required a low impedance path for current return to ground avoiding inductive loops. Two paths for returning current to ground are a) between the LM5112 device IN_REF pin and the ground of the circuit that controls the driver inputs and b) between the LM5112 device V_{EE} pin and the source of the power MOSFET being driven. Both paths must be as short as possible to reduce inductance and be as wide as possible to reduce resistance. These ground paths must be distinctly separate to avoid coupling between the high current output paths and the logic signals that drive the LM5112 device. With rise and fall times in the range of 10 nsec to 30 nsec, care is required to minimize the lengths of current carrying conductors to reduce their inductance and EMI from the high di/dt transients generated when driving large capacitive loads.

10.1.1 Thermal Considerations

The primary goal of the thermal management is to maintain the integrated circuit (IC) junction temperature (T_J) below a specified limit to ensure reliable long term operation. The maximum T_J of IC components must be estimated in worst case operating conditions. The junction temperature is calculated based on the power dissipated on the IC and the junction to ambient thermal resistance $R_{\theta JA}$ for the IC package in the application board and environment. The $R_{\theta JA}$ is not a given constant for the package and depends on the PCB design and the operating environment.

Layout Guidelines (continued)

10.1.1.1 Drive Power Requirement Calculations In LM5112

The LM5112 device is a single, low-side MOSFET driver capable of sourcing and sinking 3-A or 7-A peak currents for short intervals to drive a MOSFET without exceeding package power dissipation limits. High peak currents are required to switch the MOSFET gate quickly for operation at high frequencies.

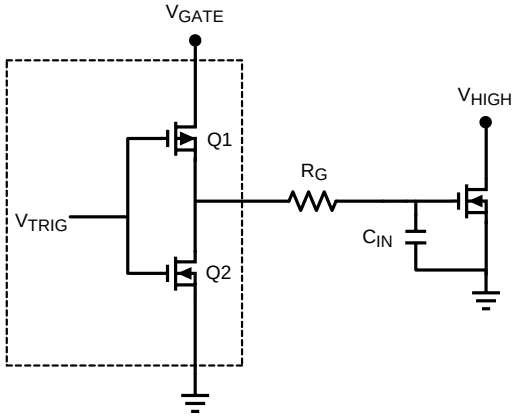


Figure 18. MOSFET Driver Diagram

Figure 18 shows a conceptual diagram of the LM5112 device output and MOSFET load. Q1 and Q2 are the switches within the gate driver. R_G is the gate resistance of the external MOSFET, and Cin is the equivalent gate capacitance of the MOSFET. The equivalent gate capacitance is a difficult parameter to measure as it is the combination of C_{GD} (gate to source capacitance) and C_{GD} (gate to drain capacitance). The C_{GD} is not a constant and varies with the drain voltage. The better way of quantifying gate capacitance is the gate charge Q_G in coloumbs. Q_G combines the charge required by C_{GD} and C_{GD} for a given gate drive voltage V_{GATE}. The gate resistance R_G is usually small and losses in it are neglected. The total power dissipated in the MOSFET driver due to gate charge is approximated by Equation 1.

$$P_{DRIVER} = V_{GATE} \times Q_G \times F_{SW}$$

where

- F_{SW} = switching frequency of the MOSFET (1)

For example, consider the MOSFET MTD6N15 whose gate charge specified as 30 nC for V_{GATE} = 12 V.

Therefore, the power dissipation in the driver due to charging and discharging of MOSFET gate capacitances at switching frequency of 300 kHz and V_{GATE} of 12 V is equal to Equation 2.

$$P_{DRIVER} = 12\ V \times 30\ nC \times 300\ kHz = 0.108\ W \quad (2)$$

In addition to the above gate charge power dissipation, - transient power is dissipated in the driver during output transitions. When either output of the LM5112 device changes state, current flows from V_{CC} to V_{EE} for a brief interval of time through the output totem-pole N and P channel MOSFETs. The final component of power dissipation in the driver is the power associated with the quiescent bias current consumed by the driver input stage and Undervoltage lockout sections.

Layout Guidelines (continued)

Characterization of the LM5112 device provides accurate estimates of the transient and quiescent power dissipation components. At 300 kHz switching frequency and 30 nC load used in the example, the transient power is 8 mW. The 1 mA nominal quiescent current and 12 V V_{GATE} supply produce a 12 mW typical quiescent power.

Therefore, the total power dissipation is calculated with Equation 3.

$$P_D = 0.118 + 0.008 + 0.012 = 0.138 \text{ W} \quad (3)$$

The junction temperature is given by Equation 4.

$$T_J = P_D \times R_{\theta JA} + T_A \quad (4)$$

Or the rise in temperature is given by Equation 5.

$$T_{RISE} = T_J - T_A = P_D \times R_{\theta JA} \quad (5)$$

For 6-pin WSON package, the integrated circuit die is attached to leadframe die pad which is soldered directly to the printed circuit board. This substantially decreases the junction to ambient thermal resistance ($R_{\theta JA}$). By providing suitable means of heat dispersion from the IC to the ambient through exposed copper pad, which can readily dissipate heat to the surroundings, $R_{\theta JA}$ as low as 40°C/W is achievable with the package. The resulting T_{RISE} for the driver example above is thereby reduced to just 5.5°C.

Therefore, T_{RISE} is equal to Equation 6.

$$T_{RISE} = 0.138 \times 40 = 5.5°C \quad (6)$$

For MSOP-PowerPAD, $R_{\theta JA}$ is typically 60°C/W.

10.2 Layout Example

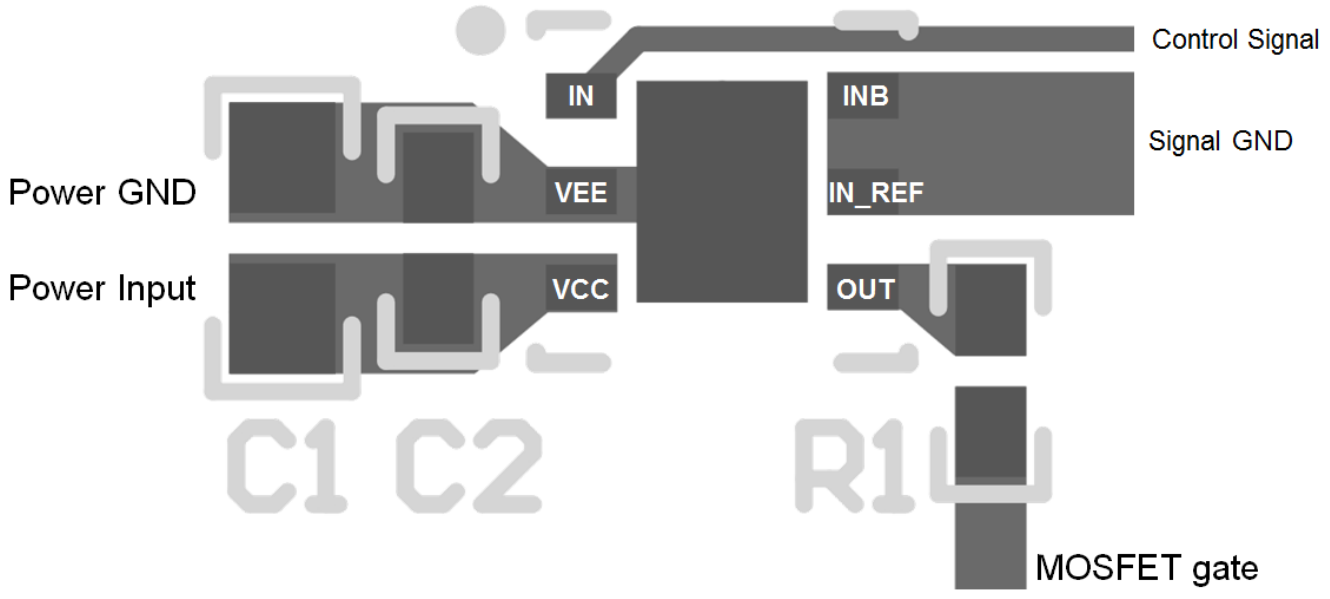


Figure 19. LM5112 Layout Example

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM5112	Click here	Click here	Click here	Click here	Click here
LM5112-Q1	Click here	Click here	Click here	Click here	Click here

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5112MY/NOPB	ACTIVE	HVSSOP	DGN	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM		SJJB	Samples
LM5112MYX/NOPB	ACTIVE	HVSSOP	DGN	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM		SJJB	Samples
LM5112Q1SD/NOPB	ACTIVE	WSON	NGG	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L250B	Samples
LM5112Q1SDX/NOPB	ACTIVE	WSON	NGG	6	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L250B	Samples
LM5112SD	NRND	WSON	NGG	6	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	L132B	
LM5112SD/NOPB	ACTIVE	WSON	NGG	6	1000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L132B	Samples
LM5112SDX/NOPB	ACTIVE	WSON	NGG	6	4500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L132B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LM5112, LM5112-Q1 :

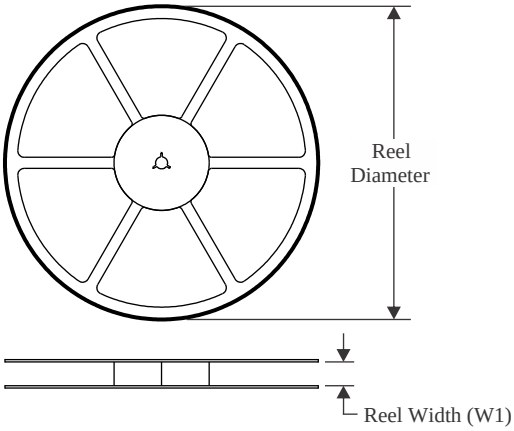
- Catalog : LM5112
- Automotive : LM5112-Q1

NOTE: Qualified Version Definitions:

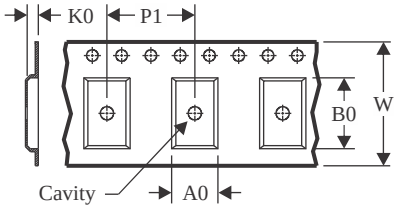
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

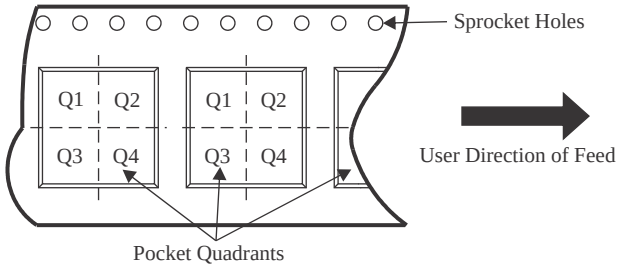


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

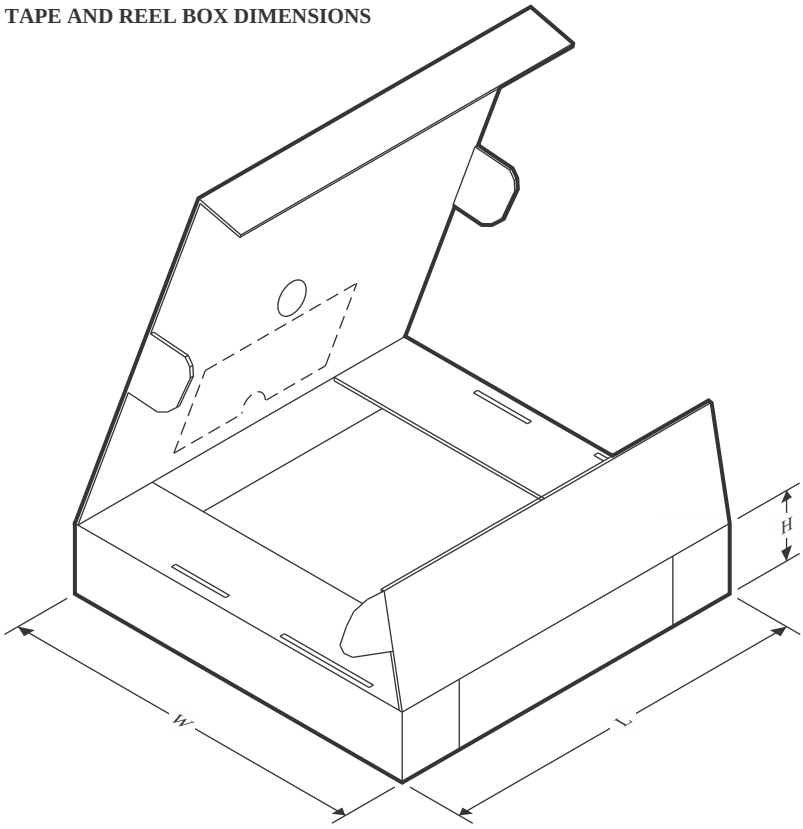
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5112MY/NOPB	HVSSOP	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5112MYX/NOPB	HVSSOP	DGN	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5112Q1SD/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM5112Q1SDX/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM5112SD/NOPB	WSON	NGG	6	1000	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM5112SD/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM5112SDX/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5112MY/NOPB	HVSSOP	DGN	8	1000	208.0	191.0	35.0
LM5112MYX/NOPB	HVSSOP	DGN	8	3500	367.0	367.0	35.0
LM5112Q1SD/NOPB	WSON	NGG	6	1000	208.0	191.0	35.0
LM5112Q1SDX/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LM5112SD/NOPB	WSON	NGG	6	1000	200.0	183.0	25.0
LM5112SD/NOPB	WSON	NGG	6	1000	208.0	191.0	35.0
LM5112SDX/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0

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