Mercury+ AA1 SoC Module

User Manual

Purpose

The purpose of this document is to present the characteristics of Mercury+ AA1 SoC module to the user, and to provide the user with a comprehensive guide to understanding and using the Mercury+ AA1 SoC module.

Summary

This document first gives an overview of the Mercury+ AA1 SoC module followed by a detailed description of its features and configuration options. In addition, references to other useful documents are included.

Product Information	Code	Name
Product	ME-AA1	Mercury+ AA1 SoC Module

Document Information	Reference	Version	Date
Reference / Version / Date	D-0000-419-001	09	16.02.2021

Approval Information	Name	Position	Date
Written by	DIUN	Design Engineer	22.04.2016
Verified by	GLAC	Design Expert	29.04.2016
Approved by	DIUN	Manager, BU SP	16.02.2021

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Document History

Version	Date	Author	Comment
09	16.02.2021	DIUN	Corrected information on number of PCIe endpoints supported, added information on Mercury heatsinks, added Mercury+ ST1 to accesories section, added information on FPGA fuses and warranty, on differential I/Os, on voltage monitoring outputs, other style updates and minor corrections
08	25.07.2019	DIUN	Added information on voltage monitoring, power supplies, heat sink, Linux how-to guide, JTAG interface, other style updates
07	21.08.2018	DIUN	Minor corrections and style updates
06	13.04.2018	DIUN	Updated MGT supply information
05	20.03.2018	DIUN	Updated information on DDR timing, MGT usage and clocking requirements, and HPS pinout configuration for UART and LEDs
04	04.05.2017	DIUN	Updated EEPROM map, block diagram and footprint information
03	19.09.2016	DIUN	Version 03, preliminary, minor corrections and updates
02	09.06.2016	DIUN	Version 02, preliminary, corrected typo on device type
01	06.06.2016	DIUN	Version 01, preliminary

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1 Overview

1.1 General

1.1.1 Introduction

The Mercury+ AA1 SoC module combines the Intel Arria®10 V ARM® processor-based SoC (System-on-Chip) device with USB 3.0 controller and PHY, USB 2.0 PHY, PCIe® Gen3 ×8, Gigabit Ethernet, DDR4 SDRAM with Error Correction Code (ECC), eMMC flash, multi-gigabit transceivers, high-speed LVDS I/O, and is available in industrial temperature range, forming a complete and powerful embedded processing system.

The use of the Mercury+ AA1 SoC module, in contrast to building a custom SoC hardware, significantly simplifies system design and thus shortens time to market and decreases the development effort of your product. Together with Mercury+ base boards, the Mercury+ AA1 SoC module allows the user to quickly build a system prototype and start with application development.

The Enclustra Build Environment [14] is available for the Mercury+ AA1 SoC module. This build system allows the user to quickly set up and run Linux on any Enclustra SoC module. It allows the user to choose the desired target, and download all the required binaries, such as bitstream and preloader. It downloads and compiles all required software, such as U-Boot, Linux, and BusyBox based root file system.

1.1.2 Warranty

Please refer to the General Business Conditions, available on the Enclustra website [1].

Warning!

Please note that the warranty of an Enclustra module is voided if the FPGA fuses are blown. This operation is done at own risk, as it is irreversible. Enclustra cannot test the module in case of a warranty product return.

1.1.3 RoHS

The Mercury+ AA1 SoC module is designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2011/65/EC).

1.1.4 Disposal and WEEE

The Mercury+ AA1 SoC module must be properly disposed of at the end of its life.

The Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable for the Mercury+ AA1 SoC module.

1.1.5 Safety Recommendations and Warnings

Mercury+ modules are not designed to be "ready for operation" for the end-user. These can only be used in combination with suitable base boards. Proper configuration of the hardware before usage is required.

Ensure that the power supply is disconnected from the board before inserting or removing the Mercury+ AA1 SoC module, connecting interfaces, or connecting jumpers.

Touching the capacitors of the DC-DC converters can lead to voltage peaks and permanent damage; overvoltage on power or signal lines can also cause permanent damage to the module.

Warning!

It is possible to mount the Mercury+ AA1 SoC module the wrong way round on the base board - always check that the mounting holes on the base board are aligned with the mounting holes of the Mercury+ AA1 SoC module.

The base board and module may be damaged if the module is mounted the wrong way round and powered up.

1.1.6 Electrostatic Discharge

Electronic boards are sensitive to electrostatic discharge (ESD). Please ensure that the product is handled with care and only in an ESD-protected environment.

1.1.7 Electromagnetic Compatibility

The Mercury+ AA1 SoC module is a Class A product (as defined in IEC 61000-3-2 standard) and is not intended for use in domestic environments. The product may cause electromagnetic interference, for which appropriate measures must be taken.

1.2 Features

- Intel Arria 10 SOC 10AS027/10AS048
  - ARM dual-core Cortex A9
  - Intel Arria 10 20 nm FPGA fabric
- 286 user I/Os up to 1.8 V
  - 18 ARM peripheral I/Os (SPI, SDIO, I2C, UART)
  - 168 FPGA I/Os (single-ended or differential)
  - 44 FPGA I/Os (single-ended or differential) shared with USB 3.0
  - 56 MGT signals (clock and data)
- *Transceiver speedgrade 4 devices*: 12 MGTs @ 10.3125 Gbit/sec and 4 reference input clock differential pairs
- *Other devices*: 12 MGTs @ 12.5 Gbit/sec and 4 reference input clock differential pairs
- PCIe Gen3 ×8 (Intel PCIe hardened IP block)
- Up to 4 GB DDR4 SDRAM with ECC
- 64 MB quad SPI flash
- 16 GB eMMC flash
- Gigabit Ethernet
- Cypress EZ-USB FX3 USB 3.0 device controller
- USB 2.0 host/device
- UART, SPI, I2C, SDIO/MMC
- Real-time clock
- 5 to 15 V supply voltage

1.3 Deliverables

- Mercury+ AA1 SoC module
- Mercury+ AA1 SoC module documentation, available via download:
  - Mercury+ AA1 SoC Module User Manual (this document)
  - Mercury+ AA1 SoC Module Reference Design [2]
  - Mercury+ AA1 SoC Module IO Net Length Excel Sheet [3]
  - Mercury+ AA1 SoC Module FPGA Pinout Excel Sheet [4]

- Mercury+ AA1 SoC Module User Schematics (PDF) [5]
- Mercury+ AA1 SoC Module Known Issues and Changes [6]
- Mercury+ AA1 SoC Module Footprint (Altium, Eagle, Orcad and PADS) [7]
- Mercury+ AA1 SoC Module 3D Model (PDF) [8]
- Mercury+ AA1 SoC Module STEP 3D Model [9]
- Mercury Mars Module Pin Connection Guidelines [10]
- Mercury Master Pinout [11]
- Mercury Heatsink Application Note [17]
- Enclustra Build Environment [14] (Linux build environment; refer to Section 1.4.2 for details)
- Enclustra Build Environment How-To Guide [15]

1.4 Accessories

1.4.1 Reference Design

The Mercury+ AA1 SoC module reference design features an example configuration for the Arria 10 SoC device, together with an example top level HDL file for the user logic.

A number of software applications are available for the reference design, that show how to initialize the peripheral controllers and how to access the external devices. Pre-compiled binaries are included in the archive, so that the user can easily check that the hardware is functional.

The reference design can be downloaded from the Enclustra download page [2].

1.4.2 Enclustra Build Environment

The Enclustra Build Environment (EBE) [14] enables the user to quickly set up and run Linux on any Enclustra SoC module or system board. It allows the user to choose the desired target, and download all the required binaries, such as bitstream and preloader/bootloader. It downloads and compiles all required software, such as U-Boot, Linux, and BusyBox based root file system.

The Enclustra Build Environment features a graphical user interface (GUI) and a command line interface (CLI) that facilitates the automatic build flow.

The Enclustra Build Environment How-To Guide [15] describes in more detail how to use the EBE to customize the provided software for the user application. The document provides information on the configuration options for U-boot, Linux kernel and Buildroot, debugging possibilities for Linux applications, customization of device trees and integration of existing or new kernel drivers.

1.4.3 Enclustra Heat Sink

For Mercury modules an Enclustra heat sink is available for purchase along with the product. Please refer to section 2.11.6 for further information on the available cooling options.

1.4.4 Mercury+ PE1 Base Board

- 168-pin Hirose FX10 module connectors (PE1-200: 2 connectors; PE1-300/400: 3 connectors)
- System controller
- Power control
- System monitor (PE1-300/400)
- Current sense (PE1-300/400)
- Low-jitter clock generator (PE1-300/400)
- microSD card holder
- User EEPROM
- eMMC managed NAND flash (PE1-300/400)
- PCIe $\times 4$ interface

- USB 3.0 device connector
- USB 2.0 host connector (PE1-200: 1 connector; PE1-300/400: 4 connectors)
- Micro USB 2.0 device (UART, SPI, I2C, JTAG) connector
- 2 × RJ45 Gigabit Ethernet connectors
- mPCIe/mSATA card holder (USB only) (PE1-300/400)
- SIM card holder (optional, PE1-300/400 only)
- SMA clock and data in/out (optional, PE1-300/400 only)
- 1 × FMC LPC connector (PE1-200)
- 1 × FMC HPC connector (PE1-300)
- 2 × FMC LPC connector (PE1-400)
- 2 × 40-pin Anios pin header
- 3 × 12-pin IO headers
- 5 to 15 V DC supply voltage
- USB bus power (with restrictions)

Please note that the available features depend on the equipped Mercury module type and on the selected base board variant.

1.4.5 Mercury+ ST1 Base Board

- 168-pin Hirose FX10 module connectors (3 connectors)
- 2 × MIPI D-PHY connectors: CSI and CSI/DSI (requires FPGA support)
- Mini DisplayPort connector (requires FPGA support)
- HDMI connector (requires FPGA support)
- SFP+ connector
- Low-jitter clock generator
- USB 3.0 device connector
- USB 3.0 host connector
- FTDI USB 2.0 device controller with micro USB device connector (UART, SPI, I2C, JTAG)
- 2 × RJ45 Gigabit Ethernet connectors
- 1 × FMC HPC connector (note: not all pins are available)
- 2 × 40-pin Anios pin header
- 3 × 12-pin IO headers
- microSD card holder
- 5 to 15 V DC supply voltage
- Form factor: 100 × 120 mm

Please note that the available features depend on the equipped Mercury module type.

1.5 Intel Tool Support

The SoC devices equipped on the Mercury+ AA1 SoC module are supported by the Quartus Prime Standard Edition (or Quartus II Subscription Edition, for older software versions), for which a paid license is required. Please contact Intel for further information.

2 Module Description

2.1 Block Diagram

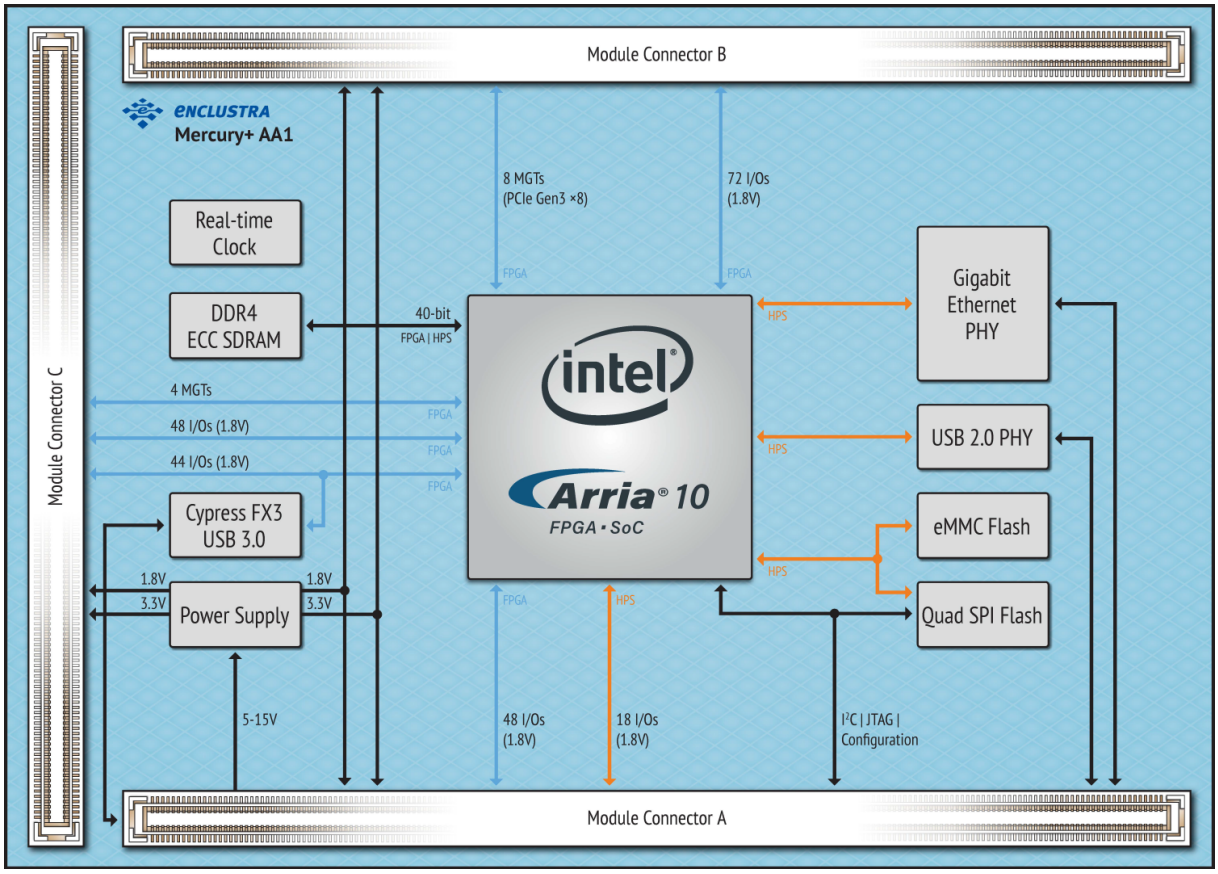

Figure 1: Hardware Block Diagram

The main component of the Mercury+ AA1 SoC module is the Intel Arria 10 SoC device. Most of its I/O pins are connected to the Mercury module connectors, making 230 regular user I/Os available to the user. Further, twelve multi-gigabit transceivers with support for PCIe Gen3 ×8 are available on the module connectors.

The SoC device can boot from the on-board QSPI flash, from the eMMC flash or from an external SD card. For development purposes, a JTAG interface is connected to Mercury module connector.

The memory subsystem is built from a 64 MB QSPI flash, 16 GB eMMC flash and 2 or 4 GB DDR4 SDRAM with ECC in the standard configuration.

Further, the module is equipped with a Gigabit Ethernet PHY and a USB 2.0 PHY, making it ideal for communication applications.

A Cypress FX3 USB 3.0 controller is fitted on the module to easily implement a communication link to a host PC.

A real-time clock is available on the module and is connected to the global I2C bus.

On-board clock generation is based on a 33.33 MHz crystal oscillator.

The module's internal supply voltages are generated from a single input supply of 5 - 15 V DC. Some of these voltages are available on the Mercury module connectors to supply circuits on the base board.

Four LEDs are connected to the SoC device's pins for status signaling.

2.2 Module Configuration and Product Codes

Table 1 describes the available standard module configurations. Custom configurations are available; please contact Enclustra for further information.

Product Code	SoC	DDR4 SDRAM	PCI Express	Temperature Range
ME-AA1-270-3E4-D11E	10AS027E4F29E3SG	2 GB	✓	0 to +85° C
ME-AA1-270-2I2-D11E	10AS027E2F29I2SG	2 GB	✓	-40 to +85° C
ME-AA1-480-1E2-D12E	10AS048E2F29E1HG	4 GB	✓	0 to +85° C
ME-AA1-480-2I3-D12E	10AS048E3F29I2SG	4 GB	✓	-40 to +85° C

Table 1: Standard Module Configurations

The product code indicates the module type and main features. Figure 2 describes the fields within the product code.

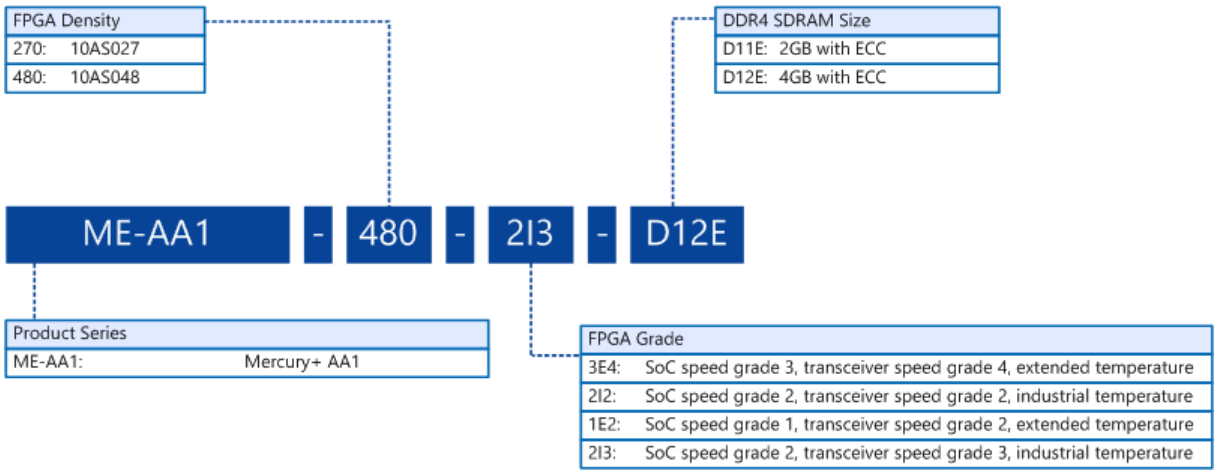

Figure 2: Product Code Fields

Please note that for the first revision modules or early access modules, the product code may not respect entirely this naming convention. Please contact Enclustra for details on this aspect.

2.3 Article Numbers and Article Codes

Every module is uniquely labeled, showing the article number and serial number. An example is presented in Figure 3.

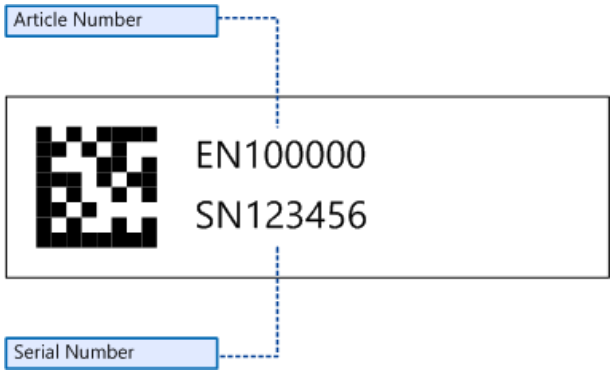

Figure 3: Module Label

The correspondence between article number and article code is shown in Table 2. The article code represents the product code, followed by the revision; the R suffix and number represent the revision number.

The revision changes and product known issues are described in the Mercury+ AA1 SoC Module Known Issues and Changes document [6].

Article Number	Article Code
EN101014	ME-AA1-480-2I-D11-R1
EN101875	ME-AA1-480-2I-D11-R1.2
EN101914	ME-AA1-270-3E4-D11E-R2
EN101915	ME-AA1-270-2I2-D11E-R2
EN101916	ME-AA1-480-1E2-D12E-R2
EN101917	ME-AA1-480-2I3-D12E-R2

Table 2: Article Numbers and Article Codes

2.4 Top and Bottom Views

2.4.1 Top View

Figure 4: Module Top View

2.4.2 Bottom View

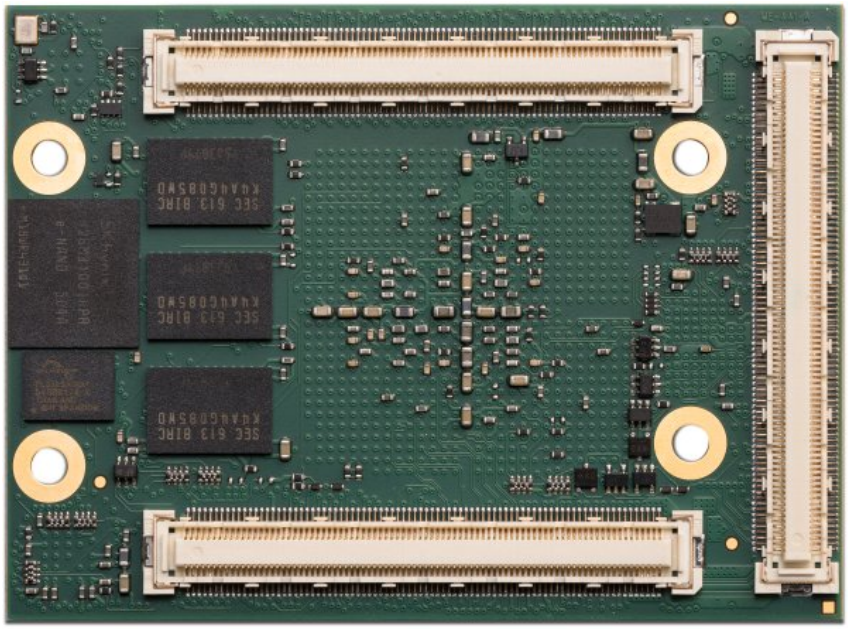

Figure 5: Module Bottom View

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.5 Top and Bottom Assembly Drawings

2.5.1 Top Assembly Drawing

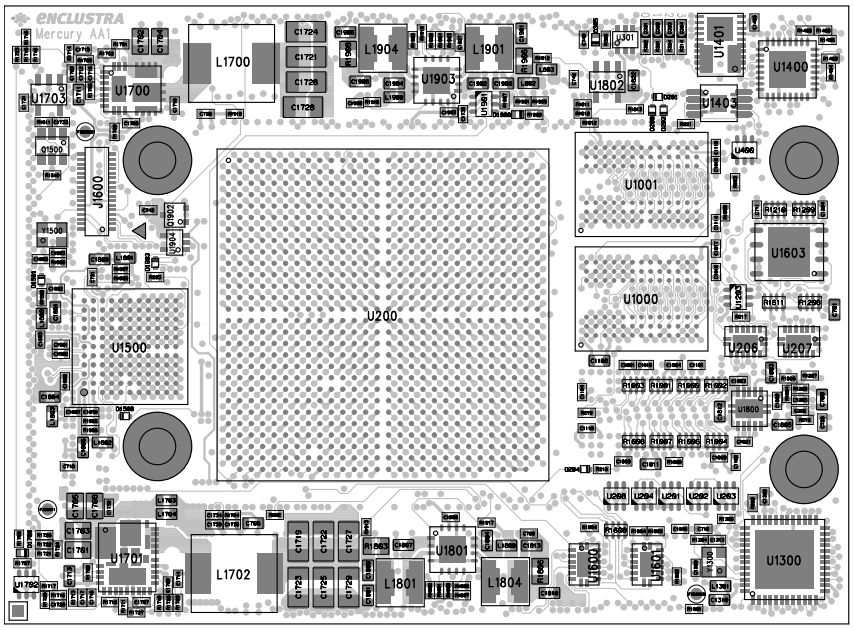

Figure 6: Module Top Assembly Drawing

2.5.2 Bottom Assembly Drawing

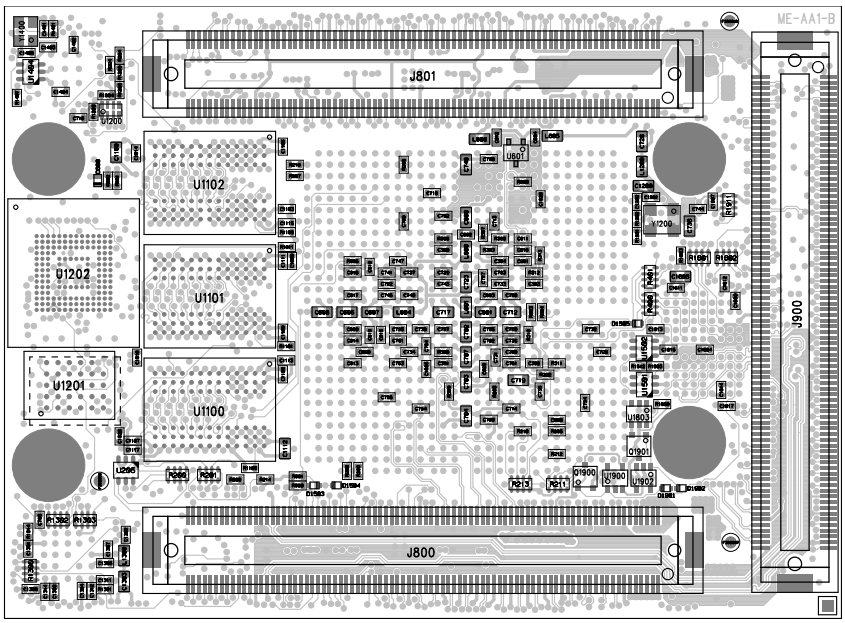

Figure 7: Module Bottom Assembly Drawing

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.6 Module Footprint

Figure 8 shows the dimensions of the module footprint on the base board.

Enclustra offers Mercury and Mercury+ modules of various geometries having widths of 56, 64, 65, 72 or 74 mm and having different topologies for the mounting holes. If different module types shall be fixed on the base board by screws, additional mounting holes may be required to accommodate different modules. The footprints of the module connectors for the base board design are available for different PCB design tools (Altium, PADS, Eagle, Orcad) [7] and include the required information on the module sizes and holes.

The maximum component height on the base board under the module is dependent on the connector type. Please refer to the Hirose FX10 series product website for detailed connector information [12].
The three connectors are called A (J800), B (J801) and C (J900).

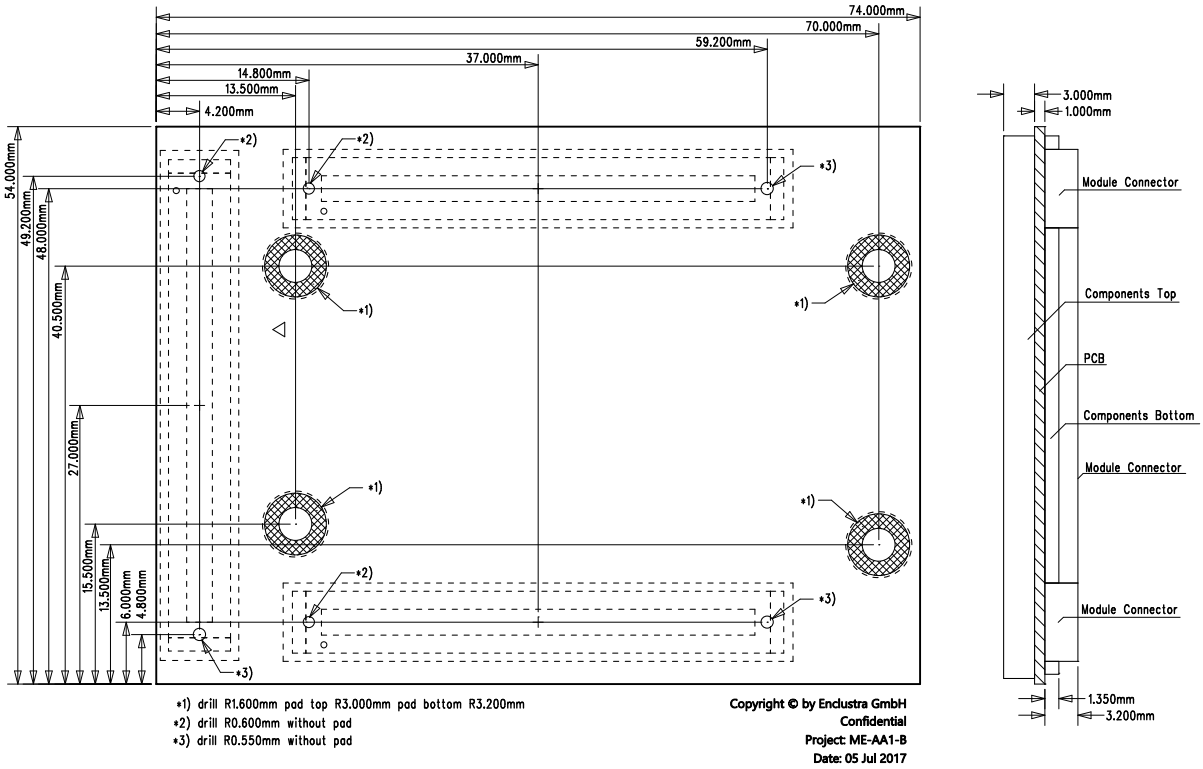

Figure 8: Module Footprint - Top View

Warning!

It is possible to mount the Mercury+ AA1 SoC module the wrong way round on the base board - always check that the mounting holes on the base board are aligned with the mounting holes of the Mercury+ AA1 SoC module.

2.7 Mechanical Data

Table 3 describes the mechanical characteristics of the Mercury+ AA1 SoC module. A 3D model (PDF) and a STEP 3D model are available [8], [9].

Symbol	Value
Size	74 × 54 mm
Component height top	3.0 mm
Component height bottom	1.35 mm
Weight	36 g

Table 3: Mechanical Data

2.8 Module Connector

Three Hirose FX10 168-pin 0.5 mm pitch headers with a total of 504 pins have to be integrated on the base board. Up to four M3 screws may be used to mechanically fasten the module to the base board. Do not use excessive force to tighten the screws, as this could damage the module.

The pinout of the module connector is found in the Mercury Master Pinout Excel Sheet [11]. The connector is available in different packaging options and different stacking heights. Some examples are presented in Table 4. Please refer to the connector datasheet for more information.

Reference	Type	Description
Mercury module connector	FX10A-168S-SV	Hirose FX10, 168-pin, 0.5 mm pitch
Base board connector	FX10A-168P-SV(71)	Hirose FX10, 168-pin, 0.5 mm pitch, 4 mm stacking height
Base board connector	FX10A-168P-SV1(71)	Hirose FX10, 168-pin, 0.5 mm pitch, 5 mm stacking height

Table 4: Module Connector Types

Figure 9 indicates the pin numbering for the Mercury module connectors from the top view of the base board. The connector pins are numbered as follows:

- Connector A: from J800-1 to J800-168
- Connector B: from J801-1 to J801-168
- Connector C: from J900-1 to J900-168

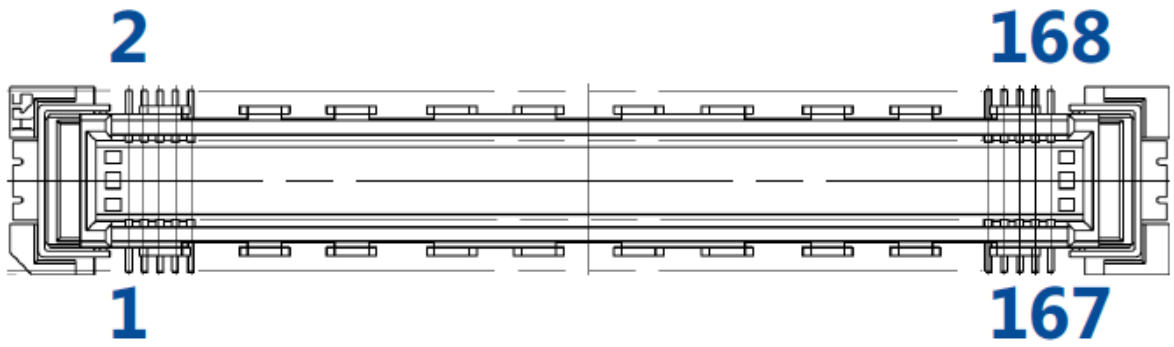

Figure 9: Pin Numbering for the Module Connector

Warning!

Do not use excessive force to latch a Mercury module into the Mercury connectors on the base board, as this could damage the module and the base board; always make sure that the module is correctly oriented before mounting it into the base board.

2.9 User I/O

2.9.1 Pinout

Information on the Mercury+ AA1 SoC module pinout can be found in the Enclustra Mercury Master Pinout [11], and in the additional document Enclustra Module Pin Connection Guidelines [10].

Warning!

Please note that the pin types on the schematics symbol of the module connector and in the Master Pinout document are for reference only. On the Mercury+ AA1 SoC module it may be possible that the connected pins do not have the targeted functions (such as primary clocks, differential pins, MGT signals, etc).

The naming convention for the user I/Os is:
IO_B<BANK>_L<PAIR><_FUNCTION>_<PACKAGE_PIN><_CONFIG_SPECIAL_FUNCTION>_<POLARITY>.

For example, IO_B3D_L13_CLK0_C7_P is located on pin C7 of I/O bank 3D, it is a clock capable pin and it has positive polarity, when used in a differential pair.

The naming convention for the user I/Os shared with the FX3 device is:
FX3_<FX3_FUNCTION>_B<BANK>_L<PAIR><_FUNCTION>_<PACKAGE_PIN>_<POLARITY>.

The clock capable pins are marked with "CLK" in the signal name. For details on their function and usage, please refer to the Intel documentation.

Table 5 includes information related to the total number of I/Os available in each I/O bank and possible limitations.

Signal Name	Signals	Pairs	Differential	Single-ended	I/O Bank
IO_B2A_<...>	48	24	In/Out	In/Out	2A
IO_B3A_<...>	48	24	In/Out	In/Out	3A
FX3_<...>	44	22	In/Out Shared with the FX3 pins	In/Out	3B
IO_B3C_<...>	48	24	In/Out	In/Out	3C
IO_B3D_<...>	24	12	In/Out	In/Out	3D
Total	**212**	**106**	-	-	-

Table 5: User I/Os

Warning!

When using the USB 3.0 on the Mercury+ AA1 SoC module, the FX3 signals must be left unconnected on the module connector C and VCC_IO_B3AB must be connected to the VCC_1V8 voltage.

Warning!

When using the signals on FPGA bank 3B as regular FPGA I/Os, the FX3 must be kept in reset by driving the FX3_RESET#_PL signal (pin V8) low.

2.9.2 I/O Pin Exceptions

The I/O pin exceptions are pins with special functions or restrictions (for example, when used in combination with certain Mercury boards they may have a specific role).

Table 6 lists the I/O pin exceptions on the Mercury+ AA1 SoC module.

I/O Name	Module Connector Pin	Description
IO_B2L_GP1IO18_MISO_J17	A-104	Connected via a 47 kΩ resistor to IO_B2A_L19_AB11_PERST#_P pin (A-34) for PCIe PERST# connection implementation
IO_B2L_GP1IO20_CLK_J18	A-98	Can optionally be connected via a 47 kΩ resistor to IO_B2A_L22_AB13_CVP_N pin (A-21) for Configuration via Protocol (CVP) implementation (CVP pin can be connected to PCIe WAKE# pin)
IO_B2A_L18_Y15_N	A-60	In order to use the MGT lines, a free running and stable clock must be supplied on CLKUSR pin (FPGA pin Y15, signal name IO_B2A_L18_Y15_N) at start of device configuration for transceiver calibration. The clock frequency of this input clock must be in the range from 100 MHz to 125 MHz. Please refer to Arria 10 Pin Connection Guidelines document [26] for details.

Table 6: I/O Pin Exceptions

When the Mercury+ AA1 SoC module is used in combination with a Mercury+ PE1 base board as a PCIe device, the PERST# signal coming from the PCIe edge connector on the module connector pin A-104 (IO_B2L_GP1IO18_MISO_J17) is driven further to IO_B2A_L19_AB11_PERST#_P.

Because the PCIe block inside the FPGA logic side requires this reset signal, the PERST# signal is connected to the FPGA pin IO_B2A_L19_AB11_PERST#_P via a 47 kΩ resistor. In situations in which a custom board is used or PCIe functionality is not required, this FPGA pin can be used in the same manner as a regular I/O pin.

The connection of the CVP pin to the PCIe WAKE# pin on the Mercury+ PE1 base board is made in a similar manner - note that the connection is not available in the standard configuration, as not all PCIe cards support the wake function. Details on the CVP implementation can be found in the Intel CVP documentation [25] and details on the WAKE# pin are available in the PCIe specification.

2.9.3 Differential I/Os

When using differential pairs, a differential impedance of 100 Ω must be matched on the base board, and the two nets of a differential pair must have the same length.

The information regarding the length of the signal lines from the SoC device to the module connector is available in Mercury+ AA1 SoC Module IO Net Length Excel Sheet [3]. This enables the user to match the total length of the differential pairs on the base board if required by the application.

Warning!

Please note that the trace length of various signals may change between revisions of the Mercury+ AA1 SoC module. Please use the information provided in the Mercury+ AA1 SoC Module IO Net Length Excel Sheet [3] to check which signals are affected. The differential signals will still be routed differentially in subsequent product revisions.

2.9.4 I/O Banks

Table 7 describes the main attributes of the FPGA and Hard Processing System (HPS) I/O banks, and indicates which peripherals are connected to each I/O bank. All I/O pins within a particular I/O bank must use the same I/O (VCC_IO) and reference (VREF) voltages.

Banks 2J and 2K are assigned to the SDRAM, with the pins mapped according to the restrictions for the usage of Intel EMIF IP solution in combination with HPS - please refer to the Intel External Memory Interface Handbook for details [23]. The remaining pins of the FPGA banks 2J and 2K are assigned to the power selection signals and peripheral interrupts; refer to Sections 2.19, 2.22, 4.2, and 2.11.1 for details.

Bank 2L has 48 pins shared between the FPGA logic side and HPS. The I/Os are split in 4 quadrants/groups; the pins belonging to the same quadrant must be all assigned either to the FPGA pins, or to the HPS pins.

Section 2.9.7 provides detailed information on the HPS/FPGA connections.

Bank	Connectivity	VCC_IO	VREF
MGT Bank 1C	Module connector	0.9/1.03 V[1]	-
MGT Bank 1D	Module connector	0.9/1.03 V[1]	-
Bank 2A	Module connector	User selectable VCC_IO_B2A	0.5 × VCC_IO_B2A
Bank 3A	Module connector	User selectable VCC_IO_B3AB	0.5 × VCC_IO_B3AB
Bank 3B	Module connector	User selectable VCC_IO_B3AB	0.5 × VCC_IO_B3AB
Bank 3C	Module connector	User selectable VCC_IO_B3CD	0.5 × VCC_IO_B3CD
Bank 3D	Module connector	User selectable	0.5 × VCC_IO_B3CD

Continued on next page...

Bank	Connectivity	VCC_IO	VREF
		VCC_IO_B3CD	
Bank 2J	DDR4 SDRAM, LEDs, power selection signals	1.2 V	0.6 V
Bank 2K	DDR4 SDRAM, power selection signals	1.2 V	0.6 V
Bank 2L	Module connector, USB PHY, Ethernet PHY, I2C, LEDs	1.8 V	0.9 V
HPS dedicated pins	Module connector, SD card/eMMC flash/QSPI flash	1.8 V	0.9 V

Table 7: I/O Banks

Warning!

The configuration for the DDR I/O banks (2J and 2K) and for the FPGA/HPS shared pins (bank 2L) is done by loading the FPGA bitstream. Without a valid bitstream, the DDR interface and other peripherals will not work properly. This also means that the HPS side cannot be used without a minimal FPGA configuration bitstream.

2.9.5 VCC_IO Usage

The VCC_IO voltages for the I/O banks located on the module connector are configurable by applying the required voltage to the VCC_IO_B[x] or VCC_CFG_[x] pins. All VCC_IO_B[x] or VCC_CFG_[x] pins of the same bank must be connected to the same voltage.

For compatibility with other Enclustra Mercury modules, it is recommended to use a single I/O voltage per module connector.

Signal Name	SoC Pins	Supported Voltages	Connector A Pins	Connector B Pins	Connector C Pins
VCC_IO_B2A	VCCIO2A	1.2 V - 1.8 V ±5%	38, 41	-	-
VCC_IO_B3AB	VCCIO3A-B	1.2 V - 1.8 V[2] ±5%	-	-	76, 116, 158
VCC_IO_B3CD	VCCIO3C-D	1.2 V - 1.8 V ±5%	-	64, 67, 88, 95, 140, 143	-

Table 8: VCC_IO Pins

[1]The voltage of the MGT transceivers can be set to 0.9 V or to 1.03 V. Refer to Section 2.11.1 for details.

If the Mercury+ AA1 SoC module is used in combination with a base board having only two module connectors, the VCC_IO_B3AB pin that powers I/O banks 3A and 3B is connected to the on-board generated 1.8 V supply voltage.

Warning!

Use only VCC_IO voltages compliant with the equipped SoC device; any other voltages may damage the equipped SoC device, as well as other devices on the Mercury+ AA1 SoC module.

Do not leave a VCC_IO pin floating, as this may damage the equipped SoC device, as well as other devices on the Mercury+ AA1 SoC module.

Warning!

Do not power the VCC_IO pins when PWR_GOOD and PWR_EN signals are not active. If the module is not powered, you need to make sure that the VCC_IO voltages are disabled (for example, by using a switch on the base board, which uses PWR_GOOD as enable signal). Figure 10 illustrates the VCC_IO power requirements.

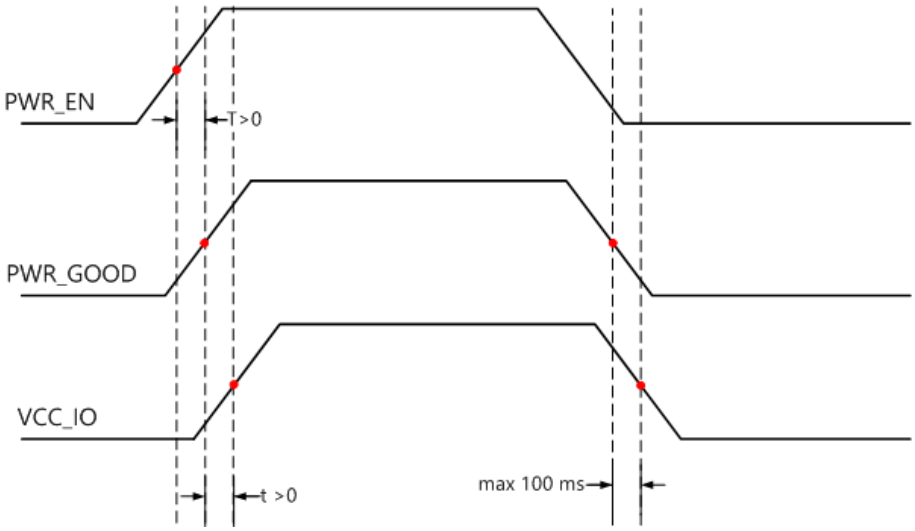

Figure 10: Power-Up Sequence - VCC_IO in Relation with PWR_GOOD and PWR_EN Signals

2.9.6 Signal Terminations

Differential Inputs

There are no external differential termination resistors on the Mercury+ AA1 SoC module for differential inputs. Differential input pairs on the module connector may be terminated either by external termination resistors on the base board (close to the module pins), or by the SoC device's internal termination resistors.

Single-Ended Outputs

There are no series termination resistors on the Mercury+ AA1 SoC module for single-ended outputs. If required, series termination resistors may be equipped on the base board (close to the module pins).

[2]VCC_IO_B3AB must be connected to the VCC_1V8 voltage when using USB 3.0 on the Mercury+ AA1 SoC module.

2.9.7 HPS dedicated and FPGA/HPS shared I/O Pins

There are 14 dedicated HPS pins available on the Mercury+ AA1 SoC module, used mainly for the boot process.

Bank 2L has 48 pins shared between the FPGA logic side and HPS; the I/Os are split in 4 quadrants/groups; the pins belonging to the same quadrant must be all assigned either to the FPGA pins, or to the HPS pins. Some of the I/Os on bank 2L are routed to the module connector and can be used as GPIOs; the suggested functions below are for reference only - always verify your pinout with the Intel device handbook.

Table 9 gives an overview over the HPS pin connections on the Mercury+ AA1 SoC module. Only the pins marked with "user functionality" are available on the module connector.

I/O Bank	Quadrant	GPIO	Function	Connection
HPS dedicated bank	- (GP2IO 0-13)	0-5	eMMC flash / QSPI flash / SD card shared pins	eMMC flash, QSPI flash, module connector
		8-11	eMMC flash data pins	eMMC flash
		6	HPS boot select 0/LED3#	Boot mode selection / On-board LED
		7	Flash selection signal	Boot mode selection
		12 13	UART TX[3]/user functionality [4] UART RX[3]/user functionality [4]	Module connector
Bank 2L	Q1 (GP0IO 0-11)	0-11	USB 2.0	USB PHY
	Q2 (GP0IO 12-23)	12-23	Gigabit Ethernet	Gigabit Ethernet PHY (RGMII)
	Q3 (GP1IO 0-11)	0-1	User functionality	Module connector
		2-3	LEDs[4]	On-board LEDs
		4	PWR_INT_VSEL	Core power selection
		5	QSPI flash output enable	Boot mode multiplexing logic
		6-7	I2C	On-board I2C bus and module connector
		8-9	User functionality	Module connector
		10-11	Ethernet MDIO interface	Gigabit Ethernet PHY
	Q4 (GP1IO 12-23)	12-17	SD card/user functionality	Module connector
		18-21	SPI/user functionality	Module connector
		22-23	User functionality	Module connector

Table 9: HPS and FPGA/HPS Shared Pins Connections

2.10 Multi-Gigabit Transceiver (MGT)

There are twelve Multi-Gigabit transceivers and four reference input clock differential pairs on the Mercury+ AA1 SoC module routed directly to the module connectors. The transceivers on the Mercury+ AA1 SoC module can reach a maximum data rate of 10.3125 Gbit/sec (for transceiver speedgrade 4 devices) and 12.5 Gbit/sec (for other devices), when the MGTs are used in high-speed mode. The high-speed mode is enabled by default starting with revision 2 modules[5]; refer to Section 2.11.1 for details on the voltage supplies.

The naming convention for the MGT I/Os is:
MGT_B<BANK>_<FUNCTION>_<PACKAGE_PIN>_<POLARITY>.

For example, MGT_B1D_TX0_R28_P is located on pin R28 of MGT I/O bank 1D, it is a transmit pin and it has positive polarity.

Warning!

In order to use the MGT lines, a free running and stable clock must be supplied on CLKUSR pin (FPGA pin Y15, signal name IO_B2A_L18_Y15_N) at start of device configuration for transceiver calibration. The clock frequency of this input clock must be in the range from 100 MHz to 125 MHz. Please refer to Arria 10 Pin Connection Guidelines document [26] for details.

The SoC devices equipped on the Mercury+ AA1 SoC module support one PCIe Gen3 hard IP block; this allows the user to have a ×8 block on the module.

Eight transceiver pairs are routed to module connector B; the order of the pins on the connector corresponds to the Intel specific PCIe pinout for ×1, ×2, ×4 and ×8 implementations. For details on the PCIe lane pinout on Intel Arria 10, please refer to the Arria 10 Avalon-MM Interface for PCIe Solutions document [22].

The other four transceivers of the Mercury+ AA1 SoC module are routed to the module connector C; these are not ordered according to the Intel PCIe pinout, therefore this step must be performed on the base board, if the MGT pairs are used for PCIe.

Warning!

The maximum data rate on the MGT lines on the Mercury+ AA1 SoC module depends on the routing path for these signals. Adequate signal integrity over the full signal path must be ensured when using MGTs at high performance rates.

Warning!

It is recommended to use redrivers on the base board for PCIe Gen3 or other high-speed interfaces implementations, and to perform channel simulation.

[3] UART RX is an SoC input; UART TX is an SoC output.

[4] On revision 1 modules, HPS dedicated pins GP2IO 12-13 are used for LED0# and LED1# signals, while FPGA/HPS shared pins GP1IO 2-3 are used for UART/GPIO signals. For details, please refer to the Mercury+ AA1 SoC Module Known Issues and Changes document [6].

[5] On revision 1 modules, the high-speed mode can be enabled by pulling PWR_MGT_VSEL low.

Warning!

No AC coupling capacitors are placed on the Mercury+ AA1 SoC module on the MGT lines - make sure capacitors are mounted, if required, on the base board (close to the module pins), to prevent MGT lines from being damaged.

2.11 Power

2.11.1 Power Generation Overview

The Mercury+ AA1 SoC module uses a 5 - 15 V DC power input for generating the on-board supply voltages (0.9/0.95 V, 0.9/1.03 V, 1.2 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V). Some of these voltages (1.8 V, 3.3 V) are accessible on the module connector.

Table 10 describes the power supplies generated on the module.

Voltage Supply Name	Voltage Value	Rated Current	Voltage Source	Shut down via PWR_EN	Influences PWR_GOOD
VCC_INT	0.9/0.95 V (Refer to Table 11)	20 A	VCC_MOD	Yes	Yes
VCC_MGT	0.9/1.03 V (Refer to Table 12)	2 A	VCC_3V3	Yes	Yes
VCC_1V2	1.2 V	2 A	VCC_3V3	Yes	Yes
VCC_1V8	1.8 V	2 A	VCC_3V3	Yes	Yes
VCC_1V8A	1.8 V	2 A	VCC_3V3	Yes	Yes
VCC_2V5	2.5 V	0.15 A	VCC_3V3	No	No
VCC_3V3	3.3 V	9 A	VCC_MOD	No	Yes
VCC_5V0	5.0 V	0.15 A	VCC_MOD	No	No

Table 10: Generated Power Supplies

Please refer to the Enclustra Module Pin Connection Guidelines for general rules on the power pins [10].

The default voltage of the ARM core is 0.9 V; if required by the application, the CPU can be switched to overdrive mode, by providing a higher voltage on the SoC device's VCC pins. In order to enable the overdrive mode (0.95 V), PWR_INT_VSEL (pin C23, HPS/FPGA shared pin GP1IO4) must be driven logic 0 - for details, refer to Table 11.

Note that the CPU overdrive mode is available only for SoC devices of speed grade -1 (in custom configurations of the Mercury+ AA1 SoC module).

PWR_INT_VSEL	VCC_INT
HiZ (default)	0.9 V (normal mode)
0	0.95 V (CPU overdrive)
1	illegal

Table 11: Power selection for the SoC core

The default voltage of the MGTs is 1.03 V corresponding to the high-speed mode; this voltage is the provided on the SoC device's VCC[R|T]_GXB pins. In order to enable/keep the high-speed mode, PWR_MGT_VSEL (pin E15) must be set as high-impedance in the FPGA - for details, refer to Table 12.

PWR_MGT_VSEL	VCC_MGT
HiZ (default)	1.03 V (high-speed mode)[6]
0	0.9 V (normal mode)[6]
1	illegal

Table 12: Power selection for the SoC transceivers

Detailed information on CPU and MGT performances are available in the Arria 10 Device Datasheet [18].

2.11.2 Power Enable/Power Good

The Mercury+ AA1 SoC module provides a power enable input on the module connector. This input may be used to shut down the DC/DC converters for 0.9/0.95 V, 0.9/1.03 V, 1.2 V, and 1.8 V. The 3.3 V supply is always active.

The PWR_EN input is pulled to VCC_3V3 on the Mercury+ AA1 SoC module with a 10 kΩ resistor. The PWR_GOOD signal is pulled to VCC_3V3 on the Mercury+ AA1 SoC module with a 10 kΩ resistor.

PWR_GOOD is an open collector signal and must not be used to drive a load directly. This signal is pulled to GND if the on-board regulators fail or if the module is disabled via PWR_EN. The list of regulators that influence the state of PWR_GOOD signal is provided in Section 2.11.1.

Pin Name	Module Connector Pin	Remarks
PWR_EN	A-10	Floating/3.3 V: Module power enabled Driven low: Module power disabled
PWR_GOOD	A-12	0 V: Module supply not ok 3.3 V: Module supply ok

Table 13: Module Power Status and Control Pins

[6] On revision 1 modules, the supply for the MGTs is by default 0.9 V, while the high-speed mode can be enabled by pulling PWR_MGT_VSEL low.

Warning!

Do not apply any other voltages to the PWR_EN pin than 3.3 V or GND, as this may damage the Mercury+ AA1 SoC module. PWR_EN pin can be left unconnected.

Do not power the VCC_IO pins (for example by connecting VCC_3V3 to VCC_IO directly) when PWR_EN is driven low to disable the module. In this case, VCC_IO needs to be switched off in the manner indicated in Figure 10.

2.11.3 Voltage Supply Inputs

Table 14 describes the power supply inputs on the Mercury+ AA1 SoC module. The VCC voltages used as supplies for the I/O banks are described in Section 2.9.5.

Pin Name	Module Connector Pins	Voltage	Description
VCC_MOD	A-1, 2, 3, 4, 5, 6, 7, 8, 9, 11	5 - 15 V ±5%	Supply for the 0.9/0.95 V and 3.3 V voltage regulators. All other supplies are generated from the 3.3 V supply. The input current is rated at 3 A (0.3 A per connector pin).
VCC_BAT	A-168	2.0 - 3.6 V	Battery for the RTC and SoC encryption key storage

Table 14: Voltage Supply Inputs

2.11.4 Voltage Supply Outputs

Table 15 presents the supply voltages generated on the Mercury+ AA1 SoC module, that are available on the module connector.

Pin Name	Module Connector Pins	Voltage	Maximum Current[7]	Comment
VCC_3V3	A-26, 29, 50, 86 B-55, 79, 115, 127, 152, 155 C-96, 103, 136, 143	3.3 V ±5%	4 A (and max 0.3 A per pin)	Always active
VCC_1V8	A-53, 62, 65, 89 B-52, 76, 108, 128 C-83, 123, 165	1.8 V ±5%	1 A (and max 0.3 A per pin)	Controlled by PWR_EN

Table 15: Voltage Supply Outputs

[7] The maximum available output current depends on your design. See sections 2.11.1 and 2.11.5 for details.

Warning!

Do not connect any power supply to the voltage supply outputs nor short circuit them to GND, as this may damage the Mercury+ AA1 SoC module.

2.11.5 Power Consumption

Please note that the power consumption of any SoC device strongly depends on the application (on the configured bitstream and I/O activity).

To estimate the power consumption of your design, please use the Intel PowerPlay Early Power Estimators (EPE) and Power Analyzer available on the Intel website.

2.11.6 Heat Dissipation

High performance devices like the Intel Arria 10 SoC need cooling in most applications; always make sure the SoC is adequately cooled.

For Mercury modules an Enclustra heat sink kit is available for purchase along with the product. It represents an optimal solution to cool the Mercury+ AA1 SoC module - the heat sink body is low profile and usually covers the whole module surface. The kit comes with a gap pad for the SoC device, a fan and required mounting material to attach the heat sink to the module PCB and baseboard PCB. With additional user configured gap pads, it is possible to cool other components on board as well.

Alternatively, if the Enclustra heat sink does not match the application requirements, a third-party heat sink body (ATS) and an additional gap pad (t-Global) may be used. Please note that the Enclustra heat sink kit already contains all necessary items for cooling the module (heat sink body, gap pad, fan, mounting material).

Table 16 lists the heat sink and thermal pad part numbers that are compatible with the Mercury+ AA1 SoC module. Details on the Mercury heatsink kit can be found in the Mercury Heatsink Application Note [17].

Product Name	Package Name	Enclustra Heat Sink	ATS Heat Sink	t-Global Thermal Pad
Mercury+ AA1	780-pin FBGA [27]	ACC-HS4-Set	ATS-52290G-C1-R0	TG-A6200-30-30-1

Table 16: Heat Sink Type

Please note that the adhesive heat sink part is recommended only for prototyping purposes. In cases where the module is used in environments subject to vibrations, additional mechanical fixation is recommended.

Warning!

Depending on the user application, the Mercury+ AA1 SoC module may consume more power than can be dissipated without additional cooling measures; always make sure the SoC is adequately cooled by installing a heat sink and/or providing air flow.

2.11.7 Voltage Monitoring

Several pins on the module connector on the Mercury+ AA1 SoC module are marked as VMON. These are voltage monitoring outputs that are used in the production test for measuring some of the on-board voltages.

It is not allowed to draw power from the voltage monitoring outputs.

Table 17 presents the VMON pins on the Mercury+ AA1 SoC module.

Pin Name	Module Connector Pin	Connection	Description
VMON_INT	A-102	VCC_INT	FPGA and HPS core voltages
VMON_1V2	B-8	VCC_1V2	1.2 V on-board voltage (default)/SoC battery voltage (assembly option)
VMON_1V8A	B-168	VCC_1V8A	1.8 V on-board voltage
VMON_MGT	B-167	VCC_MGT	MGT supply voltage

Table 17: Voltage Monitoring Outputs

Warning!

The voltage monitoring outputs are for Enclustra-use only. Pinout changes may be applied between revisions.

2.12 Clock Generation

A 33.33 MHz oscillator is used for the Mercury+ AA1 SoC module clock generation. The 33.33 MHz clock is fed to the HPS and the FPGA logic.

Signal Name	Frequency	Destination	FPGA Pin	Remark
HPS1_CLK	33.33 MHz	HPS_CLK1	G14	HPS clock 1
CLK_PLL	33.33 MHz	IO2K_L12P_CLK1	D15	PLL reference clock for the DDR4 controller

Table 18: Module Clock Resources

2.13 Reset

The cold reset signal (POR) and the HPS warm reset signal (RST) of the SoC device are available on the module connector.

Pulling HPS_POR# low resets the SoC device, the Ethernet and USB 2.0 PHYs, and the QSPI and eMMC flash devices. Further, the CONFIG# pin is pulled low to re-trigger the FPGA configuration. Please refer to the Enclustra Module Pin Connection Guidelines [10] for general rules regarding the connection of reset pins.

Pulling HPS_RST# low resets the SoC device. For details on the functions of the HPS_NPOR and HPS_NRST signals refer to the Intel documentation.

Table 19 presents the available reset signals. Both signals, HPS_POR# and HPS_RST#, have on-board 4.7 kΩ pull-up resistors to VCC_1V8.

Signal Name	Connector Pin	FPGA Pin Type	Description
HPS_POR#	A-132	HPS_NPOR	Cold reset
HPS_RST#	A-124	HPS_NRST	Warm reset

Table 19: Reset Resources

Please note that HPS_POR# is automatically asserted if PWR_GOOD is low.

2.14 LEDs

The Mercury+ AA1 SoC module is equipped with four LEDs: one of them is connected to an HPS dedicated pin, two of them are connected to FPGA/HPS shared pins, while the other one is connected to FPGA bank 3B.

Signal Name	HPS GPIO	FPGA Pin	Remarks
LED0#	GP1IO2[8]	F21	User function/active-low
LED1#	GP1IO3[8]	G21	User function/active-low
LED2#	-	T8	User function/active-low
LED3#_BS0	GP2IO13	J15	User function/active-low (used as boot selection signal in configuration mode)

Table 20: LEDs

2.15 DDR4 SDRAM

The DDR4 SDRAM on the Mercury+ AA1 SoC module is connected to FPGA I/O banks 2J and 2K. The pinout has been chosen in such manner that the DDR can be used with Intel Arria 10 EMIF IP core - both regular EMIF and EMIF for HPS (the EMIF for HPS is more restrictive on the DDR pinout).

The Intel documentation specifies that the user can choose for DDR4 the Hard Controller and Hard PHY variant or the PHY only variant (the FPGA fabric controller can be attached to the EMIF). Please refer to the Intel External Memory Interface Handbook for details [23].

The memory configuration on the Mercury+ AA1 SoC module supports ECC error detection and correction; the correction code type used is single bit error correction and double bit error detection (SEC-DED).

Five 8-bit memory chips are used to build a 40-bit wide memory: 32 bits for data and 8 bits for ECC.

The maximum memory bandwidth on the Mercury+ AA1 SoC module is:

[8] On revision 1 modules, LED0# and LED1# are mapped to HPS dedicated pins GP2IO 12-13. Starting with revision 2, these signals are mapped to FPGA/HPS shared pins GP1IO 2-3. For details, please refer to the Mercury+ AA1 SoC Module Known Issues and Changes document [6].

- *Speedgrade 1 devices*: 2400 Mbit/sec × 32 bit = 9600 MB/sec
- *Speedgrade 2 devices*: 2133 Mbit/sec × 32 bit = 8528 MB/sec
- *Speedgrade 3 devices*: 1866 Mbit/sec × 32 bit = 7464 MB/sec

2.15.1 DDR4 SDRAM Type

Table 21 describes the memory availability and configuration on the Mercury+ AA1 SoC module.

Module	SDRAM Type	Density	Configuration	Manufacturer
ME-AA1-D11E	K4A4G085WD-BIRC	4 Gbit	512 M × 8 bit	Samsung
ME-AA1-D12E	K4A8G085WB-BIRC	8 Gbit	1 G × 8 bit	Samsung

Table 21: DDR4 SDRAM Types

Warning!

Other DDR4 memory devices may be equipped in future revisions of the Mercury+ AA1 SoC module. Please check the user manual regularly for updates. Any parts with different speed bins or temperature ranges that fulfill the requirements for the module variant may be used.

Please note that on the bigger module variants (with 4 GB of DDR memory), only up to 4032 MB of memory are addressable directly from the HPS (4 GB without the peripheral region). The addressable space can decrease if FPGA slaves are used in the system. The entire 4 GB address space can be accessed through the FPGA2SDRAM interface. Please refer to the Arria 10 Hard Processor System Technical Reference Manual document [20] for details on the SDRAM address space.

2.15.2 Signal Description

Please refer to the Mercury+ AA1 SoC Module FPGA Pinout Excel Sheet [4] for detailed information on the DDR4 SDRAM connections.

2.15.3 Termination

Warning!

No external termination is implemented for the data signals on the Mercury+ AA1 SoC module. Therefore, it is strongly recommended to enable the on-die termination (ODT) feature of the DDR3 SDRAM device.

2.15.4 Parameters

Please refer to the Mercury+ AA1 SoC module reference design [2] for DDR4 settings guidelines.

The DDR4 SDRAM parameters to be set in the Quartus project are presented in Table 22.

The values given in Table 22 are for reference only. Depending on the equipped memory device on the Mercury+ AA1 SoC module and on the DDR4 SDRAM frequency, the configuration may be different to the one in the reference design. Please refer to the memory device datasheet and to the DDR controller datasheet for details.

Parameter	Value
SDRAM protocol	DDR4
PHY settings - supply voltage	1.2 V
DQ width	40 bit (ECC enabled)
Number of clocks	1
Number of chip selects	1
Row address width	15 (for 4 Gbit memory chips) or 16 (for 8 Gbit memory chips)
Column address width	10
Bank address width	2
Bank group width	2
Read DBI	Enabled only for 2400 Mbps operation

Table 22: DDR4 SDRAM Parameters

Parameter	Value			Unit
	FPGA Speedgrade 3	FPGA Speedgrade 2	FPGA Speedgrade 1	
Memory clock frequency	933.333	1066.666	1200	MHz
Memory CAS latency setting	13	15	20	
Memory write CAS latency setting	10	11	16	
Speed bin	-1866	-2133	-2400	
tIS (base)	100	80	62	ps
tIH (base)	125	105	87	ps
TdiVW	0.2	0.2	0.2	UI
VdiVW	136	136	130	mV
tDQSQ	0.16	0.16	0.16	UI
tQH	0.76	0.76	0.74	UI
tDVWP	0.66	0.69	0.72	UI
tDQSCK	195	180	175	ps
tDQSS	0.27	0.27	0.27	cycles
tQSH	0.4	0.4	0.4	cycles

Continued on next page...

Parameter	Value			Unit
	FPGA Speedgrade 3	FPGA Speedgrade 2	FPGA Speedgrade 1	
tDSH	0.18	0.18	0.18	cycles
tDSS	0.18	0.18	0.18	cycles
tWLS	140	125	110	ps
tWLH	140	125	110	ps
tMRD	8	8	8	cycles
tRAS	34	33	32	ns
tRCD	13.92	14.06	14.16	ns
tRP	13.92	14.06	14.16	ns
tWR	15	15	15	ns
tRRD_S	4	4	4	cycles
tRRD_L	5	6	6	cycles
tFAW	23	21	21	ns
tCCD_S	4	4	4	cycles
tCCD_L	5	6	6	cycles
tWTR_S	3	3	3	cycles
tWTR_L	7	8	9	cycles
tRFC	260 (4Gbit) 350 (8 Gbit)	260 (4Gbit) 350 (8 Gbit)	260 (4Gbit) 350 (8 Gbit)	ns
tREFI	7.8	7.8	7.8	us

Table 23: DDR4 SDRAM Timing Parameters

2.16 QSPI Flash

The QSPI flash can be used to boot the HPS, and to store the FPGA bitstream, ARM application code and other user data.

2.16.1 QSPI Flash Type

Table 24 describes the memory availability and configuration on the Mercury+ AA1 SoC module.

Flash Type	Size	Manufacturer
S25FL512S	512 Mbit	Cypress (Spansion)

Table 24: QSPI Flash Type

Warning!

Other flash memory devices may be equipped in future revisions of the Mercury+ AA1 SoC module. Please check the user manual regularly for updates. Any parts with different speeds and temperature ranges that fulfill the requirements for the module variant may be used.

Note that the active serial configuration of the FPGA is not permitted with the Cypress (Spansion) QSPI flash. If this configuration is required, an Intel EPCQL flash must be mounted instead of the Cypress (Spansion) part and powered with 1.8 V instead of 3.3 V. The pinout of the Cypress (Spansion) flash is compatible with the Intel EPCQL series.

2.16.2 Signal Description

The QSPI flash is connected to the FPGA SPI configuration port and to the HPS dedicated pins 0-5 via some boot selection multiplexers. Some of the signals are available on the module connector, allowing the user to program the QSPI flash from an external master.

Please refer to Section 3 for details on programming the flash memory.

Warning!

Special care must be taken when connecting the QSPI flash signals on the base board. Long traces or high capacitance may disturb the data communication between the SoC and the flash devices.

2.16.3 QSPI Flash Corruption Risk

There have been cases in which it was observed that the content of the flash device got corrupted. According to Cypress, this issue is caused by power loss during the Write Register (WRR) command. The most common reason to use the WRR command is to turn the QUAD bit ON or OFF - this operation takes place usually at the beginning of the boot process. If required, the bootloader code can be adjusted to set the QUAD bit to a fixed value, without invoking this command during boot.

For additional information on this issue, please refer to the Cypress documentation and forum discussions [28], [29].

2.17 eMMC Flash

The eMMC flash can be used to boot the HPS, and to store the FPGA bitstream, ARM application code and other user data.

2.17.1 eMMC Flash Type

Table 25 describes the memory availability and configuration on the Mercury+ AA1 SoC module.

Flash Type	Size	Manufacturer
H26M52208FPRI	16 GB	SK Hynix
EMMC16G-W525-X01U	16 GB	Kingston
EMMC16G-IB29-PZ90	16 GB	Kingston

Table 25: eMMC Flash Type

Warning!

Other flash memory devices may be equipped in future revisions of the Mercury+ AA1 SoC module. Please check the user manual regularly for updates. Any parts with different speeds and temperature ranges that fulfill the requirements for the module variant may be used.

2.17.2 Signal Description

The eMMC flash signals are connected to the HPS dedicated pins 0-5 via some boot selection multiplexers, and to HPS pins 8-11. The command signal has a 4.7 kΩ pull-up resistor to 1.8 V and the data lines have 47 kΩ pull-up resistors to 1.8 V.

The clock to the eMMC flash chip is interrupted when the flash output enable signal, FLASH_OE#, is active (for example, when booting from SD card or from QSPI flash).

2.18 SD Card

An SD card can be connected to the HPS dedicated pins (GP2IO) 0-5 via some boot selection multiplexers. This allows the Mercury+ AA1 SoC module to boot from the SD card, as well as data access after booting. The pins in bank 2L must be configured as "None" in the Intel tools, when the HPS dedicated SDIO pins are used for booting from the SD card.

The SDIO interface may also be configured to the HPS/FPGA shared pins in bank 2L, but this configuration does not allow the user to boot from the SD card. Refer to Section 3.4 for details on the available boot modes and corresponding connections.

Please note that external pull-ups and a level shifter to 3.3 V are needed for SD card operation (some level shifters also have built-in pull-ups).

2.18.1 Signal Description

HPS Dedicated Boot Pin (SD Card Boot)	HPS/FPGA Pin in Bank 2L (SD Card Access, No Boot)	SD Card Signal	Connector Pin
GP2IO0	GP1IO12	D0	A-95
GP2IO1	GP1IO13	CMD	A-93
GP2IO2	GP1IO14	CLK	A-91
GP2IO3	GP1IO15	D1	A-97
GP2IO4	GP1IO16	D2	A-101
GP2IO5	GP1IO17	D3	A-103

Table 26: SD Card Signals

2.19 Gigabit Ethernet

A 10/100/1000 Mbit Ethernet PHY is available on the Mercury+ AA1 SoC module, connected to the FPGA bank 2L via RGMII interface.

2.19.1 Ethernet PHY Type

Table 27 describes the equipped Ethernet PHY device type on the Mercury+ AA1 SoC module.

PHY Type	Manufacturer	Type
KSZ9031RNX	Microchip (Micrel)	10/100/1000 Mbit

Table 27: Gigabit Ethernet PHY Type

2.19.2 Signal Description

The RGMII interface is connected to FPGA bank 2L pins for use with the hard or soft macro MAC, depending on the pin mapping for the I/O quadrant. The reset pin is connected to the HPS power-on reset pin.

The interrupt output of the Ethernet PHY is connected to the ETH_INT# signal (FPGA pin AG19).

2.19.3 External Connectivity

The Ethernet signal lines can be connected directly to the magnetics. Please refer to the Enclustra Module Pin Connection Guidelines [10] for details regarding the connection of Ethernet signals.

2.19.4 MDIO Address

The MDIO address assigned to the Gigabit Ethernet PHY is 3. The MDIO interface is connected to the FPGA bank 2L pins.

2.19.5 PHY Configuration

The configuration of the Ethernet PHY is bootstrapped when the PHY is released from reset. Make sure all I/Os on the RGMII interface are initialized and all pull-up or pull-down resistors are disabled at that moment.

The bootstrap options of the Ethernet PHY are set as indicated in Table 28.

Please note that the RGMII delays in the Ethernet PHY need to be configured before the Ethernet interface can be used. This is done in the patch for the Preloader (SPL) provided in the Mercury+ AA1 SoC module reference design [2].

Pin	Signal Value	Description
MODE[3-0]	1110	RGMII mode: advertise all capabilities (10/100/1000, half/full duplex) except 1000Base-T half duplex.
PHYAD[2-0]	011	MDIO address 3
Clk125_EN	0	125 MHz clock output disabled
LED_MODE	1	Single LED mode
LED1/LED2	1	Active-low LEDs

Table 28: Gigabit Ethernet PHY Configuration

For the Ethernet PHY configuration via the MDIO interface, the MDC clock frequency must not exceed 2 MHz.

2.20 Cypress FX3 USB 3.0 Controller

The Mercury+ AA1 SoC module features a USB 3.0 controller from Cypress, which allows data transfers to a host computer using speeds of over 300 MB/s.

The USB controller is connected to the FPGA module using a slave FIFO interface that can be configured for 16-bit or 32-bit mode using an interface clock of 100 MHz. The USB 3.0 controller includes a 32-bit ARM926 core operating at 200 MHz using a 19.2 MHz crystal oscillator. It can access the I2C bus and the QSPI flash.

The Cypress FX3 JTAG interface is routed to the debug connector J1600. Please refer to the Mercury+ AA1 SoC Module User Schematics [5] for details.

2.20.1 Cypress FX3 Type

Table 29 describes the equipped Cypress FX3 controller type on the Mercury+ AA1 SoC module.

Type	Manufacturer	Description
CYUSB3014	Cypress	USB 3.0 device controller (Cypress FX3) including USB 3.0 and USB 2.0 PHYs

Table 29: USB 3.0 Controller Type

2.20.2 Cypress FX3 Pinout

For details on FX3 interface pinout, please refer to the Mercury+ AA1 SoC Module FPGA Pinout Excel Sheet [4] and Mercury+ AA1 SoC Module User Schematics [5].

2.20.3 Functional Description

The FX3 controller is configured to boot from the FX3 SPI flash boot by default. The flash is factory programmed with a booloader that sets up all configuration pins of the FPGA correctly - if the FX3 bootloader is deleted or overwritten, the FPGA may not work correctly anymore.

Please make sure all configuration pins are properly setup if you load a custom FX3 firmware - in case a wrong firmware has been programmed to the FX3 SPI flash, the SPI flash boot can be prevented by shorting R1501 (see Figure 11).

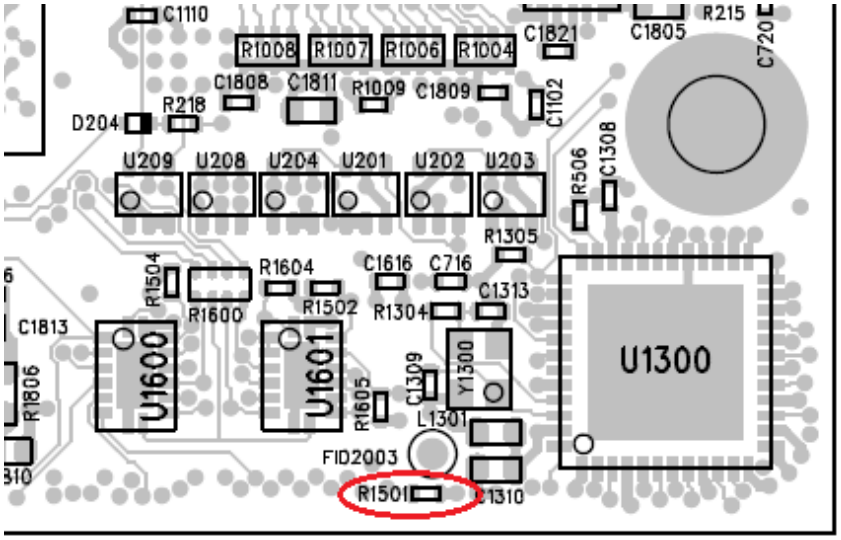

Figure 11: FX3 SPI Flash Boot Bypass (lower right corner)

For more information on the FPGA configuration pins, refer to Section 3.

2.21 USB 2.0

The Mercury+ AA1 SoC module has an on-board USB 2.0 PHY connected to the SoC device. The USB interface can be configured for USB host or for USB device.

Please note that simultaneous usage of the USB 3.0 device interface (FX3) and USB 2.0 in device mode is not USB compliant; the Mercury pinout does not support voltage detection for each USB interface.

2.21.1 USB PHY Type

Table 30 describes the equipped USB PHY device type on the Mercury+ AA1 SoC module.

PHY Type	Manufacturer	Type
USB3320C	Microchip	USB 2.0 PHY

Table 30: USB 2.0 PHY Type

2.21.2 Signal Description

The ULPI interface is connected to FPGA/HPS shared pins for use with the integrated USB controller. The USB PHY reset pin is connected to the HPS power-on reset pin.

2.22 Real-Time Clock (RTC)

A real-time clock is connected to the I2C bus. The RTC features a battery-buffered 128 bytes user SRAM and a temperature sensor. See Section 4 for details on the I2C bus on the Mercury+ AA1 SoC module.

VBAT pin of the RTC is connected to VCC_BAT on the module connector, and can be connected directly to a 3 V battery. Please refer to the Enclustra Module Pin Connection Guidelines [10] for details.

The interrupt output of the RTC is connected to the RTC_INT# signal (FPGA pin AH13).

2.22.1 RTC Type

Table 31 describes the equipped RTC device type on the Mercury+ AA1 SoC module.

Type	Manufacturer
ISL12020MIRZ	Intersil

Table 31: RTC Type

An example demonstrating how to use the RTC is included in the Mercury+ AA1 SoC module reference design [2].

2.23 Secure EEPROM

The secure EEPROM is used to store the module type and serial number, as well as the Ethernet MAC address and other information. It is connected to the I2C bus.

The secure EEPROM must not be used to store user data.

Please refer to Section 4.4 for details on the content of the EEPROM.

2.23.1 EEPROM Type

Table 32 describes the equipped EEPROM device type on the Mercury+ AA1 SoC module.

Type	Manufacturer
ATSHA204A-MAHDA-T (default)	Atmel
DS28CN01 (assembly option)	Maxim

Table 32: EEPROM Type

An example demonstrating how to read data from the EEPROM is included in the Mercury+ AA1 SoC module reference design [2].

3 Device Configuration

3.1 Configuration Signals

Tables 33, 34 and 35 describe the most important configuration pins. Detailed information on the boot options on the Mercury+ AA1 SoC module is available in Section 3.4.

Signal Name	Module Connector Pin	Comments
BOOT_MODE0	A-126	4.7 kΩ pull-up to VCC_1V8
BOOT_MODE1	A-112	4.7 kΩ pull-up to VCC_1V8

Table 33: Boot Configuration Pins

Signal Name	FPGA Pin	QSPI Flash Pin	Mod. Conn. Pin	Comments
FLASH_CLK	DCLK	SCK	A-118	4.7 kΩ pull-up to VCC_1V8
FLASH_CS#	CSO#	CS#	A-116	Depending on the boot mode
FLASH_DI	ASDATA0_ASDO	SI/IO0	A-114	4.7 kΩ pull-up to VCC_1V8
FLASH_DO	ASDATA1	SO/IO1	A-122	4.7 kΩ pull-up to VCC_1V8
FLASH_D2	ASDATA2	WP#/IO2	-	4.7 kΩ pull-up to VCC_1V8
FLASH_D3	ASDATA3	HOLD#/IO3	-	4.7 kΩ pull-up to VCC_1V8
FPGA_IOPULLUP#	IO_PULLUP#	-	-	Connected to GND
FPGA_CONFIG	CONFIG#	-	-	4.7 kΩ pull-up to VCC_1V8
FPGA_CONFDONE	CONF_DONE	-	A-130	1 kΩ pull-up to VCC_1V8

Table 34: FPGA Configuration Pins

Signal Name	HPS Pin	QSPI Flash Pin	eMMC Flash Pin	SD Card Pin	Comments
HPS_RST#	HPS_NRST	-	-	-	4.7 kΩ pull-up to VCC_1V8
HPS_POR#	HPS_NPOR	RESET#	RST#	-	4.7 kΩ pull-up to VCC_1V8

Continued on next page...

Signal Name	HPS Pin	QSPI Flash Pin	eMMC Flash Pin	SD Card Pin	Comments
EMMC_DATA0_QSPI_CLK	GP2IO0	SCK	DAT0	DAT0	47 kΩ pull-up to VCC_1V8
EMMC_CCLK_QSPI_SS0#_BS2	GP2IO2	CS#	CLK	CLK	Depending on the boot mode
EMMC_CMD_QSPI_IO0	GP2IO1	SI/IO0	CMD	CMD	4.7 kΩ pull-up to VCC_1V8
EMMC_DATA1_QSPI_IO1	GP2IO3	SO/IO1	DAT1	DAT1	47 kΩ pull-up to VCC_1V8
EMMC_DATA2_QSPI_IO2	GP2IO4	WP#/IO2	DAT2	DAT2	47 kΩ pull-up to VCC_1V8
EMMC_DATA3_QSPI_IO3	GP2IO5	HOLD#/IO3	DAT3	DAT3	47 kΩ pull-up to VCC_1V8
EMMC_DATA4	GP2IO8	-	DAT4	-	47 kΩ pull-up to VCC_1V8
EMMC_DATA5	GP2IO9	-	DAT5	-	47 kΩ pull-up to VCC_1V8
EMMC_DATA6	GP2IO10	-	DAT6	-	47 kΩ pull-up to VCC_1V8
EMMC_DATA7	GP2IO11	-	DAT7	-	47 kΩ pull-up to VCC_1V8

Table 35: HPS Configuration Pins

Warning!

All configuration signals except for BOOT_MODE must be high impedance as soon as the device is released from reset. Violating this rule may damage the equipped SoC device, as well as other devices on the Mercury+ AA1 SoC module.

HPS and FPGA Configuration Pins

The BSEL pins determine in which memory interface is the boot loader stored; details on BSEL pins when using the HPS boot are available in the Arria 10 Hard Processor System Technical Reference Manual document [20], Booting and Configuration section. The MSEL pins, which are used to select an FPGA configuration scheme, are described in the Arria 10 Core Fabric and General Purpose I/Os Handbook [19].

3.2 Module Connector C Detection

Signal C_PRSNT# (pin C-167) must be connected to GND on the base board if the designed base board has three connectors. Depending on the value of this pin, the FPGA banks routed to module connector C are supplied with the voltages provided by the user (when C_PRSNT# is low) or with a default voltage of 1.8 V (when C_PRSNT# is unconnected).

C_PRSNT# is equipped with a 4.7 kΩ pull-up resistor on the module.

3.3 Pull-Up Before and During Configuration

The I/O pull-up configuration signal (IO_PULLUP#) is connected to GND via a 1 kΩ series resistor. As this pin is an active-low signal, all FPGA I/Os will have the internal pull-up resistors enabled before and during device configuration.

3.4 Boot Mode

The BOOT_MODE signals determine whether the SoC device boots from the QSPI flash, from the eMMC flash or from an SD card connected to the SD pins on the HPS dedicated boot pins bank. Several multiplexers are used to switch between all these modes.

The clock to the eMMC flash chip is interrupted when the flash output enable signal, FLASH_OE#, is active (for example, when booting from SD card or from QSPI flash), in order to avoid contention on the clock and data signals. Figure 12 shows the boot modes available on the Mercury+ AA1 SoC module - SD card boot mode is default.

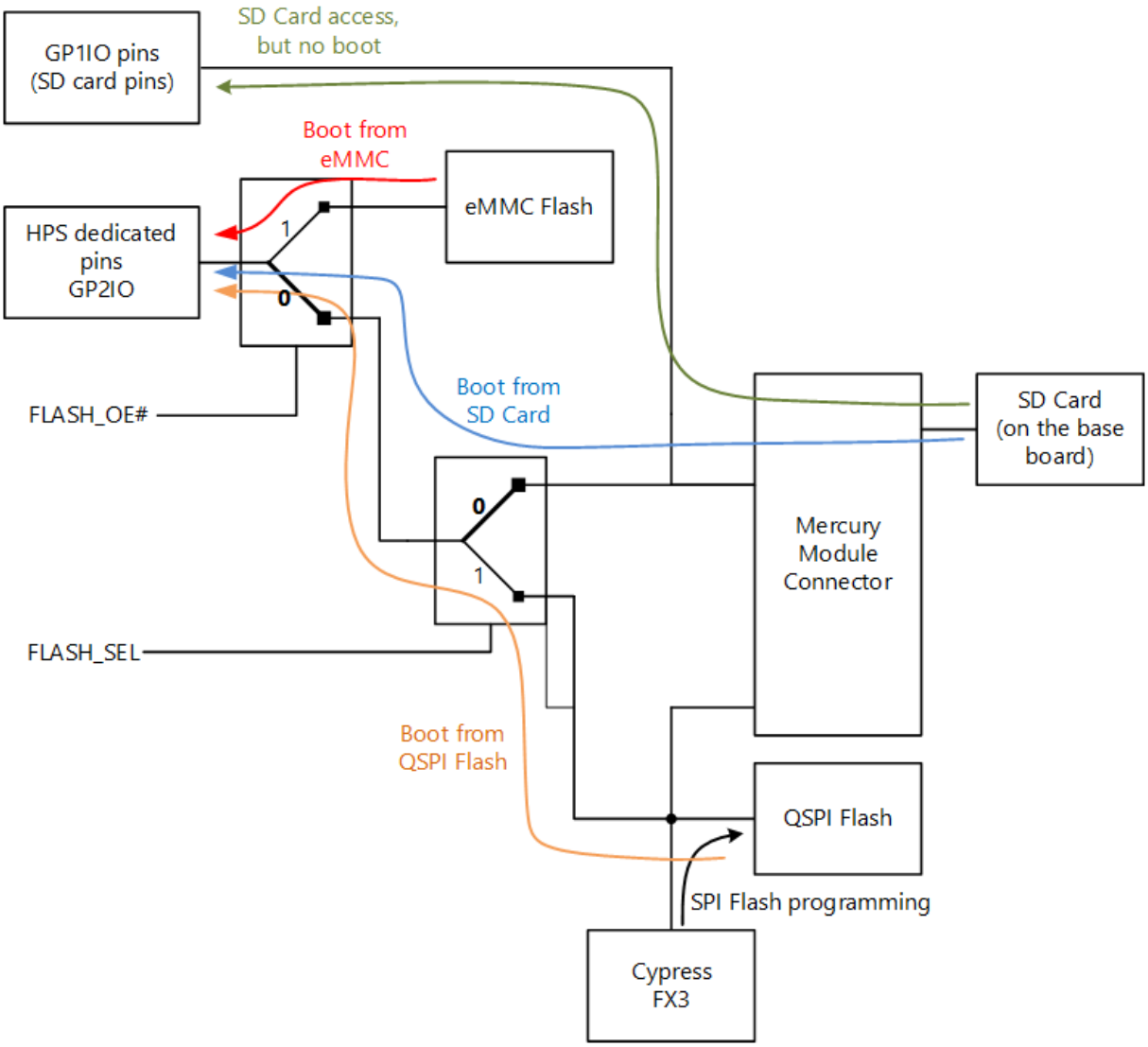

Figure 12: Boot Modes

Table 36 describes the available boot modes and the corresponding boot mode signals. FLASH_OE# and FLASH_SEL signals are generated from the boot mode signals available on the module connector; they select which of the memory devices is used for boot.

BOOT_ MODE1	BOOT_ MODE0	HPS Boot	FPGA Boot	FLASH_ OE#	FLASH_ SEL	MSEL[2:0]	BSEL[2:0]
0	0	eMMC	from HPS (or passive serial[9])	1	0	000	100
0	1	FPGA	QSPI (active serial) not supported	1	0	010	001
1	0	QSPI	from HPS	0	1	000	110
1	1	SDIO	from HPS (or passive serial[9])	0	0	000	100

Table 36: Boot Modes

The active serial mode is not supported in the standard configuration, due to the QSPI flash type; refer to Section 2.16 for details. The chip select signal for the QSPI flash is routed either to the FPGA configuration pins, or to the HPS configuration pins, depending on the boot mode signals.

The passive serial mode is available for eMMC and SD boot modes; the flash signals are available on the module connector, allowing the user to use the passive serial configuration scheme. The passive serial mode has not been tested on Enclustra side.

3.5 JTAG

The FPGA and the HPS JTAG interfaces are connected into one single chain available on the module connector. The SoC device and the QSPI flash can be configured via JTAG using Intel tools.
The Mercury+ AA1 SoC module is compatible with Intel FPGA download cable (Blaster) I and II. Terasic USB Blaster is not compatible with the module, as it does not support the required voltage of 1.8 V for the JTAG interface.

3.5.1 JTAG on Module Connector

Signal Name	Module Connector Pin	Resistor
JTAG_TCK	A-123	4.7 kΩ pull-down
JTAG_TMS	A-119	4.7 kΩ pull-up to VCC_1V8
JTAG_TDI	A-117	4.7 kΩ pull-up to VCC_1V8
JTAG_TDO	A-121	-

Table 37: JTAG Interface

3.5.2 External Connectivity

JTAG signals can be connected directly on the base board to a JTAG connector. No pull-up/pull-down resistors are necessary. The VCC pin of the programmer must be connected to VCC_1V8.

It is recommended to add 22 Ω series termination resistors between the module and the JTAG header, close to the source. Please refer to the Enclustra Module Pin Connection Guidelines for details on JTAG interface.

[9] DATA0 for passive serial configuration is mapped to IO_B2A_L1_AE10_N. Refer to Section 3.6.

3.6 Passive Serial Configuration

In the passive serial configuration mode, the FPGA bitstream is programmed from an external source into the SPI port of the FPGA. The HPS boots independently, either from the eMMC flash, or from the SD card present on the base board. The boot options on the Mercury+ AA1 SoC module are described in Section 3.4.

Please note that DATA0 dual-purpose configuration data input pin is mapped to FPGA pin AE10 (signal IO_B2A_L1_AE10_N), therefore this pin must be used in the passive serial configuration scheme to program the FPGA.

For more information on the FPGA configuration and HPS booting process, please refer to the Arria 10 Handbook [19] and to the Arria 10 Hard Processor System Technical Reference Manual document [20], Booting and Configuration section.

3.7 eMMC Boot Mode

In the eMMC boot mode, the HPS boots from the eMMC flash and configures the FPGA logic from the HPS. The FPGA can also be configured independently by using passive serial mode. The HPS configuration and the FPGA bitstream need to be stored in a boot image.

For more information, please refer to the Arria 10 Hard Processor System Technical Reference Manual document [20], Booting and Configuration section.

3.8 QSPI Boot Mode

In the QSPI boot mode, the HPS boots from the QSPI flash and configures the FPGA logic from the HPS. The HPS configuration and the FPGA bitstream need to be stored in a boot image. For more information, please refer to the Arria 10 Hard Processor System Technical Reference Manual document [20], Booting and Configuration section.

3.9 SD Card Boot Mode

In the SD card boot mode, the HPS boots from the SD card located on the base board and configures the FPGA logic from the HPS. The FPGA can also be configured independently by using passive serial mode. The HPS configuration and the FPGA bitstream need to be stored in a boot image.

For more information, please refer to the Arria 10 Hard Processor System Technical Reference Manual document [20], Booting and Configuration section.

3.10 Active Serial Configuration

In the active serial configuration mode, the FPGA reads the bitstream from the QSPI Flash in single (1x) or quad mode (4x). The HPS is configured afterwards via HPS2FPGA bridge. For more information on the FPGA configuration and HPS booting process, please refer to the Arria 10 Handbook [19] and to the Arria 10 Hard Processor System Technical Reference Manual document [20], Booting and Configuration section.

Note that in the standard configuration, the active serial mode is not supported on the Mercury+ AA1 SoC module, as Intel devices require an EPCQL series flash for this mode. Section 2.16 presents details on the QSPI flash.

3.11 eMMC Flash Programming

The eMMC flash can be formatted and/or programmed in u-boot or Linux, like a regular SD card. The boot image or independent partition files can be transmitted via Ethernet or copied from another storage device.

3.12 QSPI Flash Programming via JTAG

The Intel Quartus software offers QSPI flash programming support via JTAG. For more information, please refer to the Quartus user manual [24].

The process of programming the QSPI flash via JTAG using "quartus_hps" tool can take up to 30 minutes.

3.13 QSPI Flash Programming from an External SPI Master

The signals of the QSPI flash are directly connected to the module connector for flash access. As the flash signals are connected to the SoC device as well, the SoC device pins must be tri-stated while accessing the QSPI flash directly from an external device.

This is ensured by pulling the HPS_RST# signal to GND followed by a pulse on HPS_POR#, which puts the SoC device into reset state and tri-states all I/O pins. HPS_RST# must be low when HPS_POR# is released and kept low until the flash programming has finished. Afterwards, all SPI lines and HPS_RST# must be tri-stated and another reset impulse must be applied to HPS_POR#.

Figure 13 shows the signal diagrams corresponding to flash programming from an external master.

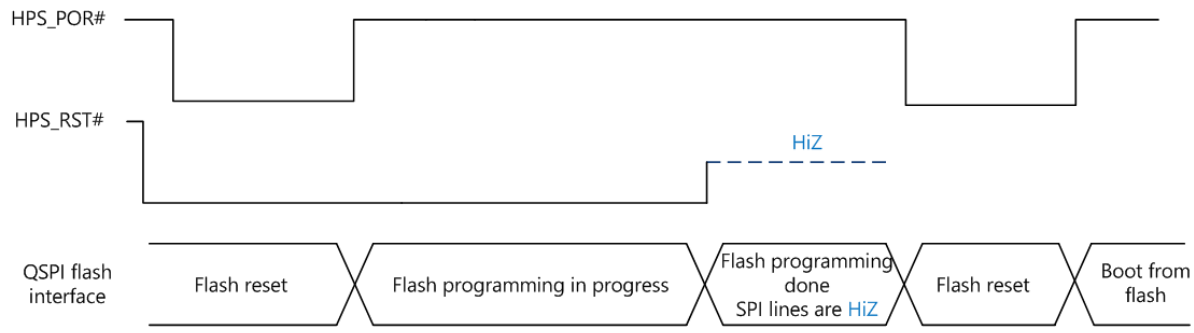

Figure 13: QSPI Flash Programming from an External SPI Master - Signal Diagrams

Warning!

Accessing the QSPI flash directly without putting the SoC device into reset may damage the equipped SoC device, as well as other devices on the Mercury+ AA1 SoC module.

3.14 Enclustra Module Configuration Tool

The QSPI flash on the Mercury+ AA1 SoC module can be programmed via Cypress FX3 using the Enclustra Module Configuration Tool (MCT) [16].

4 I2C Communication

4.1 Overview

The I2C bus on the Mercury+ AA1 SoC module is connected to the SoC device, EEPROM, RTC, FX3 USB 3.0 controller and debug connector, and is available on the module connector. This allows external devices to read the module type and to connect more devices to the I2C bus.

The I2C clock frequency should not exceed 400 kHz.

Warning!

Maximum I2C speed may be limited by the routing path and additional loads on the base board.

Warning!

If the I2C traces on the base board are very long, 100 Ω series resistors should be added between module and I2C device on the base board.

4.2 Signal Description

Table 38 describes the signals of the I2C interface. All signals have on-board pull-up resistors to VCC_3V3.

All signals must be connected to open collector outputs and must not be driven high from any source. I2C_INT# is an input to the SoC and must not be driven from the SoC device.

Level shifters are used between the I2C bus and the HPS pins, to allow I/O voltages lower than 3.3 V.

Signal Name	FPGA Pin	Connector Pin	Resistor
I2C_SDA	Bank 2L, Quadrant 3, GP1IO6 (E22)	A-113	2.2 kΩ pull-up
I2C_SCL	Bank 2L, Quadrant 3, GP1IO7 (F22)	A-111	2.2 kΩ pull-up
I2C_INT#	Bank 2J, pin AA18	A-115	4.7 kΩ pull-up

Table 38: I2C Signal Description

4.3 I2C Address Map

Table 39 describes the addresses for several devices connected on I2C bus.

Address (7-bit)	Description
0x64	Secure EEPROM
0x5C	Secure EEPROM (assembly option, refer to Section 2.23)
0x57	RTC user SRAM
0x6F	RTC registers

Table 39: I2C Addresses

4.4 Secure EEPROM

The secure EEPROM is used to store the module serial number and configuration. In the future, the EEPROM will be used for copy protection and licensing features. Please contact us for further information.

An example demonstrating how to read the module information from the EEPROM memory is included in the Mercury+ AA1 SoC module reference design.

Warning!

The secure EEPROM is for Enclustra use only. Any attempt to write data to the secure EEPROM causes the warranty to be rendered void.

4.4.1 Memory Map

Address	Length (bits)	Description
0x00	32	Module serial number
0x04	32	Module product information
0x08	40	Module configuration
0x0D	24	Reserved
0x10	48	Ethernet MAC address
0x16	48	Reserved
0x1C	32	Checksum (only for DS28CN01 EEPROM type)

Table 40: EEPROM Sector 0 Memory Map

Module Serial Number

The module serial number is a unique 32-bit number that identifies the module. It is stored using big-endian byte order (MSB on the lowest address).

Module Product Information

This field indicates the type of module and hardware revision.

Module	Product Family	Reserved	Revision	Product Information
Mercury+ AA1 SoC module	0x032D	0x[XX]	0x[YY]	0x032D [XX][YY]

Table 41: Product Information

Module Configuration

Addr.	Bits	Comment	Min. Value	Max. Value	Comment
0x08	7-4	SoC Type	0	1	See SoC type table (Table 43)
	3-2	SoC device speed grade	1	3	
	1-0	SoC transceiver speed grade	0	3	See transceiver speed grade table (Table 44)
0x09	7-6	Temperature range	0	2	See temperature range table (Table 45)
	5	Power grade	0 (Normal)	1 (Low Power)	
	4-3	Gigabit Ethernet port count	0	1	
	2	RTC equipped	0	1	
	1-0	Reserved	-	-	
0x0A	7-2	Reserved	-	-	
	1	USB 2.0 port count	0	1	
	0	USB 3.0 device port count	0	1	
0x0B	7-4	DDR4 ECC RAM size (GB)	0 (0 GB)	3 (4 GB)	Resolution = 1 GB
	3-0	QSPI flash memory size (MB)	0 (0 MB)	7 (64 MB)	Resolution = 1 MB
0x0C	7-4	eMMC flash size (GB)	0 (0 GB)	5 (16 GB)	Resolution = 1 GB
	3-0	Reserved	-	-	

Table 42: Module Configuration

The memory sizes are defined as Resolution$\times 2^{(Value-1)}$ (e.g. DRAM=0: not equipped, DRAM=1: 1 GB, DRAM=2: 2 GB, DRAM=3: 4 GB, etc).

Table 43 shows the available SoC types.

Value	SoC Device Type
0	10AS027
1	10AS048

Table 43: SoC Device Types

Table 44 shows the available transceiver speed grades.

Value	SoC Transceiver Speed Grade
0	1
1	2
2	3
3	4

Table 44: SoC Transceiver Speed Grades

Table 45 shows the available temperature ranges.

Value	Module Temperature Range
0	Commercial
1	Extended
2	Industrial

Table 45: Module Temperature Range

Ethernet MAC Address

The Ethernet MAC address is stored using big-endian byte order (MSB on the lowest address). Each module is assigned two sequential MAC addresses; only the lower one is stored in the EEPROM.

5 Operating Conditions

5.1 Absolute Maximum Ratings

Table 46 indicates the absolute maximum ratings for Mercury+ AA1 SoC module. The values given are for reference only; for details please refer to the Arria 10 Device Datasheet [18].

Symbol	Description	Rating	Unit
VCC_MOD	Supply voltage relative to GND	-0.5 to 16	V
VCC_BAT	Supply voltage for the RTC and encryption key storage	-0.3 to 3.6	V
VCC_IO_[x] VCC_CFG_[x]	Output drivers supply voltage relative to GND	-0.5 to 3.6	V
V_IO	I/O input voltage relative to GND	-0.5 to V_{CCIO}+0.5	V
Temperature	Temperature range for extended modules (C)* Temperature range for industrial modules (I)*	0 to +85 -40 to +85	°C °C

Table 46: Absolute Maximum Ratings

5.2 Recommended Operating Conditions

Table 47 indicates the recommended operating conditions for Mercury+ AA1 SoC module. The values given are for reference only; for details please refer to the Arria 10 Device Datasheet [18].

Symbol	Description	Rating	Unit
VCC_MOD	Supply voltage relative to GND	4.75 to 15.75	V
VCC_BAT	Supply voltage for the RTC and encryption key storage	2.0 to 3.45	V
VCC_IO_[x] VCC_CFG_[x]	Output drivers supply voltage relative to GND	Refer to Section 2.9.5	V
V_IO	I/O input voltage relative to GND	-0.2 to V_{CCIO}+0.2	V
Temperature	Temperature range for extended modules (C)* Temperature range for industrial modules (I)*	0 to +85 -40 to +85	°C °C

Table 47: Recommended Operating Conditions

Warning!

** The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.*

6 Ordering and Support

6.1 Ordering

Please use the Enclustra online request/order form for ordering or requesting information:
`http://www.enclustra.com/en/order/`

6.2 Support

Please follow the instructions on the Enclustra online support site:
`http://www.enclustra.com/en/support/`

List of Figures

List of Tables

References

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