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NTE74C90 & NTE74C93
Integrated Circuit
TTL– CMOS Counters
14–Lead DIP

Description:

The NTE74C90 decade counter and the NTE74C93 binary counter are complementary MOS (CMOS) integrated circuits in a 14–Lead DIP type package constructed with N– and P–channel enhancement mode transistors. The 4–bit decade counter can reset ot zero or preset to nine by applying appropriate logic level on the R_{01}, R_{02}, R_{91} and R_{92} inputs. Also, a separate flip–flop on the A–bit enables the user to operate it as a divide by 2, 5 o 10 frequency counter.

The 4–bit binary counter can be reset o zero by applying high logic level on inputs R_{01} and R_{02}, and a separate flip–flop on the A–bit enables the user to operate it as a divide–by–2, –8, or –16 divider. Counting occurs on the negative going edge of the input pulse.

All inputs are protected against static discharge damage.

Features:

- Wide Supply Range: 3V to 15V
- Guaranteed Noise Margin: 1V
- High Noise Immunity: 0.45 V_{CC} (typ)
- Low Power Compatibility:
  Fan Out of 2 TTL Driving 74L

Function:

- NTE74C90 – 4–Bit Decade Counter
- NTE74C93 – 4–Bit Binary Counter

Absolute Maximum Ratings: (Note 1)

Voltage at Any Pin (Note 1) . . . . . –0.3V to V_{CC} +0.3V
Power Dissipation, P_D 700mW
Operating V_{CC} Range . . . . . 3V to 15V
Absolute Maximum V_{CC} 18V
Operating Temperature Range, T_A . . . . . –55° to +125°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 10sec), T_L . . . . . +260°C

Note 1. “Absolute Maximum Ratings” are those values beyond which th safety of the device cannot be guaranteed. Except for “Operating Temperature Range”, they are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” provides conditions for actual device operation.

DC Electrical Characteristics: (T_A = −55° to +125°C unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
CMOS to CMOS							
Logical “1” Input Voltage	$V_{IN(1)}$	V_{CC} = 5V		3.5	–	–	V
		V_{CC} = 10V		8.0	–	–	V
Logical “0” Input Voltage	$V_{IN(0)}$	V_{CC} = 5V		–	–	1.5	V
		V_{CC} = 10V		–	–	2.0	V
Logical “1” Output Voltage	$V_{OUT(1)}$	V_{CC} = 5V	I_O = −10μA	4.5	–	–	V
		V_{CC} = 10V		9.0	–	–	V
Logical “0” Output Voltage	$V_{OUT(0)}$	V_{CC} = 5V	I_O = +10μA	–	–	0.5	V
		V_{CC} = 10V		–	–	1.0	V
Logical “1” Input Current	$I_{IN(1)}$	V_{CC} = 15V, V_{IN} = 15V		–	0.005	1.0	μA
Logical “0” Input Current	$I_{IN(0)}$	V_{CC} = 15V, V_{IN} = 0V		–1.0	–0.005	–	μA
Supply Current	I_{CC}	V_{CC} = 15V		–	0.05	300	μA
CMOS/LPTTL Interface							
Logical “1” Input Voltage	$V_{IN(1)}$	V_{CC} = 4.75V		V_{CC}–1.5	–	–	V
Logical “0” Input Voltage	$V_{IN(0)}$	V_{CC} = 4.75V		–	–	0.8	V
Logical “1” Output Voltage	$V_{OUT(1)}$	V_{CC} = 4.75V, I_O = −360μA		2.4	–	–	V
Logical “0” Output Voltage	$V_{OUT(0)}$	V_{CC} = 4.75V, I_O = −360μA		–	–	0.4	V
Output Drive (Short Circuit Current)							
Output Source Current (P−Channel)	I_{SOURCE}	V_{CC} = 5V	V_{OUT} = 0V, T_A = +25°C	–1.75	–3.3	–	mA
		V_{CC} = 10V		–8.0	–15	–	mA
Output Sink Current (N−Channel)	I_{SINK}	V_{CC} = 5V	V_{OUT} = V_{CC}, T_A = +25°C	1.75	3.3	–	mA
		V_{CC} = 10V		8.0	15	–	mA

AC Electrical Characteristics: (T_A = +25°, C_L = 50pF, Note 2 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time from A_{IN} to Q_A	t_{pd0}, t_{pd1}	V_{CC} = 5V	–	200	400	ns
		V_{CC} = 10V	–	80	150	ns
Propagation Delay Time from A_{IN} to Q_B **(NTE74C93)**	t_{pd0}, t_{pd1}	V_{CC} = 5V	–	450	850	ns
		V_{CC} = 10V	–	160	300	ns
Propagation Delay Time from A_{IN} to Q_B **(NTE74C90)**	t_{pd0}, t_{pd1}	V_{CC} = 5V	–	450	800	ns
		V_{CC} = 10V	–	160	300	ns
Propagation Delay Time from A_{IN} to Q_C **(NTE74C93)**	t_{pd0}, t_{pd1}	V_{CC} = 5V	–	500	1050	ns
		V_{CC} = 10V	–	200	400	ns
Propagation Delay Time from A_{IN} to Q_C **(NTE74C90)**	t_{pd0}, t_{pd1}	V_{CC} = 5V	–	500	1000	ns
		V_{CC} = 10V	–	200	400	ns
Propagation Delay Time from A_{IN} to Q_D **(NTE74C93)**	t_{pd0}, t_{pd1}	V_{CC} = 5V	–	600	1200	ns
		V_{CC} = 10V	–	250	500	ns
Propagation Delay Time from A_{IN} to Q_D **(NTE74C90)**	t_{pd0}, t_{pd1}	V_{CC} = 5V	–	450	800	ns
		V_{CC} = 10V	–	160	300	ns

Note 2. AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics (Cont'd): (T_A = +25°, C_L = 50pF, Note 2 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time from R_{01} or R_{02} to Q_A, Q_B, Q_C or Q_D **(NTE74C93)**	t_{pd0}, t_{pd1}	V_{CC} = 5V	–	150	300	ns
		V_{CC} = 10V	–	75	150	ns
Propagation Delay Time from R_{01} or R_{02} to Q_A, Q_B, Q_C or Q_D **(NTE74C90)**	t_{pd0}, t_{pd1}	V_{CC} = 5V	–	200	400	ns
		V_{CC} = 10V	–	75	150	ns
Propagation Delay Time from R_{91} or R_{92} to Q_A or Q_D **(NTE74C90)**	t_{pd0}, t_{pd1}	V_{CC} = 5V	–	250	500	ns
		V_{CC} = 10V	–	100	200	ns
Min. R_{01} or R_{02} Pulse Width **(NTE74C93)**	t_{PW}	V_{CC} = 5V	600	250	–	ns
		V_{CC} = 10V	30	125	–	ns
Min. R_{01} or R_{02} Pulse Width **(NTE74C90)**	t_{PW}	V_{CC} = 5V	600	250	–	ns
		V_{CC} = 10V	300	125	–	ns
Min. R_{91} or R_{92} Pulse Width **(NTE74C90)**	t_{PW}	V_{CC} = 5V	500	200	–	ns
		V_{CC} = 10V	250	100	–	ns
Maximum Clock Rise and Fall Time	t_r	V_{CC} = 10V	–	–	15	µs
	t_f		–	–	5	µs
Minimum Clock Pulse Width	t_W	V_{CC} = 5V	250	100	–	ns
		V_{CC} = 10V	100	50	–	ns
Maximum Clock Pulse Frequency	f_{MAX}	V_{CC} = 5V	2	–	–	MHz
		V_{CC} = 10V	5	–	–	MHz
Input Capacitance	C_{IN}	Any Input (Note 3)	–	5	–	pF
Power Dissipation Capacitance	C_{PD}	Per Package (Note 4)	–	45	–	pF

Note 2. AC Parameters are guaranteed by DC correlated testing.
Note 3. Capacitance is guaranteed by periodic testing.
Note 4. C_{PD} determines the no load AC power consumption of any CMOS device.

Truth Tables:

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Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Output Q_A is connected to Input B for BDC count.
H = HIGH Level
L = LOW Level
X = Irrelevant

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Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Output Q_A is connected to Input B for binary count sequence.
H = HIGH Level
L = LOW Level
X = Irrelevant

Function Tables:

Reset/Count Function Table

Reset Inputs				Output			
R_{01}	R_{02}	R_{91}	R_{92}	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	Count			
L	X	L	X	Count			
L	X	X	L	Count			
X	L	L	X	Count			

Reset/Count Function Table

Reset Inputs		Output			
R_{01}	R_{02}	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	Count			
X	L	Count			

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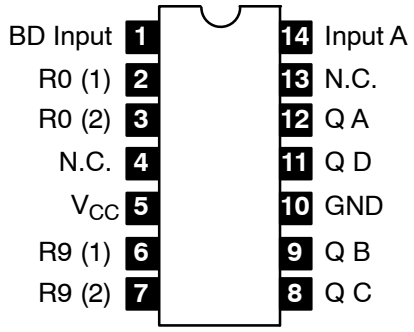

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