20 GHz to 44 GHz, GaAs, pHEMT, MMIC, Low Noise Amplifier

Data Sheet **HMC1040CHIPS**

FEATURES

- Low noise figure: 2 dB typical
- High gain: 25.0 dB typical
- P1dB output power: 13.5 dBm, 24 GHz to 40 GHz
- High output IP3: 25.5 dBm typical
- Die size: 1.309 mm × 1.48 × 0.102 mm

APPLICATIONS

- Software defined radios
- Electronic warfare
- Radar applications
- Satellite communication
- Electronic warfare
- Instrumentation
- Telecommunications

FUNCTIONAL BLOCK DIAGRAM

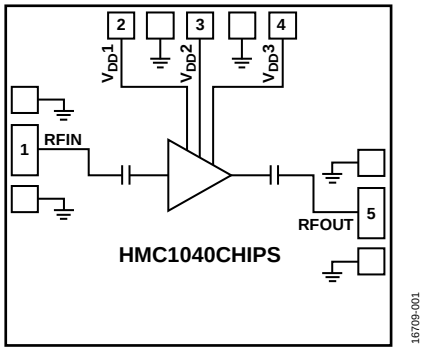

Figure 1.

GENERAL DESCRIPTION

The HMC1040CHIPS is a gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC), low noise wideband amplifier that operates from 20 GHz to 44 GHz. The HMC1040CHIPS is self biased and provides a typical gain of 25.0 dB, a 2 dB typical noise figure, and a typical output third-order intercept (IP3) of 25.5 dBm typical, requiring only 65 mA from a 2.5 V supply voltage. The typical saturated output power (P_{SAT}) of 15.5 dBm enables the low noise amplifier (LNA) to function as a local oscillator (LO) driver for many of Analog Devices, Inc., balanced, in phase quadrature (I/Q) or image rejection mixers.

The HMC1040CHIPS also feature inputs and outputs that are internally matched to 50 Ω, making it ideal for surface-mounted technology (SMT)-based, high capacity microwave radio applications.

Rev. 0 Document Feedback

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Technical Support www.analog.com

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REVISION HISTORY

4/2018—Revision 0: Initial Version

SPECIFICATIONS

20 GHz TO 24 GHz FREQUENCY RANGE

T_A = 25°C, supply voltage (V_{DD}) = 2.5 V, and supply current (I_{DQ}) = 65 mA, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit
FREQUENCY RANGE		20		24	GHz
GAIN			24.5		dB
Gain Variation Over Temperature			0.018		dB/°C
NOISE FIGURE	NF		4		dB
RETURN LOSS					
Input			18		dB
Output			18		dB
OUTPUT					
Output Power for 1 dB Compression	P1dB		12.5		dBm
Saturated Output Power	P_{SAT}		13.5		dBm
Output Third-Order Intercept	IP3		21		dBm
SUPPLY					
Current	I_{DQ}		65		mA
Voltage	V_{DD}	2	2.5	3.5	V

24 GHz TO 32 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 2.5 V, and I_{DQ} = 65 mA, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
FREQUENCY RANGE		24		32	GHz
GAIN		23	25.0		dB
Gain Variation Over Temperature			0.021		dB/°C
NOISE FIGURE	NF		2.5	2.7	dB
RETURN LOSS					
Input			13		dB
Output			13		dB
OUTPUT					
Output Power for 1 dB Compression	P1dB		13.5		dBm
Saturated Output Power	P_{SAT}		14.5		dBm
Output Third-Order Intercept	IP3		22.5		dBm
SUPPLY					
Current	I_{DQ}		65		mA
Voltage	V_{DD}	2	2.5	3.5	V

32 GHz TO 40 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 2.5 V, and I_{DQ} = 65 mA, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
FREQUENCY RANGE		32		40	GHz
GAIN		21	23		dB
Gain Variation Over Temperature			0.021		dB/°C
NOISE FIGURE	NF		2	2.7	dB
RETURN LOSS					
Input			11		dB
Output			13		dB
OUTPUT					
Output Power for 1 dB Compression	P1dB		13.5		dBm
Saturated Output Power	P_{SAT}		15.5		dBm
Output Third-Order Intercept	IP3		24.5		dBm
SUPPLY					
Current	I_{DQ}		65		mA
Voltage	V_{DD}	2	2.5	3.5	V

40 GHz TO 44 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 2.5 V, and I_{DQ} = 65 mA, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
FREQUENCY RANGE		40		44	GHz
GAIN		19	21		dB
Gain Variation Over Temperature			0.023		dB/°C
NOISE FIGURE	NF		2.5	3.2	dB
RETURN LOSS					
Input			6		dB
Output			13		dB
OUTPUT					
Output Power for 1 dB Compression	P1dB		14		dBm
Saturated Output Power	P_{SAT}		16		dBm
Output Third-Order Intercept	IP3		25.5		dBm
SUPPLY					
Current	I_{DQ}		65		mA
Voltage	V_{DD}	2	2.5	3.5	V

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Drain Bias Voltage (V_{DD})	4 V dc
Radio Frequency (RF) Input Power (RFIN)	5 dBm
Continuous Power Dissipation (P_{DISS}), T = 85°C (Derate 5.46 mW/°C Above 85°C)	0.49 W
Channel Temperature	175°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +85°C
Electrostatic Discharge (ESD) Sensitivity Human Body Model (HBM)	Class 0 passed, 100 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to system design and operating environment.

Careful attention to PCB thermal design is required.

θ_{JC} is the channel to case thermal resistance, channel to bottom of die.

Table 6. Thermal Resistance

Package Type	θ_{JC}	Unit
C-5-6	183	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

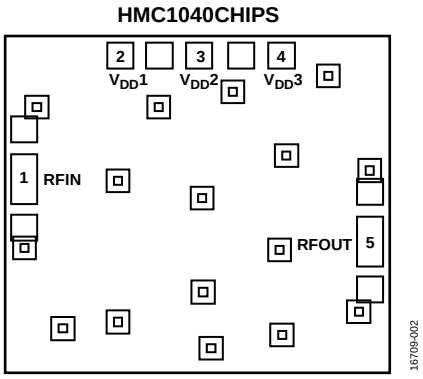

Figure 2. Pad Configuration

Table 7. Pad Function Descriptions

Pad No.	Mnemonic	Description
1	RFIN	Radio Frequency Input. This pad ac couples the RF signal, has a 5 kΩ resistor connected to GND, and is matched to 50 Ω. See Figure 3 for the interface schematic.
2, 3, 4	$V_{DD}1$, $V_{DD}2$, $V_{DD}3$	Power Supply Voltages for the Amplifier. Connect a dc bias to provide drain current (I_{DD}). See Figure 4 for the interface schematic.
5	RFOUT	RF Output. This pad ac couples the RF signal, has a 5 kΩ resistor connected to GND, and is matched to 50 Ω. See Figure 5 for the interface schematic.
Die Bottom	GND	Ground. Die bottom must be connected to RF/dc ground. See Figure 6 for the interface schematic.

INTERFACE SCHEMATICS

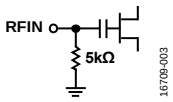

Figure 3. RFIN Interface Schematic

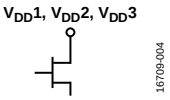

Figure 4. $V_{DD}1$, $V_{DD}2$, $V_{DD}3$, Interface Schematic

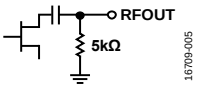

Figure 5. RFOUT Interface Schematic

Figure 6. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

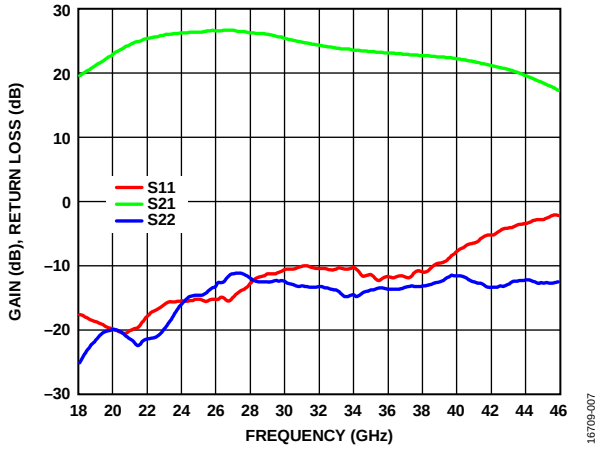

Figure 7. Gain and Return Loss vs. Frequency

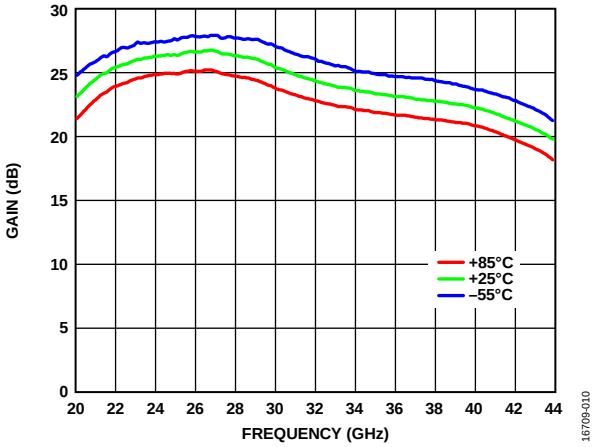

Figure 10. Gain vs. Frequency for Various Temperatures

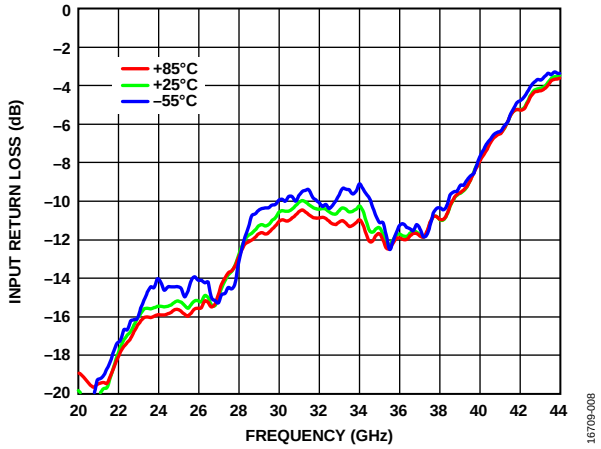

Figure 8. Input Return Loss vs. Frequency for Various Temperatures

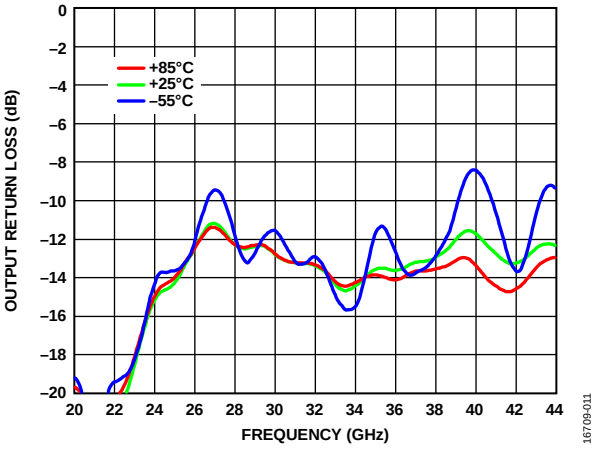

Figure 11. Output Return Loss vs. Frequency for Various Temperatures

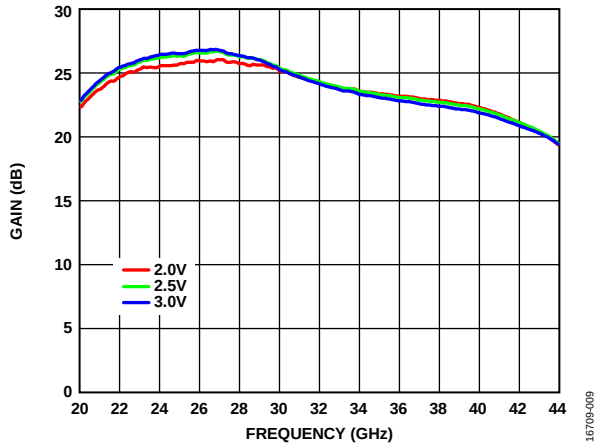

Figure 9. Gain vs. Frequency for Various Supply Voltages

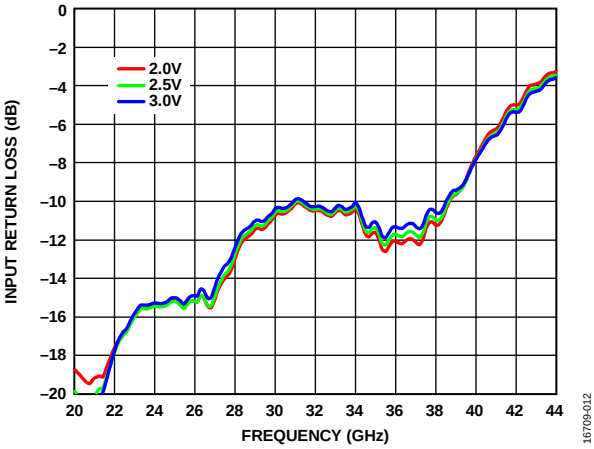

Figure 12. Input Return Loss vs. Frequency for Various Supply Voltages

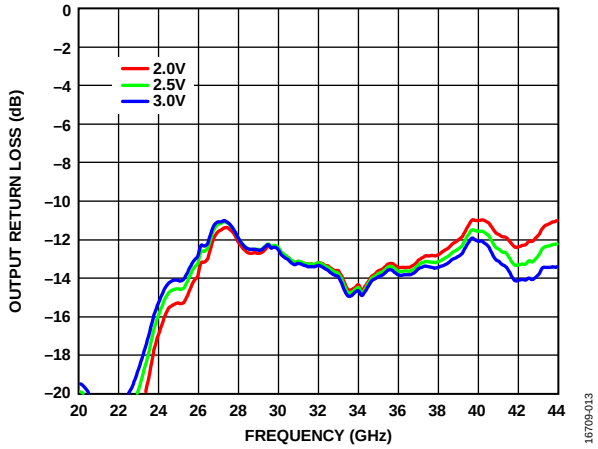

Figure 13. Output Return Loss vs. Frequency for Various Supply Voltages

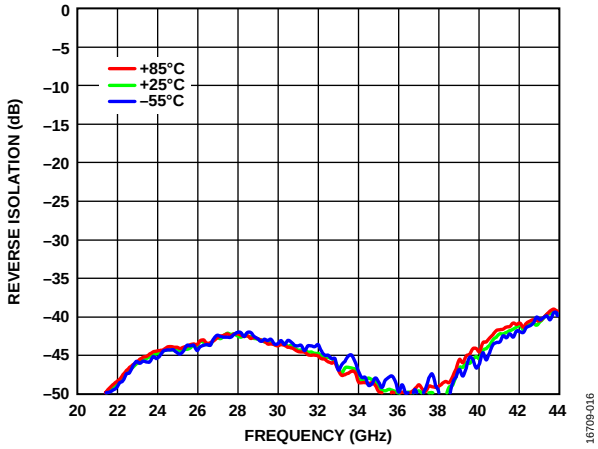

Figure 16. Reverse Isolation vs. Frequency for Various Temperatures

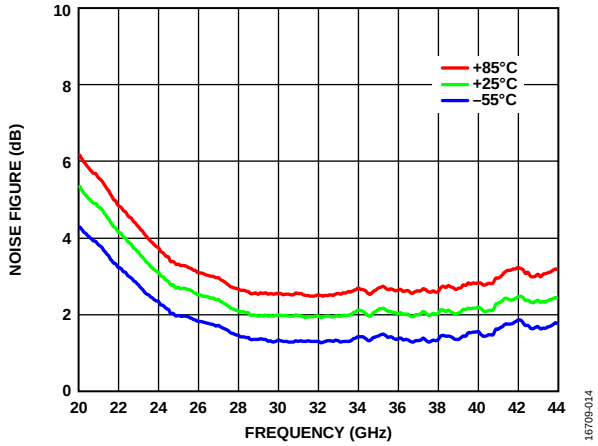

Figure 14. Noise Figure vs. Frequency for Various Temperatures

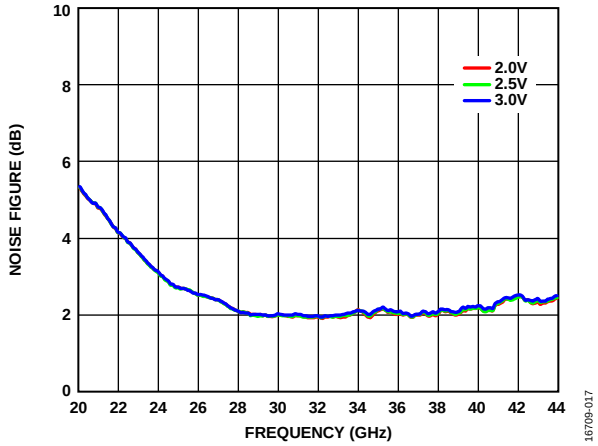

Figure 17. Noise Figure vs. Frequency for Various Supply Voltages

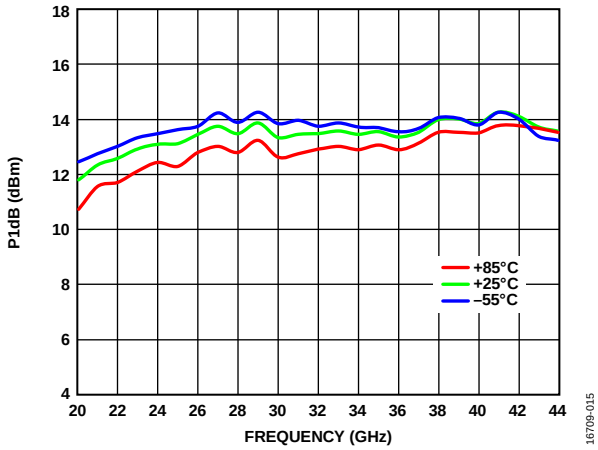

Figure 15. P1dB vs. Frequency for Various Temperatures

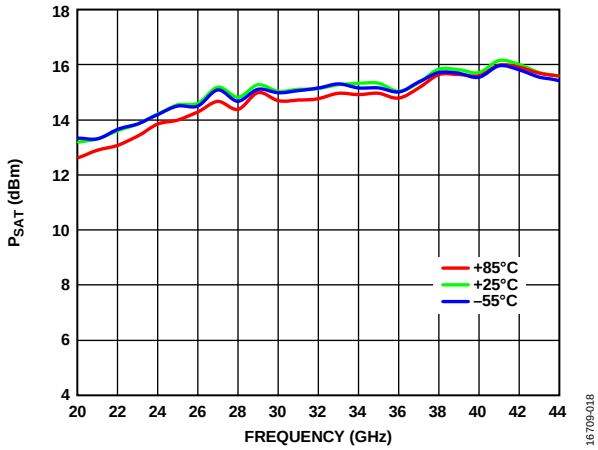

Figure 18. P_{SAT} vs. Frequency for Various Temperatures

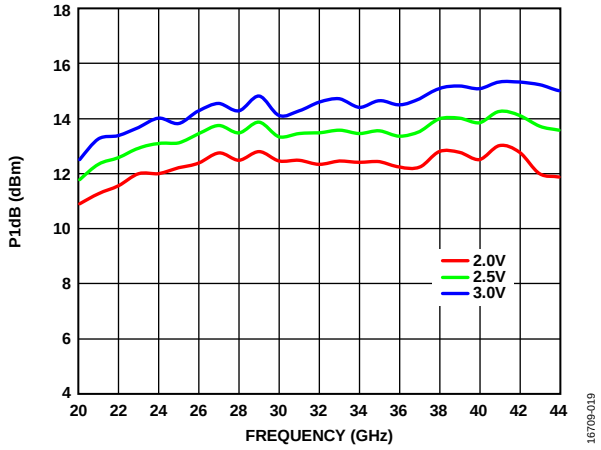

Figure 19. P1dB vs. Frequency for Various Supply Voltages

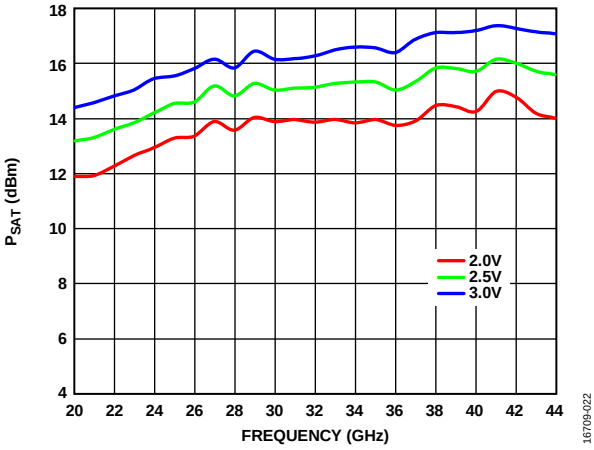

Figure 22. P_{SAT} vs. Frequency for Various Supply Voltages

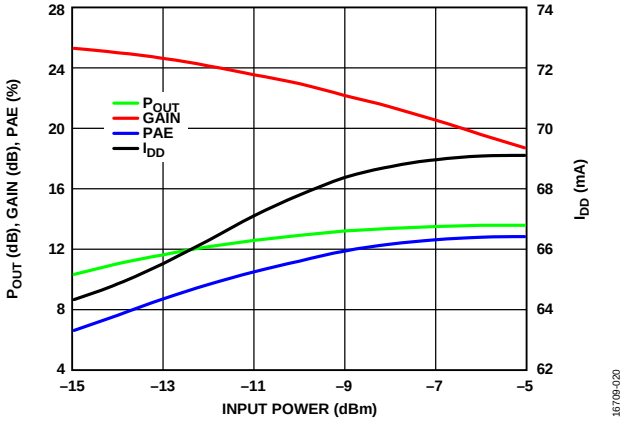

Figure 20. Output Power (P_{OUT}), Gain, Power Added Efficiency (PAE), and I_{DD} with RF Applied vs. Input Power at 22 GHz

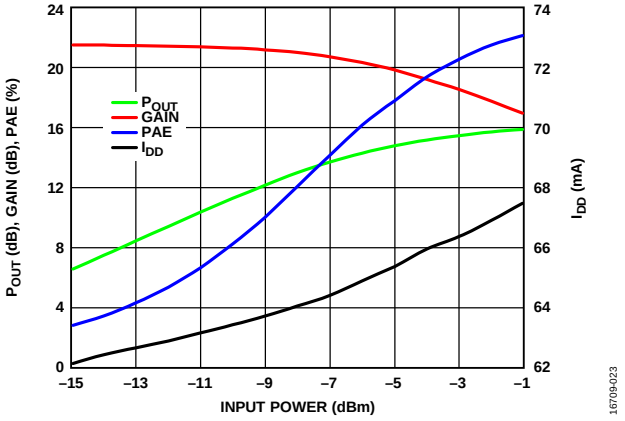

Figure 23. P_{OUT}, Gain, PAE, and I_{DD} with RF Applied vs. Input Power at 42 GHz

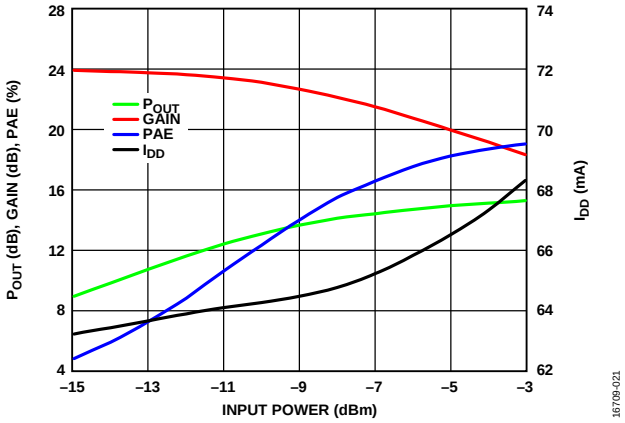

Figure 21. P_{OUT}, Gain, PAE, and I_{DD} with RF Applied vs. Input Power at 33 GHz

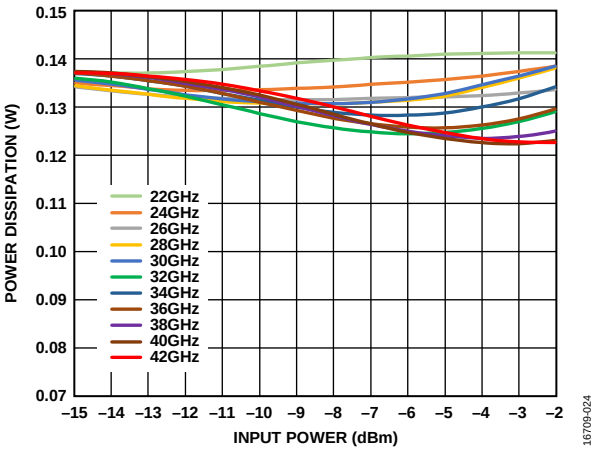

Figure 24. Power Dissipation vs. Input Power for Various Frequencies, $T_A = 85°C$

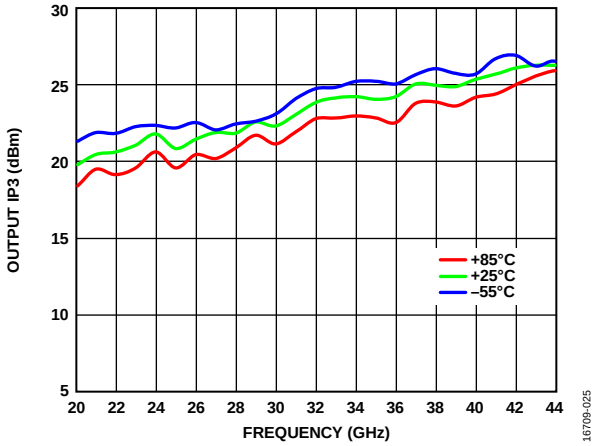

Figure 25. Output IP3 vs. Frequency for Various Temperatures, P_{OUT}/Tone = 4 dBm

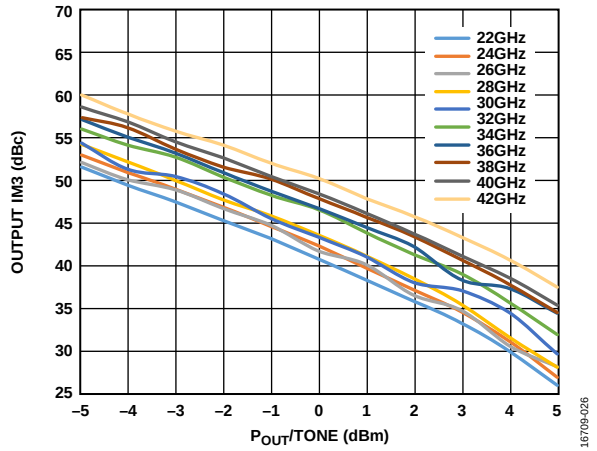

Figure 26. Output Third-Order Intermodulation (IM3) vs. P_{OUT}/Tone for Various Frequencies at V_{DD} = 2.0 V

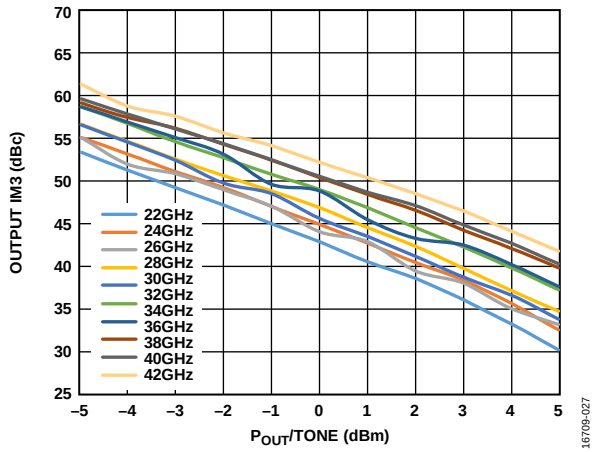

Figure 27. Output IM3 vs. P_{OUT}/Tone for Various Frequencies at V_{DD} = 2.5 V

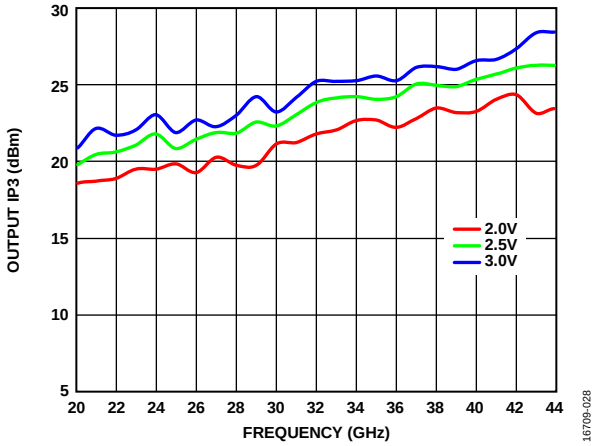

Figure 28. Output IP3 vs. Frequency for Various Supply Voltages, P_{OUT}/Tone = 4 dBm

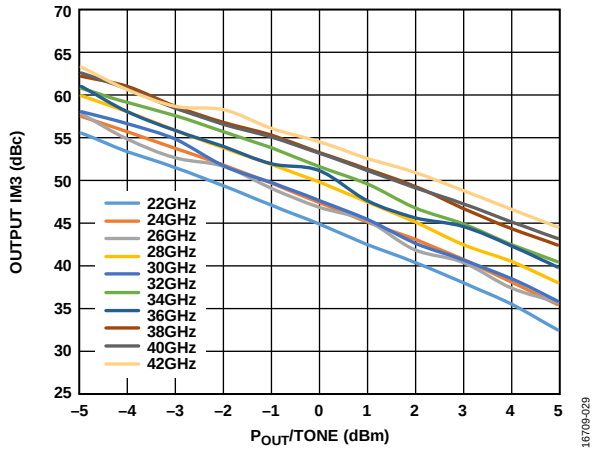

Figure 29. Output IM3 vs. P_{OUT}/Tone for Various Frequencies at V_{DD} = 3.0 V

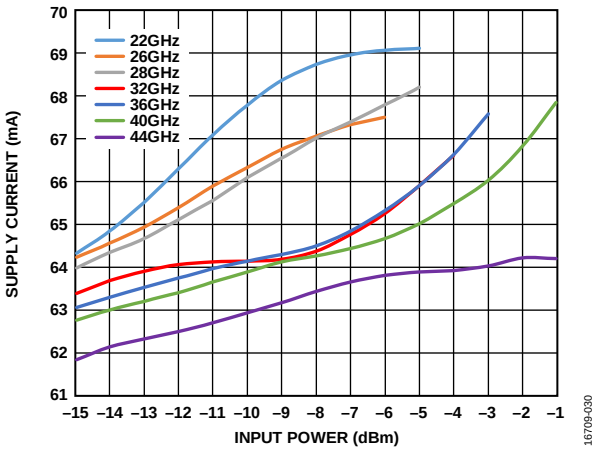

Figure 30. Supply Current vs. Input Power for Various Frequencies

THEORY OF OPERATION

The HMC1040CHIPS is a GaAs, pHEMT, MMIC, low noise, wideband amplifier. The basic architecture consists of three amplifier stages, optimized for low noise figure and high gain. Self bias removes the need for a negative bias voltage supply for the gate at each stage. A negative voltage is generated across the gate to the source when a typical voltage of 2.5 V is applied on V_{DDx} at each stage.

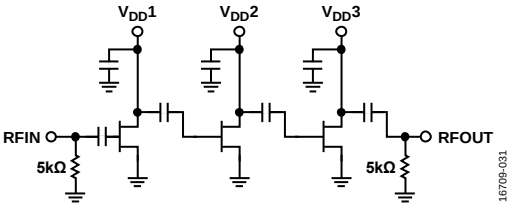

Figure 31. Architecture and Simplified Schematic

APPLICATIONS INFORMATION

RECOMMENDED BIAS SEQUENCING

Capacitive bypassing is required for $V_{DD}x$, as shown in the typical application circuit in Figure 34.

The recommended bias sequence during power-up is as follows:

1. Set $V_{DD}x$ to 2.5 V (this results in an I_{DQ} near its specified typical value).
2. Apply the RF input signal.

The recommended bias sequence during power-down is as follows:

1. Turn off the RF input signal.
2. Set $V_{DD}x$ to 0 V.

Unless otherwise noted, all measurements and data shown were taken using the typical application circuit (see Figure 34), configured as shown in the assembly diagram (see Figure 35) and biased per the conditions in the Specifications section. The bias conditions shown in the Specifications section are the operating points recommended to optimize the overall performance. Operation using other bias conditions may provide performance that differs from what is shown in this data sheet. To obtain the best performance while not damaging the device, follow the recommended biasing sequence outlined in this section.

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GaAs MMICS

Attach the die directly to the ground plane eutectically or with conductive epoxy (see the Handling Precautions section).

To bring the radio frequency to and from the chip, implementing 50 Ω transmission lines using a microstrip or coplanar waveguide on 0.127 mm (0.005") thick alumina, thin film substrates is recommended (see Figure 32). When using 0.254 mm (0.010") thick alumina, it is recommended that the die be raised to ensure that the die and substrate surfaces are coplanar. Raise the die 0.150 mm (0.005") to ensure that the surface of the die is coplanar with the surface of the substrate. To accomplish this, attach the 0.102 mm (0.004") thick die to a 0.150 mm (0.005") thick, molybdenum (Mo) heat spreader (moly tab), which can then be attached to the ground plane (see Figure 32 and Figure 33).

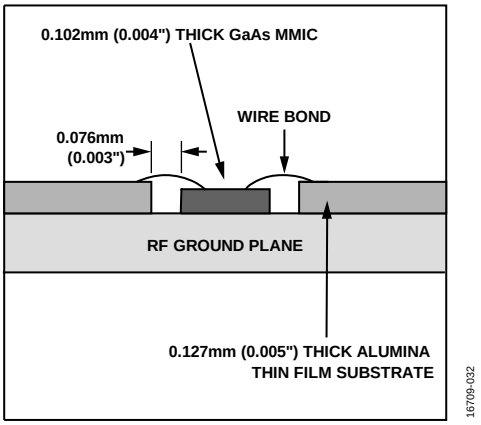

Figure 32. Die Without the Moly Tab

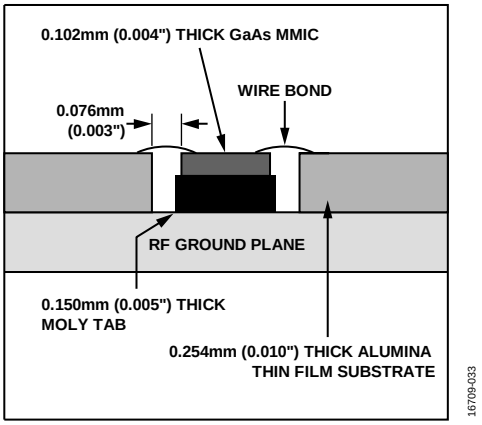

Figure 33. Die With the Moly Tab

Place microstrip substrates as close to the die as possible to minimize bond wire length. Typical die to substrate spacing is 0.076 mm to 0.152 mm (0.003" to 0.006").

Handling Precautions

To avoid permanent damage, follow these storage, cleanliness, static sensitivity, transient, and general handling precautions:

- Place all bare die in either waffle or gel-based ESD protective containers and then seal the die in an ESD protective bag for shipment. After the sealed ESD protective bag is opened, store all die in a dry nitrogen environment.
- Handle the chips in a clean environment. Do not attempt to clean the chip using liquid cleaning systems.
- Follow ESD precautions to protect against ESD strikes.
- While bias is applied, suppress instrument and bias supply transients. Use shielded signal and bias cables to minimize inductive pickup.
- Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip may have fragile air bridges and must not be touched.

TYPICAL APPLICATION CIRCUIT

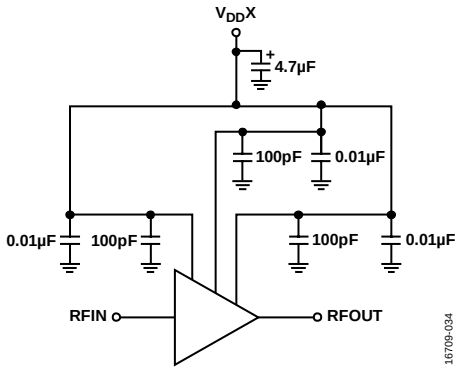

Figure 34. Typical Application Circuit

ASSEMBLY DIAGRAM

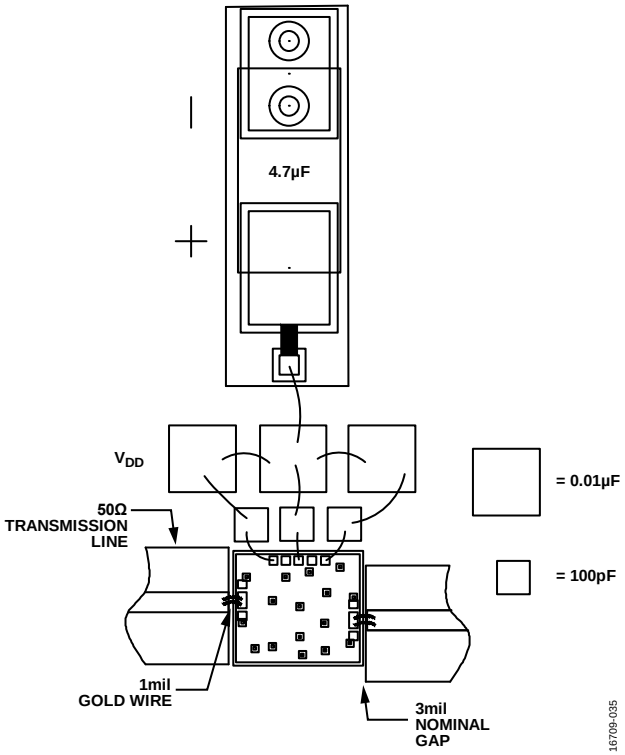

Figure 35. Assembly Diagram

OUTLINE DIMENSIONS

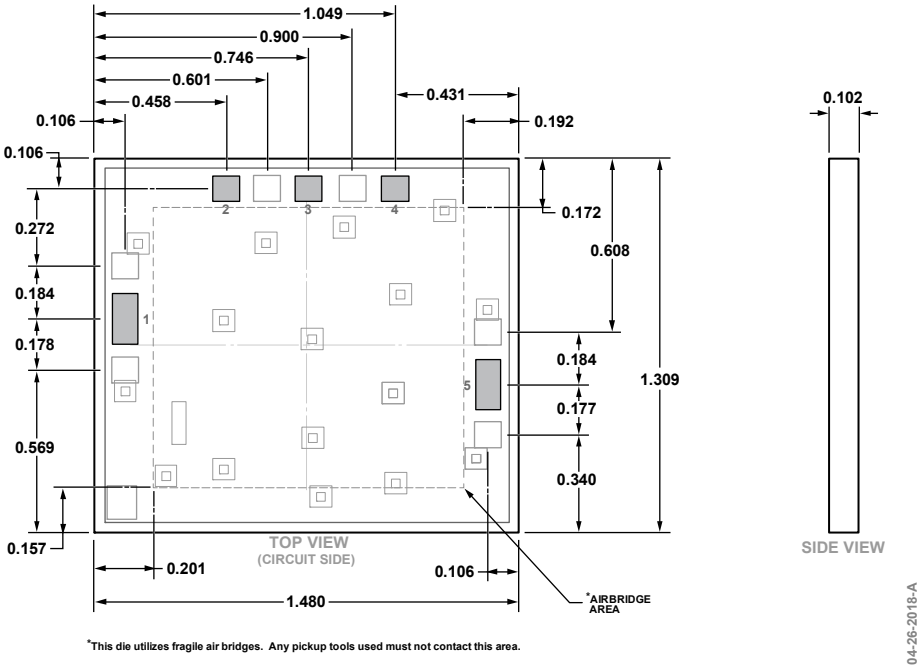

Figure 36. 5-Pad Bare Die [CHIP]
(C-5-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
HMC1040CHIPS	−55°C to +85°C	5-Pad Bare Die [CHIP]	C-5-6
HMC1040CHIPS-SX	−55°C to +85°C	5-Pad Bare Die [CHIP]	C-5-6

[1] The HMC1040CHIPS and HMC1040CHIPS-SX are RoHS Compliant Parts.