ANALOG DEVICES

EVAL-AD5423SDZ Evaluation Board User Guide

UG-1554

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Evaluating the AD5423 Single Channel, 16-Bit Current or Voltage Output DAC with HART Connectivity

FEATURES

Fully featured evaluation board for the AD5423
On board 2.5 V ADR4525 reference
ACE software for control

EVALUATION KIT CONTENTS

EVAL-AD5423SDZ evaluation board

EQUIPMENT NEEDED

SDP-S controller board
Bench top power supply and connector cables
PC/laptop

DOCUMENTS NEEDED

AD5423 data sheet
ACE user manual

SOFTWARE NEEDED

ACE software

GENERAL DESCRIPTION

This user guide describes the EVAL-AD5423SDZ evaluation board for the AD5423 single-channel, 16-bit voltage, 16-bit current output digital-to-analog converter (DAC).

The EVAL-AD5423SDZ (see Figure 1) requires the EVAL-SDP-CS1Z system demonstration platform (SDP-S) board. The EVAL-AD5423SDZ interfaces to the USB port of the PC via the SDP-S board. The Analysis, Control, Evaluation (ACE) software allows simplified programming of the AD5423, and is available to use with the EVAL-AD5423SDZ.

For full details on the AD5423, see the AD5423 data sheet. Consult the data sheet in conjunction with this user guide when using the EVAL-AD5423SDZ.

EVALUATION BOARD PHOTOGRAPH

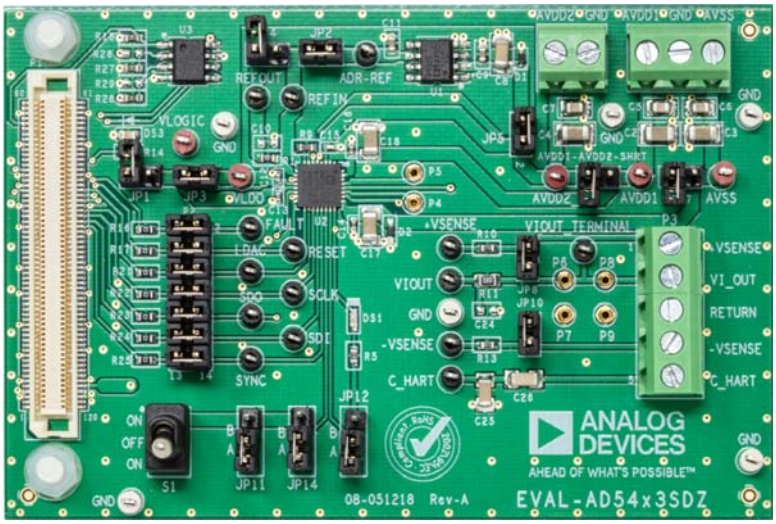

Figure 1.

TABLE OF CONTENTS

REVISION HISTORY

5/2019—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The EVAL-AD5423SDZ requires a number of power supply inputs for the AV_{DD1}, AV_{DD2}, AV_{SS}, and V_{LOGIC} pins on the AD5423. If there is only one positive rail available, connect the AV_{DD2} pin to the AV_{DD1} pin via the AVDD1-AVDD2-SHRT link on the EVAL-AD5423SDZ. The V_{LOGIC} supply can be selected from 3.3V_SDP on the SDP-S board or V_{LDO}, through the JP1 and JP3 jumpers. See Table 1 for more link options and the default link positions.

EVAL-AD5423SDZ operates with a power supply range from −33 V on AV_{SS} to +33 V on AV_{DD1} with a maximum voltage of 50 V between the two rails. AV_{DD2} requires a voltage between 5 V and 33 V. In a typical operating condition, AV_{DD2} = 5 V, AV_{DD1} = +24 V, and AV_{SS} = −24 V.

SERIAL COMMUNICATION

The SDP-S board handles the communication to the EVAL-AD5423SDZ via the PC. By default, the SDP-S board handles the serial port interface (SPI) communication, controls the $\overline{\text{RESET}}$ pin and the $\overline{\text{LDAC}}$ pin, and monitors the $\overline{\text{FAULT}}$ pin of the AD5423.

The EVAL-AD5423SDZ can disconnect from the SDP-S board and drive the digital signals from an external source by removing the appropriate links on P2 (see Table 2). An option to tie the $\overline{\text{RESET}}$ pin and the $\overline{\text{LDAC}}$ pin to high or low levels is available through the S1 switch and the JP11 link.

AD5423 DEVICE ADDRESS PINS

The device address pins (AD0 and AD1) are used in conjunction with the device address bits within the SPI frame to determine which AD5423 device is being addressed by the system controller. The AD0 pin and the AD1 pin can be configured through the JP12 and JP14 links (see Table 1).

Table 1. EVAL-AD5423SDZ Link Option Functions

Link	Default Position	Function
AVDD1-AVDD2-SHRT	Not inserted	Connects the AV_{DD2} pin to the AV_{DD1} pin.
JP1	Not inserted	Selects 3.3 V from the SDP-S as the source for the V_{LOGIC} pin.
JP2	Inserted	Selects the external reference ADR-REF as the input to REFIN.
JP3	Inserted	Selects 3.3 V from the V_{LDO} pin of the AD5423 as the source for the V_{LOGIC} pin.
JP4	Not inserted	Selects the REFOUT pin as the input to the REFIN pin.
JP5	Inserted	Powers external reference ADR-REF from the AV_{DD2} pin (the maximum supply for the ADR4525 is 15 V).
JP8	Inserted	Connects the VI_{OUT} pin to the + V_{SENSE} pin.
JP10	Inserted	Connects the $-V_{SENSE}$ pin to the RETURN signal on the EVAL-AD5423SDZ.
JP11	A	Position A connects the $\overline{\text{LDAC}}$ pin to the ground position. Position B connects $\overline{\text{LDAC}}$ to the V_{LOGIC} pin.
JP12	A	Position A connects the AD0 pin to the ground position. Position B connects the AD0 pin to the V_{LOGIC} pin.
JP14	A	Position A connects the AD1 pin to the ground position. Position B connects the AD1 pin to the V_{LOGIC} pin.
JP17	Not inserted	Connects the AV_{SS} pin to the ground position pin for the unipolar supply option (current output only).
P2	Inserted	Provides options to disconnect from the SDP-S board and to drive digital signals from an external source.
S1	Up	In the up position, this link connects the $\overline{\text{RESET}}$ pin to the V_{LOGIC} pin.
	Middle (default)	In the middle position (default), this link controls the $\overline{\text{RESET}}$ pin via the SDP-S board.
	Down	In the right position, this link connects the $\overline{\text{RESET}}$ pin to the ground position pin.

Table 2. Link Options for P2 Header

Pin No.	Position	Function
1, 2	Inserted	Connects the $\overline{\text{FAULT}}$ signal from the SDP-S to the $\overline{\text{FAULT}}$ pin on the AD5423.
	Not inserted	Disconnects the $\overline{\text{FAULT}}$ signal from the SDP-S to the $\overline{\text{FAULT}}$ pin on the AD5423.
3, 4	Inserted	Connects the $\overline{\text{RESET}}$ signal from the SDP-S to the $\overline{\text{RESET}}$ pin on the AD5423.
	Not inserted	Disconnects the $\overline{\text{RESET}}$ signal from the SDP-S to the $\overline{\text{RESET}}$ pin on the AD5423.
5, 6	Inserted	Connects the $\overline{\text{LDAC}}$ signal from the SDP-S to the $\overline{\text{LDAC}}$ pin on the AD5423.
	Not inserted	Disconnects the $\overline{\text{LDAC}}$ signal from the SDP-S to the $\overline{\text{LDAC}}$ pin on the AD5423.
7, 8	Inserted	Connects the SCLK signal from the SDP-S to the SCLK pin on the AD5423.
	Not inserted	Disconnects the SCLK signal from the SDP-S to the SCLK pin on the AD5423.
9, 10	Inserted	Connects the SDO signal from the SDP-S to the SDO pin on the AD5423.
	Not inserted	Disconnects the SDO signal from the SDP-S to the SDO pin on the AD5423.
11, 12	Inserted	Connects the SDI signal from the SDP-S to the SDI pin on the AD5423.
	Not inserted	Disconnects the SDI signal from the SDP-S to the SDI pin on the AD5423.
13, 14	Inserted	Connects the $\overline{\text{SYNC}}$ signal from the SDP-S to the $\overline{\text{SYNC}}$ pin on the AD5423.
	Not inserted	Disconnects the $\overline{\text{SYNC}}$ signal from the SDP-S to the $\overline{\text{SYNC}}$ pin on the AD5423.

SOFTWARE QUICK START PROCEDURES

INSTALLING THE ACE SOFTWARE AND EVAL-AD5423SDZ PLUGINS

The EVAL-AD5423SDZ board uses Analog Devices, Inc., ACE software. For instructions on how to install and use the ACE software, go to www.analog.com/ACE.

When the installations are finished, the EVAL-AD5423SDZ plugin will appear when you open the ACE software.

INITIAL SETUP

To set up the EVAL-AD5423SDZ, take the following steps:

1. Connect a USB cable to the PC and then to the SDP-S board.
2. Connect the SDP-S board to the EVAL-AD5423SDZ. The PC recognizes the EVAL-AD5423SDZ.
3. Power up the EVAL-AD5423SDZ with the power supplies recommended in the Power Supplies section.
4. Open the ACE software. The **EVAL-AD5423 SDZ** appears in the **Attached Hardware** pane of the ACE window.

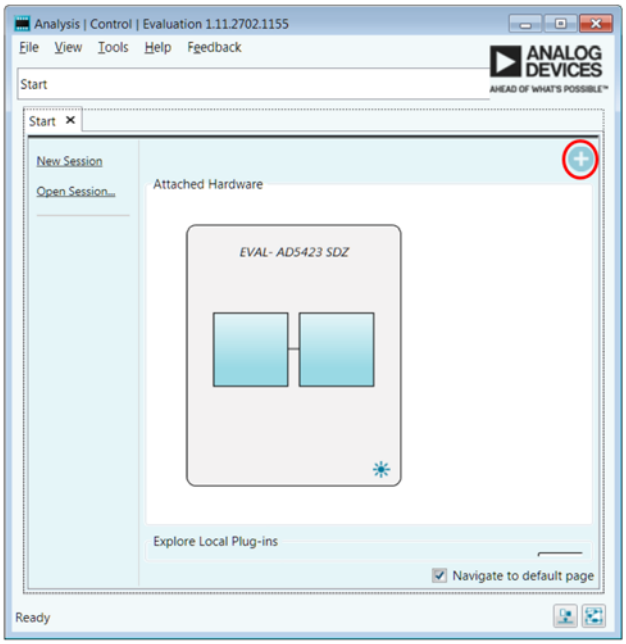

Figure 2. EVAL-AD5423SDZ Plugin Not Installed

5. When setting up the evaluation board for the first time, it can be required to install the EVAL-AD5423SDZ plugin. If the plugin appears as shown in Figure 5, then proceed to Step 7. If the plugin appears as shown in Figure 2, click on the button circled in red and the pop-up window shown in Figure 3 appears. Click **Yes**.

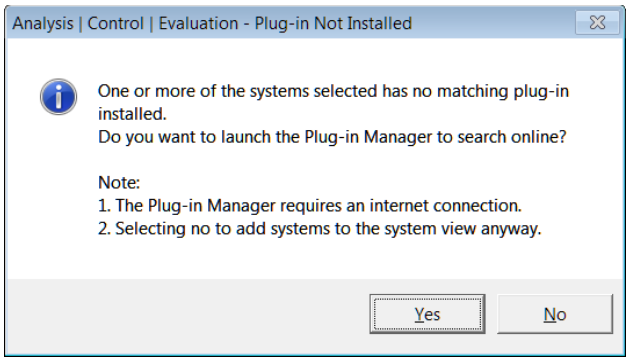

Figure 3. Installing the Plugin Pop-Up Window

6. The plugin manager window appears, as shown in Figure 4.
7. Find and select the **Board.AD5423** plugin and click **Install Selected**. The EVAL-AD5423SDZ plugin is now installed and displays as shown in Figure 5.

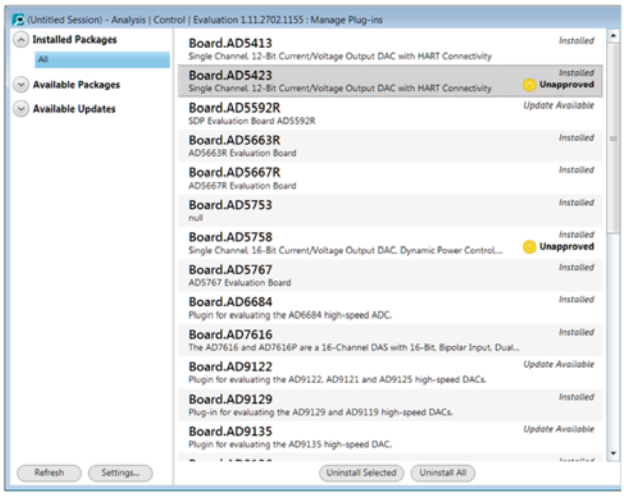

Figure 4. Plugin Manager Window

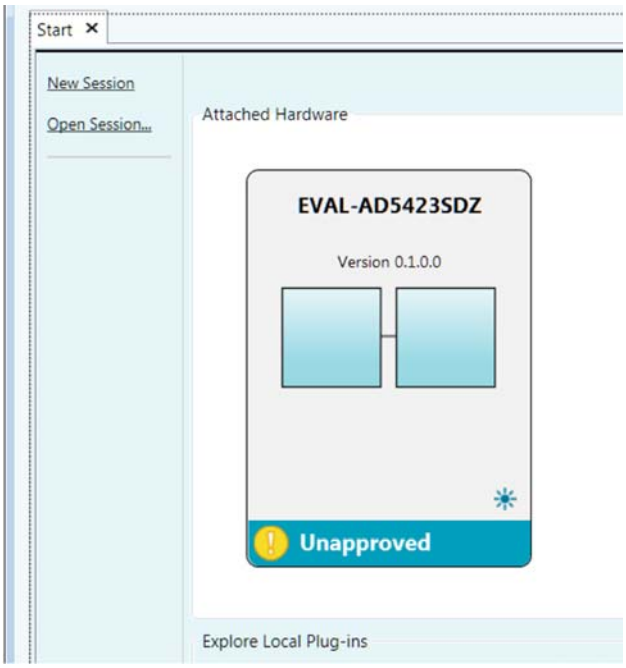

Figure 5. Attached Hardware Section with the EVAL-AD5423SDZ Plugin Connected

8. Double-click **EVAL-AD5423SDZ** to open the AD5423 block diagram (see Figure 6). The **INITIAL CONFIGURATION** pane appears on the left side of the ACE window. Several register settings can be configured in this pane and are written to the device in the appropriate order. The **RESET_OCCURED** and **CAL_MEM_UNREFRESHED** LED indicators in the **DIGITAL DIGNOSTIC RESULTS** pane are illuminated red by default.
9. Write the initial configuration values to clear these error flags. If the device is power cycled, or if the USB cable is disconnected and reconnected while the ACE software is open, contact with the EVAL-AD5423SDZ is lost. To regain contact, click the **System** tab, then click the USB symbol on the EVAL-AD5423SDZ, and then click **Acquire**.

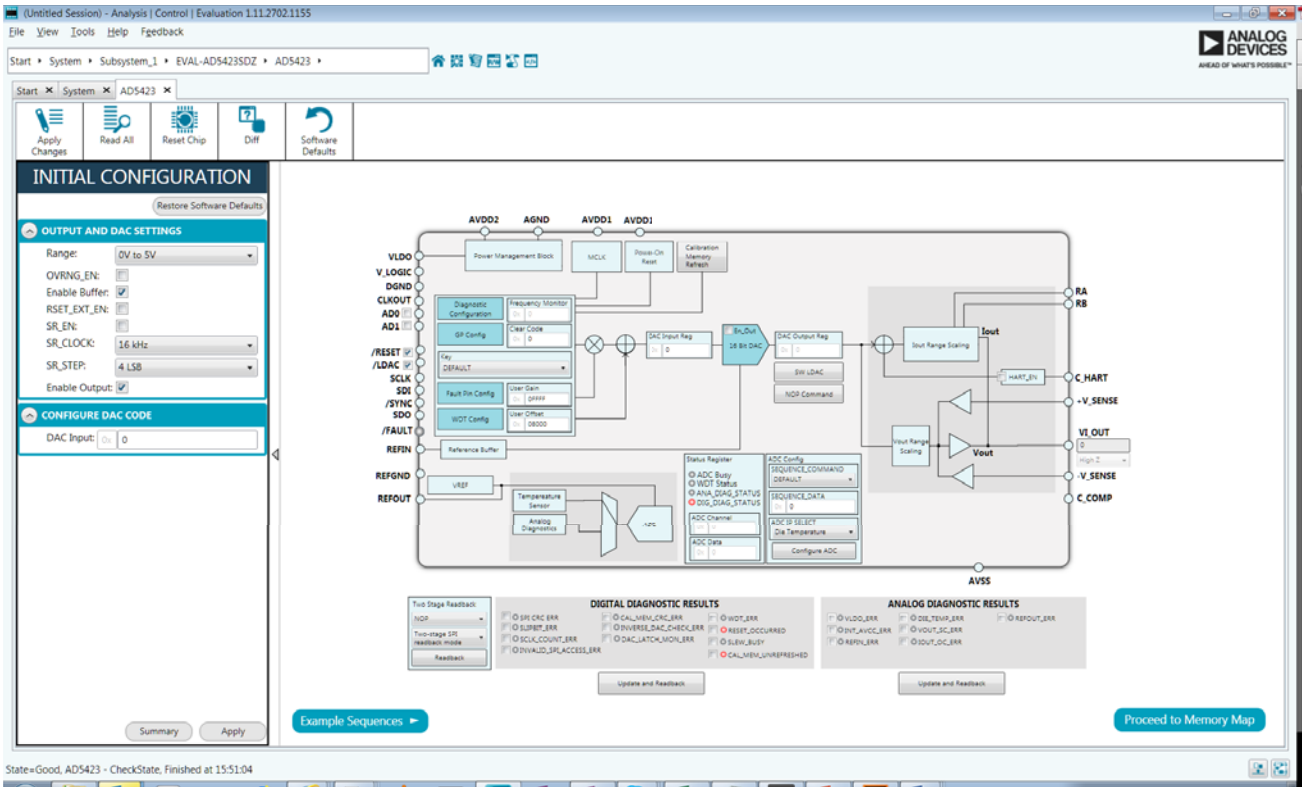

Figure 6. AD5423 Block Diagram in the ACE Software

AD5423 BLOCK DIAGRAM AND FUNCTIONS

The EVAL-AD5425SDZ plugin is organized to appear similar to the block diagram shown in the AD5423 data sheet. This graphical user interface (GUI) correlates the functions of the EVAL-AD5423SDZ with the descriptions in the AD5423 data sheet.

Full descriptions of each block and register setting are available in the AD5423 data sheet. The full screen AD5423 block diagram with labels is shown in Figure 7. Table 3 and Table 4 describe the functionality of each block.

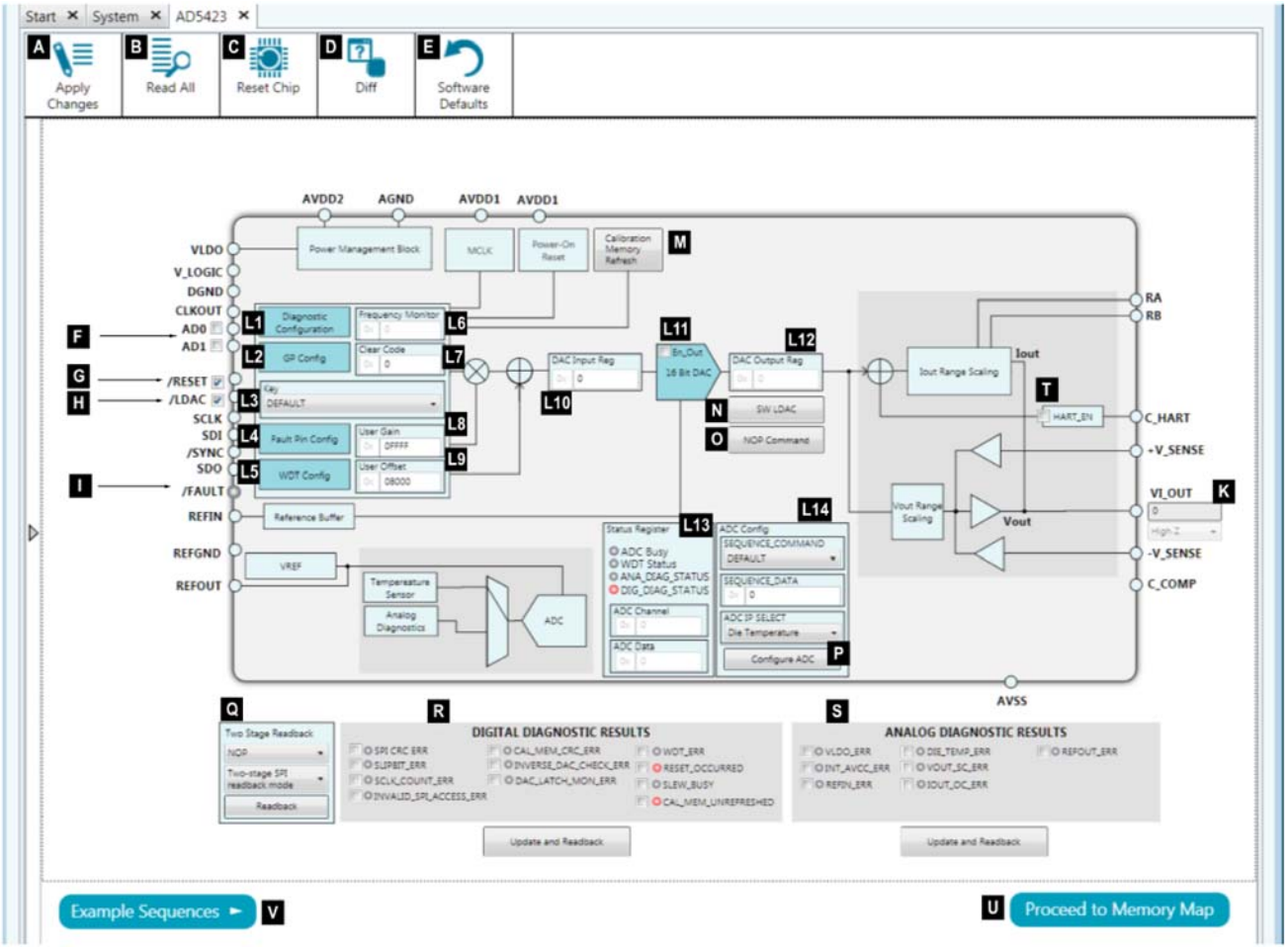

Figure 7. AD5423 Block Diagram with Labels

Table 3. AD5423 Block Diagram Label Functions (See Figure 7)

Figure Label	Function
A	To apply any changes made to the block diagram or to register values in the memory map to the device, click **Apply Changes**.
B	To read back all of the registers of the device, click **Read All**.
C	Click **Reset Chip** to reset the AD5423. The **Reset Chip** button has the same functionality as the software reset of the AD5423.
D	Click **Diff** to show the registers that are different from the data stored on the device. This function shows what has changed since the last register read.
E	Click **Software Defaults** to load the software defaults of the device. These values are not written to the hardware. Click **Apply Changes** to write the software default values to the hardware.
F	The **AD0** and **AD1** checkboxes set the AD5423 address of the device and must correspond to the JP12 and JP14 links on the hardware. If either checkbox is selected, this represents a high state. If either box is not selected, this represents a low state.
G	If the **/RESET** checkbox is selected, the SDP-S board sets the $\overline{\text{RESET}}$ pin high. Otherwise, the SDP-S board pulls the $\overline{\text{RESET}}$ pin low.
H	If the **/LDAC** checkbox is selected, the SDP-S board sets the $\overline{\text{LDAC}}$ pin high. Otherwise, the SDP-S board pulls the $\overline{\text{LDAC}}$ pin low.
I	The EVAL-AD5425SDZ plugin monitors the $\overline{\text{FAULT}}$ pin. If the $\overline{\text{FAULT}}$ pin is low, the **/FAULT** indicator LED lights up red.
K	**VI_OUT** displays the calculated output at VI_{OUT}, and displays if the output is in voltage, milliamps, or is high impedance (high-Z).

Figure Label	Function
Lx	GUI access on several registers. Pop-ups, dropdown menus, and hexadecimal textboxes are available in the GUI to configure several registers of the AD5423. To write the changes to the device, click **Apply Changes**. The functions within the GUI that control various registers are described in Table 4.
M	The **Calibration Memory Refresh** button initiates a write to the key register to perform a calibration memory refresh.
N	The **SW LDAC** button initiates a write to the key register to perform a software $\overline{\text{LDAC}}$ command.
O	The **NOP Command** button initiates a write to Address 0x00 for a no operation (NOP) command.
P	The **Configure ADC** button writes the data selected in the **ADC Config** menu to the ADC configuration register.
Q	**Two Stage Readback Select** menu. A two-stage readback is initiated through the two-stage readback select register. Click **Readback** to initiate a write to the two-stage readback select register and issue a no operation command.
R	**DIGITAL DIAGNOSTIC RESULTS** menu. Click **Update and Readback Digital Diagnostic Result** to trigger a write 1 to clear operation on the selected checkboxes and a readback from the digital diagnostic result register.
S	**ANALOG DIAGNOSTIC RESULTS** menu. Click **Update and Readback Analog Diagnostic Result** to trigger a write 1 to clear operation on the selected checkboxes and a readback from the analog diagnostic result register.
T	When the **HART_EN** checkbox is selected, the HART_EN bit = 1 in the General-Purpose Configuration 1 register.
U	Click **Proceed to Memory Map** to open the AD5423 memory map (see Figure 8).
V	Click **Example Sequences** to open the example sequences window (see Figure 13).

Table 4. Register Controls Accessible via the GUI (See Label Lx in Table 3 and in Figure 7)

Figure Label	Function
L1	**Diagnostic Configuration**. Click this button to activate the associated pop-up menu.
L2	**GP Config**. When this button is clicked, a pop-up menu appears to configure the general-purpose configuration registers.
L3	**Key** register menu. When this menu is clicked, a dropdown menu appears to configure the key register.
L4	**Fault Pin Config**. When this button is clicked, a pop-up menu appears to configure the general-purpose configuration registers.
L5	**WDT Config**. When this button is clicked, a pop-up menu appears to configure the general-purpose configuration registers.
L6	**Frequency Monitor** menu. This menu displays the value in the frequency monitor when read.
L7	**Clear Code** menu. Use the textbox in this menu to insert a clear code value in hexadecimal format.
L8	**User Gain** menu. Use the textbox in this menu to insert a user gain value in hexadecimal format.
L9	**User Offset** menu. Use the textbox in this menu to insert a user offset value in hexadecimal format.
L10	**DAC Input Reg** menu. Use the textbox in this menu to insert the DAC value in hexadecimal format.
L11	**16 Bit DAC**. When this button is clicked, a pop-up menu appears to configure the general-purpose configuration registers.
L12	**DAC Output Reg**. This menu displays the hexadecimal value currently set in the DAC output register.
L13	**Status Register**. This menu displays the contents of the status register.
L14	**ADC Config**. This menu contains a combination of dropdown menus and a textbox in which to enter the sequence data.

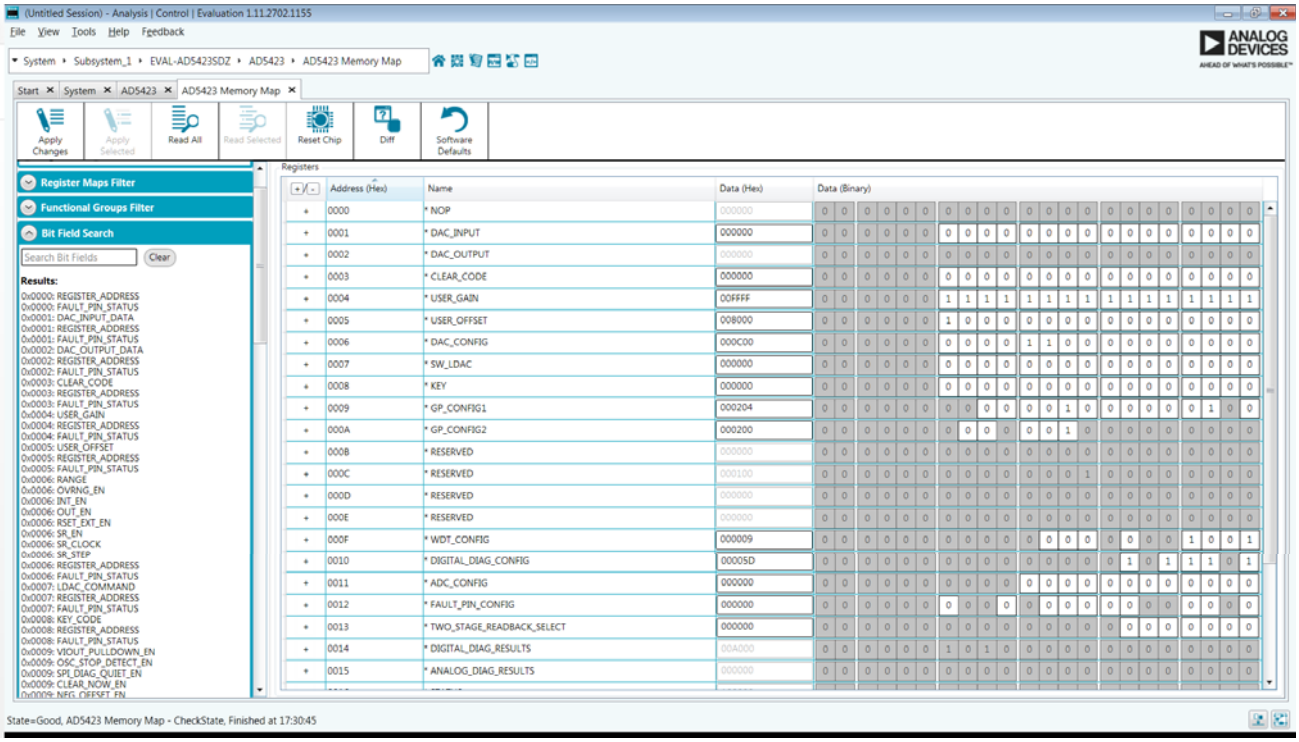

Figure 8. AD5423 Memory Map in the ACE Software

INITIAL CONFIGURATION

An initial configuration wizard is available when the AD5423 plugin opens that allows quick configuration of the AD5423, and provides configuration for the clock output in the general-purpose configuration register, the DAC configuration register, and the DAC input register. Click **Apply** to initiate the configured settings in the order of the recommended power-up sequence on the AD5423 data sheet.

SETTING THE DAC OUTPUT

To configure the DAC output, use the **DAC Config Register** pop-up menu (see Figure 9). Click the **16 Bit DAC** block in the block diagram to display the DAC configuration register. Select the appropriate settings and click **Apply Changes**. It is recommended to disable the output until the correct value in the DAC input register is written to the device.

To change the DAC voltage or current output level, write the appropriate hexadecimal code to the DAC input register, and then click **Apply Changes**. Click **SW LDAC** to issue a software $\overline{\text{LDAC}}$ command, or pull the $\overline{\text{LDAC}}$ pin low to update the DAC output register with the values in the DAC input register. To enable the DAC output, select the **OUT_EN (Enable VI_OUT)** checkbox, and then click **Apply Changes**. The programmed voltage or current is then reflected at the VI_{OUT} pin.

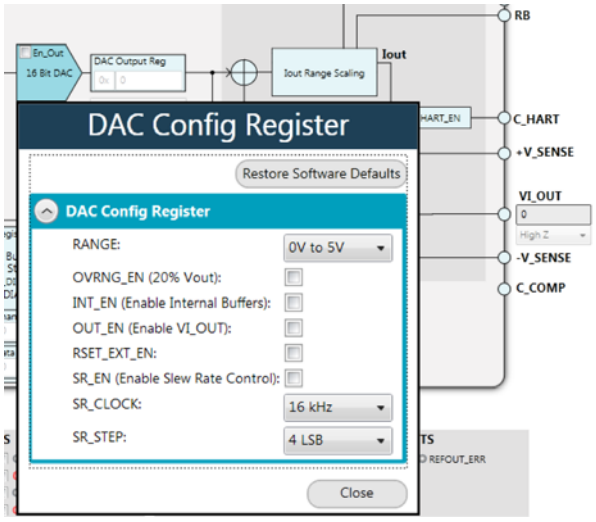

*Figure 9. AD5423 **DAC Config Register** Pop-Up Menu*

WRITING TO THE ADC CONFIGURATION REGISTER

The procedure to set up and configure the ADC input node is discussed in the AD5423 data sheet. For this reason, writing to the ADC configuration register through the **Apply Changes** function is disabled.

The dropdown list in the **SEQUENCE_COMMAND** section contains only an initiate single conversion command (**INITIATE_SINGLE_CON**). The hexadecimal text box in the **SEQUENCE_DATA** pane is unused and remains at 0. Use the dropdown list in the **ADC_IP_SELECT** pane to select the desired input node for the ADC to convert. Click **Configure ADC** to initiate a write to the ADC configuration register. A register read must be performed to see the ADC result in the status register (see Figure 10).

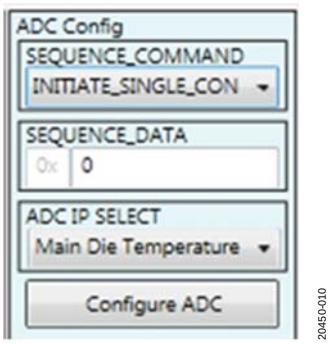

Figure 10. AD5423 ADC Configuration Register

UPDATING DIAGNOSTIC RESULTS

The AD5423 has a digital diagnostic results register and an analog diagnostic results register that contain error flags for the on-chip digital and analog diagnostic features. Write 1 to the respective error flags update the error flag status.

To update the digital and analog diagnostic result registers, click **Update and Readback**. This button initiates a write of 1 to the selected checkboxes and then reads back the updated diagnostic result. Figure 11 shows the digital diagnostic results register. Figure 12 shows the analog diagnostic results register.

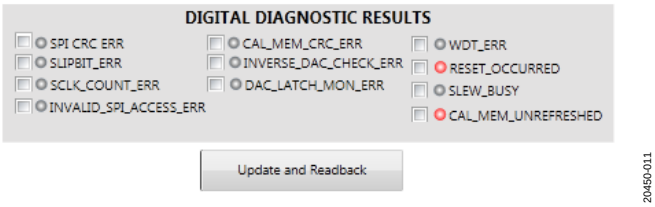

Figure 11. AD5423 Digital Diagnostic Results Register

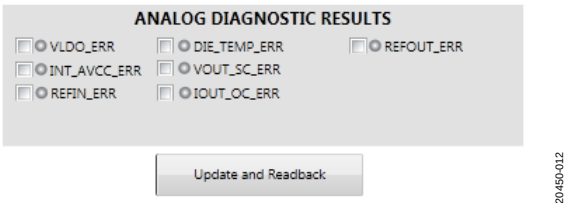

Figure 12. AD5423 Analog Diagnostic Results Register

EXAMPLE SEQUENCES

There are several example sequences available. Click **Example Sequences** and the window shown in Figure 13 opens. To enable any of the sequences, click the relevant sequence button, as shown in Figure 14. The sequence runs immediately and the output changes accordingly. To return to the main window, click **Back to the AD5423**.

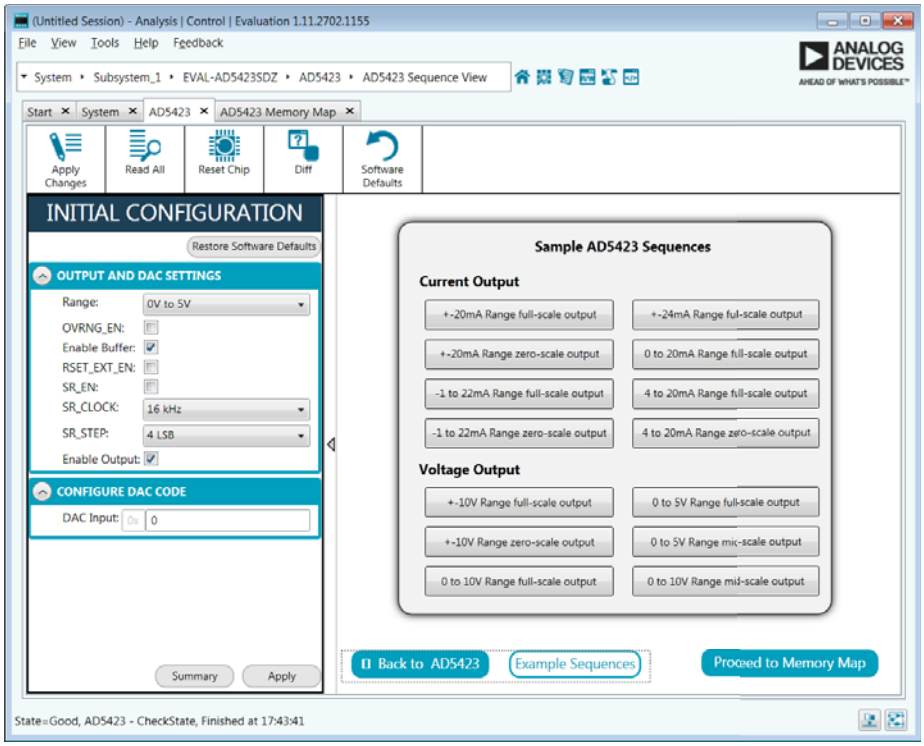

Figure 13. Example Sequences Window

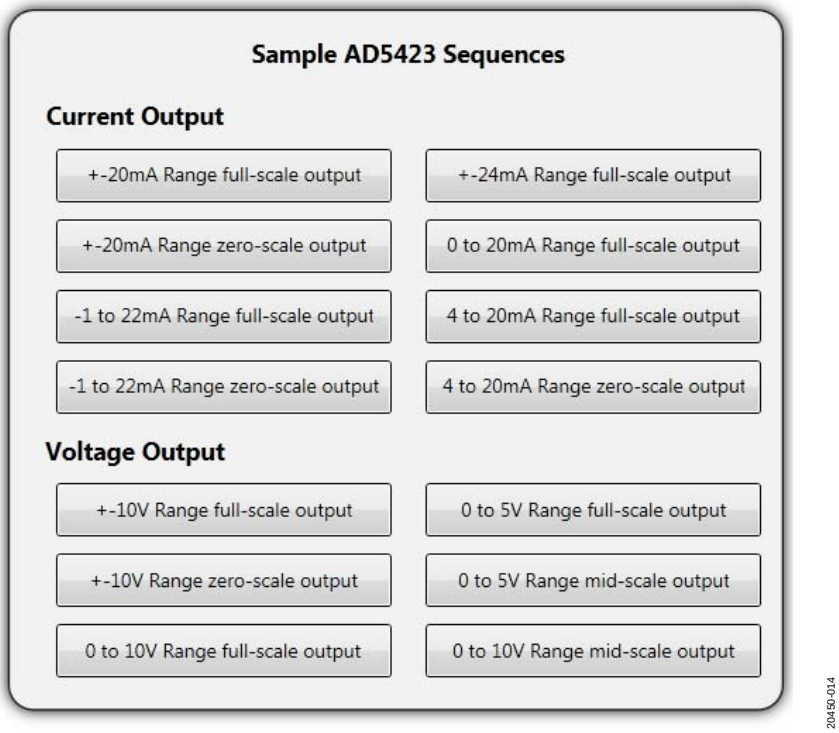

Figure 14. Selecting an Example Sequence

ACE TOOL VIEWS

The ACE software provides additional functionality to the main view described in this user guide. Open these views from the view menu item on the application toolbar. ACE features a macro tool, a register debugger tool, and an events tool.

MACRO TOOL

The macro tool allows commands to be recorded and saved as an ACE macro file. This feature is useful when sharing macros with other users to perform the same task multiple times. The user can import and run an ACE macro file.

REGISTER DEBUGGER TOOL

Use the register debugger tool to perform raw writes to and reads from the device. The register debugger affects only the hardware and does not write to the memory map of ACE.

EVENTS TOOL

The events tool view contains a list of errors, warnings, and information messages generated within the application software.

EVALUATION BOARD SCHEMATICS AND ARTWORK

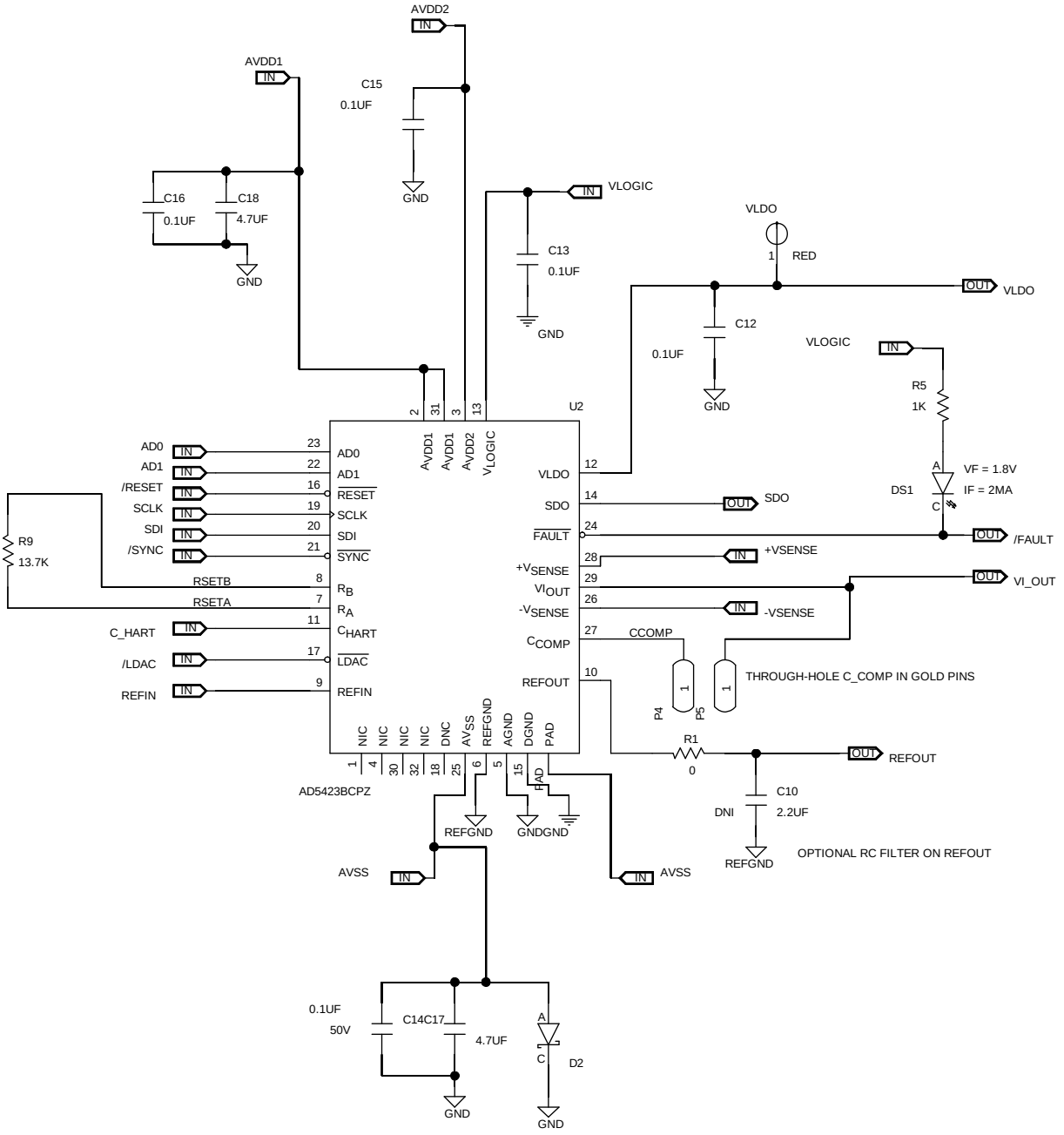

Figure 15. AD5423 Device Schematic

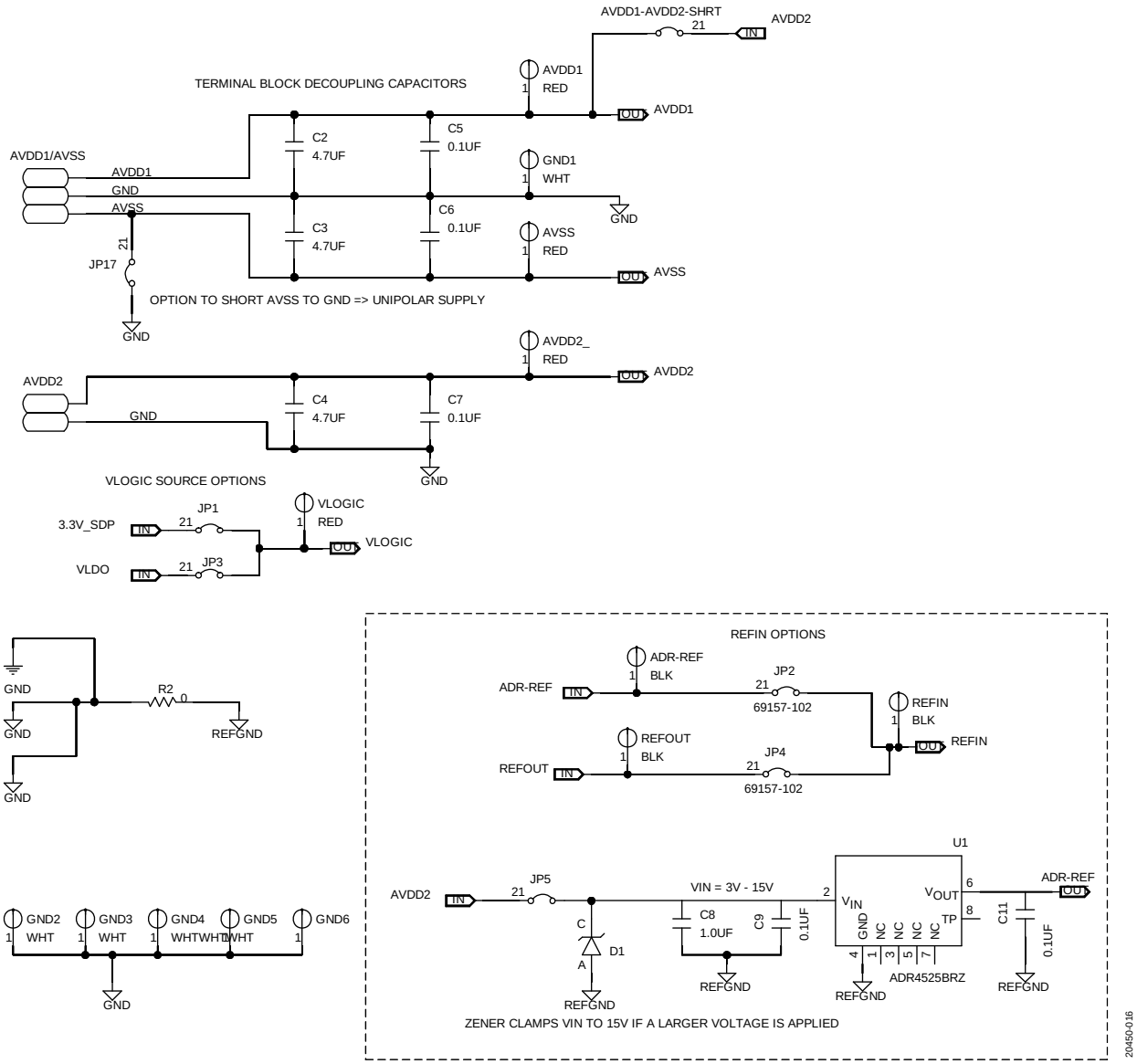

Figure 16. AD5423 Supplies and Reference Options

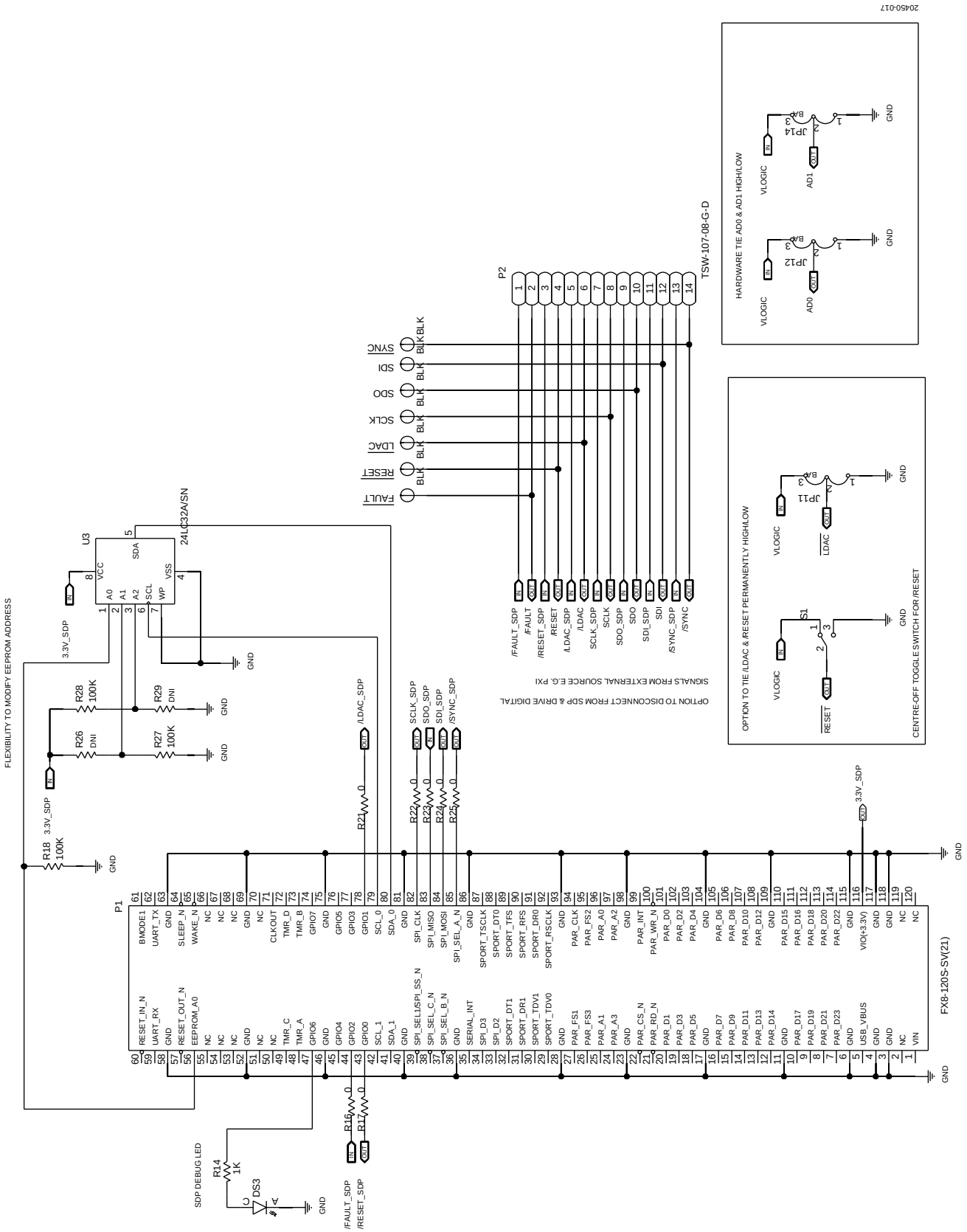

Figure 17. SDP-S Board Connections, Address Pins, $\overline{LDAC}$ and $\overline{RESET}$ Pins

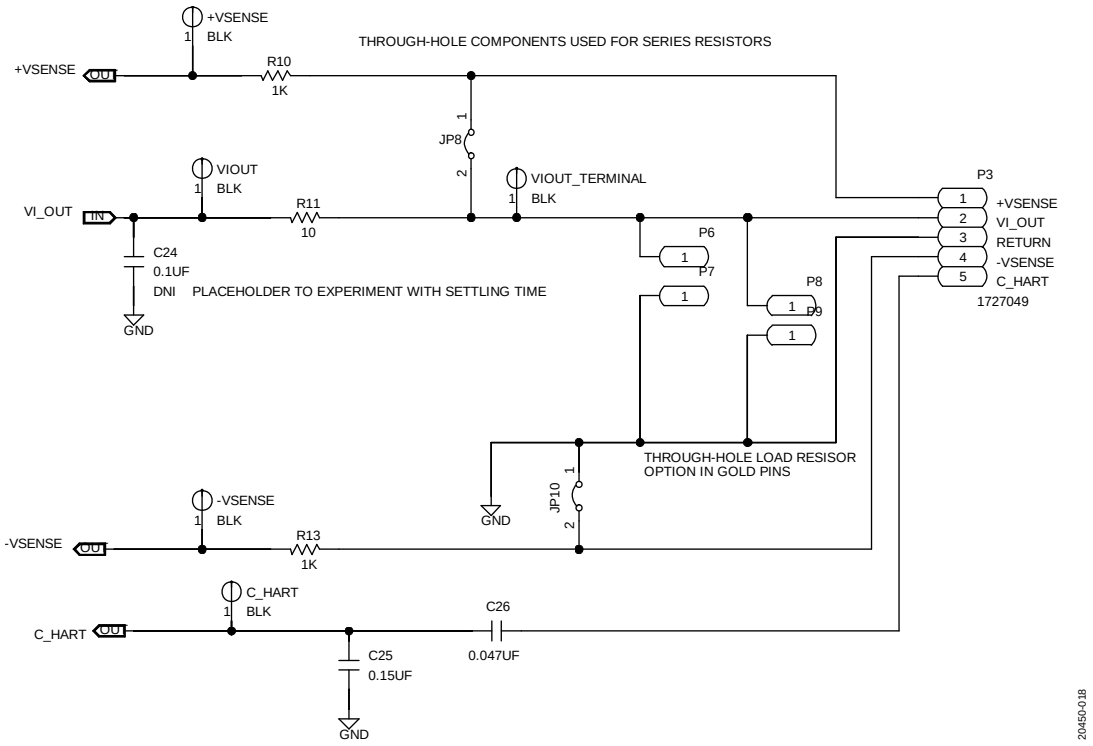

Figure 18. AD5423 Output Stage

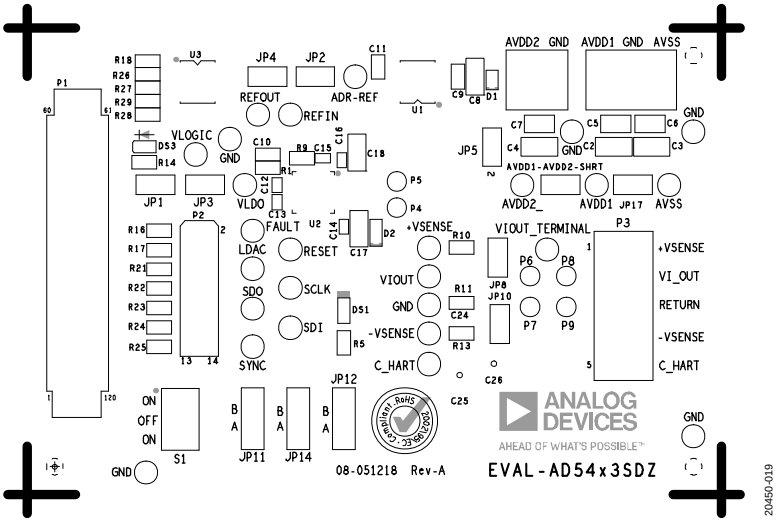

Figure 19. EVAL-AD5423SDZ Silkscreen, Primary

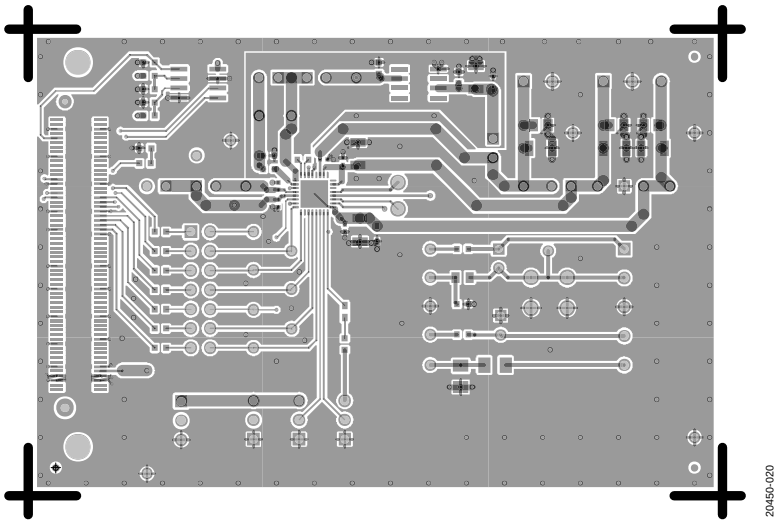

Figure 20. EVAL-AD5423SDZ Layer 1, Primary

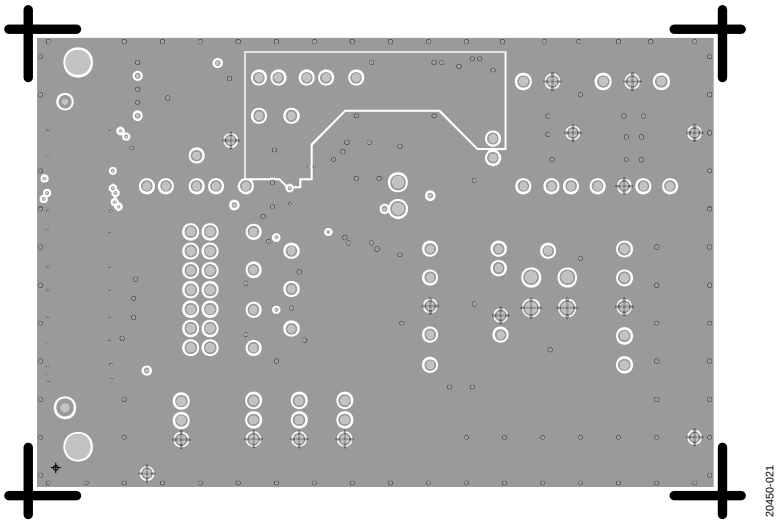

Figure 21. EVAL-AD5423SDZ Layer 2 and Layer 3

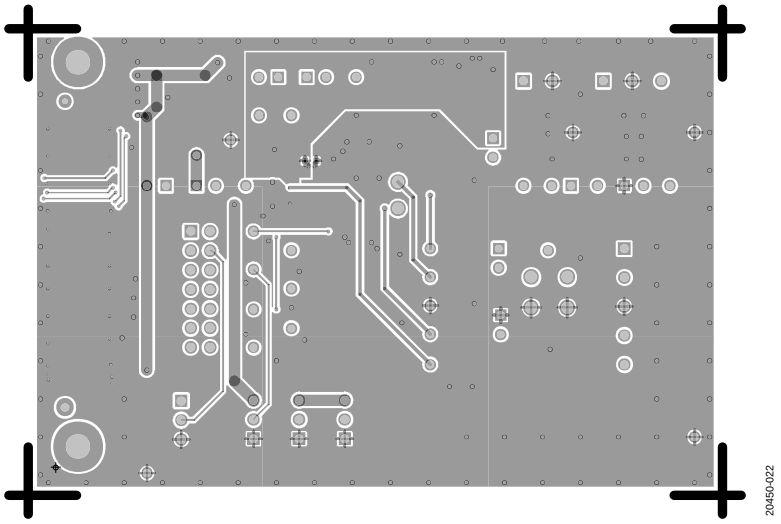

Figure 22. EVAL-AD5423SDZ Layer 4, Secondary

ORDERING INFORMATION

BILL OF MATERIALS

Table 5. Bill of Materials

Reference Designator	Description	Manufacturer	Part Number
+VSENSE, −VSENSE, ADR-REF, C_HART, FAULT, LDAC, REFIN, REFOUT, RESET, SCLK, SDI, SDO, SYNC, VIOUT, VIOUT_TERMINAL	Connectors, printed circuit board (PCB), test, point black	Vero Technologies	20-2137
AVDD1, AVDD2, AVSS, VLDO, VLOGIC	Connectors, PCB, test, point red	Keystone Electronics	5000
AVDD1-AVDD2-SHRT, JP1, JP2, JP3, JP4, JP5, JP8, JP10, JP17	Connectors, PCB, jumper, male, 2-pin,1X M000385	Amphenol FCI	69157-102
AVDD1 and AVSS	Connectors, PCB terminal block, 3-position	Phoenix Contact	1727023
AVDD2	Connector, PCB terminal block, 2-position, green	Phoenix Contact	1727010
C9, C11	Ceramic capacitors, 0603, X7R	KEMET	C0603C104K4RAC
C12, C13, C14, C15, C16	Ceramic capacitors, X7R	TDK	CGA2B3X7R1H104K050BB
C2, C3, C4, C17, C18	Ceramic capacitors, X7R, general-purpose	Murata	GRM31CR71H475KA12L
C25	Ceramic capacitor, X7R, 1206	AVX	12065C154KAT2A
C26	Ceramic capacitor, X7R, 1206	AVX	12065C473JAT2A
C5, C6, C7	Ceramic capacitors, X7R	AVX	08055C104JAT2A
C8	Ceramic capacitor, X7R, general-purpose	Yageo	CC1206KKX7R9BB105
C10	Ceramic capacitor, X7R	Murata	GCM188R70J225KE22D
C24	Ceramic capacitor 0603 X7R	KEMET	C0603C104K4RAC
D1	Diode, Zener, voltage regulator	NXP Semiconductors	BZX585-C15
D2	Diode, Schottky, small signal	ST Microelectronics	BAT54KFILM
DS1	LED, surface mount diode (SMD), 0603, red	Vishay	TLMS1000-GS08
DS3	LED, SMD, 0603, green	Lumex	SML-LX0603GW-TR
GND1, GND2, GND3, GND4, GND5, GND6	Connectors, PCB, test point, white	Keystone Electronics	5002
JP11, JP12, JP14	Connectors, PCB, 3-position male header, unshrouded, single-row, 2.54 mm pitch, 3 mm solder tail	Harwin	M20-9990345
P1	Connector, PCB, vertical type for SDP breakout board	HRS	FX8-120S-SV(21)
P2	Connector, PCB header, male, 14-position	Samtec	TSW-107-08-G-D
P3	Connector, PCB, terminal block, 5-position, green	Phoenix Contact	1727049
P4, P5, P6, P7, P8, P9	Connectors, PCB, pin socket	Vero Technologies	66-3472
R1, R2, R16, R17, R21, R22, R23, R24, R25	Resistor films, SMD, 0603	Multicomp (SPC)	MC0603WG00000T5E-TC
R10, R13	Thick film, chip, resistors	Multicomp (SPC)	MC0063W060311K
R11	Thick film, chip, precision resistor	Panasonic	ERJ-6ENF10R0V
R5, R14	Thick film, chip, resistors	Vishay	CRCW06031K00FKEAHP
R18, R27, R28	Thick film, chip, resistors	Multicomp (SPC)	MC 0.063W 0603 1% 100K
R9	Thin film, chip, resistor	TE Connectivity	RN73C1J13K7BTG
R26, R29	Thick film chip resistors	Multicomp (SPC)	MC 0.063W 0603 1% 100K
S1	Switch, tiny, washable toggle switches	Apem Components	TL39P0050
U1	Analog Devices, IC, ultralow noise, high accuracy voltage reference	Analog Devices	ADR4525BRZ
U2	Analog Devices, IC, single channel, 16-bit current or voltage output DAC with highway addressable remote transducer (HART) connectivity	Analog Devices	AD5423BCPZ-RL7
U3	IC, 32-kb serial EEPROM	Microchip Technology	24LC32A/SN

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions
By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NONINFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS ($100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.

©2019 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
UG20450-0-5/19(0)

www.analog.com