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NTE74HC151
Integrated Circuit
TTL – High Speed CMOS,
8–Channel Digital Multiplexer

Description:

The NTE74HC151 is a high speed Digital multiplexer in a 16–Lead DIP type package that utilizes advanced silicon–gate CMOS technology. Along with high noise immunity and low power dissipation of standard CMOS integrated circuits, it possesses the ability to drive 10 LS–TTL loads. The NTE74HC151 selects one of the 8 data sources, depending on the address presented on the A, B, and C inputs. It features both true (Y) and complement (W) outputs. The STROBE input must be at a low logic level to enable th multiplexer. A high logic level at the STROBE forces the W output HIGH and the Y output LOW.

The 74HC logic family is functionally, as well as pinout compatible, with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and GND.

Features:

- Typical Propagation Delay Data Select to Output Y: 26ns
- Wide Operatin Supply Voltage Range: 2V to 6V
- Low Input Current: 1μA (max)
- Low Quiescent Supply Current: 80μA (max)
- High Ooutput Drive Current: 4mA (max)

Absolute Maximum Ratings: (Note 1, Note 2)

Supply Voltage, V_{CC} . . . . . –0.5 to +7.0V
DC Input Voltage, V_{IN} . . . . . –1.5 to V_{CC} +1.5V
DC Output Voltage, V_{OUT} . . . . . –0.5 to V_{CC} + 0.5V
Clamp Diode Current, I_{IK}, I_{OK} . . . . . ±20mA
DC Output Current (Per Pin), I_{OUT} . . . . . ±25mA
DC V_{CC} or GND Current (Per Pin), I_{CC} . . . . . ±50mA
Power Dissipation (Note 3), P_D 500mW
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C
Lead Temperature (During Soldering, 10sec), T_L . . . . . +260°C

Note 1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Note 2. Unless otherwise specified, all voltages are referenced to GND.
Note 3. Power Dissipation temperature derating: 12mW/°C from +65°C to +85°C.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.0	–	6.0	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	–	V_{CC}	V
Operating Temperature Range	T_A	–40	–	+85	°C
Input Rise or Fall Times V_{CC} = 2.0V	t_r, t_f	–	–	1000	ns
V_{CC} = 4.5V		–	–	500	ns
V_{CC} = 6.0V		–	–	400	ns

DC Electrical Characteristics: (V_{CC} = 5V ±10% unless otherwise specified)

Parameter	Symbol	Test Conditions	V_{CC}	T_A = +25°C	T_A = –40° to +85°C		Unit
				Typ	Guaranteed Limits		
Minimum High Level Input Voltage	V_{IH}		2.0	–	1.5	1.5	V
			4.5	–	3.15	3.15	V
			6.0	–	4.2	4.2	V
Maximum Low Level Input Voltage	V_{IL}		2.0	–	0.5	0.5	V
			4.5	–	1.35	1.35	V
			6.0	–	1.8	1.8	V
Minimum High Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\| \le 20\mu A$	2.0	2.0	1.9	1.9	V
			4.5	4.5	4.4	4.4	V
			6.0	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\| \le 4.0mA$	4.5	4.2	3.98	3.84	V
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\| \le 5.2mA$	6.0	5.7	5.48	5.34	V
Maximum Low Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\| \le 20\mu A$	2.0	0	0.1	0.1	V
			4.5	0	0.1	0.1	V
			6.0	0	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\| \le 4.0mA$	4.5	0.2	0.26	0.33	V
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\| \le 5.2mA$	6.0	0.2	0.26	0.33	V
Maximum Input Current	I_{IN}	V_{IN} = V_{CC} or GND	6.0	–	±0.1	±1.0	µA
Maximum Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0µA	6.0	–	8	80	µA

AC Electrical Characteristics: (V_{CC} = 5V, t_r = t_f = 6ns, C_L = 15pF, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Typ	Guaranteed Limits	Unit
Maximum Propagation Delay (A, B or C to Y)	t_{PHL}, t_{PLH}		26	35	ns
Maximum Propagation Delay (A, B or C to W)	t_{PHL}, t_{PLH}		27	35	ns
Maximum Propagation Delay (Any D to Y)	t_{PHL}, t_{PLH}		22	29	ns
Maximum Propagation Delay (Any D to W)	t_{PHL}, t_{PLH}		24	32	ns
Maximum Propagation Delay (Strobe to Y)	t_{PHL}, t_{PLH}		17	23	ns
Maximum Propagation Delay (Strobe to W)	t_{PHL}, t_{PLH}		16	21	ns

AC Electrical Characteristics: (V_{CC} = 5V ±10%, $t_r = t_f$ = 6ns, C_L = 50pF unless otherwise specified)

Parameter	Symbol	Test Conditions	V_{CC}	T_A = +25°C	T_A = −40° to +85°C		Unit
				Typ	Guaranteed Limits		
Maximum Propagation Delay (A, B or C to Y)	t_{PHL}, t_{PLH}		2.0	90	205	256	ns
			4.5	31	41	51	ns
			6.0	26	35	44	ns
Maximum Propagation Delay (A, B or C to W)	t_{PHL}, t_{PLH}		2.0	95	205	256	ns
			4.5	32	41	51	ns
			6.0	27	35	44	ns
Maximum Propagation Delay (Any D to Y)	t_{PHL}, t_{PLH}		2.0	70	195	244	ns
			4.5	27	39	49	ns
			6.0	23	33	41	ns
Maximum Propagation Delay (Any D to W)	t_{PHL}, t_{PLH}		2.0	75	185	231	ns
			4.5	29	37	46	ns
			6.0	25	32	40	ns
Maximum Propagation Delay (Strobe to Y)	t_{PHL}, t_{PLH}		2.0	50	140	175	ns
			4.5	21	28	35	ns
			6.0	18	24	30	ns
Maximum Propagation Delay (Strobe to W)	t_{PHL}, t_{PLH}		2.0	45	127	159	ns
			4.5	20	25	32	ns
			6.0	17	22	28	ns
Maximum Output Rise and Fall Time	t_{TLH}, t_{THL}		2.0	30	75	95	ns
			4.5	8	15	19	ns
			6.0	7	13	16	ns
Power Dissipation Capacitance	C_{PD}	Per Package, Note 4	–	110	–	–	pF
Maximum Input Capacitance	C_{IN}		–	5	10	10	pF

Note 4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Truth Table:

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = HIGH Level
L = LOW Level
X = Don't Care
D0, D1 . . . D7 = the level of the respective D input

Pin Connection Diagram