

VR5500

High voltage PMIC with multiple SMPS and LDO

Rev. 6 — 29 January 2020

Product data sheet

1 General description

The VR5500 is an automotive high-voltage multi-output power supply integrated circuit, with focus on Radio, V2X, and Infotainment applications. It includes multiple switch mode and linear voltage regulators. It offers external frequency synchronization input and output, for optimized system EMC performance and it is qualified in compliance with AEC-Q100 rev H (Grade1, MSL3).

Several device versions are available, offering choice in number of output rails, output voltage setting, operating frequency, and power up sequencing, to address multiple applications.

2 Features and benefits

- 60 V DC maximum input voltage for 12 V and 24 V applications
- VPRE synchronous buck controller with external MOSFETs. Configurable output voltage, switching frequency, and current capability up to 10 A peak.
- Low voltage integrated synchronous BUCK1 converter, dedicated to MCU core supply with SVS capability. Configurable output voltage and current capability up to 3.6 A peak.
- Low voltage integrated synchronous BUCK2 converter. Configurable output voltage and current capability up to 3.6 A peak. Multi-phase capability with BUCK1 to extend the current capability up to 7.2 A peak on a single rail. Static voltage scaling capability.
- Low voltage integrated synchronous BUCK3 converter. Configurable output voltage and current capability up to 3.6 A peak.
- BOOST converter with integrated low-side switch. Configurable output voltage and max input current up to 1.5 A peak.
- EMC optimization techniques including SMPS frequency synchronization, spread spectrum, slew rate control, manual frequency tuning
- Two linear voltage regulators for MCU IOs and ADC supply, external physical layer. Configurable output voltage and current capability up to 400 mA DC.
- OFF mode with very low sleep current (10 μ A typ)
- Two input pins for wake-up detection and battery voltage sensing
- Device control via I2C interface with CRC
- Power synchronization pin to operate two VR5500 devices or VR5500 plus an external PMIC
- Three voltage monitoring circuits, dedicated interface for MCU monitoring, power good, reset, and interrupt outputs
- Configuration by OTP programming. Prototype enablement to support custom setting during project development in engineering mode.



3 Simplified application diagram

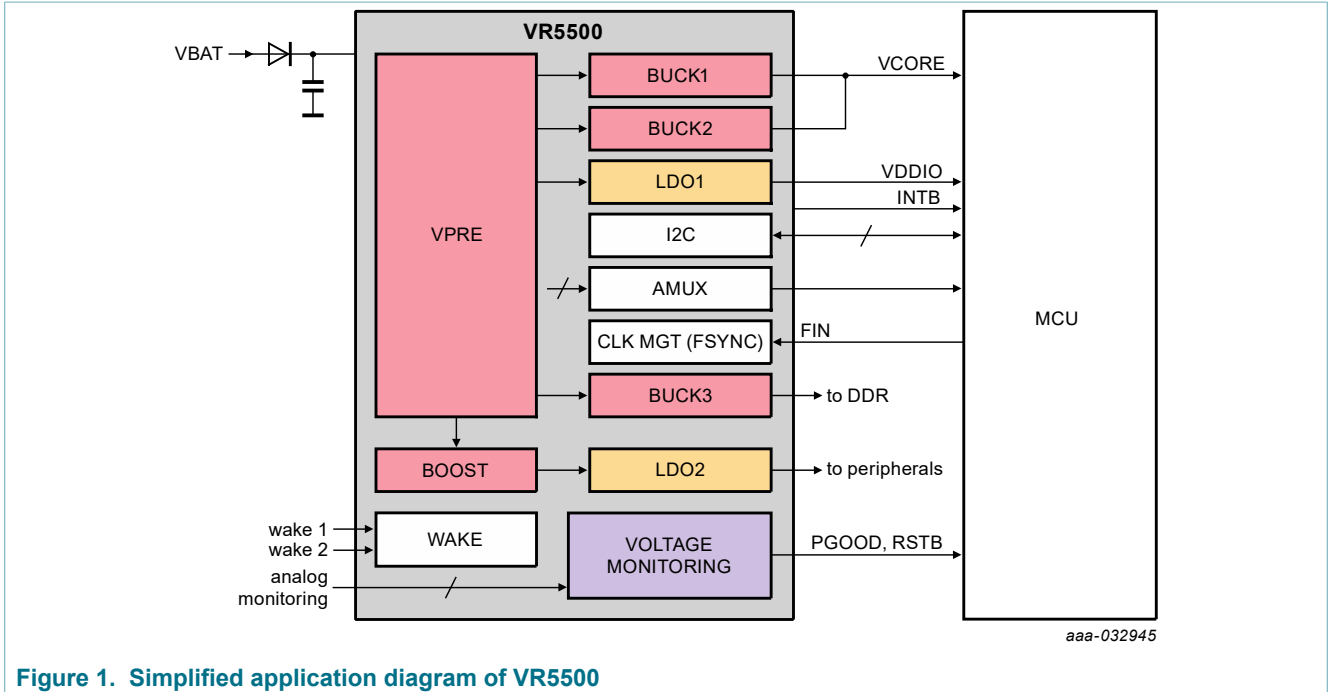


Figure 1. Simplified application diagram of VR5500

4 Ordering information

Table 1. Ordering information

| Part number ^[1] | Package | | | OTP ID |
|-------------------------------|---------|--|-----------|---|
| | Name | Description | Version | |
| MC33VR5500V0ES ^[2] | HPQFN56 | HPQFN56, plastic, thermally enhanced very thin quad flat package, no lead, wettable flanks | SOT684-23 | — |
| MC33VR5500V1ES ^[3] | | | | http://www.nxp.com/MC33VR5500V1ES-OTP-Report |

[1] To order parts in tape and reel, add the R2 suffix to the part number.
 [2] V0: Non-programmed part
 [3] V1: Radio mercury reference design

V0 part is a non-programmed OTP configuration. Pre-programmed OTP configurations (other than BUCK regulators) are managed through suffix V1 to XZ.

5 Applications

- Radio
- V2x
- Infotainment

6 Block diagram

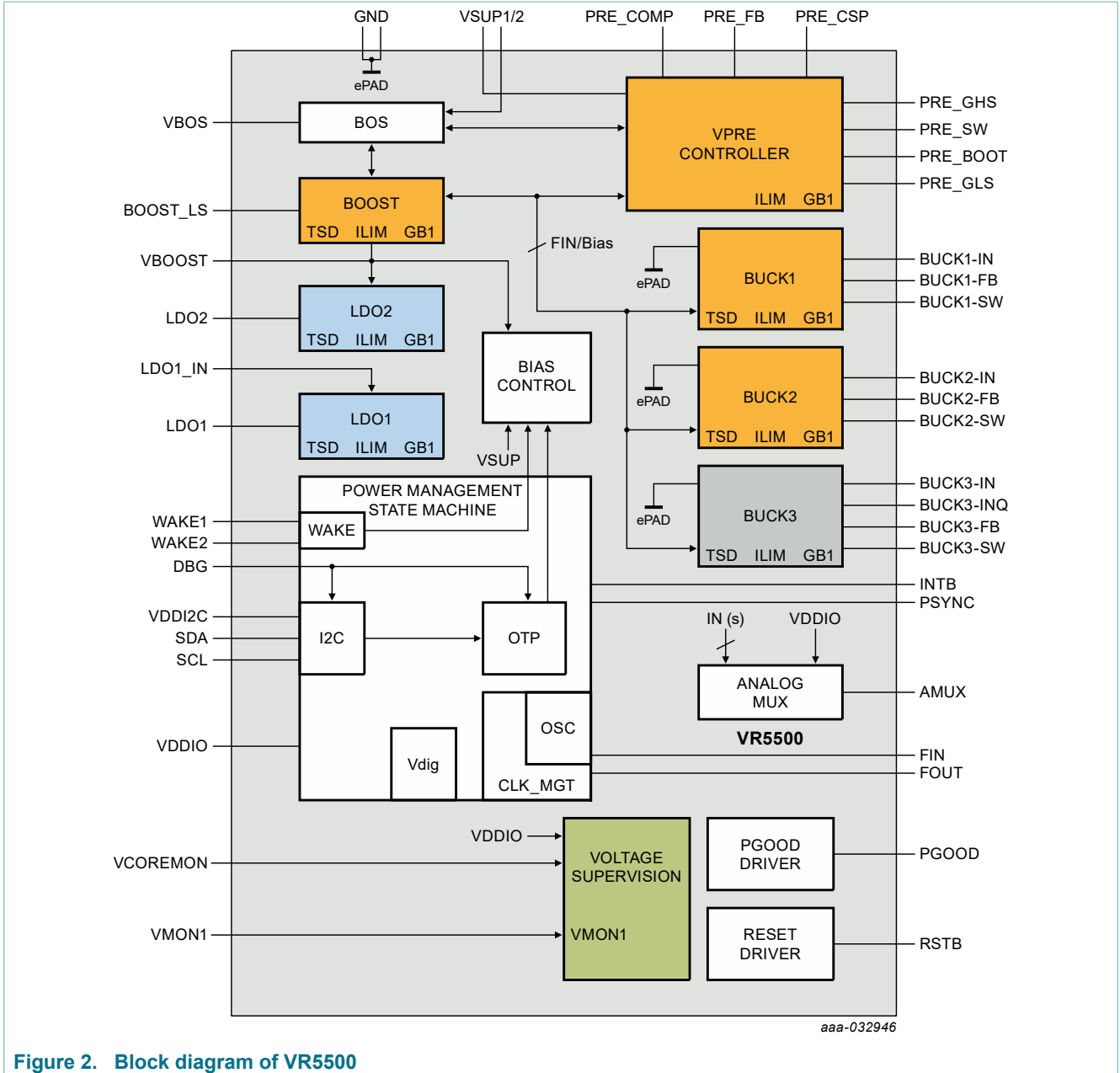


Figure 2. Block diagram of VR5500

7 Pinning information

7.1 Pinning

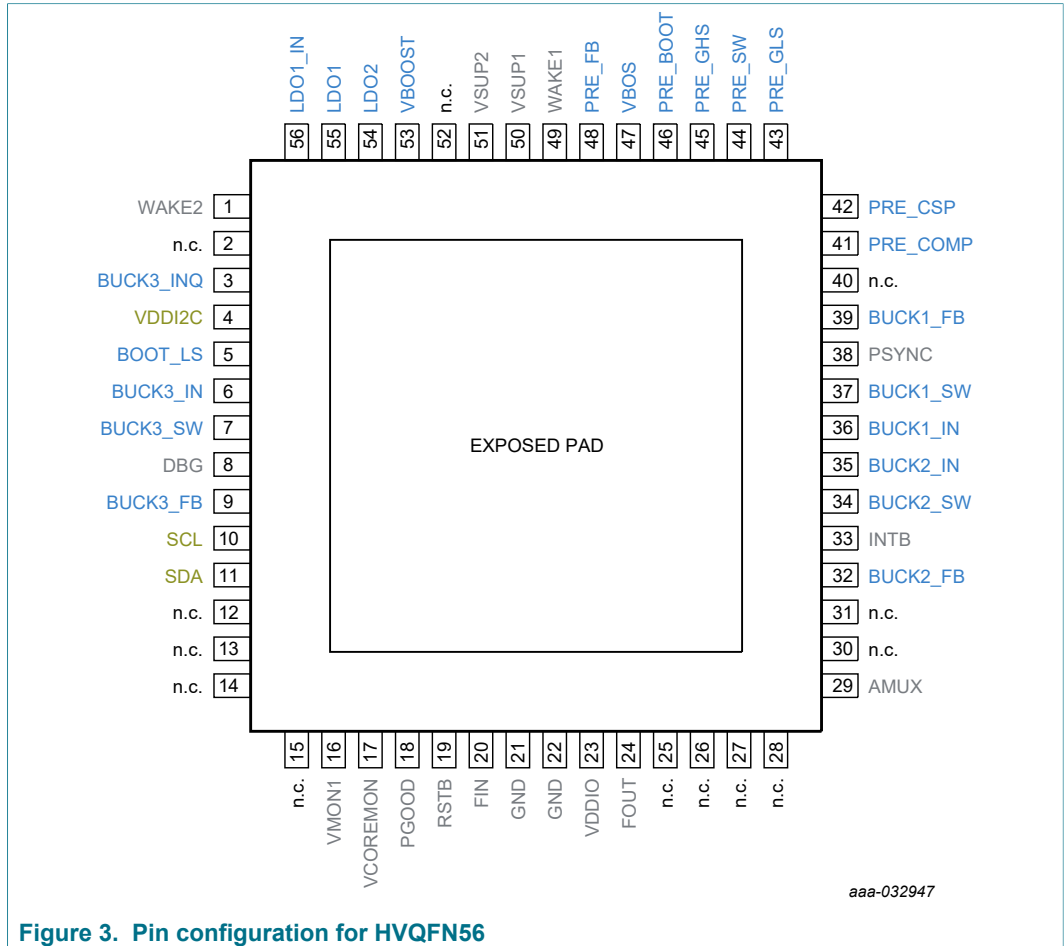


Figure 3. Pin configuration for HVQFN56

7.2 Pin description

See [Section 8](#) for connection of unused pins.

Table 2. Pin description

| Symbol | Pin | Type | Description |
|-----------|-----|-------------|---|
| WAKE2 | 1 | A_IN / D_IN | Wake-up input 2 An external serial resistor is required if WAKE2 is a global pin |
| n.c. | 2 | n.c. | Not connected pin |
| BUCK3_INQ | 3 | A_IN | Low voltage Buck3 quiet input voltage |
| VDDI2C | 4 | A_IN | Input voltage for I2C buffers |
| BOOST_LS | 5 | A_IN | Boost low-side drain of internal MOSFET |
| BUCK3_IN | 6 | A_IN | Low voltage Buck3 input voltage |
| BUCK3_SW | 7 | A_OUT | Low voltage Buck3 switching node |
| DBG | 8 | A_IN | Debug mode entry |
| BUCK3_FB | 9 | A_IN | Low voltage Buck3 voltage feedback |

| Symbol | Pin | Type | Description |
|----------|-----|----------|---|
| SCL | 10 | D_IN | I2C-bus Clock input |
| SDA | 11 | D_IN/OUT | I2C-bus Bidirectional data line |
| n.c. | 12 | n.c. | Not connected pin |
| n.c. | 13 | n.c. | Not connected pin |
| n.c. | 14 | n.c. | Not connected pin |
| n.c. | 15 | n.c. | Not connected pin |
| VMON1 | 16 | A_IN | Voltage monitoring input 1 |
| VCOREMON | 17 | A_IN | VCORE monitoring input: Must be connected to Buck1 output voltage |
| PGOOD | 18 | D_OUT | Power good output Active low Pull up to VDDIO mandatory |
| RSTB | 19 | D_OUT | Reset output Active low The main function is to reset the MCU. Reset input voltage is monitored to detect external reset and fault condition. Pull up to VDDIO mandatory |
| FIN | 20 | D_IN | Frequency synchronization input |
| GND | 21 | GND | Ground |
| GND | 22 | GND | Ground |
| VDDIO | 23 | A_IN | Input voltage FOUT and AMUX buffers Allow voltage compatibility with MCU I/Os |
| FOUT | 24 | D_OUT | Frequency synchronization output |
| n.c. | 25 | n.c. | Not connected pin |
| n.c. | 26 | n.c. | Not connected pin |
| n.c. | 27 | GND | External pull down to GND |
| n.c. | 28 | n.c. | Not connected pin |
| AMUX | 29 | A_OUT | Multiplexed output to connect to MCU ADC Selection of the analog parameter through I2C |
| n.c. | 30 | n.c. | Not connected pin |
| n.c. | 31 | n.c. | Not connected pin |
| BUCK2_FB | 32 | A_IN | Low voltage Buck2 voltage feedback |
| INTB | 33 | D_OUT | Interrupt output |
| BUCK2_SW | 34 | A_OUT | Low voltage Buck2 switching node |
| BUCK2_IN | 35 | A_IN | Low voltage Buck2 input voltage |
| BUCK1_IN | 36 | A_IN | Low voltage Buck1 input voltage |
| BUCK1_SW | 37 | A_OUT | Low voltage Buck1 switching node |
| PSYNC | 38 | D_IN/OUT | Power synchronization input/output |
| BUCK1_FB | 39 | A_IN | Low voltage Buck1 voltage feedback |
| n.c. | 40 | GND | External pull down to GND |
| PRE_COMP | 41 | A_IN | VPRE compensation network |
| PRE_CSP | 42 | A_IN | VPRE positive current sense input |

| Symbol | Pin | Type | Description |
|----------|-----|-------------|--|
| PRE_GLS | 43 | A_OUT | VPRE low-side gate driver for external MOSFET |
| PRE_SW | 44 | A_OUT | VPRE switching node |
| PRE_GHS | 45 | A_OUT | VPRE high-side gate driver for external MOSFET |
| PRE_BOOT | 46 | A_IN/OUT | VPRE bootstrap capacitor |
| VBOS | 47 | A_OUT | Best of supply output voltage |
| PRE_FB | 48 | A_IN | VPRE voltage feedback and negative current sense input |
| WAKE1 | 49 | A_IN / D_IN | Wake up input 1 An external serial resistor is required if WAKE1 is a global pin |
| VSUP1 | 50 | A_IN | Power supply 1 of the device An external reverse battery protection diode in series is mandatory |
| VSUP2 | 51 | A_IN | Power supply 2 of the device An external reverse battery protection diode in series is mandatory |
| n.c. | 52 | n.c. | Not connected pin |
| VBOOST | 53 | A_IN | VBOOST voltage feedback |
| LDO2 | 54 | A_OUT | Linear regulator 2 output voltage |
| LDO1 | 55 | A_OUT | Linear regulator 1 output voltage |
| LDO1_IN | 56 | A_IN | Linear regulator 1 input voltage |
| EP | 57 | GND | Exposed pad (BUCK1, BUCK2 and BUCK3 low-side GNDs are connected to the expose pad) Must be connected to GND |

8 Connection of unused pins

Table 3. Connection of unused pins

| Pin | Name | Type | Connection if not used |
|-----|-----------|-------------|---|
| 1 | WAKE2 | A_IN / D_IN | External pull down to GND |
| 2 | n.c. | n.c. | Open |
| 3 | BUCK3_INQ | A_IN | Open |
| 4 | VDDI2C | A_IN | Open |
| 5 | BOOST_LS | A_IN | See Section 21.5 "VBOOST not populated" |
| 6 | BUCK3_IN | A_IN | Open |
| 7 | BUCK3_SW | A_OUT | Open |
| 8 | DBG | A_IN | Connection mandatory |
| 9 | BUCK3_FB | A_IN | Open – 1.5 MΩ internal resistor bridge pull down to GND |
| 10 | SCL | D_IN | External pull down to GND |
| 11 | SDA | D_IN/OUT | External pull down to GND |
| 12 | n.c. | n.c. | Open |
| 13 | n.c. | n.c. | Open |
| 14 | n.c. | n.c. | Open |
| 15 | n.c. | n.c. | Open |
| 16 | VMON1 | A_IN | Open – 2 MΩ internal pull down to GND, OTP_VMON1_EN=0 |

| Pin | Name | Type | Connection if not used |
|-----|----------|-------------|---|
| 17 | VCOREMON | A_IN | Connection mandatory |
| 18 | PGOOD | D_OUT | Connection mandatory |
| 19 | RSTB | D_OUT | Connection mandatory |
| 20 | FIN | D_IN | External pull down to GND |
| 21 | GND | GND | Connection mandatory |
| 22 | GND | GND | Connection mandatory |
| 23 | VDDIO | A_IN | Connection mandatory |
| 24 | FOUT | D_OUT | Open – push pull structure |
| 25 | n.c. | n.c. | Open |
| 26 | n.c. | n.c. | Open |
| 27 | n.c. | GND | External pull down to GND |
| 28 | n.c. | n.c. | Open |
| 29 | AMUX | A_OUT | Open |
| 30 | n.c. | n.c. | Open |
| 31 | n.c. | n.c. | Open |
| 32 | BUCK2_FB | A_IN | Open – 1.5 MΩ Internal resistor bridge pull down to GND |
| 33 | INTB | D_OUT | Open – 10 kΩ internal pull up to VDDIO |
| 34 | BUCK2_SW | A_OUT | Open |
| 35 | BUCK2_IN | A_IN | Open |
| 36 | BUCK1_IN | A_IN | Connection mandatory |
| 37 | BUCK1_SW | A_OUT | Connection mandatory |
| 38 | PSYNC | D_IN/OUT | External pull up to VBOS |
| 39 | BUCK1_FB | A_IN | Connection mandatory |
| 40 | n.c. | n.c. | External pull down to GND |
| 41 | PRE_COMP | A_IN | See Section 20.7 "VPRE not populated" |
| 42 | PRE_CSP | A_IN | See Section 20.7 "VPRE not populated" |
| 43 | PRE_GLS | A_OUT | See Section 20.7 "VPRE not populated" |
| 44 | PRE_SW | A_OUT | See Section 20.7 "VPRE not populated" |
| 45 | PRE_GHS | A_OUT | See Section 20.7 "VPRE not populated" |
| 46 | PRE_BOOT | A_IN/OUT | See Section 20.7 "VPRE not populated" |
| 47 | VBOS | A_OUT | Connection mandatory |
| 48 | PRE_FB | A_IN | See Section 20.7 "VPRE not populated" |
| 49 | WAKE1 | A_IN / D_IN | External pull down to GND |
| 50 | VSUP1 | A_IN | Connection mandatory |
| 51 | VSUP2 | A_IN | Connection mandatory |
| 52 | n.c. | n.c. | Open |
| 53 | VBOOST | A_OUT | See Section 21.5 "VBOOST not populated" |
| 54 | LDO2 | A_OUT | Open – power sequence slot 7, OTP_LDO1S[2:0] = '111' |
| 55 | LDO1 | A_OUT | Open – power sequence slot 7, OTP_LDO2S[2:0] = '111' |
| 56 | LDO1_IN | A_IN | Open |
| 57 | EP | GND | Connection mandatory |

9 Maximum ratings

Table 4. Maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-------------------|-------------------------------|--|------|------|------|
| Voltage ratings | | | | | |
| VSUP1/2 | DC voltage | power supply VSUP1,2 pins | -0.3 | 60 | V |
| WAKE1/2 | DC voltage | WAKE1,2 pins; external serial resistor mandatory | -1.0 | 60 | V |
| PRE_SW | DC voltage | PRE_SW pin | -2.0 | 60 | V |
| VMON1, VCOREMON | DC voltage | VMON1, VCOREMON pins | -0.3 | 60 | V |
| PRE_GHS, PRE_BOOT | DC voltage | PRE_GHS, PRE_BOOT pins | -0.3 | 65.5 | V |
| DBG | DC voltage | DBG pin | -0.3 | 10 | V |
| BOOST_LS | DC voltage | BOOST_LS pin | -0.3 | 8.5 | V |
| VBOOST, LDO1_IN | DC voltage | VBOOST, LDO1_IN pins | -0.3 | 6.5 | V |
| BUCKx_IN | DC voltage | BUCK1_IN, BUCK2_IN, BUCK3_IN, BUCK3_INQ | -1.0 | 5.5 | V |
| BUCKx_IN | Transient voltage < 3 μ s | BUCK1_IN, BUCK2_IN, BUCK3_IN, BUCK3_INQ | -1.0 | 6.5 | V |
| BUCKx_SW | Transient voltage < 20 ns | BUCK1_SW, BUCK2_SW, BUCK3_SW | -2.0 | 6.5 | V |
| All other pins | DC voltage | at all other pins | -0.3 | 5.5 | V |
| Current ratings | | | | | |
| I_WAKE | Maximum current capability | WAKE1,2 | -5.0 | 5.0 | mA |
| I_SUP | Maximum current capability | VSUP1,2 | -5.0 | — | mA |

10 Electrostatic discharge

10.1 Human body model (JESD22/A114)

The device is protected up to ± 2 kV, according to the human body model standard with 100 pF and 1.5 k Ω . This protection is ensured at all pins.

10.2 Charged device model

The device is protected up to ± 500 V, according to the AEC-Q100 - 011 charged device model standard. This protection is ensured at all pins.

10.3 Discharged contact test

The device is protected up to ± 8 kV, according to the following discharged contact tests.

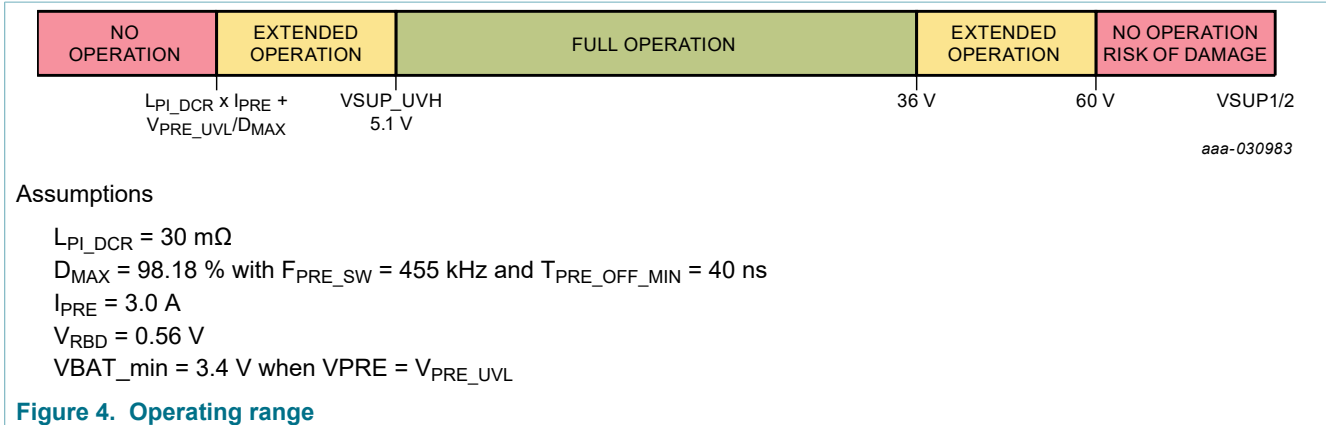
Discharged contact test (IEC61000-4-2) at 150 pF and 330 Ω

Discharged contact test (ISO10605.2008) at 150 pF and 2 k Ω

Discharged contact test (ISO10605.2008) at 330 pF and 2 k Ω

This protection is ensured at VSUP1, VSUP2, WAKE1, WAKE2 pins.

11 Operating range



- Below VSUP_UVH threshold, the extended operation range depends on VPRE output voltage configuration and external components.
 - When VPRE is configured at 5.0 V, VPRE may not remain in its regulation range
 - VSUP minimum voltage depends on external components (L_{PI_DCR}) and application conditions (I_{PRE} , F_{PRE_SW})
- The VR5500 maximum continuous operating voltage is 36 V when VPRE is switching at 455 kHz. It has been validated at 48 V for limited duration of 15 minutes at room temperature to satisfy the jump-start requirement of 24 V applications. It can sustain 58 V load dump without external protection.
- When VPRE is switching at 2.2 MHz, the VR5500 maximum continuous operating voltage is 18 V. It is validated at 26 V for limited duration of 2 minutes at room temperature to satisfy the jump-start requirement of 12 V applications and 35 V load dump.

12 Thermal ratings

Table 5. Thermal ratings

| Symbol | Parameter | Conditions | Min | Max | Unit |
|----------------------|--|---|-----|-----|------|
| $R_{\theta JA}$ | Thermal resistance junction to ambient | 2s2p circuit board [1] | — | 31 | °C/W |
| $R_{\theta JA}$ | Thermal resistance junction to ambient | 2s6p circuit board [1] | — | 23 | °C/W |
| $R_{\theta JB}$ | Thermal resistance junction to board | 2s2p circuit board [1] | — | 15 | °C/W |
| $R_{\theta JB}$ | Thermal resistance junction to board | 2s6p circuit board [1] | — | 10 | °C/W |
| $R_{\theta JC_BOT}$ | Thermal resistance junction to case bottom | between the die and the solder pad on the bottom of the package [1] | — | 1 | °C/W |
| $R_{\theta JP_TOP}$ | Thermal resistance junction to package top | between package top and the junction temperature [1] | — | 3 | °C/W |
| T_A | Ambient temperature (Grade 1) | | -40 | 125 | °C |
| T_J | Junction temperature (Grade 1) | | -40 | 150 | °C |
| T_{STG} | Storage temperature | | -55 | 150 | °C |

[1] per JEDEC JESD51-2 and JESD51-8

13 Characteristics

Table 6. Electrical characteristics

$T_A = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$, unless otherwise specified. $V_{SUP} = V_{SUP_UVH}$ to 36 V , unless otherwise specified. All voltages referenced to ground.

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------------------|--|-----|-----|-----|---------------|
| Power supply | | | | | |
| I_{SUP_NORMAL} | Current in Normal mode, all regulators ON ($I_{OUT} = 0$) | — | 15 | 25 | mA |
| $I_{SUP_STANDBY}$ | Current in Standby mode, all regulators OFF except VBOS | — | 5 | 10 | mA |
| I_{SUP_OFF1} | Current in OFF mode (power down), $T_A < 85\text{ }^\circ\text{C}$ | — | 10 | 15 | μA |
| I_{SUP_OFF2} | Current in OFF mode (power down), $T_A = 125\text{ }^\circ\text{C}$ | — | — | 25 | μA |
| V_{SUP_UV7} | VSUP undervoltage threshold (7.0 V) | 7.2 | 7.5 | 7.8 | V |
| V_{SUP_UVH} | VSUP undervoltage threshold high (during power-up and V_{sup} rising) OTP_VSUP_CFG = 0 | 4.7 | — | 5.1 | V |
| | VSUP undervoltage threshold high (during power-up and V_{sup} rising) OTP_VSUP_CFG = 1 | 6.0 | — | 6.4 | V |
| V_{SUP_UVL} | VSUP undervoltage threshold low (during power-up and V_{sup} falling) OTP_VSUP_CFG = 0 | 4.0 | — | 4.4 | V |
| | VSUP undervoltage threshold low (during power-up and V_{sup} falling) OTP_VSUP_CFG = 1 | 5.3 | — | 5.7 | V |
| T_{SUP_UV} | V_{SUP_UV7} , V_{SUP_UVH} , and V_{SUP_UVL} filtering time | 6.0 | 10 | 15 | μs |

14 Functional description

The VR5500 device has two independent logic blocks. The main state machine manages the power management, the Standby mode and the wake-up sources. The fail-safe state machine manages the voltage monitoring of the power management.

14.1 Simplified functional state diagram

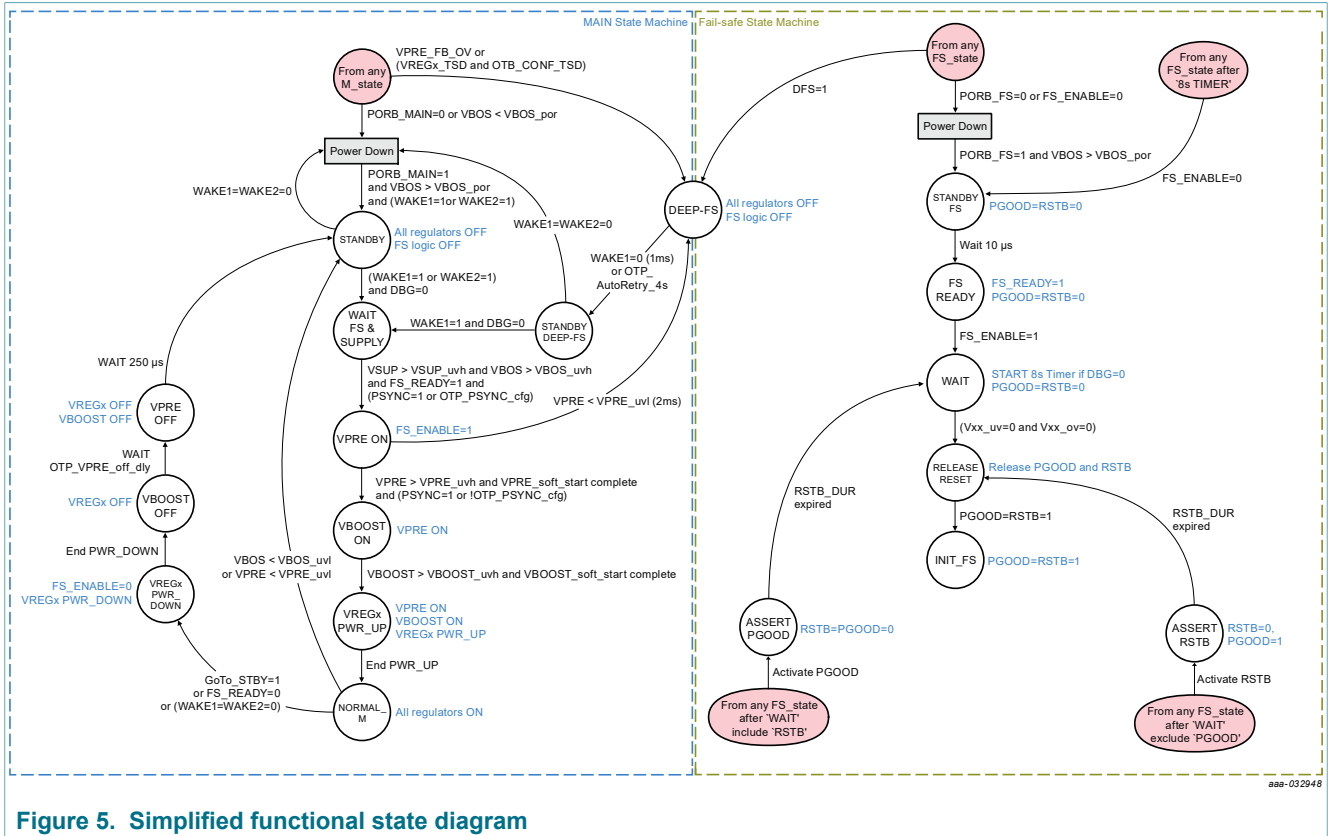


Figure 5. Simplified functional state diagram

14.2 Main state machine

The VR5500 start when $VSUP > VSUP_{UVH}$ and $WAKE1$ or $WAKE2 > WAKE12_{VIH}$ with $VBOS$ first, followed by $VPRE$, $VBOOST$, and the power-up sequencing from the OTP programming for the remaining regulators if $PSYNC$ pin is pulled up to $VBOS$. If during the power-up sequence $VSUP < VSUP_{UVL}$, the device goes back to Standby mode. When the power-up is finished, the main state machine is in Normal_M mode which is the application running mode with all the regulators ON and $VSUP_{UVL}$ has no effect even if $VSUP < VSUP_{UVL}$. See Figure 4 for the minimum operating voltage.

The power-up sequence can be synchronized with another PMIC using the $PSYNC$ pin in order to stop before or after $VPRE$ is ON and wait for the PMIC feedback on $PSYNC$ pin before allowing VR5500 to continue its power-up sequence. If the power-up sequence from $VPRE$ ON to $NORMAL_M$ is not completed within 1 second, the device goes back to Standby mode. $VPRE$ restarts when $VSUP > VSUP_{UVH}$ and $WAKE1$ or $WAKE2 > WAKE12_{VIH}$.

The device goes to Standby mode by a I2C command from the MCU. The device goes to Standby mode when both $WAKE1$ and $WAKE 2 = 0$. The device goes to Standby mode following the power down sequence to stop all the regulators in the reverse order of the power-up sequence. $VPRE$ shutdown can be delayed from 250 μs to 32 ms by $OTP_VPRE_off_dly$ bit in case $VPRE$ is supplying an external PMIC to wait its power down sequence completion.

In case of loss of VPRE ($VPRE < V_{PRE_UVL}$) or loss of VBOS ($VBOS < V_{BOS_UVL}$), the device stops and goes directly to Standby mode without power down sequence. VPRE restarts when $VSUP > V_{SUP_UVH}$ and $WAKE1$ or $WAKE2 > WAKE12_{VIH}$.

In case of VPRE_FB_OV detection, or TSD detection on a regulator depending on OTP_conf_tsd[5:0] bits configuration, or deep fail-safe request from the fail-safe state machine when DFS = 1, the device stops and goes directly to DEEP-FS mode without power down sequence.

Exit of DEEP-FS mode is only possible by $WAKE1 = 0$ or after 4 s if the autoretry feature is activated by OTP_Autoretry_en bit. The number of autoretry can be limited to 15 or infinite depending on OTP_Autoretry_infinite bit. VPRE restarts when $VSUP > V_{SUP_UVH}$ and $WAKE1 > WAKE12_{VIH}$.

14.3 Fail-safe state machine

The fail-safe state machine starts when $VBOS > V_{BOS_POR}$. RSTB and PGOOD pins are released and the initialization of the device is opened.

When RSTB and PGOOD pins are released, the device is ready for application running mode with all the selected monitoring activated. From now on, the VR5500 reacts by asserting the pins (PGOOD, RSTB) according to its configuration when a fault is detected.

14.4 Power sequencing

VPRE is the first regulator to start automatically, followed by the BOOST, before the SLOT_0. The other regulators are starting from the OTP power sequencing configuration. Seven slots are available to program the start-up sequence of BUCK1, BUCK 2, BUCK 3, LDO1, and LDO2 regulators. The delay between each slot is configurable to 250 μ s or 1 ms by OTP using OTP_Tslot bit to accommodate the different ramp up speed of BUCK1, BUCK2, and BUCK3.

The power-up sequence starts at SLOT_0 and ends at SLOT_7 while the power down sequence is executed in reverse order. All the SLOTS are executed even if there is no regulator assigned to a SLOT. The regulators assigned to SLOT_7 are not started during the power-up sequence. They can be started (or not) later in Normal_M mode with a I2C command to write in M_REG_CTRL1 register, if enabled by OTP.

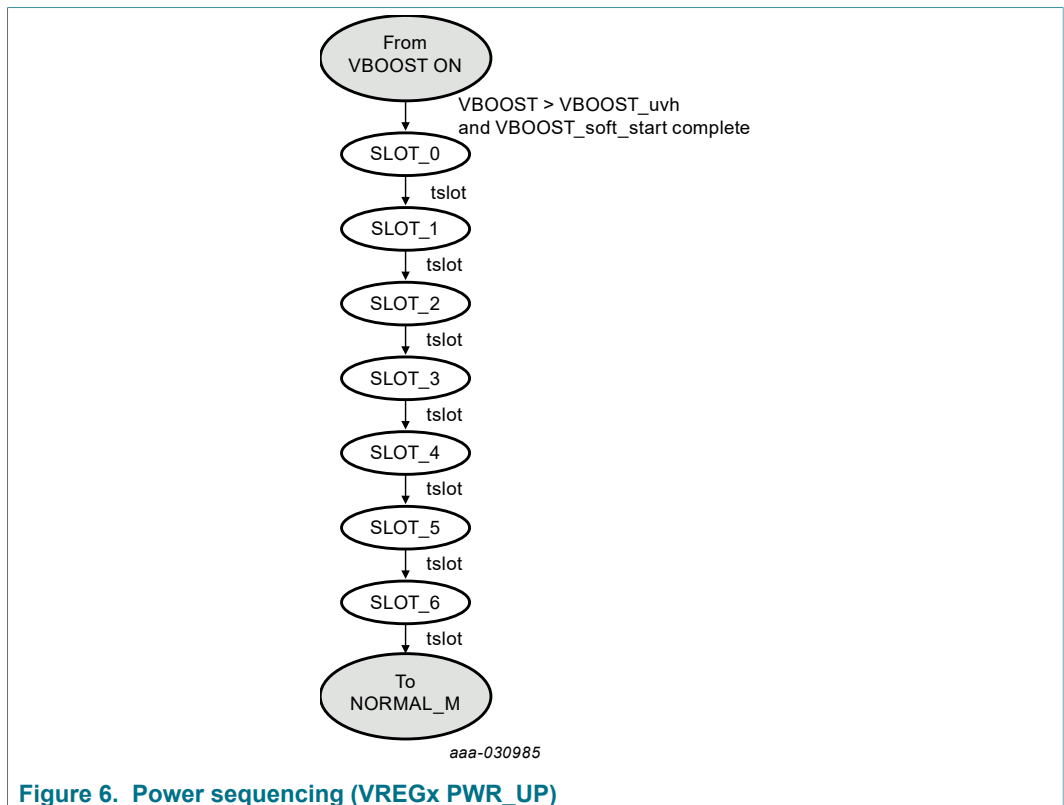
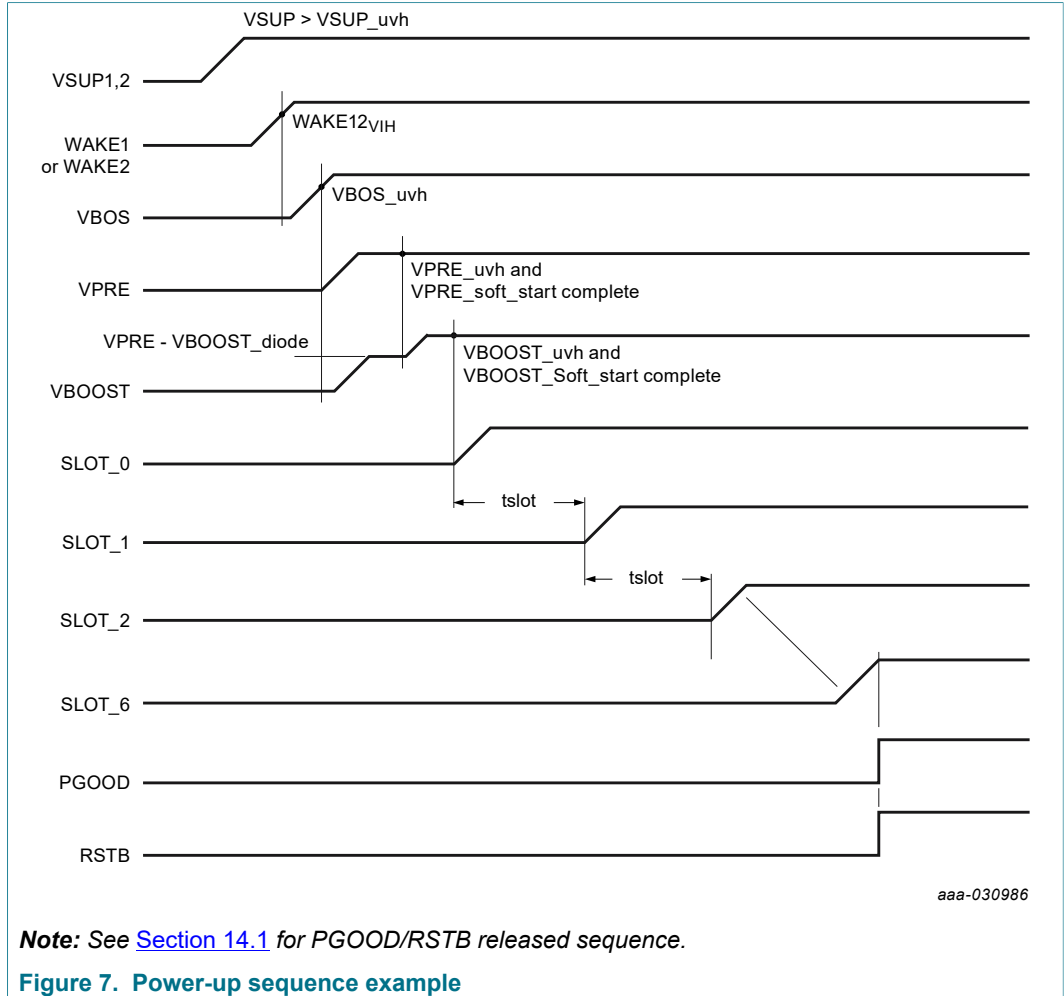


Figure 6. Power sequencing (VREGx PWR_UP)

Each regulator is assigned to a SLOT by OTP configuration using OTP_VB1S[2:0] for BUCK1, OTP_VB2S[2:0] for BUCK2, OTP_VB3S[2:0] for BUCK3, OTP_LDO1S[2:0] for LDO1 and OTP_LDO2S[2:0] for LDO2.

The different soft start duration of the BUCKs and the LDOs should be considered in the SLOT assignment to achieve the correct sequence.



The VR5500_OTP_Mapping file used to generate the OTP configuration of the device draws the power-up sequence of an OTP configuration in the OTP_conf_summary sheet.

14.5 Debug mode

The VR5500 enters in Debug mode with the sequence described in [Figure 8](#):

1. $DBG\ pin = V_{DBG}$ and $VSUP > V_{SUP_UVH}$
2. $WAKE1$ or $WAKE2 > WAKE12_{VIH}$

V_{DBG} and $VSUP$ can come up at the same time as long as $WAKE1$ or $WAKE2$ comes up the last.

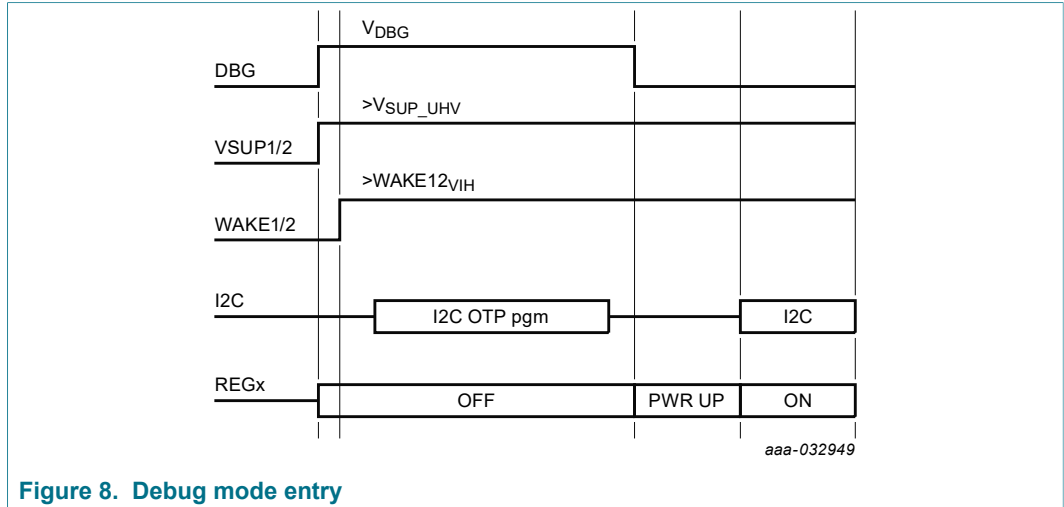


Figure 8. Debug mode entry

When the DBG pin is asserted low after T_{DBG} without I2C command access, the device starts with the internal OTP configuration.

If V_{DBG} voltage is maintained at DBG pin, a new OTP configuration can be emulated or programmed by I2C communication using NXP FlexGUI interface and NXP socket EVB. When the OTP process is completed, the device starts with the new OTP configuration when DBG pin is asserted low. The OTP emulation/programming is possible for during engineering development only. The OTP programming in production is done by NXP only.

In OTP Debug mode (DBG = 5.0 V), the I2C address is fixed to 0x20 for the main digital access and 0x21 for the fail-safe digital access.

Refer to AN12589 for more details on Debug mode entry implementation.

Table 7. Electrical characteristics

$T_A = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$, unless otherwise specified. $VSUP = VSUP_{UVH}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------|--|-----|-----|-----|------|
| V_{DBG} | Debug mode entry threshold | 4.5 | — | 5.5 | V |
| T_{DBG} | Debug mode entry filtering time (minimum duration of $DBG = V_{DBG}$ after $VSUP > VSUP_{UVH}$ and $WAKE1$ or $WAKE2 > WAKE12_{VIH}$) | 7.0 | — | — | ms |

15 Register mapping

| Register | M/FS | Address | | | | | | R/W I2C | Read / Write | Reference |
|------------------------------|------|---------|-------|-------|-------|-------|-------|---------|----------------------------------|-------------------------------|
| | | Adr_5 | Adr_4 | Adr_3 | Adr_2 | Adr_1 | Adr_0 | | | |
| M_FLAG | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1/0 | Read / Write | Section 16.3 |
| M_MODE | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1/0 | Read / Write | Section 16.4 |
| M_REG_CTRL1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1/0 | Read / Write | Section 16.5 |
| M_REG_CTRL2 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1/0 | Read / Write | Section 16.6 |
| M_AMUX | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1/0 | Read / Write | Section 16.7 |
| M_CLOCK | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1/0 | Read / Write | Section 16.8 |
| M_INT_MASK1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1/0 | Read / Write | Section 16.9 |
| M_INT_MASK2 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1/0 | Read / Write | Section 16.10 |
| M_FLAG1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1/0 | Read / Write | Section 16.11 |
| M_FLAG2 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1/0 | Read / Write | Section 16.12 |
| M_VMON_REGX | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1/0 | Read / Write | Section 16.13 |
| M_LVB1_SVS | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | Read only | Section 16.14 |
| M_MEMORY0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1/0 | Read / Write | Section 16.15 |
| M_MEMORY1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1/0 | Read / Write | Section 16.16 |
| M_DEVICEID | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | Read only | Section 16.17 |
| FS_GRL_FLAGS | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Read only | Section 17.3 |
| FS_I_OVUV_SAFE_REACTION1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1/0 | Write during INIT then Read only | Section 17.4 |
| FS_I_NOT_OVUV_SAFE_REACTION1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1/0 | Write during INIT then Read only | |
| FS_I_OVUV_SAFE_REACTION2 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1/0 | Write during INIT then Read only | Section 17.5 |
| FS_I_NOT_OVUV_SAFE_REACTION2 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1/0 | Write during INIT then Read only | |
| FS_I_FSSM | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1/0 | Write during INIT then Read only | Section 17.6 |
| FS_I_NOT_FSSM | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1/0 | Write during INIT then Read only | |
| FS_I_SVS | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1/0 | Write during INIT then Read only | Section 17.7 |
| FS_I_NOT_SVS | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1/0 | Write during INIT then Read only | |
| FS_OVUVREG_STATUS | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1/0 | Read / Write | Section 17.8 |
| FS_SAFE_IOS | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1/0 | Read / Write | Section 17.9 |
| FS_DIAG | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1/0 | Read / Write | Section 17.10 |
| FS_INTB_MASK | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1/0 | Read / Write | Section 17.11 |
| FS_STATES | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1/0 | Read / Write | Section 17.12 |

16 Main register mapping

16.1 Main writing registers overview

Table 8. Main writing registers overview

| Logic | Register name | bit 23 | bit 22 | bit 21 | bit 20 | bit 19 | bit 18 | bit 17 | bit 16 | |
|-------|---------------|---------------|-------------------|-------------|---------------|---------------|-----------------|---------------|--------------|----------|
| | | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | |
| Main | M_FLAG | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | I2C_M_CRC | I2C_M_REQ | |
| | M_MODE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | 0 | EXT_FIN_DIS | 0 | 0 | 0 | 0 | W2DIS | W1DIS | GoToSTBY |
| | M_REG_CTRL1 | VPRE_PD_DIS | VPDIS | BOOSTDIS | BUCK1DIS | BUCK2DIS | BUCK3DIS | LDO1DIS | LDO2DIS | |
| | | 0 | VPEN | BOOSTEN | BUCK1EN | BUCK2EN | BUCK3EN | LDO1EN | LDO2EN | |
| | M_REG_CTRL2 | VBSTSR[1:0] | | BOOSTTSDCFG | BUCK1TSDCFG | BUCK2TSDCFG | BUCK3TSDCFG | LDO1TSDCFG | LDO2TSDCFG | |
| | | 0 | 0 | 0 | VPRESRLS[1:0] | | 0 | VPRESRHS[1:0] | | |
| | M_AMUX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | 0 | 0 | RATIO | AMUX[4:0] | | | | | |
| | M_CLOCK | MOD_CONF | FOUT_MUX_SEL[3:0] | | | | FOUT_PHASE[2:0] | | | |
| | | FOUT_CLK_SEL | EXT_FIN_SEL | FIN_DIV | MOD_EN | CLK_TUNE[3:0] | | | | |
| | M_INT_MASK1 | 0 | VPREOC_M | 0 | BUCK1OC_M | BUCK2OC_M | BUCK3OC_M | LDO1OC_M | LDO2OC_M | |
| | | 0 | 0 | BOOSTTSD_M | BUCK1TSD_M | BUCK2TSD_M | BUCK3TSD_M | LDO1TSD_M | LDO2TSD_M | |
| | M_INT_MASK2 | 0 | 0 | 0 | 0 | VBOOSTOV_M | VBOSUVH_M | COM_M | VPRE_FB_OV_M | |
| | | VBOOST_UVH_M | VSUPUV7 | 0 | VPREUVH | VSUPUVL_M | VSUPUVH_M | WAKE1_M | WAKE2_M | |
| | M_FLAG1 | VBOSUVH | VBOOSTUVH | VPREOC | BUCK1OC | BUCK2OC | BUCK3OC | LDO1OC | LDO2OC | |
| | | 0 | VBOOSTOV | VBOOSTOT | BUCK1OT | BUCK2OT | BUCK3OT | LDO1OT | LDO2OT | |
| | M_FLAG2 | VPRE_FB_OV | VSUPUV7 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | VPREUVL | VPREUVH | VSUPUVL | VSUPUVH | 0 | 0 | WK2FLG | WK1FLG | |
| | M_VMON_REGX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | 0 | 0 | 0 | 0 | 0 | VMON1_REG[2:0] | | | |
| | M_MEMORY0 | MEMORY0[15:0] | | | | | | | | |
| | M_MEMORY1 | MEMORY1[15:0] | | | | | | | | |

16.2 Main reading registers overview

Table 9. Main reading registers overview

| Logic | Register name | bit 23 | bit 22 | bit 21 | bit 20 | bit 19 | bit 18 | bit 17 | bit 16 |
|-------|---------------|----------------|-------------------|-------------|---------------|-----------------|-------------|----------------|--------------|
| | | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 |
| Main | M_FLAG | COM_ERR | WU_G | VPRE_G | VBOOST_G | VBUCK1_G | VBUCK2_G | VBUCK3_G | VLDO1_G |
| | | VLDO2_G | 0 | 0 | 0 | 0 | 0 | I2C_M_CRC | I2C_M_REQ |
| | M_MODE | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | PLL_LOCK_RT |
| | | EXT_FIN_SEL_RT | RESERVED | MAIN_NORMAL | RESERVED | RESERVED | W2DIS | W1DIS | RESERVED |
| | M_REG_CTRL1 | VPRE_PD_DIS | VPDIS | BOOSTDIS | BUCK1DIS | BUCK2DIS | BUCK3DIS | LDO1DIS | LDO2DIS |
| | | 0 | VPEN | BOOSTEN | BUCK1EN | BUCK2EN | BUCK3EN | LDO1EN | LDO2EN |
| | M_REG_CTRL2 | VBSTSR[1:0] | | BOOSTTSDCFG | BUCK1TSDCFG | BUCK2TSDCFG | BUCK3TSDCFG | LDO1TSDCFG | LDO2TSDCFG |
| | | RESERVED | RESERVED | RESERVED | VPRESRLS[1:0] | | RESERVED | VPRESRHS[1:0] | |
| | M_AMUX | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| | | RESERVED | RESERVED | RATIO | AMUX[4:0] | | | | |
| | M_CLOCK | MOD_CONF | FOUT_MUX_SEL[3:0] | | | FOUT_PHASE[2:0] | | | |
| | | FOUT_CLK_SEL | RESERVED | FIN_DIV | MOD_EN | CLK_TUNE[3:0] | | | |
| | M_INT_MASK1 | RESERVED | VPREOC_M | RESERVED | BUCK1OC_M | BUCK2OC_M | BUCK3OC_M | LDO1OC_M | LDO2OC_M |
| | | RESERVED | RESERVED | BOOSTTSD_M | BUCK1TSD_M | BUCK2TSD_M | BUCK3TSD_M | LDO1TSD_M | LDO2TSD_M |
| | M_INT_MASK2 | RESERVED | RESERVED | RESERVED | RESERVED | VBOOSTOV_M | VBOSUVH_M | COM_M | VPRE_FB_OV_M |
| | | VBOOST_UVH_M | VSUPUV7_M | RESERVED | VPREUVH_M | VSUPUV_M | VSUPUVH_M | WAKE1_M | WAKE2_M |
| | M_FLAG1 | VBOSUVH | VBOOSTUVH | VPREOC | BUCK1OC | BUCK2OC | BUCK3OC | LDO1OC | LDO2OC |
| | | CLK_FIN_DIV_OK | VBOOSTOV | VBOOSTOT | BUCK1OT | BUCK2OT | BUCK3OT | LDO1OT | LDO2OT |
| | M_FLAG2 | VPRE_FB_OV | VSUPUV7 | BOOST_ST | BUCK1_ST | BUCK2_ST | BUCK3_ST | LDO1_ST | LDO2_ST |
| | | VPREUVL | VPREUVH | VSUPUVL | VSUPUVH | WK2RT | WK1RT | WK2FLG | WK1FLG |
| | M_VMON_REGX | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| | | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | VMON1_REG[2:0] | |
| | M_LVB1_SVS | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| | | RESERVED | RESERVED | RESERVED | LVB1_SVS[4:0] | | | | |
| | M_MEMORY0 | MEMORY0[15:0] | | | | | | | |
| | M_MEMORY1 | MEMORY1[15:0] | | | | | | | |
| | M_DEVICEID | FM_REV[3:0] | | | | MM_REV[3:0] | | | |
| | | DEVICEID[7:0] | | | | | | | |

16.3 M_FLAG register

Table 10. M_FLAG register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|------|--------|----------|----------|----------|----------|---------|
| Write | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read | COM_ERR | WU_G | VPRE_G | VBOOST_G | VBUCK1_G | VBUCK2_G | VBUCK3_G | VLDO1_G |
| Reset | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------|---------|----|----|----|----|----|-----------|-----------|
| Write | 0 | 0 | 0 | 0 | 0 | 0 | I2C_M_CRC | I2C_M_REQ |
| Read | VLDO2_G | 0 | 0 | 0 | 0 | 0 | I2C_M_CRC | I2C_M_REQ |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 11. M_FLAG register bit description

| Bit | Symbol | Description |
|-----|----------|--|
| 23 | COM_ERR | Report an error in the communication (I2C) COM_ERR = I2C_M_CRC or I2C_M_REQ or FS_COM_G |
| | | 0 No failure |
| | | 1 Failure |
| | | Reset condition: Real-time information - cleared when all individual bits are cleared |
| 22 | WU_G | Report a wake-up event by WAKE1 or WAKE2 WU_G = WK1FLG or WK2FLG |
| | | 0 No wake event |
| | | 1 Wake event |
| | | Reset condition: Real-time information - cleared when all individual bits are cleared |
| 21 | VPRE_G | Report an event on VPRE (status change or failure) VPRE_G = VPREOC or VPREUVH or VPREUVL or VPRE_FB_OV |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: Real-time information - cleared when all individual bits are cleared |
| 20 | VBOOST_G | Report an event on VBOOST (status change or failure) VBOOST_G = VBOOSTOT or BOOSTOV |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: Real-time information - cleared when all individual bits are cleared |
| 19 | VBUCK1_G | Report an event on BUCK1 (status change or failure) VBUCK1_G = BUCK1OC or BUCK1OT |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: Real-time information - cleared when all individual bits are cleared |
| 18 | VBUCK2_G | Report an event on BUCK2 (status change or failure) VBUCK2_G = BUCK2OC or BUCK2OT |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: Real-time information - cleared when all individual bits are cleared |
| 17 | VBUCK3_G | Report an event on BUCK3 (status change or failure) VBUCK3_G = BUCK3OC or BUCK3OT |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: Real-time information - cleared when all individual bits are cleared |
| 16 | VLDO1_G | Report an event on LDO1 (status change or failure) VLDO1_G = LDO1OC or LDO1OT |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: Real-time information |

| Bit | Symbol | Description |
|-----|-----------|---|
| 15 | VLDO2_G | Report an event on LDO2 (status change or failure) VLDO2_G = LDO2OC or LDO2OT |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: Real-time information |
| 9 | I2C_M_CRC | Main domain I2C communication CRC issue |
| | | 0 No error |
| | | 1 Error detected in the I2C CRC |
| | | Reset condition: POR / clear on write (write '1') |
| 8 | I2C_M_REQ | Invalid main domain I2C access (wrong Write or Read, Write to INIT registers in normal mode, wrong address) |
| | | 0 No error |
| | | 1 I2C violation |
| | | Reset condition: POR / clear on Write (write '1') |

16.4 M_MODE register

Table 12. M_MODE register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----------|----------|----------|----------|----------|----------|-------------|
| Write | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | PLL_LOCK_RT |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------|----------------|-------------|-------------|----------|----------|-------|-------|----------|
| Write | 0 | EXT_FIN_DIS | 0 | 0 | 0 | W2DIS | W1DIS | GoToSTBY |
| Read | EXT_FIN_SEL_RT | RESERVED | MAIN_NORMAL | RESERVED | RESERVED | W2DIS | W1DIS | RESERVED |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

Table 13. M_MODE register bit description

| Bit | Symbol | Description |
|-----|----------------|---|
| 16 | PLL_LOCK_RT | Real-time status of the PPL |
| | | 0 PLL not locked |
| | | 1 PLL locked |
| | | Reset condition: POR |
| 15 | EXT_FIN_SEL_RT | Real-time status of FIN clock selection |
| | | 0 Internal clock oscillator is selected |
| | | 1 External FIN clock is selected |
| | | Reset condition: POR |

| Bit | Symbol | Description |
|-----|-------------|---|
| 14 | EXT_FIN_DIS | Disable request of EXT FIN selection at PLL input |
| | | 0 No effect |
| | | 1 Disable FIN selection |
| | | Reset condition: POR |
| 13 | MAIN_NORMAL | Main state machine status |
| | | 0 Main state machine is not in Normal mode |
| | | 1 Main state machine is in Normal mode |
| | | Reset condition: POR |
| 10 | W2DIS | WAKE2 wake up disable |
| | | 0 wake up enable |
| | | 1 wake up disable |
| | | Reset condition: POR |
| 9 | W1DIS | WAKE1 wake up disable |
| | | 0 Wake up enable |
| | | 1 Wake up disable |
| | | Reset condition: POR |
| 8 | GOTOSTBY | Standby mode request |
| | | 0 Device remains in current state |
| | | 1 Device enters in Standby mode |
| | | Reset condition: POR |

16.5 M_REG_CTRL1 register

Table 14. M_REG_CTRL1 register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------|----------|----------|----------|----------|----------|----------|----------|
| Write | VPRE_PD_DIS | VPDIS | BOOSTDIS | BUCK1DIS | BUCK2DIS | BUCK3DIS | LDO1DIS | LDO2DIS |
| Read | VPRE_PD_DIS | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|--------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Write | 0 | VPEN | BOOSTEN | BUCK1EN | BUCK2EN | BUCK3EN | LDO1EN | LDO2EN |
| Read | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 15. M_REG_CTRL1 register bit description

| Bit | Symbol | Description |
|-----|-------------|---|
| 23 | VPRE_PD_DIS | Force disable of VPRE pull-down |
| | | 0 No effect (VPRE pull-down is automatically controlled by the logic) |
| | | 1 VPRE pull-down disable request |
| | | Reset condition: POR |

| Bit | Symbol | Description |
|-----|----------|---|
| 22 | VPDIS | Disable request of VPRE |
| | | 0 No effect (regulator remains in existing state) |
| | | 1 VPRE disable request |
| | | Reset condition: POR |
| 21 | BOOSTDIS | Disable request of BOOST |
| | | 0 No effect (regulator remains in existing state) |
| | | 1 BOOST disable request |
| | | Reset condition: POR |
| 20 | BUCK1DIS | Disable request of BUCK1 |
| | | 0 No effect (regulator remains in existing state) |
| | | 1 BUCK1 disable request |
| | | Reset condition: POR |
| 19 | BUCK2DIS | Disable request of BUCK2 |
| | | 0 No effect (regulator remains in existing state) |
| | | 1 BUCK2 disable request |
| | | Reset condition: POR |
| 18 | BUCK3DIS | Disable request of BUCK3 |
| | | 0 No effect (regulator remains in existing state) |
| | | 1 BUCK3 disable request |
| | | Reset condition: POR |
| 17 | LDO1DIS | Disable request of LDO1 |
| | | 0 No effect (regulator remains in existing state) |
| | | 1 LDO1 disable request |
| | | Reset condition: POR |
| 16 | LDO2DIS | Disable request of LDO2 |
| | | 0 no effect (regulator remains in existing state) |
| | | 1 LDO2 disable request |
| | | Reset condition: POR |
| 14 | VPEN | Enable request of VPRE |
| | | 0 No effect (regulator remains in existing state) |
| | | 1 VPRE enable request (after a VPDIS request) |
| | | Reset condition: POR |
| 13 | BOOSTEN | Enable request of BOOST |
| | | 0 No effect (regulator remains in existing state) |
| | | 1 BOOST enable request |
| | | Reset condition: POR |
| 12 | BUCK1EN | Enable request of BUCK1 |
| | | 0 No effect (regulator remains in existing state) |
| | | 1 BUCK1 enable request |
| | | Reset condition: POR |

| Bit | Symbol | Description |
|-----|---------|---|
| 11 | BUCK2EN | Enable request of BUCK2 |
| | | 0 No effect (regulator remains in existing state) |
| | | 1 BUCK2 enable request |
| | | Reset condition: POR |
| 10 | BUCK3EN | Enable request of BUCK3 |
| | | 0 No effect (regulator remains in existing state) |
| | | 1 BUCK3 enable request |
| | | Reset condition: POR |
| 9 | LDO1EN | Enable request of LDO1 |
| | | 0 No effect (regulator remains in existing state) |
| | | 1 LDO1 enable request |
| | | Reset condition: POR |
| 8 | LDO2EN | Enable request of LDO2 |
| | | 0 no effect (regulator remains in existing state) |
| | | 1 LDO2 enable request |
| | | Reset condition: POR |

16.6 M_REG_CTRL2 register

Table 16. M_REG_CTRL2 register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------|-----|-----------------|-----------------|-----------------|-----------------|----------------|----------------|
| Write | VBSTSR[1:0] | | BOOSTT SDCFG | BUCK1T SDCFG | BUCK2T SDCFG | BUCK3T SDCFG | LDO1T SDCFG | LDO2T SDCFG |
| Read | VBSTSR[1:0] | | BOOSTT SDCFG | BUCK1T SDCFG | BUCK2T SDCFG | BUCK3T SDCFG | LDO1T SDCFG | LDO2T SDCFG |
| Reset | OTP | OTP | OTP | OTP | OTP | OTP | OTP | OTP |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|--------------|----------|----------|----------|---------------|----|----------|---------------|-----|
| Write | 0 | 0 | 0 | VPRESRLS[1:0] | | 0 | VPRESRHS[1:0] | |
| Read | RESERVED | RESERVED | RESERVED | VPRESRLS[1:0] | | RESERVED | VPRESRHS[1:0] | |
| Reset | 0 | 0 | 0 | 1 | 1 | 0 | OTP | OTP |

Table 17. M_REG_CTRL2 register bit description

| Bit | Symbol | Description |
|----------|-------------|-----------------------------------|
| 23 to 22 | VBSTSR[1:0] | VBOOST low-side slew rate control |
| | | 00 50 V/μs - slow |
| | | 01 100 V/μs – medium |
| | | 10 300 V/μs – fast |
| | | 11 500 V/μs – ultra fast |
| | | Reset condition: POR |

| Bit | Symbol | Description |
|----------------------|---------------|--|
| 21 | BOOSTTSDCFG | BOOST behavior in case of TSD |
| | | 0 Regulator shutdown |
| | | 1 Regulator shutdown and state machine transition to DEEP-FS |
| | | Reset condition: POR |
| 20 | BUCK1TSDCFG | BUCK1 behavior in case of TSD |
| | | 0 Regulator shutdown |
| | | 1 Regulator shutdown and state machine transition to DEEP-FS |
| | | Reset condition: POR |
| 19 | BUCK2TSDCFG | BUCK2 behavior in case of TSD |
| | | 0 Regulator shutdown |
| | | 1 Regulator shutdown and state machine transition to DEEP-FS |
| | | Reset condition: POR |
| 18 | BUCK3TSDCFG | BUCK3 behavior in case of TSD |
| | | 0 Regulator shutdown |
| | | 1 Regulator shutdown and state machine transition to DEEP-FS |
| | | Reset condition: POR |
| 17 | LDO1TSDCFG | LDO1 behavior in case of TSD |
| | | 0 Regulator shutdown |
| | | 1 Regulator shutdown and state machine transition to DEEP-FS |
| | | Reset condition: POR |
| 16 | LDO2TSDCFG | LDO2 behavior in case of TSD |
| | | 0 Regulator shutdown |
| | | 1 Regulator shutdown and state machine transition to DEEP-FS |
| | | Reset condition: POR |
| 12 to 11 | VPRESRLS[1:0] | VPRE low-side slew rate control |
| | | 00 130 mA typical drive capability - slow |
| | | 01 260 mA typical drive capability - medium |
| | | 10 520 mA typical drive capability - fast |
| | | 11 900 mA typical drive capability - ultra fast |
| Reset condition: POR | | |
| 9 to 8 | VPRESRHS[1:0] | VPRE high-side slew rate control |
| | | 00 130 mA typical drive capability - slow |
| | | 01 260 mA typical drive capability - medium |
| | | 10 520 mA typical drive capability - fast |
| | | 11 900 mA typical drive capability - ultra fast |
| Reset condition: POR | | |

16.7 M_AMUX register

Table 18. M_AMUX register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----------|----------|----------|----------|----------|----------|----------|
| Write | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------|----------|----------|-------|-----------|----|----|---|---|
| Write | 0 | 0 | RATIO | AMUX[4:0] | | | | |
| Read | RESERVED | RESERVED | RATIO | AMUX[4:0] | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 19. M_AMUX register bit description

| Bit | Symbol | Description |
|---------|-----------|--|
| 13 | RATIO | Selection of divider ratio for V _{SUP} , Wake1 and Wake 2 inputs |
| | | 0 Ratio = 7.5 when V _{SUP} is selected, 7.45 when WAKE1 or WAKE2 are selected |
| | | 1 Ratio = 14 when V _{SUP} is selected, 13.85 when WAKE1 or WAKE2 are selected |
| | | Reset condition |
| 12 to 8 | AMUX[4:0] | See Table 77 |

16.8 M_CLOCK register

Table 20. M_CLOCK register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|-------------------|----|----|----|-----------------|----|----|
| Write | MOD_CONF | FOUT_MUX_SEL[3:0] | | | | FOUT_PHASE[2:0] | | |
| Read | MOD_CONF | FOUT_MUX_SEL[3:0] | | | | FOUT_PHASE[2:0] | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------|--------------|-------------|---------|--------|---------------|----|---|---|
| Write | FOUT_CLK_SEL | EXT_FIN_SEL | FIN_DIV | MOD_EN | CLK_TUNE[3:0] | | | |
| Read | FOUT_CLK_SEL | RESERVED | FIN_DIV | MOD_EN | CLK_TUNE[3:0] | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 21. M_CLOCK register bit description

| Bit | Symbol | Description |
|----------|-------------------|---|
| 23 | MOD_CONF | Modulation configuration of main oscillator |
| | | 0 range $\pm 5\%$ 23 kHz |
| | | 1 range $\pm 5\%$ 94 kHz |
| | | Reset condition: POR |
| 22 to 19 | FOUT_MUX_SEL[3:0] | See Table 75 |

| Bit | Symbol | Description |
|----------|-----------------|--|
| 18 to 16 | FOUT_PHASE[2:0] | FOUT phase shifting configuration (see Section 25.2 "Phase shifting") |
| | | 000 No shift |
| | | 001 Shifted by 1 clock cycle of CLK running at 20 MHz |
| | | 010 Shifted by 2 clock cycle of CLK running at 20 MHz |
| | | 011 Shifted by 3 clock cycle of CLK running at 20 MHz |
| | | 100 Shifted by 4 clock cycle of CLK running at 20 MHz |
| | | 101 Shifted by 5 clock cycle of CLK running at 20 MHz |
| | | 110 Shifted by 6 clock cycle of CLK running at 20 MHz |
| | | 111 Shifted by 7 clock cycle of CLK running at 20 MHz |
| | | Reset condition: POR |
| 15 | FOUT_CLK_SEL | FOUT_clk frequency selection (CLK1 or CLK2) |
| | | 0 FOUT_clk = CLK1 |
| | | 1 FOUT_clk = CLK2 |
| | | Reset condition: POR |
| 14 | EXT_FIN_SEL | Enable request of EXT FIN selection at PLL input |
| | | 0 No effect |
| | | 1 FIN selection request |
| | | Reset condition: POR |
| 13 | FIN_DIV | FIN input signal divider selection |
| | | 0 Divider by 1 |
| | | 1 Divider by 6 |
| | | Reset condition: POR |
| 12 | MOD_EN | Modulation activation of main oscillator |
| | | 0 Modulation disabled |
| | | 1 Modulation enabled |
| | | Reset condition: POR |
| 11 to 8 | CLK_TUNE[3:0] | See Table 74 |

16.9 M_INT_MASK1 register

Table 22. M_INT_MASK1 register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----------|----------|-----------|-----------|-----------|----------|----------|
| Write | 0 | VPREOC_M | 0 | BUCK1OC_M | BUCK2OC_M | BUCK3OC_M | LDO1OC_M | LDO2OC_M |
| Read | RESERVED | VPREOC_M | RESERVED | BUCK1OC_M | BUCK2OC_M | BUCK3OC_M | LDO1OC_M | LDO2OC_M |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------|----------|----------|------------|------------|------------|------------|-----------|-----------|
| Write | 0 | 0 | BOOSTTSD_M | BUCK1TSD_M | BUCK2TSD_M | BUCK3TSD_M | LDO1TSD_M | LDO2TSD_M |
| Read | RESERVED | RESERVED | BOOSTTSD_M | BUCK1TSD_M | BUCK2TSD_M | BUCK3TSD_M | LDO1TSD_M | LDO2TSD_M |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 23. M_INT_MASK1 register bit description

| Bit | Symbol | Description |
|-----|------------|--|
| 22 | VPREOC_M | Inhibit INTERRUPT for VPRE overcurrent |
| | | 0 INT not masked |
| | | 1 INT masked |
| | | Reset condition: POR |
| 20 | BUCK1OC_M | Inhibit INTERRUPT for BUCK1 overcurrent |
| | | 0 INT not masked |
| | | 1 INT masked |
| | | Reset condition: POR |
| 19 | BUCK2OC_M | Inhibit INTERRUPT for BUCK3 overcurrent |
| | | 0 INT not masked |
| | | 1 INT masked |
| | | Reset condition: POR |
| 18 | BUCK3OC_M | Inhibit INTERRUPT for BUCK3 overcurrent |
| | | 0 INT not masked |
| | | 1 INT masked |
| | | Reset condition: POR |
| 17 | LDO1OC_M | Inhibit INTERRUPT for LDO1 overcurrent |
| | | 0 INT not masked |
| | | 1 INT masked |
| | | Reset condition: POR |
| 16 | LDO2OC_M | Inhibit INTERRUPT for LDO2 overcurrent |
| | | 0 INT not masked |
| | | 1 INT masked |
| | | Reset condition: POR |
| 13 | BOOSTTSD_M | Inhibit INTERRUPT for BOOST overtemperature shutdown event |
| | | 0 INT not masked |
| | | 1 INT masked |
| | | Reset condition: POR |
| 12 | BUCK1TSD_M | Inhibit INTERRUPT for BUCK1 overtemperature shutdown event |
| | | 0 INT not masked |
| | | 1 INT masked |
| | | Reset condition: POR |

| Bit | Symbol | Description |
|-----|------------|--|
| 11 | BUCK2TSD_M | Inhibit INTERRUPT for BUCK2 overtemperature shutdown event |
| | | 0 INT not masked |
| | | 1 INT masked |
| | | Reset condition: POR |
| 10 | BUCK3TSD_M | Inhibit INTERRUPT for BUCK3 overtemperature shutdown event |
| | | 0 INT not masked |
| | | 1 INT masked |
| | | Reset condition: POR |
| 9 | LDO1TSD_M | Inhibit INTERRUPT for LDO1 overtemperature shutdown event |
| | | 0 INT not masked |
| | | 1 INT masked |
| | | Reset condition: POR |
| 8 | LDO2TSD_M | Inhibit INTERRUPT for LDO2 overtemperature shutdown event |
| | | 0 INT not masked |
| | | 1 INT masked |
| | | Reset condition: POR |

16.10 M_INT_MASK2 register

Table 24. M_INT_MASK2 register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----------|----------|----------|------------|-----------|-------|--------------|
| Write | 0 | 0 | 0 | 0 | VBOOSTOV_M | VBOSUVH_M | COM_M | VPRE_FB_OV_M |
| Read | RESERVED | RESERVED | RESERVED | RESERVED | VBOOSTOV_M | VBOSUVH_M | COM_M | VPRE_FB_OV_M |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------|--------------|-----------|----------|-----------|-----------|-----------|---------|---------|
| Write | VBOOST_UVH_M | VSUPUV7_M | 0 | VPREUVH_M | VSUPUVL_M | VSUPUVH_M | WAKE1_M | WAKE2_M |
| Read | VBOOST_UVH_M | VSUPUV7_M | RESERVED | VPREUVH_M | VSUPUVL_M | VSUPUVH_M | WAKE1_M | WAKE2_M |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 25. M_INT_MASK2 register bit description

| Bit | Symbol | Description |
|-----|------------|--|
| 19 | VBOOSTOV_M | Inhibit INTERRUPT for VBOOST_OV any transition |
| | | 0 INT not masked |
| | | 1 INT masked |
| | | Reset condition: POR |

| Bit | Symbol | Description |
|-----|--------------|---|
| 18 | VBOSUVH_M | Inhibit INTERRUPT for VBOS_UVH any transition |
| | | 0 INT not masked |
| | | 1 INT masked |
| | | Reset condition: POR |
| 17 | COM_M | Inhibit INTERRUPT for COM any transition |
| | | 0 INT not masked |
| | | 1 INT masked |
| | | Reset condition: POR |
| 16 | VPRE_FB_OV_M | Inhibit INTERRUPT for VPRE_FB_OV |
| | | 0 INT not masked |
| | | 1 INT masked |
| | | Reset condition: POR |
| 15 | VBOOSTUVH_M | Inhibit INTERRUPT for VBOOST_UVH |
| | | 0 INT not masked |
| | | 1 INT masked |
| | | Reset condition: POR |
| 14 | VSUPUV7_M | Inhibit INTERRUPT for VSUP_UV7 |
| | | 0 INT not masked |
| | | 1 INT masked |
| | | Reset condition: POR |
| 12 | VREUVH_M | Inhibit INTERRUPT for VSUP_UVH |
| | | 0 INT not masked |
| | | 1 INT masked |
| | | Reset condition: POR |
| 11 | VSUPUVL_M | Inhibit INTERRUPT for VSUP_UVL |
| | | 0 INT not masked |
| | | 1 INT masked |
| | | Reset condition: POR |
| 10 | VSUPUVH_M | Inhibit INTERRUPT for VPRE_UVH |
| | | 0 INT not masked |
| | | 1 INT masked |
| | | Reset condition: POR |
| 9 | WAKE1_M | Inhibit INTERRUPT for WAKE1 any transition |
| | | 0 INT not masked |
| | | 1 INT masked |
| | | Reset condition: POR |
| 8 | WAKE2_M | Inhibit INTERRUPT for WAKE2 any transition |
| | | 0 INT not masked |
| | | 1 INT masked |
| | | Reset condition: POR |

16.11 M_FLAG1 register

When device starts-up, it is recommended to clear all the flags by writing 1 on all bits.

Table 26. M_FLAG1 register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|---------------|--------|---------|---------|---------|--------|--------|
| Write | VBOSUVH | VBOO STUVH | VPREOC | BUCK1OC | BUCK2OC | BUCK3OC | LDO1OC | LDO2OC |
| Read | VBOSUVH | VBOO STUVH | VPREOC | BUCK1OC | BUCK2OC | BUCK3OC | LDO1OC | LDO2OC |
| Reset | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------|--------------------|----------|----------|---------|---------|---------|--------|--------|
| Write | 0 | VBOOSTOV | VBOOSTOT | BUCK1OT | BUCK2OT | BUCK3OT | LDO1OT | LDO2OT |
| Read | CLK_FIN_ DIV_OK | VBOOSTOV | VBOOSTOT | BUCK1OT | BUCK2OT | BUCK3OT | LDO1OT | LDO2OT |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 27. M_FLAG1 register bit description

| Bit | Symbol | Description |
|-----|-----------|---|
| 23 | VBOSUVH | VBOS undervoltage high event (falling) |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: POR / Clear on Write (write '1') |
| 22 | VBOOSTUVH | VBOOST undervoltage high event (falling) |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: POR / Clear on Write (write '1') |
| 21 | VPREOC | VPRE overcurrent event |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: POR / Clear on Write (write '1') |
| 20 | BUCK1OC | BUCK1 overcurrent event |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: POR / Clear on Write (write '1') |
| 19 | BUCK2OC | BUCK3 overcurrent event |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: POR / Clear on Write (write '1') |
| 18 | BUCK3OC | BUCK3 overcurrent |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: POR / Clear on Write (write '1') |

| Bit | Symbol | Description |
|-----|----------------|--|
| 17 | LDO1OC | LDO2 overcurrent |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: POR / Clear on Write (write '1') |
| 16 | LDO2OC | LDO1 overcurrent |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: POR / Clear on Write (write '1') |
| 15 | CLK_FIN_DIV_OK | CLK_FIN_DIV monitoring |
| | | 0 Not OK: $FIN_{ERR_LONG} < CLK_FIN_DIV \text{ deviation} < FIN_{ERR_SHORT}$ |
| | | 1 OK: $FIN_{ERR_SHORT} < CLK_FIN_DIV \text{ deviation} < FIN_{ERR_LONG}$ |
| | | Reset condition: Real time information |
| 14 | VBOOSTOV | VBOOST overvoltage protection event |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: POR / Clear on Write (write '1') |
| 13 | VBOOSTOT | VBOOST overtemperature shutdown event |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: POR / Clear on Write (write '1') |
| 12 | BUCK1OT | BUCK1 overtemperature shutdown event |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: POR / Clear on Write (write '1') |
| 11 | BUCK2OT | BUCK2 overtemperature shutdown event |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: POR / Clear on Write (write '1') |
| 10 | BUCK3OT | BUCK3 overtemperature shutdown event |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: POR / Clear on Write (write '1') |
| 9 | LDO1OT | LDO1 overtemperature shutdown event |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: POR / Clear on Write (write '1') |
| 8 | LDO2OT | LDO2 overtemperature shutdown event |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: POR / Clear on Write (write '1') |

16.12 M_FLAG2 register

When device starts-up, it is recommended to clear all the flags by writing 1 on all bits.

Table 28. M_FLAG2 register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|---------|----------|----------|----------|----------|---------|---------|
| Write | VPRE_FB_OV | VSUPUV7 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read | VPRE_FB_OV | VSUPUV7 | BOOST_ST | BUCK1_ST | BUCK2_ST | BUCK3_ST | LDO1_ST | LDO2_ST |
| Reset | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------|---------|---------|---------|---------|-------|-------|--------|--------|
| Write | VPREUVL | VPREUVH | VSUPUVL | VSUPUVH | 0 | 0 | WK2FLG | WK1FLG |
| Read | VPREUVL | VPREUVH | VSUPUVL | VSUPUVH | WK2RT | WK1RT | WK2FLG | WK1FLG |
| Reset | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |

Note: Reset value for VR5500, wake up by Wake1, all regulators started by default during power-up sequence.

Table 29. M_FLAG2 register bit description

| Bit | Symbol | Description |
|-----|------------|---|
| 23 | VPRE_FB_OV | VPRE_FB_OV event |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: POR / Clear on Write (write '1') |
| 22 | VSUPUV7 | VSUP_UV7 event |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: POR / Clear on Write (write '1') |
| 21 | BOOST_ST | BOOST state |
| | | 0 Regulator OFF |
| | | 1 Regulator ON |
| | | Reset condition: Real-time information |
| 20 | BUCK1_ST | BUCK1 state |
| | | 0 Regulator OFF |
| | | 1 Regulator ON |
| | | Reset condition: Real-time information |
| 19 | BUCK2_ST | BUCK2 state |
| | | 0 Regulator OFF |
| | | 1 Regulator ON |
| | | Reset condition: Real-time information |
| 18 | BUCK3_ST | BUCK3 state |
| | | 0 Regulator OFF |
| | | 1 Regulator ON |
| | | Reset condition: Real-time information |

| Bit | Symbol | Description |
|-----|---------|---|
| 17 | LDO1_ST | LDO1 state |
| | | 0 regulator OFF |
| | | 1 regulator ON |
| | | Reset condition: Real-time information |
| 16 | LDO2_ST | LDO2 state |
| | | 0 regulator OFF |
| | | 1 regulator ON |
| | | Reset condition: Real-time information |
| 15 | VPREUVL | VPRE_UVL event |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: POR / Clear on Write (write '1') |
| 14 | VPREUVH | VPRE_UVH event |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: POR / Clear on Write (write '1') |
| 13 | VSUPUVL | VSUP_UVL event |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: POR / Clear on Write (write '1') |
| 12 | VSUPUVH | VSUP_UVH event |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: POR / Clear on Write (write '1') |
| 11 | WK2RT | Report event: WAKE2 real-time state |
| | | 0 WAKE2 is low level |
| | | 1 WAKE2 is high |
| | | Reset condition: Real-time information |
| 10 | WK1RT | Report event: WAKE1 real-time state |
| | | 0 WAKE1 is low level |
| | | 1 WAKE1 is high |
| | | Reset condition: Real-time information |
| 9 | WK2FLG | WAKE2 wake up source flag |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: POR / Clear on Write (write '1') |
| 8 | WK1FLG | WAKE1 wake up source flag |
| | | 0 No event |
| | | 1 Event occurred |
| | | Reset condition: POR / Clear on Write (write '1') |

16.13 M_VMON_REG1 register

Table 30. M_VMON_REG1 register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----------|----------|----------|----------|----------|----------|----------|
| Write | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------|----------|----------|----------|----------|----------|----------------|---|---|
| Write | 0 | 0 | 0 | 0 | 0 | VMON1_REG[2:0] | | |
| Read | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | VMON1_REG[2:0] | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 31. M_VMON_REG1 register bit description

| Bit | Symbol | Description |
|---------|----------------|-------------------------------|
| 10 to 8 | VMON1_REG[2:0] | Regulator assignment to VMON1 |
| | | 000 External regulator |
| | | 001 VPRE |
| | | 010 LDO1 |
| | | 011 LDO2 |
| | | 100 BUCK2 |
| | | 101 BUCK3 |
| | | 11x External regulator |
| | | Reset condition: POR |

16.14 M_LVB1_SVS register

Table 32. M_LVB1_SVS register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----------|----------|----------|----------|----------|----------|----------|
| Read | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------|----------|----------|----------|---------------|----|----|---|---|
| Read | RESERVED | RESERVED | RESERVED | LVB1_SVS[4:0] | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 33. M_LVB1_SVS register bit description

| Bit | Symbol | Description |
|---------------|---------------|--|
| 12 to 8 | LVB1_SVS[4:0] | Static voltage scaling negative offset |
| | | 00000 0 mV |
| | | 00001 -6.25 mV |
| | | 00010 -12.50 mV |
| | | 00011 -18.75 mV |
| | | 00100 -25 mV |
| | | 00101 -31.25 mV |
| | | 00110 -37.5 mV |
| | | 00111 -43.75 mV |
| | | 01000 -50 mV |
| | | 01001 -56.25 mV |
| | | 01010 -62.5 mV |
| | | 01011 -68.75 mV |
| | | 01100 -75 mV |
| | | 01101 -81.25 mV |
| | | 01110 -87.5 mV |
| | | 01111 -93.75 mV |
| 10000 -100 mV | | |
| | | Reset condition: POR |

16.15 M_MEMORY0 register

Table 34. M_MEMORY0 register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|
| Write | MEMORY0[15:8] | | | | | | | |
| Read | MEMORY0[15:8] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------|--------------|----|----|----|----|----|---|---|
| Write | MEMORY0[7:0] | | | | | | | |
| Read | MEMORY0[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 35. M_MEMORY0 register bit description

| Bit | Symbol | Description |
|---------|---------------|------------------------------------|
| 23 to 8 | MEMORY0[15:0] | Free memory field for data storage |
| | | 0... 16 bits free memory |
| | | ...1 |
| | | Reset condition: POR |

16.16 M_MEMORY1 register

Table 36. M_MEMORY1 register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|
| Write | MEMORY1[15:0] | | | | | | | |
| Read | MEMORY1[15:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------|---------------|----|----|----|----|----|---|---|
| Write | MEMORY1[15:0] | | | | | | | |
| Read | MEMORY1[15:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 37. M_MEMORY1 register bit description

| Bit | Symbol | Description |
|---------|---------------|--|
| 23 to 8 | MEMORY1[15:0] | Free memory field for data storage 0... 16 bits free memory ...1 Reset condition: POR |

16.17 M_DEVICEID register

Table 38. M_DEVICEID register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|----|----|----|------------|----|----|----|
| Read | FMREV[3:0] | | | | MMREV[3:0] | | | |
| Reset | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------|---------------|----|----|----|----|----|---|---|
| Read | DEVICEID[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 39. M_DEVICEID register bit description

| Bit | Symbol | Description |
|----------|---------------|---|
| 23 to 20 | FMREV[3:0] | Full mask revision Full mask revision configured by metal connection Reset condition: POR |
| 19 to 16 | MMREV[3:0] | Metal Mask Revision Metal mask revision configured by metal connection Reset condition: POR |
| 15 to 8 | DEVICEID[7:0] | Device ID x...x Device ID from OTP_DEVICEID[7:0] bits Reset condition: POR |

17 Fail-safe register mapping

17.1 Fail-safe writing registers overview

Table 40. Fail-safe writing registers overview

| Logic | Register name | bit 23 | bit 22 | bit 21 | bit 20 | bit 19 | bit 18 | bit 17 | bit 16 | |
|-----------|--------------------------|----------------------------|---------------------|----------------------------|------------------------|-------------------------|---------------|-------------------------|-----------|---|
| | | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | |
| Fail-safe | FS_I_OVUV_SAFE_REACTION1 | VCOREMON_OV_FS_IMPACT[1:0] | | VCOREMON_UV_FS_IMPACT[1:0] | | 0 | RESERVED | RESERVED | RESERVED | |
| | | RESERVED | RESERVED | RESERVED | 0 | VDDIO_OV_FS_IMPACT[1:0] | | VDDIO_UV_FS_IMPACT[1:0] | | |
| | FS_I_OVUV_SAFE_REACTION2 | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | |
| | | RESERVED | RESERVED | RESERVED | RESERVED | VMON1_OV_FS_IMPACT[1:0] | | VMON1_UV_FS_IMPACT[1:0] | | |
| | FS_I_FSSM | FLT_ERR_CNT_LIMIT[1:0] | | 0 | RESERVED | RESERVED | 0 | RSTB_DUR | 0 | |
| | | RESERVED | 0 | RESERVED | DIS_8s | 0 | 0 | 0 | 0 | |
| | FS_I_SVS | SVS_OFFSET[4:0] | | | | | | 0 | 0 | 0 |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | FS_OVUVREG_STATUS | VCOREMON_OV | VCOREMON_UV | VDDIO_OV | VDDIO_UV | RESERVED | RESERVED | RESERVED | RESERVED | |
| | | RESERVED | RESERVED | VMON1_OV | VMON1_UV | 0 | FS_DIG_REF_OV | FS_OSC_DRIFT | 0 | |
| | FS_SAFE_IOS | PGOOD_DIAG | PGOOD_EVENT | 0 | EXT_RSTB | 0 | 0 | RSTB_EVENT | RSTB_DIAG | |
| | | RSTB_REQ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | FS_DIAG | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | |
| | | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | I2C_FS_CRC | I2C_FS_REQ | RESERVED | |
| | FS_INTB_MASK | 0 | 0 | 0 | 0 | 0 | 0 | RESERVED | RESERVED | |
| | | RESERVED | INT_INH_VMON1_OV_UV | INT_INH_VDDIO_OV_UV | INT_INH_VCOREMON_OV_UV | RESERVED | RESERVED | RESERVED | RESERVED | |
| FS_STATES | 0 | DBG_EXIT | 0 | 0 | OTP_CORRUPT | 0 | REG_CORRUPT | 0 | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |

17.2 Fail-safe reading registers overview

Table 41. Fail-safe reading registers overview

| Logic | Register name | bit 23 | bit 22 | bit 21 | bit 20 | bit 19 | bit 18 | bit 17 | bit 16 |
|-----------|--------------------------|----------------------------|---------------------|----------------------------|------------------------|-------------------------|---------------|-------------------------|-----------|
| | | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 |
| Fail-safe | FS_GRL_FLAGS | FS_COM_G | RESERVED | FS_IO_G | FS_REG_OVUV_G | RESERVED | RESERVED | RESERVED | RESERVED |
| | | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| | FS_I_OVUV_SAFE_REACTION1 | VCOREMON_OV_FS_IMPACT[1:0] | | VCOREMON_UV_FS_IMPACT[1:0] | | RESERVED | RESERVED | RESERVED | RESERVED |
| | | RESERVED | RESERVED | RESERVED | RESERVED | VDDIO_OV_FS_IMPACT[1:0] | | VDDIO_UV_FS_IMPACT[1:0] | |
| | FS_I_OVUV_SAFE_REACTION2 | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| | | RESERVED | RESERVED | RESERVED | RESERVED | VMON1_OV_FS_IMPACT[1:0] | | VMON1_UV_FS_IMPACT[1:0] | |
| | FS_I_FSSM | FLT_ERR_CNT_LIMIT[1:0] | | RESERVED | RESERVED | RESERVED | RESERVED | RSTB_DUR | RESERVED |
| | | RESERVED | RESERVED | RESERVED | DIS_8s | FLT_ERR_CNT[3:0] | | | |
| | FS_I_SVS | SVS_OFFSET[4:0] | | | | | RESERVED | RESERVED | RESERVED |
| | | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| | FS_OVUVREG_STATUS | VCOREMON_OV | VCOREMON_UV | VDDIO_OV | VDDIO_UV | RESERVED | RESERVED | RESERVED | RESERVED |
| | | RESERVED | RESERVED | VMON1_OV | VMON1_UV | RESERVED | FS_DIG_REF_OV | FS_OSC_DRIFT | RESERVED |
| | FS_SAFE_IOS | PGOOD_DIAG | PGOOD_EVENT | PGOOD_SNS | EXT_RSTB | RSTB_DRV | RSTB_SNS | RSTB_EVENT | RSTB_DIAG |
| | | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| | FS_DIAG | RESERVED | RESERVED | RESERVED | RESERVED | ERRMON | RESERVED | RESERVED | RESERVED |
| | | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | I2C_FS_CRC | I2C_FS_REQ | RESERVED |
| | FS_INTB_MASK | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| | | RESERVED | INT_INH_VMON1_OV_UV | INT_INH_VDDIO_OV_UV | INT_INH_VCOREMON_OV_UV | RESERVED | RESERVED | RESERVED | RESERVED |
| | FS_STATES | RESERVED | RESERVED | DBG_MODE | RESERVED | OTP_CORRUPT | RESERVED | REG_CORRUPT | RESERVED |
| | | RESERVED | RESERVED | RESERVED | FSM_STATE[4:0] | | | | |

17.3 FS_GRL_FLAGS register

Table 42. FS_GRL_FLAGS register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----------|---------|---------------|----------|----------|----------|----------|
| Read | FS_COM_G | RESERVED | FS_IO_G | FS_REG_OVUV_G | RESERVED | RESERVED | RESERVED | RESERVED |
| Reset | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------|----------|----------|----------|----------|----------|----------|----------|----------|
| Read | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 43. FS_GRL_FLAGS register bit description

| Bit | Symbol | Description |
|-----|---------------|--|
| 23 | FS_COM_G | Report an issue in the communication (I2C) FS_COM_G = I2C_FS_CRC or I2C_FS_REQ |
| | | 0 No failure |
| | | 1 Failure |
| | | Reset condition: Real time information - cleared when all individual bits are cleared |
| 21 | FS_IO_G | Report an issue in one of the fail-safe IOs FS_IO_G = PGOOD_DIAG or RSTB_DIAG |
| | | 0 No failure |
| | | 1 Failure |
| | | Reset condition: real time information - cleared when all individual bits are cleared |
| 20 | FS_REG_OVUV_G | Report an issue in one of the voltage monitoring (OV or UV) FS_REG_OVUV_G = VCOREMON_OV or VCOREMON_UV or VDDIO_OV or VDDIO_UV or VMON1_OV or VMON1_UV |
| | | 0 No failure |
| | | 1 Failure |
| | | Reset condition: real time information - cleared when all individual bits are cleared |

17.4 FS_I_OVUV_SAFE_REACTION1 register

Table 44. FS_I_OVUV_SAFE_REACTION1 register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------------|----|----------------------------|----|----------|----------|----------|----------|
| Write | VCOREMON_OV_FS_IMPACT[1:0] | | VCOREMON_UV_FS_IMPACT[1:0] | | 0 | RESERVED | RESERVED | RESERVED |
| Read | VCOREMON_OV_FS_IMPACT[1:0] | | VCOREMON_UV_FS_IMPACT[1:0] | | RESERVED | RESERVED | RESERVED | RESERVED |
| Reset | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------|----------|----------|----------|----------|-------------------------|----|-------------------------|---|
| Write | RESERVED | RESERVED | RESERVED | 0 | VDDIO_OV_FS_IMPACT[1:0] | | VDDIO_UV_FS_IMPACT[1:0] | |
| Read | RESERVED | RESERVED | RESERVED | RESERVED | VDDIO_OV_FS_IMPACT[1:0] | | VDDIO_UV_FS_IMPACT[1:0] | |
| Reset | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |

Table 45. FS_I_OVUV_SAFE_REACTION1 register bit description

| Bit | Symbol | Description |
|----------|----------------------------|--------------------------|
| 23 to 22 | VCOREMON_OV_FS_IMPACT[1:0] | Table 87 |
| 21 to 20 | VCOREMON_UV_FS_IMPACT[1:0] | Table 87 |
| 11 to 10 | VDDIO_OV_FS_IMPACT[1:0] | Table 90 |
| 9 to 8 | VDDIO_UV_FS_IMPACT[1:0] | Table 90 |

17.5 FS_I_OVUV_SAFE_REACTION2 register

Table 46. FS_I_OVUV_SAFE_REACTION2 register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----------|----------|----------|----------|----------|----------|----------|
| Write | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Read | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Reset | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------|----------|----------|----------|----------|-------------------------|----|-------------------------|---|
| Write | RESERVED | RESERVED | RESERVED | RESERVED | VMON1_OV_FS_IMPACT[1:0] | | VMON1_UV_FS_IMPACT[1:0] | |
| Read | RESERVED | RESERVED | RESERVED | RESERVED | VMON1_OV_FS_IMPACT[1:0] | | VMON1_UV_FS_IMPACT[1:0] | |
| Reset | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |

Table 47. FS_I_OVUV_SAFE_REACTION2 register bit description

| Bit | Symbol | Description |
|----------|-------------------------|------------------------------|
| 11 to 10 | VMON1_OV_FS_IMPACT[1:0] | See Table 92 |
| 9 to 8 | VMON1_UV_FS_IMPACT[1:0] | |

17.6 FS_I_FSSM register

Table 48. FS_I_FSSM register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------------|----|----------|----------|----------|----------|----------|----------|
| Write | FLT_ERR_CNT_LIMIT[1:0] | | 0 | RESERVED | RESERVED | 0 | RSTB_DUR | 0 |
| Read | FLT_ERR_CNT_LIMIT[1:0] | | RESERVED | RESERVED | RESERVED | RESERVED | RSTB_DUR | RESERVED |
| Reset | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------|----------|----------|----------|--------|------------------|----|---|---|
| Write | RESERVED | 0 | RESERVED | DIS_8s | 0 | 0 | 0 | 0 |
| Read | RESERVED | RESERVED | RESERVED | DIS_8s | FLT_ERR_CNT[3:0] | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Table 49. FS_I_FSSM register bit description

| Bit | Symbol | Description |
|----------|------------------------|-----------------------------------|
| 23 to 22 | FLT_ERR_CNT_LIMIT[1:0] | See Table 95 |
| 17 | RSTB_DUR | RSTB pulse duration configuration |
| | | 0 10 ms |
| | | 1 1.0 ms |
| | | Reset condition: POR |

| Bit | Symbol | Description |
|--|------------------|--|
| 12 | DIS_8s | Disable 8 s timer |
| | | 0 RSTB low 8 s counter enabled |
| | | 1 RSTB low 8 s counter disabled |
| | | Reset condition: POR |
| 11 to 8 | FLT_ERR_CNT[3:0] | Reflect the value of the fault error counter |
| | | 0000 0 |
| | | 0001 1 |
| | | 0010 2 |
| | | 0011 3 |
| | | 0100 4 |
| | | 0101 5 |
| | | 0110 6 |
| | | 0111 7 |
| | | 1000 8 |
| | | 1001 9 |
| | | 1010 10 |
| | | 1011 11 |
| | | 1100 12 |
| Reset condition: Real time information | | |

17.7 FS_I_SVS register

Table 50. FS_I_SVS register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----------|----------|----------|
| Write | SVS_OFFSET[4:0] | | | | | 0 | 0 | 0 |
| Read | SVS_OFFSET[4:0] | | | | | RESERVED | RESERVED | RESERVED |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------|----------|----------|----------|----------|----------|----------|----------|----------|
| Write | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 51. FS_I_SVS register bit description

| Bit | Symbol | Description |
|----------------|-----------------|--|
| 23 to 19 | SVS_OFFSET[4:0] | Static voltage scaling negative offset |
| | | 0 0000 0 mV |
| | | 0 0001 -6.25 mV |
| | | 0 0010 -12.50 mV |
| | | 0 0011 -18.75 mV |
| | | 0 0100 -25 mV |
| | | 0 0101 -31.25 mV |
| | | 0 0110 -37.5 mV |
| | | 0 0111 -43.75 mV |
| | | 0 1000 -50 mV |
| | | 0 1001 -56.25 mV |
| | | 0 1010 -62.5 mV |
| | | 0 1011 -68.75 mV |
| | | 0 1100 -75 mV |
| | | 0 1101 -81.25 mV |
| | | 0 1110 -87.5 mV |
| | | 0 1111 -93.75 mV |
| 1 0000 -100 mV | | |
| | | Reset condition: POR |

17.8 FS_OVUVREG_STATUS register

Table 52. FS_OVUVREG_STATUS register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------|-------------|----------|----------|----------|----------|----------|----------|
| Write | VCOREMON_OV | VCOREMON_UV | VDDIO_OV | VDDIO_UV | RESERVED | RESERVED | RESERVED | RESERVED |
| Read | VCOREMON_OV | VCOREMON_UV | VDDIO_OV | VDDIO_UV | RESERVED | RESERVED | RESERVED | RESERVED |
| Reset | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|--------------|----------|----------|----------|----------|----------|---------------|--------------|----------|
| Write | RESERVED | RESERVED | VMON1_OV | VMON1_UV | 0 | FS_DIG_REF_OV | FS_OSC_DRIFT | 0 |
| Read | RESERVED | RESERVED | VMON1_OV | VMON1_UV | RESERVED | FS_DIG_REF_OV | FS_OSC_DRIFT | RESERVED |
| Reset | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

Table 53. FS_OVUVREG_STATUS register bit description

| Bit | Symbol | Description |
|-----|---------------|--|
| 23 | VCOREMON_OV | Overvoltage monitoring on VCOREMON |
| | | 0 No overvoltage |
| | | 1 Overvoltage reported on VCOREMON |
| | | Reset condition: POR / clear on write (write '1') |
| 22 | VCOREMON_UV | Undervoltage monitoring on VCOREMON |
| | | 0 No undervoltage |
| | | 1 Undervoltage reported on VCOREMON |
| | | Reset condition: POR / clear on write (write '1') |
| 21 | VDDIO_OV | Overvoltage monitoring on VDDIO |
| | | 0 No overvoltage |
| | | 1 Overvoltage reported on VDDIO |
| | | Reset POR / clear on write (write '1') condition |
| 20 | VDDIO_UV | Undervoltage monitoring on VDDIO |
| | | 0 No undervoltage |
| | | 1 Undervoltage reported on VDDIO |
| | | Reset condition: POR / clear on write (write '1') |
| 13 | VMON1_OV | Overvoltage monitoring on VMON1 |
| | | 0 No overvoltage |
| | | 1 Overvoltage reported on VMON1 |
| | | Reset condition: POR / clear on write (write '1') |
| 12 | VMON1_UV | Undervoltage monitoring on VMON1 |
| | | 0 No undervoltage |
| | | 1 Undervoltage reported on VMON1 |
| | | Reset condition: POR / clear on write (write '1') |
| 9 | FS_DIG_REF_OV | Overvoltage of the internal digital fail-safe reference voltage |
| | | 0 No overvoltage |
| | | 1 Overvoltage reported of the internal digital fail-safe reference voltage |
| | | Reset condition: POR / clear on write (write '1') |
| 8 | FS_OSC_DRIFT | Drift of the fail-safe OSC |
| | | 0 No drift |
| | | 1 Oscillator drift |
| | | Reset condition: POR / clear on write (write '1') |

17.9 FS_SAFE_IOS register

Table 54. FS_SAFE_IOS register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|-------------|-----------|----------|----------|----------|------------|-----------|
| Write | PGOOD_DIAG | PGOOD_EVENT | 0 | EXT_RSTB | 0 | 0 | RSTB_EVENT | RSTB_DIAG |
| Read | PGOOD_DIAG | PGOOD_EVENT | PGOOD_SNS | EXT_RSTB | RSTB_DRV | RSTB_SNS | RSTB_EVENT | RSTB_DIAG |
| Reset | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------|----------|----------|----------|----------|----------|----------|----------|----------|
| Write | RSTB_REQ | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 55. FS_SAFE_IOS register bit description

| Bit | Symbol | Description |
|-----|-------------|---|
| 23 | PGOOD_DIAG | Report a PGOOD Short to High |
| | | 0 No failure |
| | | 1 Short circuit HIGH |
| | | Reset condition: POR / clear on write (write '1') |
| 22 | PGOOD_EVENT | Report a Power GOOD event |
| | | 0 No Power GOOD |
| | | 1 Power GOOD event occurred |
| | | Reset condition: POR / clear on write (write '1') |
| 21 | PGOOD_SNS | Sense of PGOOD pad |
| | | 0 PGOOD pad sensed low |
| | | 1 PGOOD pad sensed high |
| | | Reset condition: Real-time information |
| 20 | EXT_RSTB | Report an external RESET |
| | | 0 No external RESET |
| | | 1 External RESET |
| | | Reset condition: POR / clear on write (write '1') |
| 19 | RSTB_DRV | RSTB driver – digital command |
| | | 0 RSTB driver command sensed low |
| | | 1 RSTB driver command sensed high |
| | | Reset condition: Real-time information |
| 18 | RSTB_SNS | Sense of RSTB pad |
| | | 0 RSTB pad sensed low |
| | | 1 RSTB pad sensed high |
| | | Reset condition: Real-time information |

| Bit | Symbol | Description |
|-----|------------|---|
| 17 | RSTB_EVENT | Report a RSTB event |
| | | 0 No RESET |
| | | 1 RESET occurred |
| | | Reset condition: POR / clear on write (write '1') |
| 16 | RSTB_DIAG | Report a RSTB short to high |
| | | 0 No failure |
| | | 1 Short circuit high |
| | | Reset condition: POR / clear on write (write '1') |
| 15 | RSTB_REQ | Request assertion of RSTB (Pulse) |
| | | 0 No assertion |
| | | 1 RSTB assertion (pulse) |
| | | Reset condition: POR |

17.10 FS_DIAG register

Table 56. FS_DIAG register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----------|----------|----------|----------|----------|----------|----------|
| Write | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Read | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------|----------|----------|----------|----------|----------|------------|------------|----------|
| Write | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | I2C_FS_CRC | I2C_FS_REQ | RESERVED |
| Read | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | I2C_FS_CRC | I2C_FS_REQ | RESERVED |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Table 57. FS_DIAG register bit description

| Bit | Symbol | Description |
|-----|------------|---|
| 10 | I2C_FS_CRC | Invalid fail-safe I2C access (wrong write or read, write to INIT registers in normal mode, wrong address) |
| | | 0 No error |
| | | 1 I2C violation |
| | | Reset condition: POR / clear on write (write '1') |
| 9 | I2C_FS_REQ | Fail-safe I2C communication CRC issue |
| | | 0 No error |
| | | 1 Error detected in the CRC |
| | | Reset condition: POR / clear on write (write '1') |

17.11 FS_INTB_MASK register

Table 58. FS_INTB_MASK register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----------|----------|----------|----------|----------|----------|----------|
| Write | 0 | 0 | 0 | 0 | 0 | 0 | RESERVED | RESERVED |
| Read | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------|----------|---------------------|---------------------|------------------------|----------|----------|----------|----------|
| Write | RESERVED | INT_INH_VMON1_OV_UV | INT_INH_VDDIO_OV_UV | INT_INH_VCOREMON_OV_UV | RESERVED | RESERVED | RESERVED | RESERVED |
| Read | RESERVED | INT_INH_VMON1_OV_UV | INT_INH_VDDIO_OV_UV | INT_INH_VCOREMON_OV_UV | RESERVED | RESERVED | RESERVED | RESERVED |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 59. FS_INTB_MASK register bit description

| Bit | Symbol | Description |
|-----|------------------------|---|
| 14 | INT_INH_VMON1_OV_UV | Inhibit INTERRUPT on VMON1 OV and UV event |
| | | 0 Interrupt NOT MASKED |
| | | 1 Interrupt MASKED |
| | | Reset condition: POR |
| 13 | INT_INH_VDDIO_OV_UV | Inhibit INTERRUPT on VDDIO OV and UV event |
| | | 0 Interrupt NOT MASKED |
| | | 1 Interrupt MASKED |
| | | Reset condition: POR |
| 12 | INT_INH_VCOREMON_OV_UV | Inhibit INTERRUPT on VCOREMON OV and UV event |
| | | 0 Interrupt NOT MASKED |
| | | 1 Interrupt MASKED |
| | | Reset condition: POR |

17.12 FS_STATES register

Table 60. FS_STATES register bit allocation

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----------|----------|----------|-------------|----------|-------------|----------|
| Write | 0 | DBG_EXIT | 0 | 0 | OTP_CORRUPT | 0 | REG_CORRUPT | 0 |
| Read | RESERVED | RESERVED | DBG_MODE | RESERVED | OTP_CORRUPT | RESERVED | REG_CORRUPT | RESERVED |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------|----------|----------|----------|----------------|----|----|---|---|
| Write | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read | RESERVED | RESERVED | RESERVED | FSM_STATE[4:0] | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

Table 61. FS_STATES register bit description

| Bit | Symbol | Description |
|---------|----------------|---|
| 22 | DBG_EXIT | Leave DEBUG mode |
| | | 0 No action |
| | | 1 Leave DEBUG mode |
| | | Reset condition: POR |
| 21 | DBG_MODE | DEBUG mode status |
| | | 0 NOT in DEBUG mode |
| | | 1 In DEBUG mode |
| | | Reset condition: Real-time information |
| 19 | OTP_CORRUPT | OTP bits corruption detection (5 ms cyclic check) |
| | | 0 No error |
| | | 1 OTP CRC error detected |
| | | Reset condition: POR / clear on write (write '1') |
| 16 7 | REG_CORRUPT | INIT register corruption detection (real-time comparison) |
| | | 0 No error |
| | | 1 INIT register content error detected (mismatch between FS_I_Register / FS_I_NOT_Register) |
| | | Reset condition: POR / clear on write (write '1') |
| 12 to 8 | FSM_STATE[4:0] | Report fail-safe state machine current state |
| | | 0 0110 INIT_FS |
| | | Reset condition: Real-time information |

18 OTP bits configuration

18.1 Overview

Table 62. Main OTP_REGISTERS

Legend: **bold** — Regulator behavior in case of TSD, VPRES, and VBOOST slew rate parameters can be changed later by I2C.

| Name | Address | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 | |
|-----------------|---------|-----------------|------------------|----------------------|----------------|-------------------|-----------------------|----------------------|---------------|--|
| OTP_CFG_VPRE_1 | 14 | 0 | 0 | VPREV[5:0] | | | | | | |
| OTP_CFG_VPRE_2 | 15 | 0 | 0 | VPRESC[5:0] | | | | | | |
| OTP_CFG_VPRE_3 | 16 | VPREILIM[1:0] | | 1 | 0 | 1 | 1 | VPRESRHS[1:0] | | |
| OTP_CFG_BOOST_1 | 17 | 0 | 0 | VPRE_MODE | 0 | VBSTV[3:0] | | | | |
| OTP_CFG_BOOST_2 | 18 | BOOSTEN | VBSTTONTIME[1:0] | | VBSTSC[4:0] | | | | | |
| OTP_CFG_BOOST_3 | 19 | 0 | 0 | 0 | 0 | 0 | 1 | VBSTSR[1:0] | | |
| OTP_CFG_BUCK1_1 | 1A | VB1V[7:0] | | | | | | | | |
| OTP_CFG_BUCK1_2 | 1B | 0 | 0 | 0 | VB1INDOPT[1:0] | | VB1SWILIM[1:0] | | VB12M ULTI PH | |
| OTP_CFG_BUCK2_1 | 1C | VB2V[7:0] | | | | | | | | |
| OTP_CFG_BUCK2_2 | 1D | 0 | VB2INDOPT[1:0] | | BUCK2EN | VB2SWILIM[1:0] | | 0 | 0 | |
| OTP_CFG_BUCK3_1 | 1E | BUCK3EN | VB3INDOPT[1:0] | | VB3V[4:0] | | | | | |
| OTP_CFG_BUCK3_2 | 1F | VB2GMCOMP[2:0] | | | VB1GMCOMP[2:0] | | | VB3SWILIM[1:0] | | |
| OTP_CFG_LDO | 20 | LDO2ILIM | LDO2V[2:0] | | | LDO1ILIM | LDO1V[2:0] | | | |
| OTP_CFG_SEQ_1 | 21 | 0 | 0 | VB2S[2:0] | | | VB1S[2:0] | | | |
| OTP_CFG_SEQ_2 | 22 | 0 | 0 | LDO2S[2:0] | | | LDO1S[2:0] | | | |
| OTP_CFG_SEQ_3 | 23 | DVS_BUCK12[1:0] | | DVS_BUCK3[1:0] | | Tslot | 0 | VB3S[2:0] | | |
| OTP_CFG_CLOCK_1 | 24 | 0 | 0 | VPRE_ph[2:0] | | | 1 | 0 | 0 | |
| OTP_CFG_CLOCK_2 | 25 | 0 | 0 | BUCK1_ph[2:0] | | | VBST_ph[2:0] | | | |
| OTP_CFG_CLOCK_3 | 26 | 0 | 0 | BUCK3_ph[2:0] | | | BUCK2_ph[2:0] | | | |
| OTP_CFG_CLOCK_4 | 27 | BUCK3_clk_sel | BUCK2_clk_sel | BUCK1_clk_sel | VBST_clk_sel | VPRE_clk_sel | PLL_sel | 0 | 1 | |
| OTP_CFG_SM_1 | 28 | 0 | 0 | conf_TSD[5:0] | | | | | | |
| OTP_CFG_SM_2 | 29 | 0 | 0 | 0 | VPRE_off_dly | 1 | 1 | PSYNC_CFG | PSYNC_EN | |
| OTP_CFG_VSUP_UV | 2A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VSUPCFG | |
| OTP_CFG_I2C | 2B | 0 | 0 | 0 | 0 | M_I2CDEVADDR[3:0] | | | | |
| OTP_CFG_OV | 2C | 0 | 0 | 0 | 0 | 0 | VDDIO_REG_ASSIGN[2:0] | | | |
| OTP_CFG_DEVID | 2D | DeviceID[7:0] | | | | | | | | |

Table 63. Fail-safe OTP_REGISTERS

| Name | Address | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|--------------------|---------|----------------|------------|--------------------|----------------------|--------------------|--------------------|-------------|---------------|
| OTP_CFG_UVOV_1 | 0A | VCORE_V[7:0] | | | | | | | |
| OTP_CFG_UVOV_2 | 0B | VDDIOOVTH[3:0] | | | | VCOREOVTH[3:0] | | | |
| OTP_CFG_UVOV_3 | 0C | 0 | 0 | VDDIO_V | VCORE_SVS_CLAMP[4:0] | | | | |
| OTP_CFG_UVOV_4 | 0D | 0 | 0 | 0 | 0 | VMON1OVTH[3:0] | | | |
| OTP_CFG_UVOV_5 | 0E | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| OTP_CFG_UVOV_6 | 0F | VDDIOUVTH[3:0] | | | | VCOREUVTH[3:0] | | | |
| OTP_CFG_UVOV_7 | 10 | 0 | 0 | 0 | 0 | VMON1UVTH[3:0] | | | |
| OTP_CFG_UVOV_8 | 11 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| OTP_CFG_PGOOD | 12 | 0 | PGOOD_RSTB | 0 | 0 | 0 | PGOOD_VMON1 | PGOOD_VDDIO | PGOOD_VCORE |
| OTP_CFG_ABIST1 | 13 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| OTP_CFG_ASIL | 14 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | VMON1_EN |
| OTP_CFG_I2C | 15 | 0 | 0 | 0 | 0 | FS_I2CDEVADDR[3:0] | | | |
| OTP_CFG_DGLT_DUR_1 | 16 | 0 | 0 | VCORE_UV_DGLT[1:0] | | VCORE_OV_DGLT | VDDIO_UV_DGLT[1:0] | | VDDIO_OV_DGLT |
| OTP_CFG_DGLT_DUR_2 | 17 | 0 | 0 | 0 | 0 | 0 | VMON1_UV_DGLT[1:0] | | VMON1_OV_DGLT |

18.2 Main OTP bit description

Table 64. Main OTP bit description

| Address | Register | Bit | Symbol | Value | Description |
|---------|----------------|--------|-------------|---------|-------------------------|
| 14 | OTP_CFG_VPRE_1 | 5 to 0 | VPREV[5:0] | | VPRE output voltage |
| | | | | 00 1111 | 3.3 V |
| | | | | 01 0100 | 3.8 V |
| | | | | 01 0111 | 4.1 V |
| | | | | 10 0000 | 5.0 V |
| 15 | OTP_CFG_VPRE_2 | 5 to 0 | VPRESC[5:0] | | VPRE slope compensation |
| | | | | 00 0100 | 40 mV/μs |
| | | | | 00 0101 | 50 mV/μs |
| | | | | 00 0110 | 60 mV/μs |
| | | | | 00 0111 | 70 mV/μs |
| | | | | 00 1000 | 80 mV/μs |
| | | | | 00 1001 | 90 mV/μs |
| | | | | 00 1010 | 100 mV/μs |
| | | | | 00 1110 | 140 mV/μs |
| | | | | 01 0001 | 170 mV/μs |
| | | | | 01 0100 | 200 mV/μs |
| | | | | 01 1000 | 240 mV/μs |

| Address | Register | Bit | Symbol | Value | Description | | |
|---------|-----------------|--------|------------------|--------|--|---|-------------------------------|
| 16 | OTP_CFG_VPRE_3 | 7 to 6 | VPREILIM[1:0] | | VPRE current limitation threshold | | |
| | | | | 00 | 50 mV | | |
| | | | | 01 | 80 mV | | |
| | | | | 10 | 120 mV | | |
| | | 3 to 2 | VPRESRLS[1:0] | | VPRE low-side slew rate control | | |
| | | | | 11 | PU/PD/900 mA | | |
| | | 1 to 0 | VPRESRHS[1:0] | | VPRE high-side slew rate control | | |
| | | | | 00 | PU/PD/130 mA | | |
| | | | | 01 | PU/PD/260 mA | | |
| | | | | 10 | PU/PD/520 mA | | |
| | | 17 | OTP_CFG_BOOST_1 | 5 | VPRE_MODE | | VPRE mode (PWM, APS) |
| | | | | | | 0 | Force PWM for 455 kHz setting |
| 3 to 0 | VBSTV[3:0] | | | 1 | Automatic Pulse Skipping (APS) for 2.2 MHz setting | | |
| | | | | | VBOOST output voltage | | |
| | | | | 0110 | 5.0 V | | |
| 1101 | 5.74 V | | | | | | |
| 18 | OTP_CFG_BOOST_2 | 7 | BOOSTEN | | BOOST enable | | |
| | | | | 0 | Disabled | | |
| | | 6 to 5 | VBSTTONTIME[1:0] | 1 | Enabled | | |
| | | | | | BOOST minimum ON time | | |
| | | 4 to 0 | VBSTSC[4:0] | 00 | 60 ns | | |
| | | | | 01 | 50 ns | | |
| | | | | | VBOOST slope compensation | | |
| | | | | 0 0110 | 160 mV/μs | | |
| | | | | 0 1100 | 125 mV/μs | | |
| | | | | 0 1110 | 79 mV/μs | | |
| 19 | OTP_CFG_BOOST_3 | 1 to 0 | VBSTSR[1:0] | | VBOOST low-side slew rate control | | |
| | | | | 10 | 300 V/μs | | |
| | | | | 11 | 500 V/μs | | |

| Address | Register | Bit | Symbol | Value | Description | | |
|-----------|-----------------|--------|----------------|-----------|--------------------------|--|---|
| 1A | OTP_CFG_BUCK1_1 | 7 to 0 | VB1V[7:0] | | VBUCK1 output voltage | | |
| | | | | 0100 0000 | 0.8 V | | |
| | | | | 0100 0100 | 0.825 V | | |
| | | | | 0101 0000 | 0.9 V | | |
| | | | | 0101 1000 | 0.95 V | | |
| | | | | 0110 0000 | 1.0 V | | |
| | | | | 01100100 | 1.025 V | | |
| | | | | 0110 0101 | 1.03125 V | | |
| | | | | 0111 0000 | 1.1 V | | |
| | | | | 1000 0000 | 1.2 V | | |
| | | | | 1000 1000 | 1.25 V | | |
| | | | | 1001 0000 | 1.3 V | | |
| | | | | 1001 1000 | 1.35 V | | |
| | | | | 1010 0000 | 1.4 V | | |
| 1011 0000 | 1.5 V | | | | | | |
| 1011 0001 | 1.8 V | | | | | | |
| 1B | OTP_CFG_BUCK1_2 | 4 to 3 | VB1INDOPT[1:0] | | BUCK1 inductor selection | | |
| | | | | 00 | 1 μ H | | |
| | | | | 01 | 0.47 μ H | | |
| | | | | 2 to 1 | VB1SWILIM{1:0] | | BUCK1 current limitation |
| | | 01 | Reserved | | | | |
| | | | | 0 | VB12MULTIPH | | VBUCK1 and VBUCK2 multiphase operation enable |
| | | 0 | Disabled | | | | |
| | | 1 | Enabled | | | | |

| Address | Register | Bit | Symbol | Value | Description |
|-----------|-----------------|--------|----------------|-----------|--------------------------|
| 1C | OTP_CFG_BUCK2_1 | 7 to 0 | VB2V[7:0] | | VBUCK2 output voltage |
| | | | | 0100 0000 | 0.8 V |
| | | | | 0100 0100 | 0.825 V |
| | | | | 0101 0000 | 0.9 V |
| | | | | 0101 1000 | 0.95 V |
| | | | | 0110 0000 | 1.0 V |
| | | | | 01100100 | 1.025 V |
| | | | | 0110 0101 | 1.03125 V |
| | | | | 0111 0000 | 1.1 V |
| | | | | 1000 0000 | 1.2 V |
| | | | | 1000 1000 | 1.25 V |
| | | | | 1001 0000 | 1.3 V |
| | | | | 1001 1000 | 1.35 V |
| | | | | 1010 0000 | 1.4 V |
| 1011 0000 | 1.5 V | | | | |
| 1011 0001 | 1.8 V | | | | |
| 1D | OTP_CFG_BUCK2_2 | 6 to 5 | VB2INDOPT[1:0] | | BUCK2 inductor selection |
| | | | | 00 | 1 μ H |
| | | | | 01 | 0.47 μ H |
| | | | | 10 | 1.5 μ H |
| | | 4 | BUCK2EN | | BUCK2 enable |
| | | | | 0 | Disabled |
| | | | | 1 | Enabled |
| | | 3 to 2 | VB2SWILIM[1:0] | | BUCK2 current limitation |
| | | | | 01 | Reserved |
| | | | | 11 | 4.5 A |
| | | | | | |

| Address | Register | Bit | Symbol | Value | Description |
|---------|-----------------|--------|----------------|--------|----------------------------|
| 1E | OTP_CFG_BUCK3_1 | 7 | BUCK3EN | | BUCK3 enable |
| | | | | 0 | Disabled |
| | | | | 1 | Enabled |
| | | 6 to 5 | VB3INDOPT[1:0] | | BUCK3 inductor selection |
| | | | | 00 | 1 μ H |
| | | | | 01 | 0.47 μ H |
| | | | | 10 | 1.5 μ H |
| | | 4 to 0 | VB3V[4:0] | | VBUCK3 output voltage |
| | | | | 0 0000 | 1.0 V |
| | | | | 0 0001 | 1.1 V |
| | | | | 0 0010 | 1.2 V |
| | | | | 0 0011 | 1.25 V |
| | | | | 0 0100 | 1.3 V |
| | | | | 0 0101 | 1.35 V |
| | | | | 0 0110 | 1.5 V |
| | | | | 0 0111 | 1.6 V |
| | | | | 0 1000 | 1.8 V |
| | | | | 0 1110 | 2.3 V |
| | | | | 1 0000 | 2.5 V |
| 1F | OTP_CFG_BUCK3_2 | 7 to 5 | VB2GMCOMP[2:0] | | BUCK2 compensation network |
| | | | | 001 | 16.25 GM |
| | | | | 010 | 32.5 GM |
| | | | | 011 | 48.75 GM |
| | | | | 100 | 65 GM |
| | | | | 101 | 81.25 GM |
| | | | | 110 | 97.5 GM |
| | | 4 to 2 | VB1GMCOMP[2:0] | | BUCK1 compensation network |
| | | | | 001 | 16.25 GM |
| | | | | 010 | 32.5 GM |
| | | | | 011 | 48.75 GM |
| | | | | 100 | 65 GM |
| | | | | 101 | 81.25 GM |
| | | 1 to 0 | VB3SWLIM[1:0] | | BUCK3 current limitation |
| | | | | 01 | 2.6 A |
| | | | 11 | 4.5 A | |

| Address | Register | Bit | Symbol | Value | Description |
|---------|-------------|--------|------------|-------|--------------------------|
| 20 | OTP_CFG_LDO | 7 | LDO2ILIM | | VLDO2 current limitation |
| | | | | 0 | 400 mA |
| | | | | 1 | 150 mA |
| | | 6 to 4 | LDO2V[2:0] | | VLDO2 output voltage |
| | | | | 000 | 1.1 V |
| | | | | 001 | 1.2 V |
| | | | | 010 | 1.6 V |
| | | | | 011 | 1.8 V |
| | | | | 100 | 2.5 V |
| | | | | 101 | 2.8 V |
| | | | | 110 | 3.3 V |
| | | | | 111 | 5.0 V |
| | | 3 | LDO1ILIM | | VLDO1 current limitation |
| | | | | 0 | 400 mA |
| | | | | 1 | 150 mA |
| | | 2 to 0 | LDO1V[2:0] | | VLDO1 output voltage |
| | | | | 000 | 1.1 V |
| | | | | 001 | 1.2 V |
| | | | | 010 | 1.6 V |
| 011 | 1.8 V | | | | |
| 100 | 2.5 V | | | | |
| 101 | 2.8 V | | | | |
| 110 | 3.3 V | | | | |
| 111 | 5.0 V | | | | |

| Address | Register | Bit | Symbol | Value | Description |
|---------|---|--------|---|-------|------------------------------------|
| 21 | OTP_CFG_SEQ_1 | 5 to 3 | VB2S[2:0] | | BUCK2 sequencing slot |
| | | | | 000 | Regulator start and stop in Slot 0 |
| | | | | 001 | Regulator start and stop in Slot 1 |
| | | | | 010 | Regulator start and stop in Slot 2 |
| | | | | 011 | Regulator start and stop in Slot 3 |
| | | | | 100 | Regulator start and stop in Slot 4 |
| | | | | 101 | Regulator start and stop in Slot 5 |
| | | 110 | Regulator start and stop in Slot 6 | | |
| | | 111 | Regulator does not start (enabled by I2C) | | |
| | | 2 to 0 | VB1S[2:0] | | BUCK1 sequencing slot |
| | | | | 000 | Regulator start and stop in Slot 0 |
| | | | | 001 | Regulator start and stop in Slot 1 |
| | | | | 010 | Regulator start and stop in Slot 2 |
| | | | | 011 | Regulator start and stop in Slot 3 |
| 100 | Regulator start and stop in Slot 4 | | | | |
| 101 | Regulator start and stop in Slot 5 | | | | |
| 110 | Regulator start and stop in Slot 6 | | | | |
| 111 | Regulator does not start (enabled by I2C) | | | | |

| Address | Register | Bit | Symbol | Value | Description |
|---------|----------------|--------|---------------------------------------|-------|---|
| 22 | OTP_CFG_SEQ_2 | 5 to 3 | LDO2S[2:0] | | LDO2 sequencing slot |
| | | | | 000 | Regulator start and stop in Slot 0 |
| | | | | 001 | Regulator start and stop in Slot 1 |
| | | | | 010 | Regulator start and Stop in Slot 2 |
| | | | | 011 | Regulator start and stop in Slot 3 |
| | | | | 100 | Regulator start and stop in Slot 4 |
| | | | | 101 | Regulator start and stop in Slot 5 |
| | | | | 110 | Regulator start and stop in Slot 6 |
| | | | | 111 | Regulator does not start (enabled by I2C) |
| | | 2 to 0 | LDO1S[2:0] | | LDO1 sequencing slot |
| | | | | 000 | Regulator start and stop in Slot 0 |
| | | | | 001 | Regulator start and stop in Slot 1 |
| | | | | 010 | Regulator start and stop in Slot 2 |
| | | | | 011 | Regulator start and stop in Slot 3 |
| | | | | 100 | Regulator start and stop in Slot 4 |
| | | | | 101 | Regulator start and stop in Slot 5 |
| | | | | 110 | Regulator start and stop in Slot 6 |
| | | | | 111 | Regulator does not start (enabled by I2C) |
| | | | | 23 | OTP_CFG_SEQ_3 |
| 00 | 7.81 mV/μs | | | | |
| 01 | 3.13 mV/μs | | | | |
| 10 | 2.6 mV/μs | | | | |
| 11 | 2.23 mV/μs | | | | |
| 5 to 4 | DVS_BUCK3[1:0] | | BUCK3 soft start/stop configurability | | |
| | | 00 | 10.41 mV/μs | | |
| | | 01 | 3.47 mV/μs | | |
| | | 10 | 2.6 mV/μs | | |
| 3 | Tslot | | Power up/down slot duration | | |
| | | 01 | 3.47 mV/μs | | |
| | | 10 | 2.6 mV/μs | | |
| | | 11 | 2.08 mV/μs | | |

| Address | Register | Bit | Symbol | Value | Description |
|---------|-----------------|--------|--------------|-------|---|
| | | | | 0 | 250 μ s |
| | | | | 1 | 1.0 ms |
| | | 2 to 0 | VB3S[2:0] | | BUCK3 sequencing slot |
| | | | | 000 | Regulator start and stop in Slot 0 |
| | | | | 001 | Regulator start and stop in Slot 1 |
| | | | | 010 | Regulator start and Stop in Slot 2 |
| | | | | 011 | Regulator start and stop in Slot 3 |
| | | | | 100 | Regulator start and stop in Slot 4 |
| | | | | 101 | Regulator start and stop in Slot 5 |
| | | | | 110 | Regulator start and stop in Slot 6 |
| | | | | 111 | Regulator does not start (enabled by I2C) |
| 24 | OTP_CFG_CLOCK_1 | 5 to 3 | VPRE_ph[2:0] | | VPRE phase (delay) selection |
| | | | | 000 | no delay |
| | | | | 001 | delay 1 |
| | | | | 010 | delay 2 |
| | | | | 011 | delay 3 |
| | | | | 100 | delay 4 |
| | | | | 101 | delay 5 |
| | | | | 110 | delay 6 |
| | | | | 111 | delay 7 |

| Address | Register | Bit | Symbol | Value | Description |
|---------|-----------------|--------|---------------|-------|--------------------------------|
| 25 | OTP_CFG_CLOCK_2 | 5 to 3 | BUCK1_ph[2:0] | | VBUCK1 phase (delay) selection |
| | | | | 000 | no delay |
| | | | | 001 | delay 1 |
| | | | | 010 | delay 2 |
| | | | | 011 | delay 3 |
| | | | | 100 | delay 4 |
| | | | | 101 | delay 5 |
| | | 110 | delay 6 | | |
| | | 111 | delay 7 | | |
| | | 2 to 0 | VBST_ph[2:0] | | VBOOST phase (delay) selection |
| | | | | 000 | no delay |
| | | | | 001 | delay 1 |
| | | | | 010 | delay 2 |
| | | | | 011 | delay 3 |
| 100 | delay 4 | | | | |
| 101 | delay 5 | | | | |
| 110 | delay 6 | | | | |
| 111 | delay 7 | | | | |
| 26 | OTP_CFG_CLOCK_3 | 5 to 3 | BUCK3_ph[2:0] | | VBUCK3 phase (delay) selection |
| | | | | 000 | no delay |
| | | | | 001 | delay 1 |
| | | | | 010 | delay 2 |
| | | | | 011 | delay 3 |
| | | | | 100 | delay 4 |
| | | | | 101 | delay 5 |
| | | 110 | delay 6 | | |
| | | 111 | delay 7 | | |
| | | 2 to 0 | BUCK2_ph[2:0] | | VBUCK2 phase (delay) selection |
| | | | | 000 | no delay |
| | | | | 001 | delay 1 |
| | | | | 010 | delay 2 |
| | | | | 011 | delay 3 |
| 100 | delay 4 | | | | |
| 101 | delay 5 | | | | |
| 110 | delay 6 | | | | |
| 111 | delay 7 | | | | |

| Address | Register | Bit | Symbol | Value | Description | | |
|---------|-----------------|--------|---------------|-------|-------------------------------|---|----------------------|
| 27 | OTP_CFG_CLOCK_4 | 7 | BUCK3_clk_sel | | BUCK3 clock selection | | |
| | | | | 0 | CLK_DIV1 = 2.22 MHz | | |
| | | 6 | BUCK2_clk_sel | | BUCK2 clock selection | | |
| | | | | 0 | CLK_DIV1 = 2.22 MHz | | |
| | | 5 | BUCK1_clk_sel | | BUCK1 clock selection | | |
| | | | | 0 | CLK_DIV1 = 2.22 MHz | | |
| | | 4 | VBST_clk_sel | | VBOOST clock selection | | |
| | | | | 0 | CLK_DIV1 = 2.22 MHz | | |
| | | 3 | VPRE_clk_sel | | VPRE clock selection | | |
| | | | | 0 | CLK_DIV1 = 2.22 MHz | | |
| | | | | 1 | CLK_DIV2 = 455 kHz | | |
| | | 2 | PLL_sel | | PLL enable | | |
| | | | | 0 | Disabled | | |
| | | | | 1 | Enabled | | |
| 28 | OTP_CFG_SM_1 | 5 to 0 | conf_TSD[5] | | BOOST behavior in case of TSD | | |
| | | | | 0 | BOOST shutdown | | |
| | | | | 1 | BOOST shutdown + DFS | | |
| | | | conf_TSD[4] | | BUCK1 behavior in case of TSD | 0 | BUCK1 shutdown |
| | | | | | | 1 | BUCK1 shutdown + DFS |
| | | | conf_TSD[3] | | BUCK2 behavior in case of TSD | 0 | BUCK2 shutdown |
| | | | | | | 1 | BUCK2 shutdown + DFS |
| | | | conf_TSD[2] | | BUCK3 behavior in case of TSD | 0 | BUCK3 shutdown |
| | | | | | | 1 | BUCK3 Shutdown + DFS |
| | | | conf_TSD[1] | | LDO1 behavior in case of TSD | 0 | LDO1 shutdown |
| | | | | | | 1 | LDO1 shutdown + DFS |
| | | | conf_TSD[0] | | LDO2 behavior in case of TSD | 0 | LDO2 shutdown |
| | | | | | | 1 | LDO2 shutdown + DFS |

| Address | Register | Bit | Symbol | Value | Description | |
|---------|-----------------|--------|-----------------------|-------|--|----------------------------------|
| 29 | OTP_CFG_SM_2 | 4 | VPRE_off_dly | | Delay to turn OFF VPRES at device power down | |
| | | | | 0 | 250 μs | |
| | | | | 1 | 32 ms | |
| | | 1 | PSYNC_CFG | | | Power up synchronization |
| | | | | 0 | 2x VR5500 | |
| | | | | 1 | 1x VR5500 and 1x external PMIC | |
| | | 0 | PSYNC_EN | | | Synchronization with two devices |
| | | | | 0 | Disabled | |
| | | | | 1 | Enabled | |
| 2A | OTP_CFG_VSUP_UV | 0 | VSUP_CFG | | VSUP undervoltage threshold configuration | |
| | | | | 0 | 4.9 V for Vpre < 4.5 V | |
| | | | | 1 | 6.2 V for Vpre > 4.5 V | |
| 2B | OTP_CFG_I2C | 3 to 0 | M_I2CDEVADDR[3:0] | | Device I2C address | |
| | | | | 0000 | Address D0 | |
| | | | | ... | ... | |
| | | | | 1111 | Address D15 | |
| 2C | OTP_CFG_OV | 2 to 0 | VDDIO_REG_ASSIGN[2:0] | | Regulator assigned to VDDIO | |
| | | | | 000 | External regulator | |
| | | | | 001 | VPRE | |
| | | | | 010 | LDO1 | |
| | | | | 011 | LDO2 | |
| | | | | 100 | BUCK3 | |
| | | | | 101 | External regulator | |
| | | | | 110 | External regulator | |
| | | | | 111 | External regulator | |
| 2D | OTP_CFG_DEVID | 7 to 0 | DeviceID[7:0] | | Device ID | |

18.3 Fail-safe OTP bit description

Table 65. Fail-safe OTP bit description

| Address | Register | Bit | Symbol | Value | Description |
|-----------|----------------|--------|--------------|-----------|-----------------------------------|
| 0A | OTP_CFG_UVOV_1 | 7 to 0 | VCORE_V[7:0] | | VCORE (VBUCK1) monitoring voltage |
| | | | | 0100 0000 | 0.8 V |
| | | | | 0100 0100 | 0.825 V |
| | | | | 0101 0000 | 0.9 V |
| | | | | 0101 1000 | 0.95 V |
| | | | | 0110 0000 | 1 V |
| | | | | 01100100 | 1.025 V |
| | | | | 0110 0101 | 1.03125 V |
| | | | | 0110 0000 | 1.1 V |
| | | | | 1000 0000 | 1.2 V |
| | | | | 1000 1000 | 1.25 V |
| | | | | 1001 0000 | 1.3 V |
| | | | | 1001 1000 | 1.35 V |
| | | | | 1010 0000 | 1.4 V |
| | | | | 1011 0000 | 1.5 V |
| 1011 0001 | 1.8 V | | | | |

| Address | Register | Bit | Symbol | Value | Description |
|---------|----------------|--------|----------------------|-------|--|
| 0B | OTP_CFG_UVOV_2 | 7 to 4 | VDDIOOVTH[3:0] | | VDDIO overvoltage threshold configuration |
| | | | | 0000 | 104.5 % |
| | | | | 0001 | 105 % |
| | | | | 0010 | 105.5 % |
| | | | | 0011 | 106 % |
| | | | | 0100 | 106.5 % |
| | | | | 0101 | 107 % |
| | | | | 0110 | 107.5 |
| | | | | 0111 | 108 % |
| | | | | 1000 | 108.5 % |
| | | | | 1001 | 109 % |
| | | | | 1010 | 109.5 % |
| | | | | 1011 | 110 % |
| | | | | 1100 | 110.5 % |
| | | 1101 | 111 % | | |
| | | 1110 | 111.5 % | | |
| | | 1111 | 112 % | | |
| | | 3 to 0 | VCOREOVTH[3:0] | | VCOREMON overvoltage threshold configuration |
| | | | | 0000 | 104.5 % |
| | | | | 0001 | 105 % |
| | | | | 0010 | 105.5 % |
| | | | | 0011 | 106 % |
| | | | | 0100 | 106.5 % |
| | | | | 0101 | 107 % |
| | | | | 0110 | 107.5 |
| | | | | 0111 | 108 % |
| 1000 | 108.5 % | | | | |
| 1001 | 109 % | | | | |
| 1010 | 109.5 % | | | | |
| 1011 | 110 % | | | | |
| 1100 | 110.5 % | | | | |
| 1101 | 111 % | | | | |
| 1110 | 111.5 % | | | | |
| 1111 | 112 % | | | | |
| 0C | OTP_CFG_UVOV_3 | 5 | VDDIO_V | | VDDIO voltage selection |
| | | | | 0 | 3.3 V |
| | | | | 1 | 5 V |
| | | 4 to 0 | VCORE_SVS_CLAMP[4:0] | | SVS max value allowed (mask) |
| | | | | 00000 | 2 steps available (-12.5 mV) |
| | | | | 00001 | 4 steps available (-25 mV) |

| Address | Register | Bit | Symbol | Value | Description |
|---------|----------------|--------|----------------|-------|---|
| | | | | 00011 | 8 steps available (-50 mV) |
| | | | | 00100 | 16 steps available (-100 mV) |
| 0D | OTP_CFG_UVOV_4 | 3 to 0 | VMON1OVTH[3:0] | | VMON1 overvoltage threshold configuration |
| | | | | 0000 | 104.5 % |
| | | | | 0001 | 105 % |
| | | | | 0010 | 105.5 % |
| | | | | 0011 | 106 % |
| | | | | 0100 | 106.5 % |
| | | | | 0101 | 107 % |
| | | | | 0110 | 107.5 |
| | | | | 0111 | 108 % |
| | | | | 1000 | 108.5 % |
| | | | | 1001 | 109 % |
| | | | | 1010 | 109.5 % |
| | | | | 1011 | 110 % |
| | | | | 1100 | 110.5 % |
| | | | | 1101 | 111 % |
| | | | | 1110 | 111.5 % |
| | | | | 1111 | 112 % |

| Address | Register | Bit | Symbol | Value | Description | | |
|---------|----------------|--------|----------------|-------|--|------|---|
| 0F | OTP_CFG_UVOV_6 | 7 to 4 | VDDIOUVTH[3:0] | | VDDIO undervoltage threshold configuration | | |
| | | | | 0000 | 95.5 % | | |
| | | | | 0001 | 95 % | | |
| | | | | 0010 | 94.5 % | | |
| | | | | 0011 | 94 % | | |
| | | | | 0100 | 93.5 % | | |
| | | | | 0101 | 93 % | | |
| | | | | 0110 | 92.5 % | | |
| | | | | 0111 | 92 % | | |
| | | | | 1000 | 91.5 % | | |
| | | | | 1001 | 91 % | | |
| | | | | 1010 | 90.5 % | | |
| | | | | 1011 | 90 % | | |
| | | | | 1100 | 89.5 % | | |
| | | | | 1101 | 89 % | | |
| | | | | 1110 | 88.5 % | | |
| | | 1111 | 88 % | | | | |
| | | 3 to 0 | VCOREUVTH[3:0] | | | | VCOREMON undervoltage threshold configuration |
| | | | | | | 0000 | 95.5 % |
| | | | | | | 0001 | 95 % |
| | | | | | | 0010 | 94.5 % |
| | | | | | | 0011 | 94 % |
| | | | | | | 0100 | 93.5 % |
| | | | | | | 0101 | 93 % |
| | | | | | | 0110 | 92.5 % |
| | | | | | | 0111 | 92 % |
| | | | | | | 1000 | 91.5 % |
| | | | | | | 1001 | 91 % |
| 1010 | 90.5 % | | | | | | |
| 1011 | 90 % | | | | | | |
| 1100 | 89.5 % | | | | | | |
| 1101 | 89 % | | | | | | |
| 1110 | 88.5 % | | | | | | |
| 1111 | 88 % | | | | | | |

| Address | Register | Bit | Symbol | Value | Description |
|---------|----------------|--------|--------------------|-------|--|
| 10 | OTP_CFG_UVOV_7 | 3 to 0 | VMON1UVTH[3:0] | | VMON1 undervoltage threshold configuration |
| | | | | 0000 | 95.5 % |
| | | | | 0001 | 95 % |
| | | | | 0010 | 94.5 % |
| | | | | 0011 | 94 % |
| | | | | 0100 | 93.5 % |
| | | | | 0101 | 93 % |
| | | | | 0110 | 92.5 % |
| | | | | 0111 | 92 % |
| | | | | 1000 | 91.5 % |
| | | | | 1001 | 91 % |
| | | | | 1010 | 90.5 % |
| | | | | 1011 | 90 % |
| | | | | 1100 | 89.5 % |
| | | | | 1101 | 89 % |
| | | | | 1110 | 88.5 % |
| 1111 | 88 % | | | | |
| 12 | OTP_CFG_PGOOD | 6 | PGOOD_RSTB | | RSTB assignment to PGOOD |
| | | | | 0 | Not assigned |
| | | 1 | Assigned | | |
| | | 2 | PGOOD_VMON1 | | VMON1 assignment to PGOOD |
| | | | | 0 | Not assigned |
| | | 1 | Assigned | | |
| | | 1 | PGOOD_VDDIO | | VDDIO assignment to PGOOD |
| | | | | 0 | Not assigned |
| | | 1 | Assigned | | |
| | | 0 | PGOOD_VCORE | | VCORE (BUCK1) assignment to PGOOD |
| | | | | 0 | Not assigned |
| | | 1 | Assigned | | |
| 14 | OTP_CFG_ASIL | 0 | VMON1_EN | | VMON1 monitoring enable |
| | | | | 0 | Disabled |
| | | | | 1 | Enabled |
| 15 | OTP_CFG_I2C | 3 to 0 | FS_I2CDEVADDR[3:0] | | Device I2C address |
| | | | | 0000 | Address D0 |
| | | | | ... | ... |
| | | | | 1111 | Address D15 |

| Address | Register | Bit | Symbol | Value | Description |
|---------|--------------------|--------|--------------------|-------|-----------------------------------|
| 16 | OTP_CFG_DGLT_DUR_1 | 5 to 4 | VCORE_UV_DGLT[1:0] | | VCORE undervoltage filtering time |
| | | | | 00 | 5 μ s |
| | | | | 01 | 15 μ s |
| | | | | 10 | 25 μ s |
| | | | | 11 | 40 μ s |
| | | 3 | VCORE_OV_DGLT | | VCORE overvoltage filtering time |
| | | | | 0 | 25 μ s |
| | | | | 1 | 45 μ s |
| | | 2 to 1 | VDDIO_UV_DGLT[1:0] | | VDDIO undervoltage filtering time |
| | | | | 00 | 5 μ s |
| | | | | 01 | 15 μ s |
| | | | | 10 | 25 μ s |
| | | | | 11 | 40 μ s |
| | | 0 | VDDIO_OV_DGLT | | VDDIO overvoltage filtering time |
| | | | | 0 | 25 μ s |
| | | | | 1 | 45 μ s |
| 17 | OTP_CFG_DGLT_DUR_2 | 2 to 1 | VMON1_UV_DGLT[1:0] | | VMON1 undervoltage filtering time |
| | | | | 00 | 5 μ s |
| | | | | 01 | 15 μ s |
| | | | | 10 | 25 μ s |
| | | | | 11 | 40 μ s |
| | | 0 | VMON1_OV_DGLT | | VMON1 overvoltage filtering time |
| | | | | 0 | 25 μ s |
| | | | | 1 | 45 μ s |

19 Best of supply

19.1 Functional description

VBOS regulator manages the best of supply from VSUP, VPRE, and VBOOST to efficiently generate 5.0 V output to supply the internal biasing of the device. VBOS is also the supply of VPRE high-side and low-side gate drivers and VBOOST low-side gate driver.

VBOS undervoltage may not guarantee the full functionality of the device. Consequently, VBOS_UVL detection powers down the device.

V_{SUP_UV7} undervoltage threshold is used to enable the path from VSUP to VBOS when $VSUP < V_{SUP_UV7}$ to have a low drop path from VSUP, while VPRE is going low and to power up the device when VPRE is not started. When $VSUP > V_{SUP_UV7}$, VBOS is forced to use either VPRE or VBOOST to optimize the efficiency.

19.2 Best of supply electrical characteristics

Table 66. Best of supply electrical characteristics

$T_A = -40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$, unless otherwise specified. $V_{SUP} = V_{SUP_UVH}$ to 36 V, unless otherwise specified. All voltages referenced to ground.

| Symbol | Parameter | Min | Typ | Max | Unit |
|----------------|--|-----|-----|------|---------------|
| V_{BOS} | Best of supply output voltage | 3.3 | 5.0 | 5.25 | V |
| V_{BOS_UVH} | VBOS undervoltage threshold high (VBOS rising) | 4.1 | — | 4.5 | V |
| V_{BOS_UVL} | VBOS undervoltage threshold low (VBOS falling) | 3.2 | — | 3.4 | V |
| T_{BOS_UV} | V_{BOS_UVH} and V_{BOS_UVL} filtering time | 6.0 | 10 | 15 | μs |
| V_{BOS_POR} | VBOS power-on reset threshold | — | — | 2.5 | V |
| T_{BOS_POR} | V_{BOS_POR} filtering time | 0.5 | — | 1.5 | μs |
| I_{BOS} | Best of supply current capability | — | — | 60 | mA |
| C_{OUT_BOS} | Effective output capacitor | 4.7 | — | 10 | μF |
| | Output decoupling capacitor | — | 0.1 | — | μF |

20 High voltage buck: VPRE

20.1 Functional description

VPRE block is a high voltage, synchronous, peak current mode buck controller. VPRE is working with external logical level NMOS in force PWM mode at 455 kHz and in Automatic Pulse Skipping (APS) mode at 2.22 MHz. The APS mode helps to maintain the correct output voltage at high input voltage by skipping some turn ON cycles of the HS FET below the minimum duty cycle. VPRE input voltage is naturally limited to $V_{SUP} = L_{PI_DCR} \times I_{PRE} + V_{PRE_UVL} / D_{MAX}$ with $D_{MAX} = 1 - (F_{PRE_SW} \times T_{PRE_OFF_MIN})$.

A bootstrap capacitor is required to supply the gate drive circuit of the high-side NMOS. The output voltage is configurable by OTP from 3.3 V to 5.0 V, and the switching frequency is configurable by OTP at 455 kHz for 12 V and 24 V transportation applications or 2.22 MHz for 12 V automotive applications. The stability is ensured by an external Type 2 compensation network with slope compensation.

The output current is sensed via an external shunt in series with the inductor and the maximum current capability is defined by the external components (NMOS gate charge, inductor, shunt resistor), the gate driver current capability, and the switching frequency. An overcurrent detection is implemented to protect the external MOSFETs. If an overcurrent is detected after the HS minimum TON time, the HS is turned OFF and will be turned ON again at the next rising edge of the switching clock. The overcurrent induces a duty cycle reduction that could lead to the output voltage gradually dropping, causing an undervoltage condition on VPRE and/or one of the cascaded regulators.

The maximum input voltage is 60 V and allows operation in 24 V truck applications without external protection to sustain ISO 16750-2:2012 load dump pulse 5b. VPRE must be the input supply of the BOOST and BUCK1,2. VPRE can be the input supply of BUCK3 and LDO1. VPRE can be the supply of local loads remaining inside the ECU.

By default, VPRE switching frequency is derived from the internal oscillator, and can be synchronized with an external frequency signal applied at FIN input pin. The change from internal oscillator to external clock or vice versa is controlled by I2C.

V_{PRE_UVH} , V_{PRE_UVL} , and $V_{PRE_FB_OV}$ thresholds are monitored from PRE_FB pin and manage some transitions of the main state machine described in [Section 14.1 "Simplified functional state diagram"](#).

20.2 Application schematic

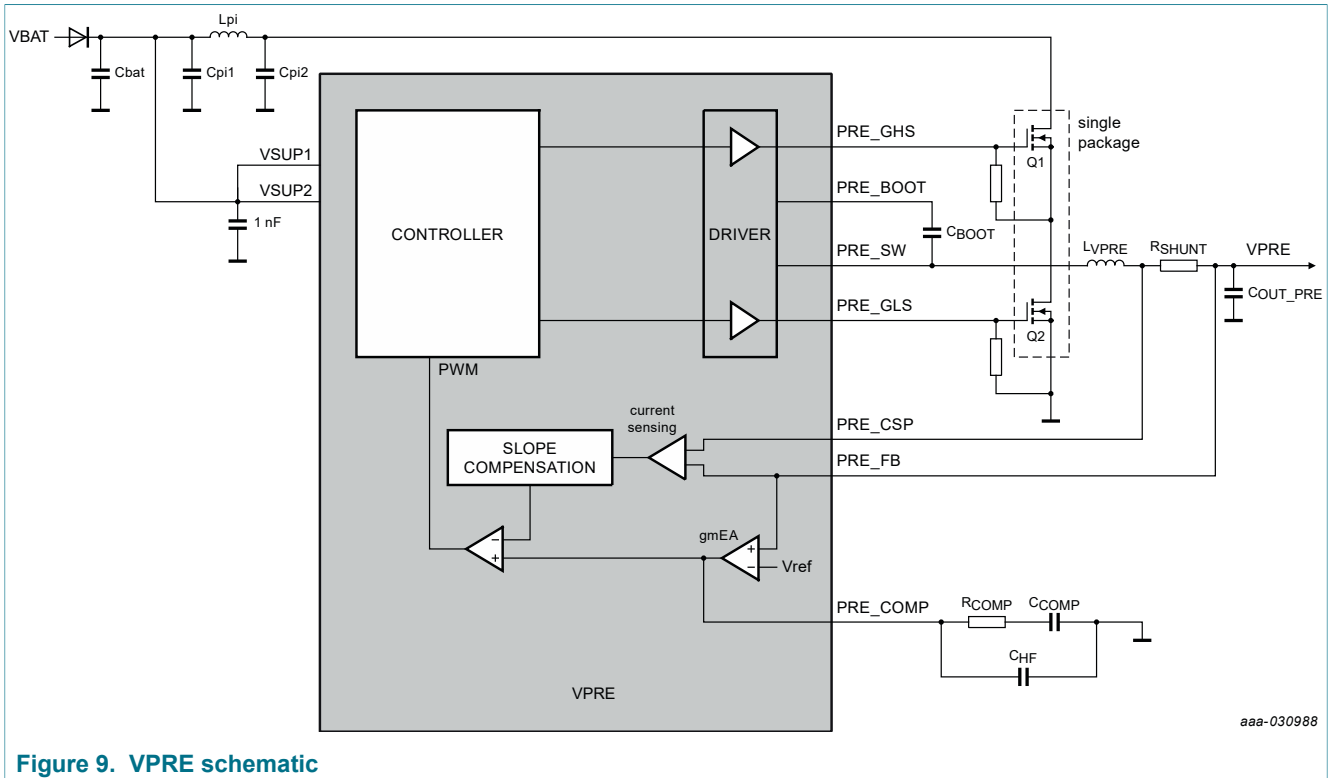


Figure 9. VPRES schematic

A PI filter, with $F_{RES} = 1 / [2\pi \times \sqrt{LC_{pi1}}]$ and calculated for $F_{res} < F_{PRE_SW} / 10$, is required to filter VPRES switching frequency on the Battery line. VSUP1,2 pins must be connected before the PI filter for a clean biasing of the device. Cpi1 capacitor shall be implemented close to VSUP1,2 pins. Cpi2 capacitor shall be implemented close to Q1. The bootstrap capacitor value should be sized to be >10 times the gate source capacitor of Q1. Gate to source resistor on Q1 and Q2 is recommended in case of pin disconnection to guarantee a passive switch OFF of the transistors.

20.3 Compensation network and stability

The external compensation network, made with R_{COMP} , C_{COMP} , and C_{HF} shall be calculated for best compromise between stability and transient response, based on below conceptual plot of Type 2 compensation network transfer function.

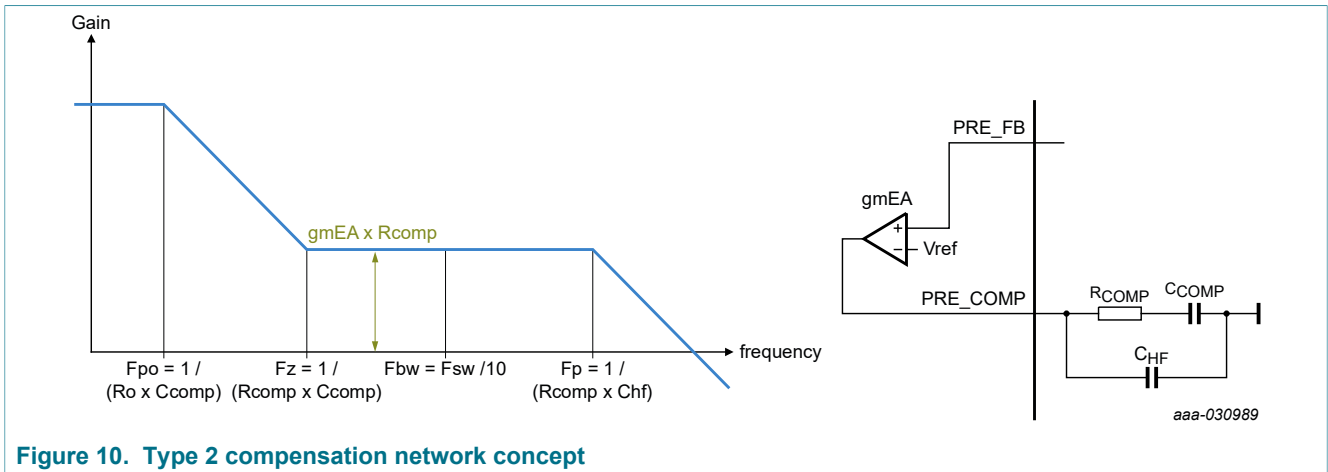


Figure 10. Type 2 compensation network concept

Calculation guideline

- System bandwidth for VPRE = 455 kHz: $F_{bw} = F_{PRE_SW} / 10$
System bandwidth for VPRE = 2.22 MHz: $F_{bw} = F_{PRE_SW} / 15$
- Compensation zero: $F_z = F_{bw} / 10$
- Compensation pole for VPRE = 455 kHz: $F_p = F_{PRE_SW} / 2$
- Compensation pole for VPRE = 2.22 MHz: $F_p = F_{PRE_SW} / 4$
- $F_{GBW} = 1 / (2\pi \times R_{SHUNT} \times V_{PRE_LIM_GAIN} \times C_{OUT_PRE})$
- Error amplifier gain: $EA_gain = (V_{REF} / V_{PRE}) \times gmEA_{PRE} \times R_{COMP} = 10^{LOG(F_{BW} / F_{GBW})}$
- $V_{REF} = 1.0\text{ V}$, $R_{COMP} = V_{PRE} \times (EA_gain / gmEA_{PRE})$
- $C_{COMP} = 1 / (2\pi \times F_z \times R_{COMP})$
- $C_{HF} = 1 / (2\pi \times F_p \times R_{COMP})$
- Slope compensation: $Se > (V_{PRE} / L_{VPRE}) \times R_{SHUNT} \times V_{PRE_LIM_GAIN}$

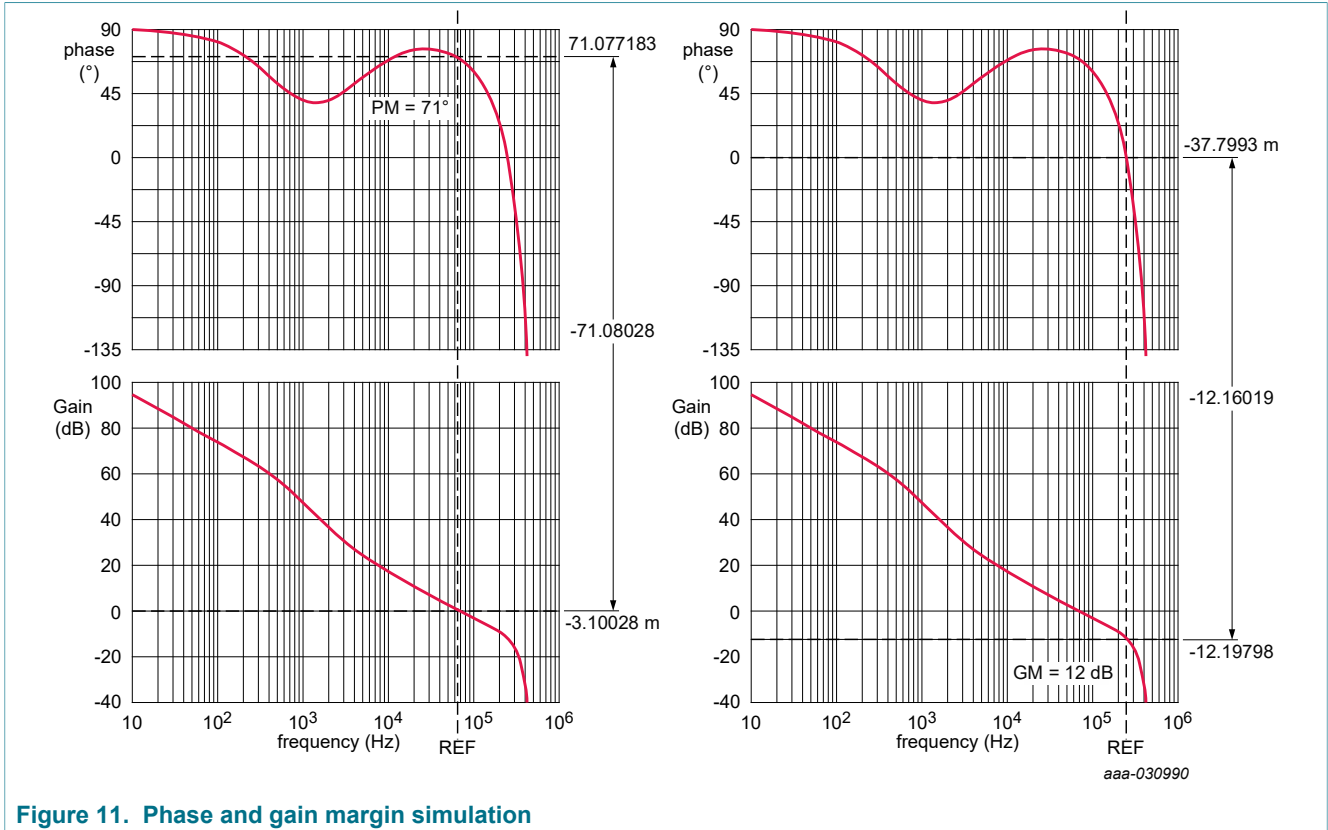
The compensation network can be automatically calculated in the VR5500_OTP_Config.xlsm file which is using the same formulas. A Simplis simulation is recommended to verify the Phase and Gain Margin with normalized components.

Use case calculation with VPRE = 4.1 V, LVPRE = 6.8 μH, FPRE_SW = 455 kHz, COUT_PRE = 66 μF, RSHUNT = 10.0 mΩ

- System bandwidth: $F_{bw} = 45\text{ kHz}$
- Compensation zero: $F_z = 4.5\text{ kHz}$
- Compensation pole: $F_p = 227.5\text{ kHz}$
- $F_{GBW} = 53\text{ kHz}$
- Error amplifier gain: $EA_gain = 10^{LOG(F_{BW} / F_{GBW})} = 0.86$
- $R_{COMP} = 2.34\text{ k}\Omega = 2.2\text{ k}\Omega$
- $C_{COMP} = 15.9\text{ nF} = 16\text{ nF}$
- $C_{HF} = 318\text{ pF} = 330\text{ pF}$
- Slope compensation: $Se > 30\text{ mV}/\mu\text{s}$

Use case stability verification

- Phase margin target $PM > 45^\circ$ and gain margin target $GM > 6\text{ dB}$.



Use case transient response verification

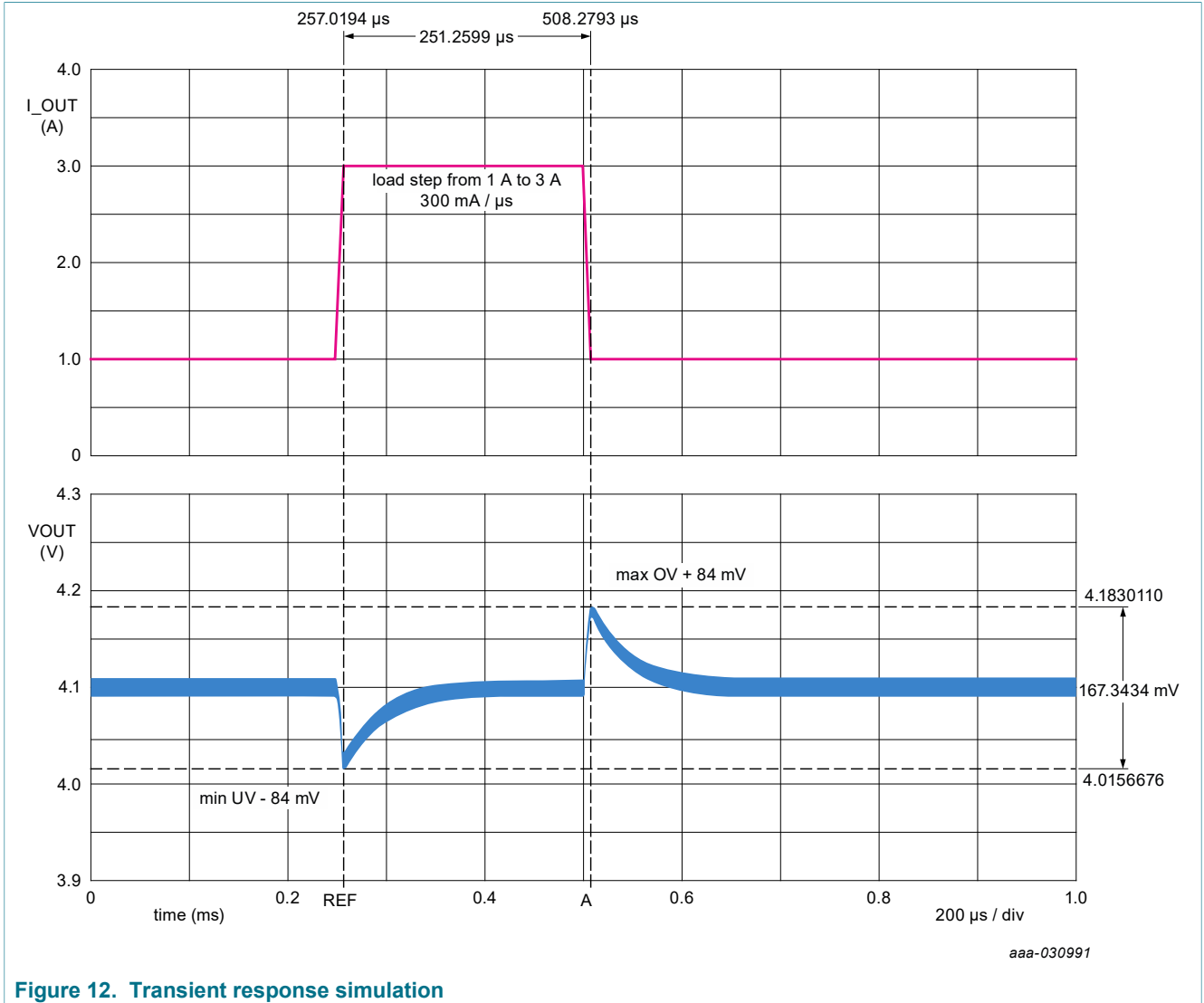


Figure 12. Transient response simulation

20.4 VPRE electrical characteristics

Table 67. VPRE electrical characteristics

$T_A = -40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$, unless otherwise specified. $VSUP = VSUP_UVH$ to 36 V, unless otherwise specified. All voltages referenced to ground.

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------------------------|---------------------------------------|------|-----|------|------|
| V _{PRE} | Output voltage (OTP_VPREV[5:0] bits) | 3.2 | 3.3 | 3.4 | V |
| | | 3.68 | 3.8 | 3.92 | V |
| | | 3.98 | 4.1 | 4.22 | V |
| | | 4.85 | 5.0 | 5.15 | V |
| V _{PRE_SOFT_START} | Output voltage from 10 % to 90 % | 250 | 450 | 650 | μs |
| | Digital DAC soft start completion | — | — | 1.35 | ms |
| V _{PRE_STARTUP} | Overshoot at startup | — | — | 3 | % |
| V _{PRE_FB_OV} | Over voltage threshold protection | 5.5 | 6.0 | 6.5 | V |
| T _{PRE_FB_OV} | V _{PRE_FB_OV} filtering time | 1 | 2 | 3 | μs |

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------------------------------|--|------|------|-------|------|
| V _{PRE_UVH} | Under voltage threshold high | 2.9 | — | 3.1 | V |
| V _{PRE_UVL} | Under voltage threshold low | 2.5 | — | 2.7 | V |
| T _{PRE_UV} | V _{PRE_UVH} and V _{PRE_UVL} filtering time | 6.0 | 10 | 15 | μs |
| F _{PRE_SW} | Switching frequency range (OTP_VPRE_clk_sel bit) | 430 | 455 | 480 | kHz |
| | | 2.1 | 2.22 | 2.35 | MHz |
| L _{VPRE} | Typical inductor value for F _{PRE_SW} = 455 kHz | 4.7 | 6.8 | 10 | μH |
| | Typical inductor value for F _{PRE_SW} = 2.22 MHz | 1.5 | 2.2 | 4.7 | μH |
| V _{PRE_LOAD_REG_455k} | Transient load regulation at 455 kHz VSUP = 6.0 V to 36 V (L _{VPRE} = 6.8 μH, C _{OUT_PRE} = 66 μF, from 1.0 A to 3.0 A, di/dt = 300 mA/μs) | -3 | — | 3 | % |
| V _{PRE_LOAD_REG_2.2M} | Transient load regulation at 2.22 MHz VSUP = 6.0 V to 18 V (L _{VPRE} = 2.2 μH, C _{OUT_PRE} = 44 μF, from 1.0 A to 3.0 A, di/dt = 300 mA/μs) | -3 | — | 3 | % |
| V _{PRE_LINE_REG_455k} | Transient line regulation at 455 kHz VSUP = 6.0 V to 18 V and VSUP = 12 V to 36 V (C _{in} = 47 μF + PI filter, L _{VPRE} = 6.8 μH, C _{OUT_PRE} = 66 μF, dv/dt = 100 mV/μs) | -3 | — | 3 | % |
| V _{PRE_LINE_REG_2.2M} | Transient line regulation at 2.22 MHz VSUP = 6.0 V to 18 V (C _{in} = 47 μF + PI filter, L _{VPRE} = 2.2 μH, C _{OUT_PRE} = 44 μF, dv/dt = 100 mV/μs) | -3 | — | 3 | % |
| V _{PRE_RIPPLE_455k} | Ripple at 455 kHz VSUP = 12 V and VSUP = 24 V (L _{VPRE} = 6.8 μH, C _{OUT_PRE} = 66 μF, V _{PRE} = 3.3 V and 5.0 V, I _{PRE} = 4A) | -1 | — | 1 | % |
| V _{PRE_RIPPLE_2.2M} | Ripple at 2.22 MHz VSUP = 12 V (L _{VPRE} = 2.2 μH, C _{OUT_PRE} = 44 μF, V _{PRE} = 3.3 V and 5.0 V, I _{PRE} = 2A) | -0.5 | — | 0.5 | % |
| T _{PRE_ON_MIN} | HS minimum ON time | 15 | 25 | 35 | ns |
| T _{PRE_OFF_MIN} | HS minimum OFF time | 20 | 40 | 60 | ns |
| R _{SHUNT} | Current sense resistor (±1 %) | 10 | — | 20 | mΩ |
| V _{PRE_LIM_GAIN} | Current sense amplifier gain | 4.5 | 5 | 5.5 | |
| V _{PRE_LIM_TH1} | Current sense amplifier peak detection threshold (OTP_VPREILIM[1:0] bits) Note: 150 mV setting is not available for 2.22 MHz | 37 | 50 | 63 | mV |
| | | 60.8 | 80 | 99.2 | mV |
| | | 93.6 | 120 | 146.4 | mV |
| | | 117 | 150 | 183 | mV |
| I _{LIM_PRE} | I _{LIM_PRE} = V _{PRE_LIM_TH} / R _{SHUNT} Inductor peak current limitation range (R _{SHUNT} = 10 mΩ, V _{PRE_LIM_TH1} = 50 mV) | 3.75 | 5 | 6.25 | A |
| | Inductor peak current limitation range (R _{SHUNT} = 10 mΩ, V _{PRE_LIM_TH1} = 150 mV) To be recalculated for different R _{SHUNT} and different V _{PRE_LIM_TH} | 12 | 15 | 18 | A |
| V _{PRE_DRV} | HS and LS gate driver output voltage | — | VBOS | — | V |

| Symbol | Parameter | Min | Typ | Max | Unit |
|---------------------------|--|-----|-------|------|-------|
| I _{PRE_GATE_DRV} | HS and LS gate driver pull up and pull down current capability (OTP_VPRESRHS[1:0] and OTP_VPRESRLS[1:0] bits by default + VPRESRHS[1:0] and VPRESRLS[1:0] bits by I2C) | 60 | 130 | 220 | mA |
| | | 120 | 260 | 430 | mA |
| | | 220 | 520 | 860 | mA |
| | | 420 | 900 | 1490 | mA |
| C _{OUT_PRE} | Effective output capacitor for F _{PRE_SW} = 455 kHz | 40 | 66 | 220 | μF |
| | Effective output capacitor for F _{PRE_SW} = 2.22 MHz | 20 | 44 | 110 | μF |
| | Output decoupling capacitor | — | 0.1 | — | μF |
| C _{IN_PRE} | Effective input capacitor (C _{pi2}) | 20 | — | — | μF |
| | Input decoupling capacitor | — | 0.1 | — | μF |
| I _{PRE_DRV} | Combined HS + LS gate driver average current capability I _{PRE_DRV} < F _{PRE_SW} × (QC _{HS} + QC _{LS}) with QC _{HS} = gate charge of Q2 at VBOS with QC _{LS} = gate charge of Q1 at VBOS | — | — | 30 | mA |
| gmEA _{PRE} | Error amplifier transconductance | 1.0 | 1.5 | 2.1 | mS |
| V _{PRE_SLOPE} | Slope compensation (OTP_VPRESC[5:0] bits) | 29 | 40 | 51 | mV/μs |
| | | 36 | 50 | 64 | mV/μs |
| | | 43 | 60 | 77 | mV/μs |
| | | 51 | 70 | 89 | mV/μs |
| | | 58 | 80 | 102 | mV/μs |
| | | 65 | 90 | 115 | mV/μs |
| | | 73 | 100 | 127 | mV/μs |
| | | 102 | 140 | 178 | mV/μs |
| | | 124 | 170 | 216 | mV/μs |
| | | 146 | 200 | 254 | mV/μs |
| 175 | 240 | 305 | mV/μs | | |
| T _{PRE_UV_DFS} | V _{PRE_UVL} filtering time to go to DEEP-FS during V _{PRE} startup | 1.8 | 2 | 2.2 | ms |
| T _{PRE_DT} | Dead time to avoid cross conduction (this timing does not take into account the external FET turn ON/OFF times) | 20 | 30 | 40 | ns |
| V _{PRE_OFF_DLY} | Wait time between VBOOST OFF and VPRE OFF (OTP_VPRE_off_dly bit) | — | 250 | — | μs |
| | | — | 32 | — | ms |
| R _{PRE_DIS} | Discharge resistor (when VPRE is disabled) | 250 | 500 | 1000 | Ω |
| I _{PRE_SW_LKG} | PRE_SW leakage | — | — | 10 | μA |
| R _{DRV_OFF} | HS and LS gate driver pull-down resistor when VPRE is disabled | 5 | — | 35 | kΩ |
| R _{BOOT_OFF} | PRE_BOOT pull-down resistor when VPRE is disabled | 1.2 | — | 2.6 | kΩ |
| I _{BOOT_LKG} | PRE_BOOT leakage | — | — | 10 | μA |

20.5 VPRE external MOSFETs

MOSFETs selection:

- Logical level NMOS, gate drive comes from VBOS (5.0 V)
- VDS > 60 V for 24 V truck, bus applications
- VDS > 40 V for 12 V automotive applications
- Qg < 15 nC at Vgs = 5.0 V is recommended for 455 kHz
Qg < 7 nC at Vgs = 5.0 V is recommended for 2.22 MHz
- Recommended example references

Table 68. VPRE external MOSFETs recommendation

| Applications | Fpre | Ipre < 2.0 A | Ipre < 4.0 A | Ipre < 6.0 A | Ipre < 10 A |
|--------------|----------|-----------------------------|-----------------------------|-----------------------------|---|
| 12 V | 455 kHz | BUK9K25-40E, BUK9K18-40E | BUK9K25-40E, BUK9K18-40E | BUK9K18-40E | BUK9K18-40E, NVTFS5C471NLWFTAG, HS = BUK9M9R5-40H, LS = BUK9M3R3-40H |
| | 2.22 MHz | BUK9K25-40E, BUK9Y29-40E | BUK9K25-40E, BUK9Y29-40E | BUK9K25-40E, BUK9Y29-40E | N/A |
| 24 V | 455 kHz | BUK9K35-60E, BUK9K52-60E | BUK9K35-60E, BUK9K52-60E | BUK9K35-60E | , BUK9K12-60E |

Other MOSFETs are possible but should have similar performances as compared to the recommended references. The maximum current at 2.22 MHz is limited to 6.0 A for which the efficiency is equivalent to 10 A at 455 kHz. The power dissipation in the external MOSFETs is important and the junction temperature may rise above 175 °C.

VPRE switching slew rate can be configured by I2C to align with external MOSFET selection, VPRE switching frequency, and to optimize power dissipation and EMC performance. It is recommended to configure the maximum slew rate by OTP and reduce it later by I2C if needed. VR5500 is using current source to drive the external MOSFET so adding an external serial resistor with the gate does not affect the slew rate. It is recommended to change the current source selection by I2C to change the slew rate.

VPRE MOSFET switching time can be estimated to $T_{SW} = (Q_{GD} + Q_{GS} / 2) / I_{PRE_GATE_DRV}$ using the gate charge definition from Figure 13. Q_{GD} and Q_{GS} can be extracted from the MOSFET data sheet.

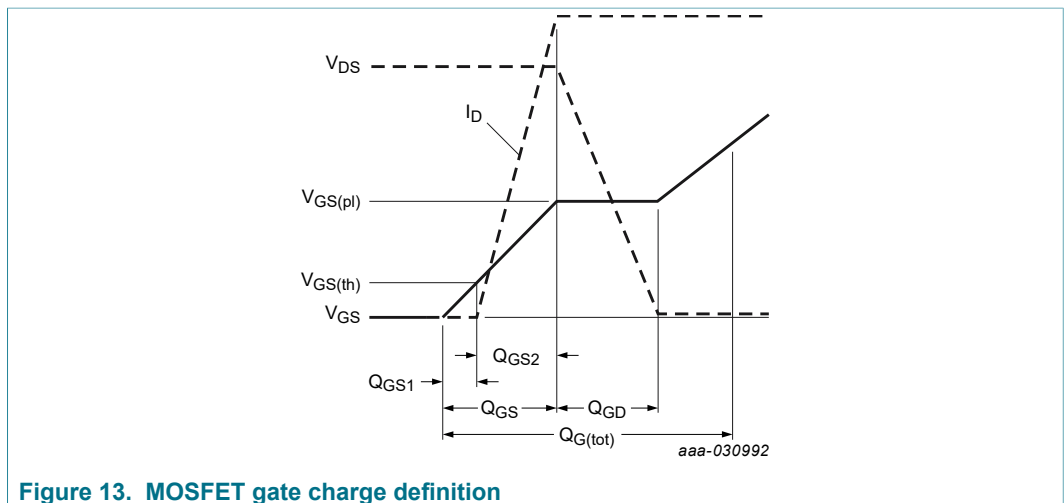


Figure 13. MOSFET gate charge definition

20.6 VPRE efficiency

VPRE efficiency versus current load is given for information based on external component criteria provided and VSUP voltage 14 V. If the conditions change, it has to be recalculated with the VR5500_PDTCAL tool. The real efficiency has to be verified by measurement at the application level.

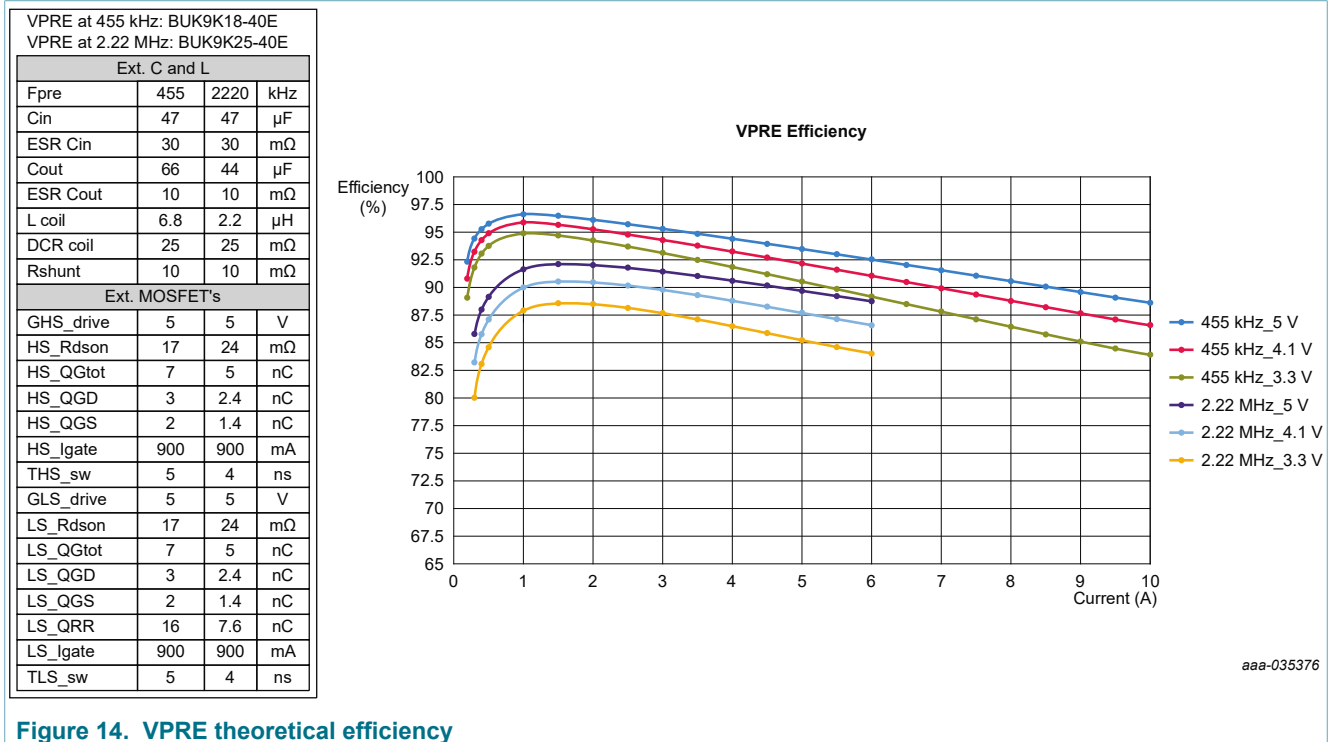


Figure 14. VPRE theoretical efficiency

20.7 VPRE not populated

When two VR5500 are used, only one VPRE may be required. It is possible to not populate the external components of the second VPRE to optimize the bill of material.

In that case, specific connection of the VPRE2 pins is required:

- PRE_FB2 must be connected to PRE_FB1
- PRE_CSP2 must be connected to PRE_FB1
- PRE_COMP2 must be left open
- PRE_SW2 must be connected to GND
- PRE_BOOT2 must be connected to VBOS2
- PRE_GHS2 and PRE_GLS2 must be left open

After the startup phase, VPRE2 shall be disabled by I2C with VPDIS bit.

21 Low voltage boost: VBOOST

21.1 Functional description

VBOOST block is a low voltage, asynchronous, peak current mode boost converter. VBOOST works in PWM and uses an external diode and an internal low-side FET.

VBOOST enters Skip mode to maintain the correct output voltage in light load condition. The output voltage is configurable by OTP at 5.0 V or 5.74 V, the switching frequency is 2.22 MHz and the output current is limited to 1.5 A peak input current. The input of the boost is connected to the output of VPRE. This block is intended to supply LDO1, LDO2, BUCK3, or an external regulator. The stability is ensured by an internal Type 2 compensation network with slope compensation.

By default, VBOOST switching frequency is derived from the internal oscillator, and can be synchronized with an external frequency signal applied on FIN input pin. The change from internal oscillator to external clock or vice versa is controlled by I2C.

An overcurrent detection and a thermal shutdown are implemented to protect the internal MOSFET. If an overcurrent is detected after the LS minimum TON time, the LS is turned OFF and will be turned ON again at the next rising edge of the switching clock. The overcurrent induces a duty cycle reduction that could lead to the output voltage gradually dropping, causing an undervoltage condition on one of the cascaded regulators.

Since the current limitation is on the input current, [Table 69](#) summarizes the expected output current capability depending on VPRE and VBOOST voltage configurations and $L = 4.7 \mu\text{H}$.

Table 69. Output current capability

| VPRE | VBOOST | IBOOST_OUT |
|-------|--------|------------|
| 3.3 V | 5.0 V | 800 mA |
| | 5.74 V | 700 mA |
| 4.1 V | 5.0 V | 1 A |
| | 5.74 V | 900 mA |
| 5.0 V | 5.74 V | 1.1 A |

An overvoltage protection is implemented on BOOST_LS pin. When $V_{\text{BOOST_OV}}$ is detected during two consecutive turn ON cycles, VBOOST is disabled. An I2C command is required to enable it again.

21.2 Application schematic

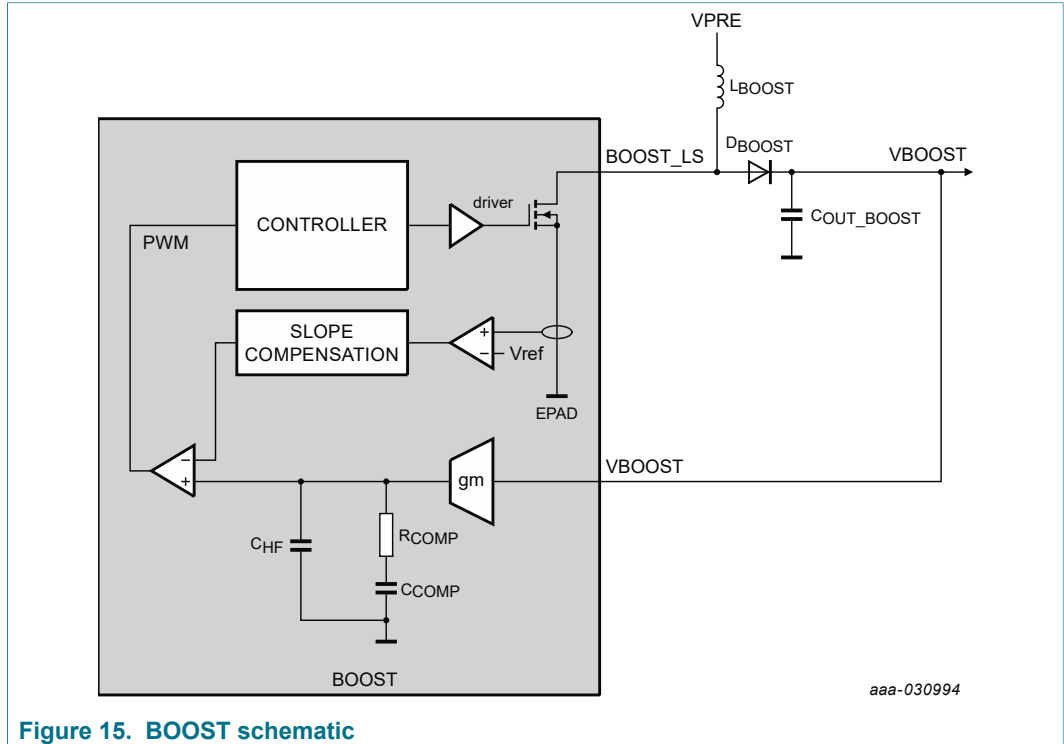


Figure 15. BOOST schematic

It is recommended to select a Schottky diode for D_{BOOST} to limit the impact on the SMPS efficiency.

21.3 Compensation network and stability

The internal compensation network, made with R_{COMP} , C_{COMP} , and C_{HF} is optimized for best compromise between stability and transient response with $R_{COMP} = 750\text{ k}\Omega$, $C_{COMP} = 125\text{ pF}$, and $C_{HF} = 2.0\text{ pF}$.

Use case with $V_{BOOST} = 5.74\text{ V}$, $L_{VBOOST} = 4.7\text{ }\mu\text{H}$, $F_{BOOST_sw} = 2.22\text{ MHz}$, $C_{OUT_BOOST} = 22\text{ }\mu\text{F}$

Use case stability verification

- Phase margin target $PM > 45^\circ$ and gain margin target $GM > 6\text{ dB}$.

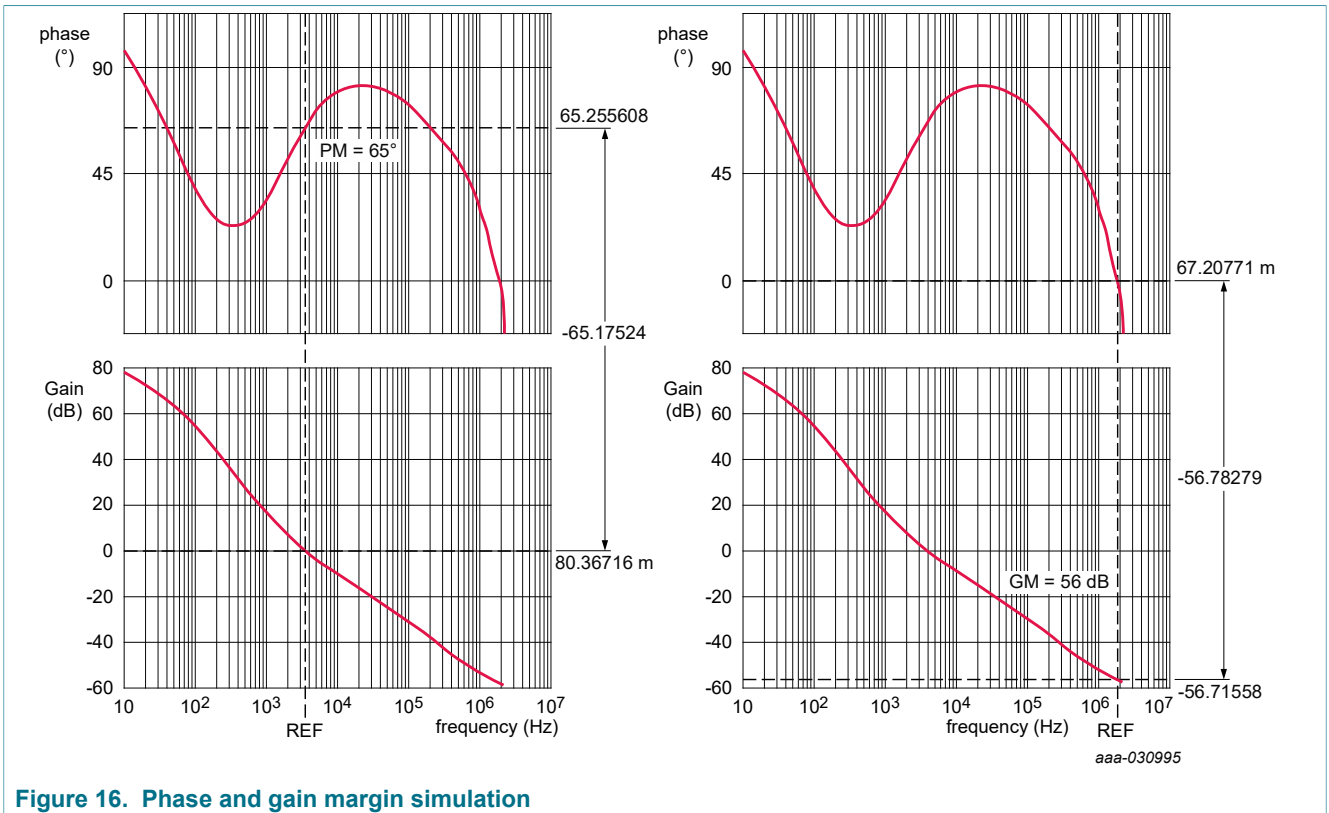


Figure 16. Phase and gain margin simulation

Use case transient response verification

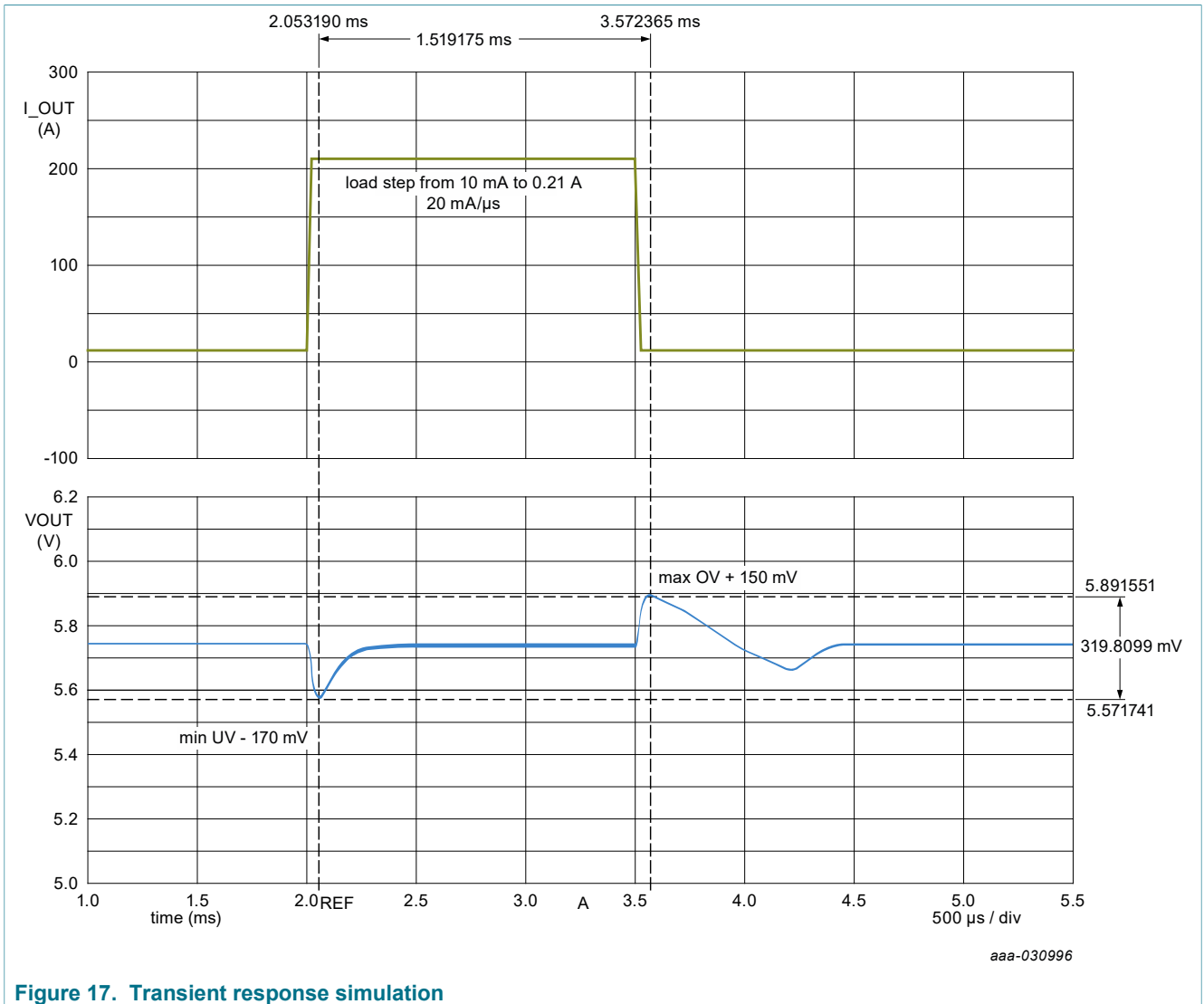


Figure 17. Transient response simulation

21.4 VBOOST electrical characteristics

Table 70. VBOOST electrical characteristics

$T_A = -40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$, unless otherwise specified. $VSUP = VSUP_UVH$ to 36 V, unless otherwise specified. All voltages referenced to ground.

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------------------------|---------------------------------------|------|------|------|------|
| V _{BOOST} | Output voltage (OTP_VBSTV[3:0] bits) | 5.57 | 5.74 | 5.91 | V |
| | | 4.85 | 5.0 | 5.15 | V |
| V _{BOOST_SOFT_START} | Output voltage from 10 % to 90 % | — | 500 | — | μs |
| | Digital DAC soft start completion | — | — | 825 | μs |
| V _{BOOST_STARTUP} | Overshoot at startup | — | — | 3 | % |
| V _{BOOST_UVH} | Undervoltage threshold high | 3.3 | — | 3.7 | V |
| T _{BOOST_UVH} | V _{BOOST_UVH} filtering time | 6.0 | 10 | 15 | μs |
| V _{BOOST_OV} | Overvoltage protection threshold | 7.4 | — | 7.9 | V |
| F _{BOOST_SW} | Switching frequency range | 2.1 | 2.22 | 2.35 | MHz |

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------------------------|---|-----|-----|------|-------|
| L _{BOOST} | Inductor for V _{BOOST_SW} = 2.22 MHz | 2.2 | 4.7 | 6.8 | μH |
| C _{OUT_BOOST} | Effective output capacitor | 22 | — | 66 | μF |
| V _{BOOST_LOAD_REG} | Transient load regulation (C _{OUT_BOOST} = 22 μF, from 10 mA to 400 mA, di/dt = 200 mA/μs) | — | — | 750 | mV |
| V _{BOOST_LOAD_REG} | Transient load regulation (C _{OUT_BOOST} = 22 μF, from 1.0 mA to 20 mA, di/dt = 200 mA/μs) | — | — | 500 | mV |
| I _{LIM_BOOST} | Inductor peak current limitation range (OTP_VBSTILIM[1:0] bits) | 1.5 | 2.0 | 2.75 | A |
| T _{BOOST_ON_MIN} | LS minimum ON time (OTP_VBSTTONTIME[1:0] bits) | 40 | 60 | 90 | ns |
| | | 30 | 50 | 80 | ns |
| R _{BOOST RON} | LS NMOS RDSon | — | 150 | 280 | mΩ |
| T _{BOOST_SR} | Switching output slew rate (OTP_VBSTSR[1:0] bits by default + VBSTSR[1:0] bits by I2C) | — | 500 | 1500 | V/μs |
| | | — | 300 | 750 | V/μs |
| gmEA _{BOOST} | Error amplifier transconductance | 3.5 | 7.0 | 9.0 | μS |
| V _{BOOST_SLOPE} | Slope compensation (OTP_VBSTSC[3:0] bits) | 40 | 79 | 110 | mV/μs |
| | | 70 | 125 | 190 | mV/μs |
| | | 90 | 160 | 230 | mV/μs |
| R _{COMP} | Compensation network resistor | 500 | 750 | 1200 | kΩ |
| | | 250 | 500 | 1000 | kΩ |
| C _{COMP} | Compensation network capacitor | 90 | 125 | 175 | pF |
| TSD _{BOOST} | Thermal shutdown threshold | 160 | — | — | °C |
| TSD _{BOOST_HYST} | Thermal shutdown threshold hysteresis | — | 9 | — | °C |
| T _{BOOST_TSD} | Thermal shutdown filtering time | 3.0 | 5.0 | 8.0 | μs |

21.5 VBOOST not populated

It is possible to not use the VBOOST when VPRE is configured at 4.1 V or 5.0 V. In this case, the external VBOOST components can be unpopulated to optimize the bill of material. The OTP_BOOSTEN bit shall be programmed to 0 and VBOOST pin must be connected to VPRE. BOOST_LS pin must be left open.

VBOOST must be used when VPRE is configured at 3.3 V or 3.8 V to supply VBOS.

22 Low voltage buck: BUCK1 and BUCK2

22.1 Functional description

BUCK1 and BUCK2 blocks are low voltage, synchronous, valley current mode buck converters with integrated HS PMOS and LS NMOS. BUCK1 and BUCK2 work in force PWM and the output voltage is configurable by OTP from 0.8 V to 1.8 V, the switching frequency is 2.22 MHz and the output current is limited to 3.6 A peak. The input of these blocks must be connected to the output of VPRE. The stability is ensured by an internal Type 2 compensation network with slope compensation.

By default, BUCK1 and BUCK2 switching frequency is derived from the internal oscillator and can be synchronized with an external frequency signal applied on FIN input pin. The change from internal oscillator to external clock or vice versa is controlled by I2C.

BUCK1 and BUCK2 can work independently or in Dual phase mode to double the output current capability. When BUCK1 and BUCK2 are used in dual phase, they must have the same output voltage configuration. Any action like TSD, OV, disable by I2C, on BUCK1 affects BUCK2 and vice versa.

An overcurrent detection and a thermal shutdown are implemented on BUCK1 and BUCK2 to protect the internal MOSFETs. The overcurrent induces a duty cycle reduction that could lead to the output voltage gradually dropping, causing an undervoltage condition.

The ramp up and ramp down of BUCK1 and BUCK2 when they are enabled and disabled is configurable with OTP_DVS_BUCK12[1:0] bits to accommodate multiple MCU soft start requirements. Static Voltage Scaling (SVS) feature is available to decrease the output voltage after power up during INIT_FS Programmable phase shift control is implemented, see [Section 25 "Clock management"](#).

22.2 Application schematic: Single phase mode

In this configuration, BUCK1 and BUCK2 are configured as independent outputs, working independently. Each output is configured and controlled independently by I2C.

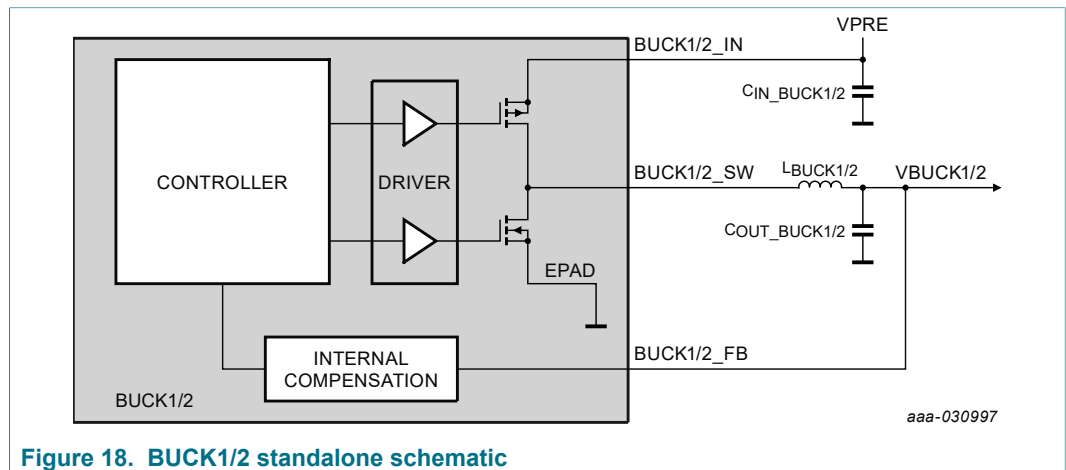


Figure 18. BUCK1/2 standalone schematic

22.3 Application schematic: Dual phase mode

In this configuration, BUCK1 and BUCK2 are configured in dual phase mode to double the output current capability. The dual phase mode is enable with OTP_VB12MULTIPH bit. The PCB layout of BUCK1 phase and BUCK2 must be symmetric for optimum EMC performance.

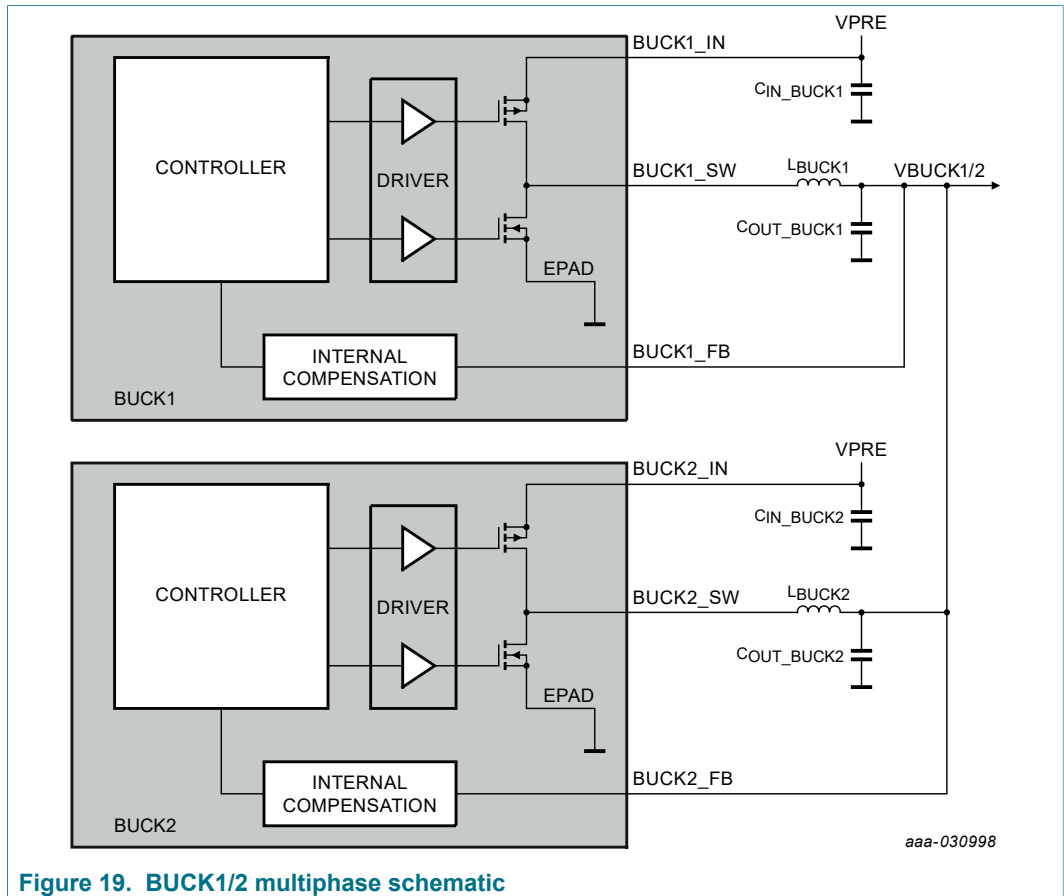


Figure 19. BUCK1/2 multiphase schematic

22.4 Compensation network and stability

The internal compensation network ensures the stability and the transient response performance of the buck converter. The error amplifier gain is configurable with OTP_VBxGMCOMP[2:0] bits for each BUCK 1 and BUCK2 regulators. It is recommended to use the default value that covers most of the use cases.

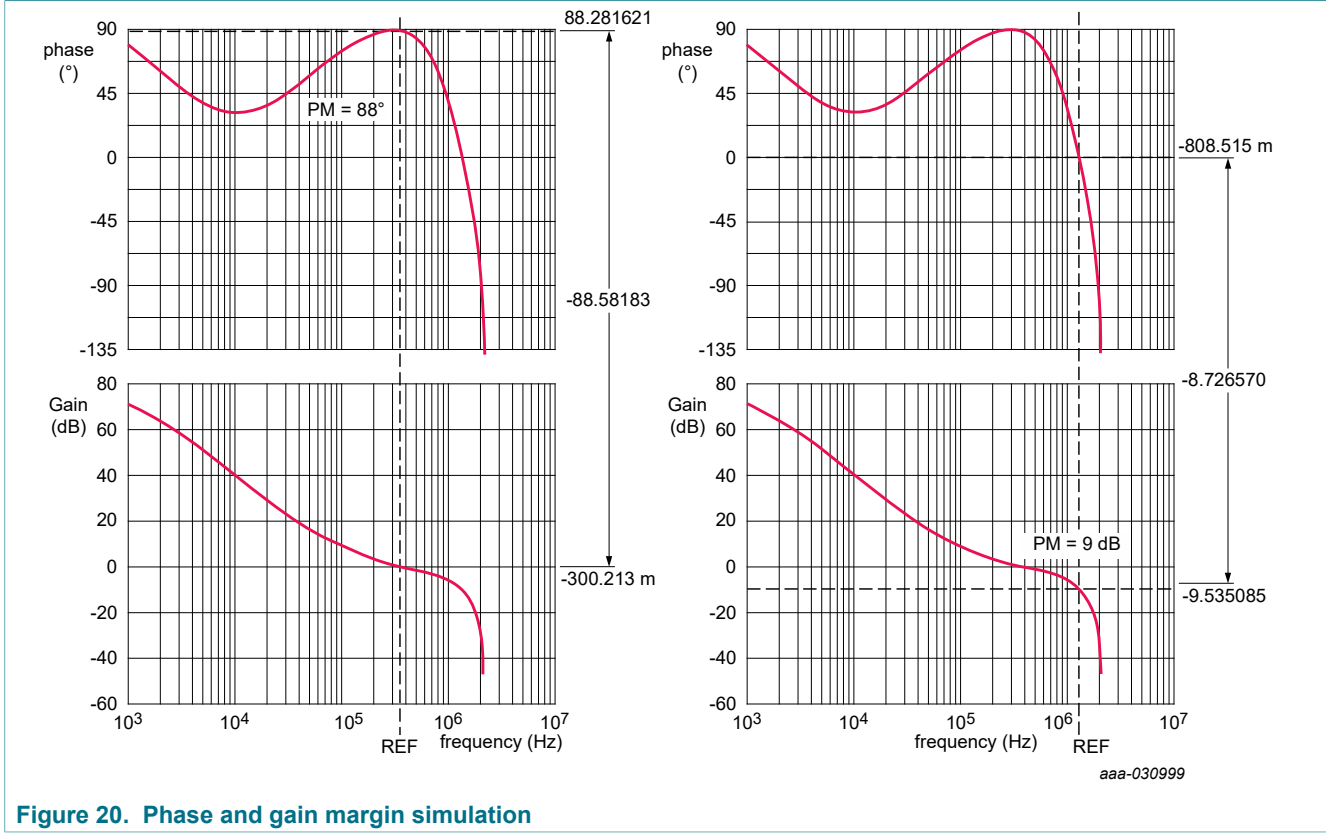
Decreasing the gain reduces the regulation bandwidth and increase the phase and gain margin but transient performance is degraded. Increasing the gain enlarges the regulation bandwidth and improves the transient performance but the phase and gain margin is degraded.

OTP_VBxINDOPT[1:0] scales the slope compensation and the zero cross detection according to the inductor value. 1.0 μH is the recommended inductor value for BUCK1 and BUCK2.

Use case with $V_{\text{PRE}} = 3.3 \text{ V}$, $V_{\text{BUCK1}} = 1.0 \text{ V}$, $L_{\text{VBUCK1}} = 1.0 \mu\text{H}$, $V_{\text{BUCK1_sw}} = 2.22 \text{ MHz}$, $C_{\text{OUT_BUCK1}} = 44 \mu\text{F}$, default Err Amp gain

Use case stability verification

- Phase margin target $\text{PM} > 45^\circ$ and gain margin target $\text{GM} > 6 \text{ dB}$.



Use case transient response verification

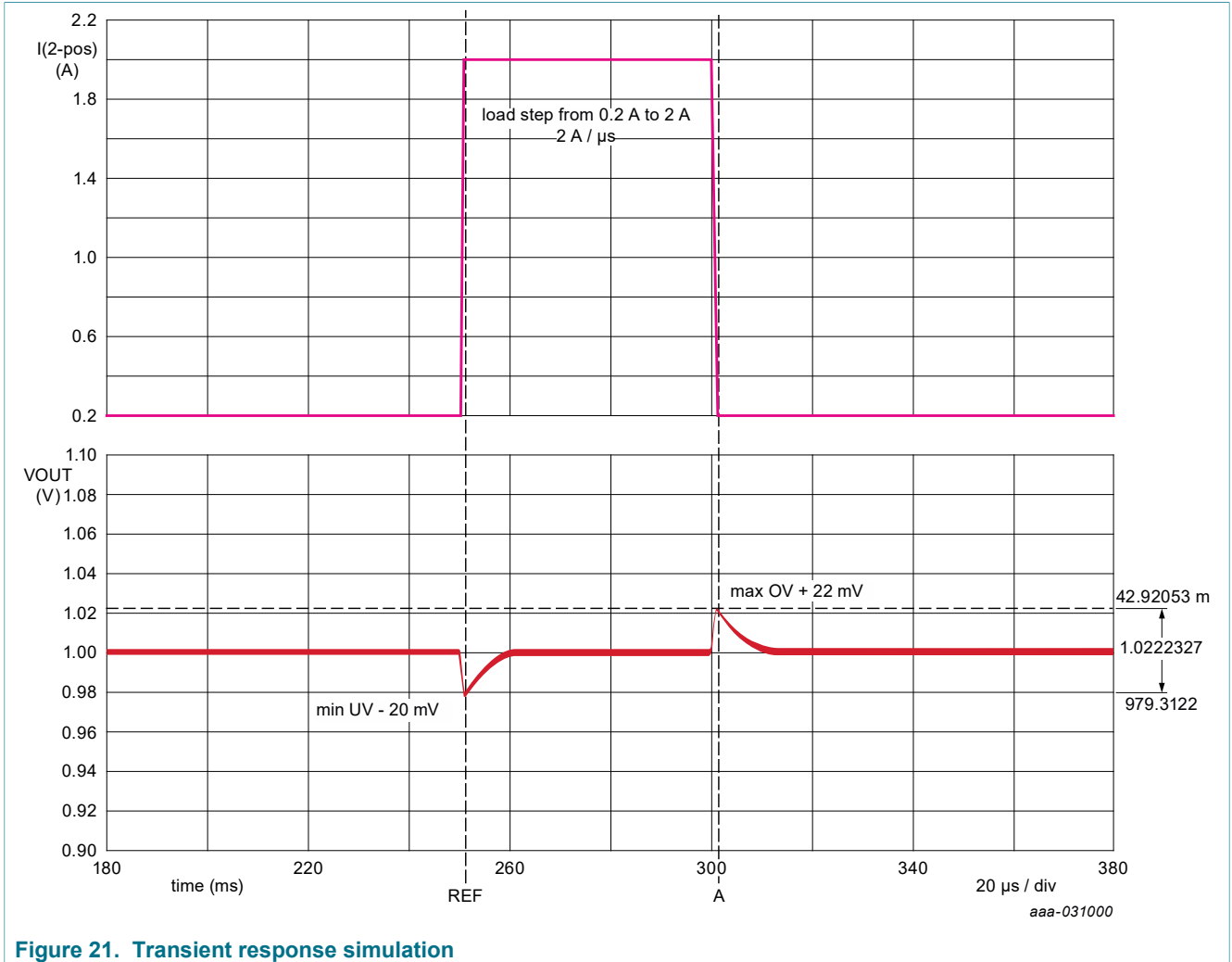


Figure 21. Transient response simulation

22.5 BUCK1 and BUCK2 electrical characteristics

Table 71. BUCK1 and BUCK2 electrical characteristics

$T_A = -40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$, unless otherwise specified. $VSUP = VSUP_UVH$ to 36 V, unless otherwise specified. All voltages referenced to ground.

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------------|--|------|------|------|---------------|
| V_{BUCK12_IN} | Input voltage range | 2.5 | — | 5.5 | V |
| V_{BUCK12} | Output voltage (OTP_VB1V[7:0] and OTP_VB2V[7:0] bits) 0.8 V, 0.825 V, 0.9 V, 0.95 V, 1.0 V, 1.025 V, 1.03125 V, 1.075 V, 1.1 V, 1.1375 V, 1.2 V, 1.25 V, 1.3 V, 1.35 V, 1.4 V, 1.5 V, 1.8 V | 0.8 | — | 1.8 | V |
| I_{BUCK12} | DC output current capability (one phase) | — | — | 2.5 | A |
| V_{BUCK12_ACC} | Output voltage accuracy ($I_{OUT} < 2.5\text{ A}$) | -2 | — | +2 | % |
| V_{BUCK12_SW} | Switching frequency range | 2.1 | 2.22 | 2.35 | MHz |
| L_{BUCK12} | Inductor for $V_{BUCK12_SW} = 2.22\text{ MHz}$ (OTP_VB1INDOPT[1:0] and OTP_VB2INDOPT[1:0] bits) | 0.47 | 1.0 | 1.5 | μH |

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|-------|-------|-------|-------|
| C _{OUT_BUCK12} | Effective Output capacitor | 40 | — | 160 | μF |
| | Output decoupling capacitor | — | 0.1 | — | μF |
| C _{IN_BUCK12} | Effective Input capacitor (close to BUCK1_IN and BUCK2_IN pins) | 4.7 | — | — | μF |
| | Input decoupling capacitor (close to BUCK1_IN and BUCK2_IN pins) | — | 0.1 | — | μF |
| V _{BUCK12_TLR} | Transient load regulation for V _{BUCK12} < 1.2 V (C _{out} = 40 μF, from 200 mA to 1.0 A, di/dt = 2.0 A/μs), single phase (C _{out} = 40 μF, from 400 mA to 2.0 A, di/dt = 4.0 A/μs), dual phase | -25 | — | +25 | mV |
| V _{BUCK12_TLR} | Transient load regulation for V _{BUCK12} > 1.2 V (C _{out} = 40 μF, from 200 mA to 1.0 A, di/dt = 2.0 A/μs), single phase (C _{out} = 40 μF, from 400 mA to 2.0 A, di/dt = 4.0 A/μs), dual phase | -3 | — | +3 | % |
| I _{LIM_BUCK12} | Inductor peak current limitation range for one phase (OTP_VB1SWILIM[1:0] and OTP_VB2SWILIM[1:0] bits) | 3.6 | 4.5 | 5.45 | A |
| V _{BUCK12_DVS_UP} (for V _{BUCK12} up to 1.5 V) | Ramp up speed, OTP_DVS_BUCK12[1:0] = 00 | 5.86 | 7.81 | 9.77 | mV/μs |
| | Ramp up speed, OTP_DVS_BUCK12[1:0] = 01 | 2.34 | 3.13 | 3.91 | mV/μs |
| | Ramp up speed, OTP_DVS_BUCK12[1:0] = 10 | 1.95 | 2.60 | 3.26 | mV/μs |
| | Ramp up speed, OTP_DVS_BUCK12[1:0] = 11 | 1.67 | 2.23 | 2.79 | mV/μs |
| V _{BUCK12_DVS_UP} (for V _{BUCK12} = 1.8 V) | Ramp up speed, OTP_DVS_BUCK12[1:0] = 00 | 7.33 | 9.763 | 12.21 | mV/μs |
| | Ramp up speed, OTP_DVS_BUCK12[1:0] = 01 | 2.93 | 3.91 | 4.89 | mV/μs |
| | Ramp up speed, OTP_DVS_BUCK12[1:0] = 10 | 2.44 | 3.25 | 4.08 | mV/μs |
| | Ramp up speed, OTP_DVS_BUCK12[1:0] = 11 | 2.09 | 2.79 | 3.49 | mV/μs |
| V _{BUCK12_DVS_DOWN} (for V _{BUCK12} up to 1.5 V) | Ramp down speed, OTP_DVS_BUCK12[1:0] = 00 | 3.91 | 5.21 | 6.51 | mV/μs |
| | Ramp down speed, OTP_DVS_BUCK12[1:0] = 01 | 2.34 | 3.13 | 3.91 | mV/μs |
| | Ramp down speed, OTP_DVS_BUCK12[1:0] = 10 | 1.95 | 2.6 | 3.26 | mV/μs |
| | Ramp down speed, OTP_DVS_BUCK12[1:0] = 11 | 1.67 | 2.23 | 2.79 | mV/μs |
| V _{BUCK12_DVS_DOWN} (for V _{BUCK12} = 1.8 V) | Ramp down speed, OTP_DVS_BUCK12[1:0] = 00 | 4.89 | 6.51 | 8.14 | mV/μs |
| | Ramp down speed, OTP_DVS_BUCK12[1:0] = 01 | 2.93 | 3.91 | 4.89 | mV/μs |
| | Ramp down speed, OTP_DVS_BUCK12[1:0] = 10 | 2.44 | 3.25 | 4.08 | mV/μs |
| | Ramp down speed, OTP_DVS_BUCK12[1:0] = 11 | 2.09 | 2.79 | 3.49 | mV/μs |
| T _{BUCK12_SOFT_START} | V _{BUCK12_SOFT_START} = V _{BUCK12} / V _{BUCK12_DVS_UP} Soft start for V _{BUCK12} = 1.2 V and OTP_DVS_BUCK12[1:0] = 00 | 122.9 | 153.6 | 204.8 | μs |
| | Soft start for V _{BUCK12} = 1.2 V and OTP_DVS_BUCK12[1:0] = 11 To be recalculated for different V _{BUCK12} and different V _{BUCK12_DVS_UP} | 430.1 | 538.1 | 718.5 | μs |
| V _{BUCK12_STARTUP} | Overshoot at startup | — | — | 50 | mV |
| T _{BUCK12_OFF_MIN} | HS minimum OFF time | 9 | 30 | 54 | ns |
| T _{BUCK12_DT} | Dead time to avoid cross conduction | 0.01 | 3 | 20 | ns |
| R _{BUCK12_HS_RON} | HS PMOS R _{DSon} | — | — | 135 | mΩ |

| Symbol | Parameter | Min | Typ | Max | Unit |
|----------------------------|---|-----|-----|------|------|
| R _{BUCK12_LS_RON} | LS NMOS RD _{SON} | — | — | 80 | mΩ |
| R _{BUCK12_DISch} | Discharge resistance (when BUCK1,2 is disabled) | 250 | 500 | 1000 | Ω |
| TSD _{BUCK12} | Thermal shutdown threshold | 160 | — | — | °C |
| TSD _{BUCK12_HYST} | Thermal shutdown threshold hysteresis | — | 9 | — | °C |
| T _{BUCK12_TSD} | Thermal shutdown filtering time | 3 | 5 | 8 | μs |

22.6 BUCK1 and BUCK2 efficiency

BUCK1 and BUCK2 efficiency versus current load is given for information based on external component criteria provided and VP_{RE} voltage 4.1 V. If the conditions change, it has to be recalculated with the VR5500_PDT_{CAL} tool. The real efficiency has to be verified by measurement at the application level.

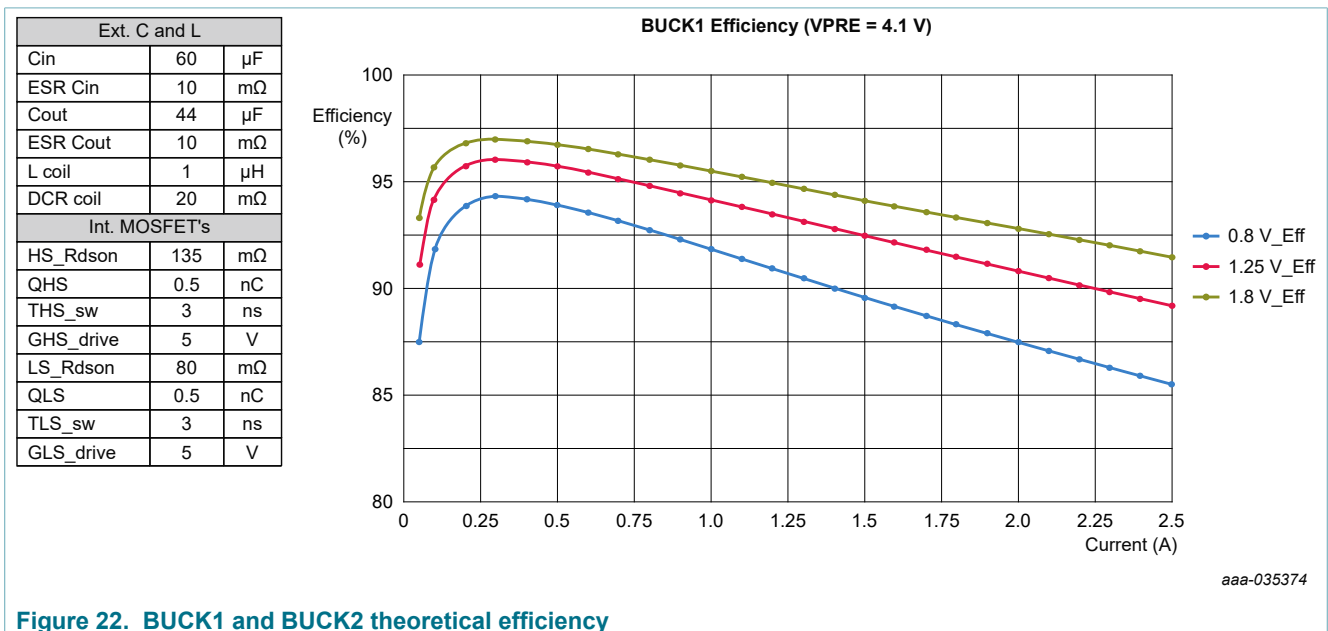


Figure 22. BUCK1 and BUCK2 theoretical efficiency

23 Low voltage buck: BUCK3

23.1 Functional description

BUCK3 block is a low voltage, synchronous, peak current mode buck converter with integrated HS PMOS and LS NMOS. BUCK3 works in force PWM and the output voltage is configurable by OTP from 1.0 V to 3.3 V, the switching frequency is 2.22 MHz and the output current is limited to 3.6 A peak. The input of this block can be connected to the output of VP_{RE} or VBOOST when VBOOST = 5.0 V only. The stability is ensured by an internal Type 2 compensation network with slope compensation.

By default, BUCK3 switching frequency is derived from the internal oscillator, and can be synchronized with an external frequency signal applied on FIN input pin. The change from internal oscillator to external clock or vice versa is controlled by I2C.

An overcurrent detection and a thermal shutdown are implemented on BUCK3 to protect the internal MOSFETs. The overcurrent induces a duty cycle reduction that could lead to the output voltage gradually dropping, causing an undervoltage condition.

BUCK3 is part number dependent according to OTP_BUCK3EN bit. BUCK3_INQ pin, used to bias internal BUCK3 driver, and must be connected to the same source pin than BUCK3_IN pin. The ramp up and ramp down of BUCK3 when it is enabled and disabled is configurable with OTP_DVS_BUCK3[1:0] bits to accommodate multiple MCU soft start requirements.

Programmable phase shift control is implemented, see [Section 25 "Clock management"](#).

23.2 Application schematic

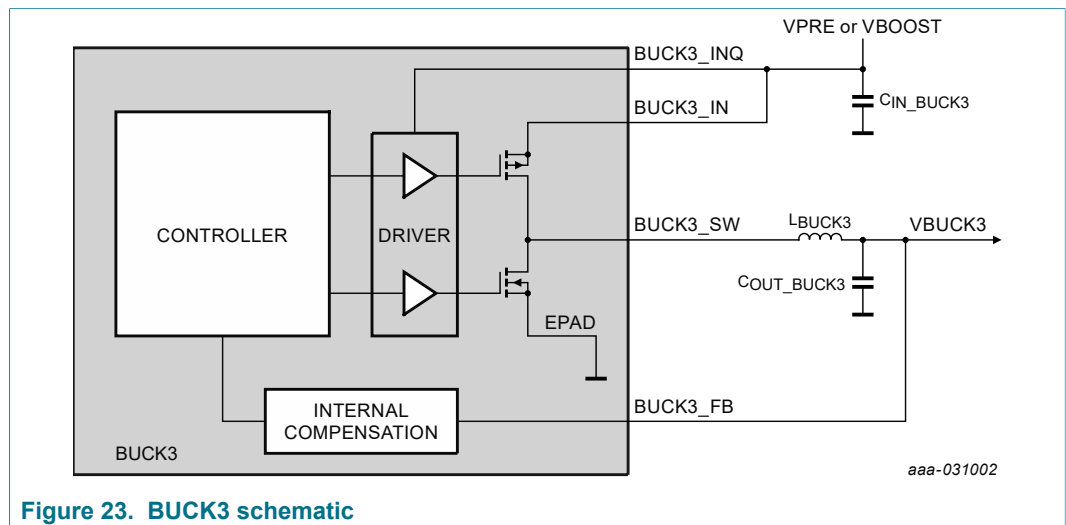


Figure 23. BUCK3 schematic

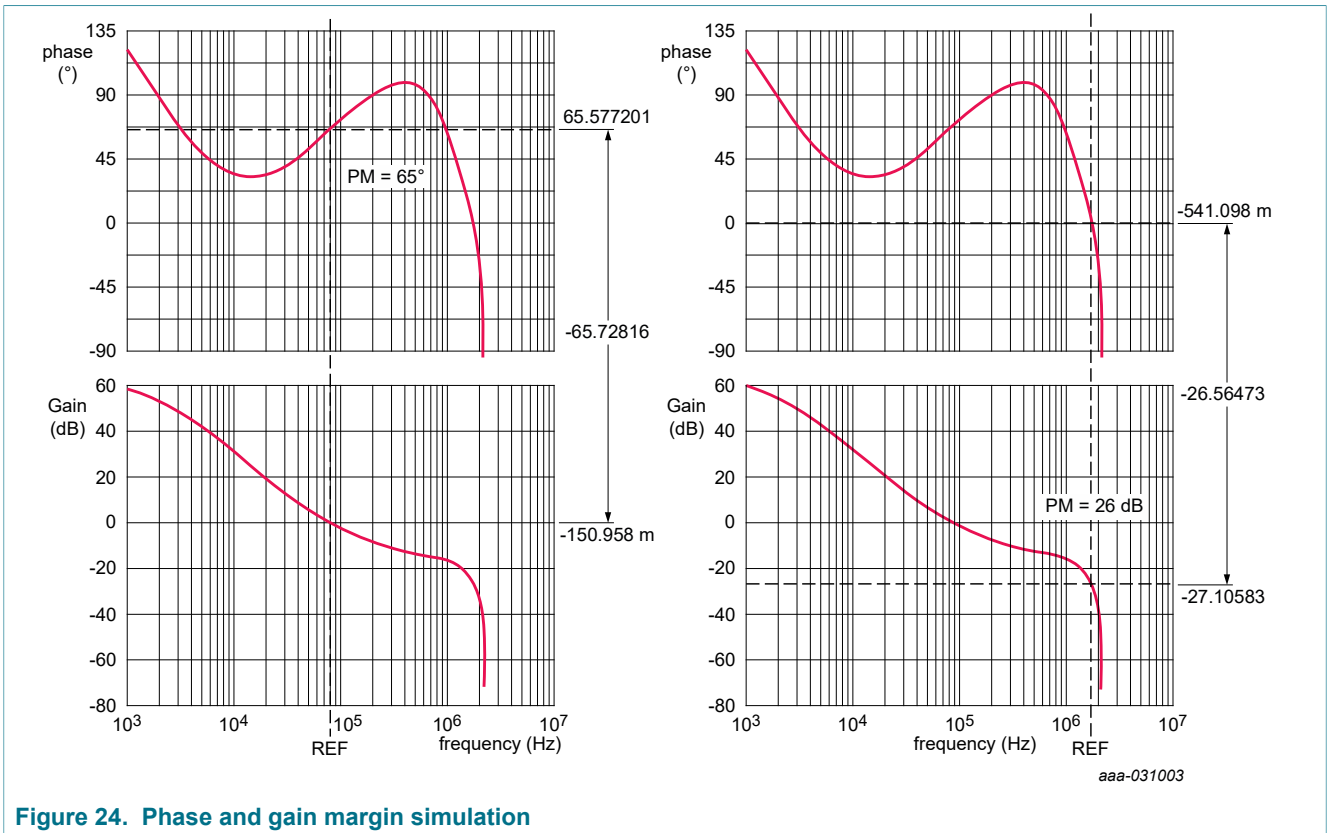
23.3 Compensation network and stability

The internal compensation network ensures the stability and the transient response performance of the buck converter. OTP_VB3INDOPT[1:0] scales the slope compensation and the zero cross detection according to inductor value. 1.0 μH is the recommended inductor value for BUCK3.

Use case with $V_{\text{PRE}} = 3.3 \text{ V}$, $V_{\text{BUCK3}} = 2.3 \text{ V}$, $L_{\text{VBUCK3}} = 1.0 \mu\text{H}$, $F_{\text{BUCK3_SW}} = 2.22 \text{ MHz}$, $C_{\text{OUT_BUCK3}} = 44 \mu\text{F}$

Use case stability verification

- Phase margin target $\text{PM} > 45^\circ$ and gain margin target $\text{GM} > 6 \text{ dB}$.



Use case transient response verification

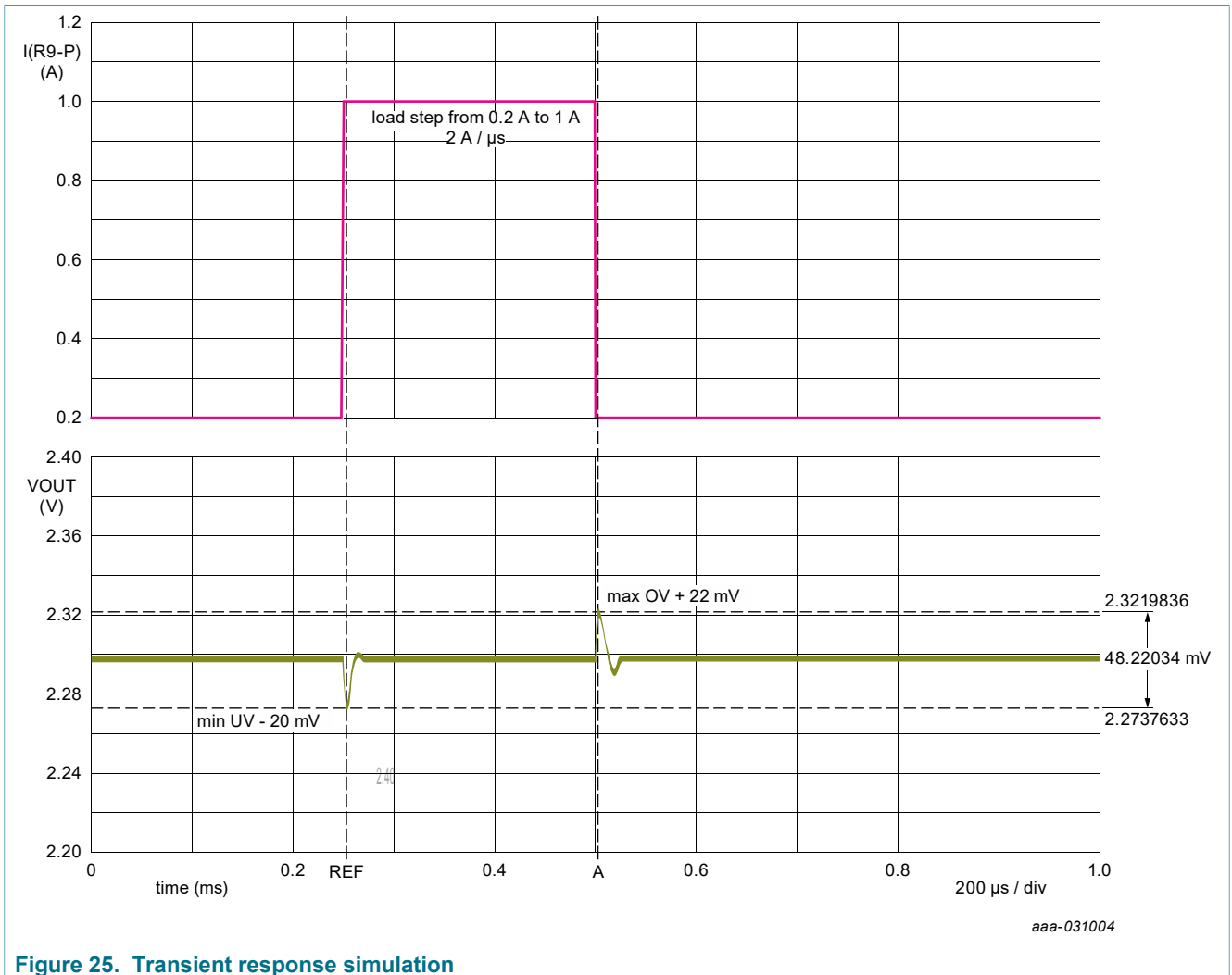


Figure 25. Transient response simulation

23.4 BUCK3 electrical characteristics

Table 72. BUCK3 electrical characteristics

$T_A = -40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$, unless otherwise specified. $VSUP = VSUP_UVH$ to 36 V, unless otherwise specified. All voltages referenced to ground.

| Symbol | Parameter | Min | Typ | Max | Unit |
|------------------|---|------|------|------|---------------|
| V_{BUCK3_IN} | Input voltage range | 2.5 | — | 5.5 | V |
| V_{BUCK3} | Output voltage (OTP_VB3V[4:0] bits) 1.0 V, 1.1 V, 1.2 V, 1.25 V, 1.3 V, 1.35 V, 1.5 V, 1.6 V, 1.8 V, 2.3 V, 2.5 V, 2.8 V, 3.3 V | 1.0 | — | 3.3 | V |
| I_{BUCK3} | DC output current capability | — | 2.5 | — | A |
| V_{BUCK3_ACC} | Output voltage accuracy ($I_{out} < 2.5\text{ A}$) | -2 | — | +2 | % |
| V_{BUCK3_SW} | Switching frequency range | 2.1 | 2.22 | 2.35 | MHz |
| L_{BUCK3} | Inductor for $V_{BUCK3_SW} = 2.22\text{ MHz}$ (OTP_VB3INDOPT[1:0] bits) | 0.47 | 1.0 | 1.5 | μH |
| C_{OUT_BUCK3} | Effective output capacitor | 40 | — | 120 | μF |
| | Output decoupling capacitor | — | 0.1 | — | μF |

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------------------------------|---|-------|-------|--------|-------|
| C _{IN_BUCK3} | Effective input capacitor (close to BUCK3_IN pin) | 4.7 | — | — | μF |
| | Input decoupling capacitor (close to BUCK3_IN pin) | — | 0.1 | — | μF |
| V _{BUCK3_TLR} | Transient load regulation (C _{out} = 40 μF, from 200 mA to 1.0 A, di/dt = 2.0 A/μs) | -50 | — | +50 | mV |
| I _{LIM_BUCK3} | Inductor peak current limitation range (OTP_VB3SWILIM[1:0] bits) | 2.0 | 2.6 | 3.1 | A |
| | | 3.6 | 4.5 | 5.45 | A |
| T _{BUCK3_ON_MIN} | HS minimum ON time | 5 | 50 | 80 | ns |
| V _{BUCK3_DVS_UP_DOWN} | Ramp up and ramp down speed, OTP_DVS_BUCK3[1:0] = 00 | 7.81 | 10.42 | 13.02 | mV/μs |
| | Ramp up and ramp down speed, OTP_DVS_BUCK3[1:0] = 01 | 2.6 | 3.47 | 4.34 | mV/μs |
| | Ramp up and ramp down speed, OTP_DVS_BUCK3[1:0] = 10 | 1.95 | 2.6 | 3.26 | mV/μs |
| | Ramp up and ramp down speed, OTP_DVS_BUCK3[1:0] = 11 | 1.56 | 2.08 | 2.60 | mV/μs |
| T _{BUCK3_SOFT_START} | V _{BUCK3_SOFT_START} = V _{BUCK3} / V _{BUCK3_DVS_UP} Soft start for V _{BUCK3} = 1.8 V and OTP_DVS_BUCK3[1:0] = 00 | 84.8 | 105.6 | 140.08 | μs |
| | Soft start for V _{BUCK3} = 1.8 V and OTP_DVS_BUCK3[1:0] = 11 To be recalculated for different V _{BUCK3} and different V _{BUCK3_DVS_UP_DOWN} | 422.4 | 528 | 704 | μs |
| V _{BUCK3_STARTUP} | Overshoot at startup | — | — | 50 | mV |
| T _{BUCK3_DT} | Dead time to avoid cross conduction | 0.01 | 3 | 20 | ns |
| R _{BUCK3_HS_RON} | HS PMOS R _{DSon} | — | — | 135 | mΩ |
| R _{BUCK3_LS_RON} | LS NMOS R _{DSon} | — | — | 80 | mΩ |
| R _{BUCK3_DISCH} | Discharge resistance (when BUCK3 is disabled) | 250 | 500 | 1000 | Ω |
| TSD _{BUCK3} | Thermal shutdown threshold | 160 | — | — | °C |
| TSD _{BUCK3_HYST} | Thermal shutdown threshold hysteresis | — | 9 | — | °C |
| T _{BUCK3_TSD} | Thermal shutdown filtering time | 3 | 5 | 8 | μs |

23.5 BUCK3 efficiency

BUCK3 efficiency versus current load is given for information based on external component criteria provided and VPRE voltage 4.1 V. If the conditions change, it has to be recalculated with the VR5500_PDTCAL tool. The real efficiency has to be verified by measurement at the application level.

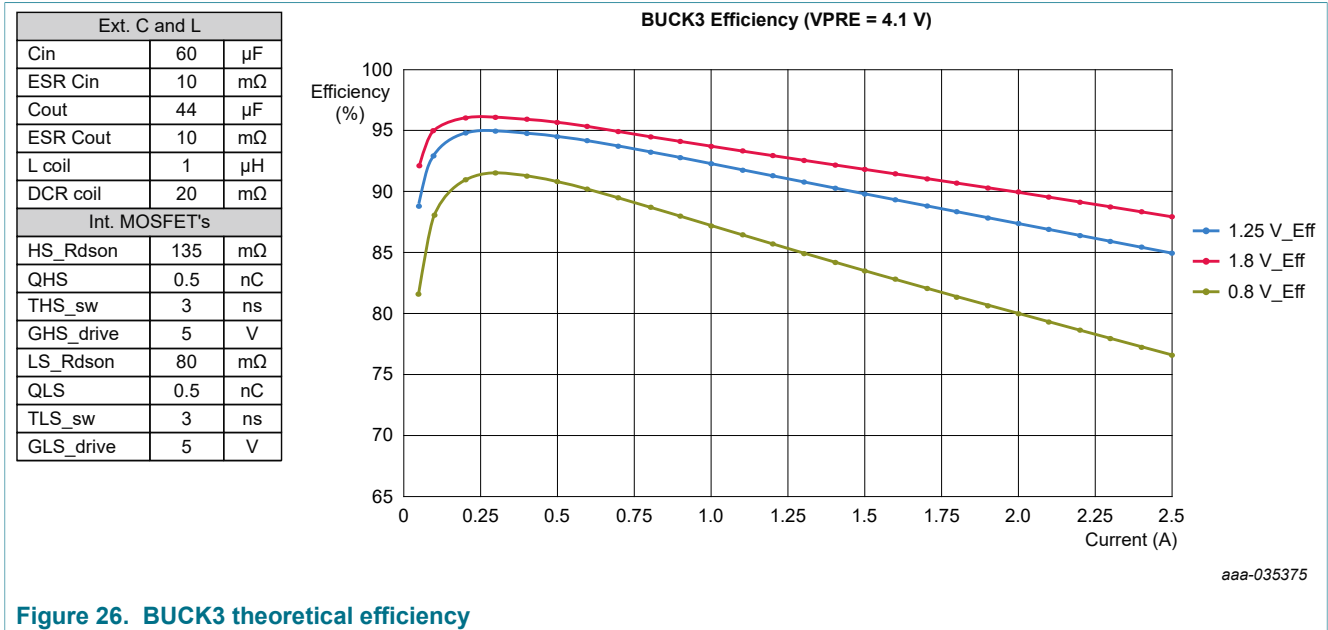


Figure 26. BUCK3 theoretical efficiency

24 Linear voltage regulator: LDO1, LDO2

24.1 Functional description

LDO1 and LDO2 blocks are two linear voltage regulators. The output voltage is configurable by OTP from 1.1 V to 5.0 V. A minimum voltage drop is required depending on the output current capability (0.5 V for 150 mA and 1.0 V for 400 mA). The LDO current capability is linear with the voltage drop and can be estimated to $I(\text{mA}) = 500 \times V_{\text{LDO12_DROP}} - 100$ for intermediate voltage drop between 0.5 V and 1.0 V.

LDO1 input supply is externally connected to VPRES, VBOOST, or another supply. LDO2 input supply is internally connected to the output of VBOOST. An overcurrent detection and a thermal shutdown are implemented on LDO1 and LDO2 to protect the internal pass device.

24.2 Application schematics

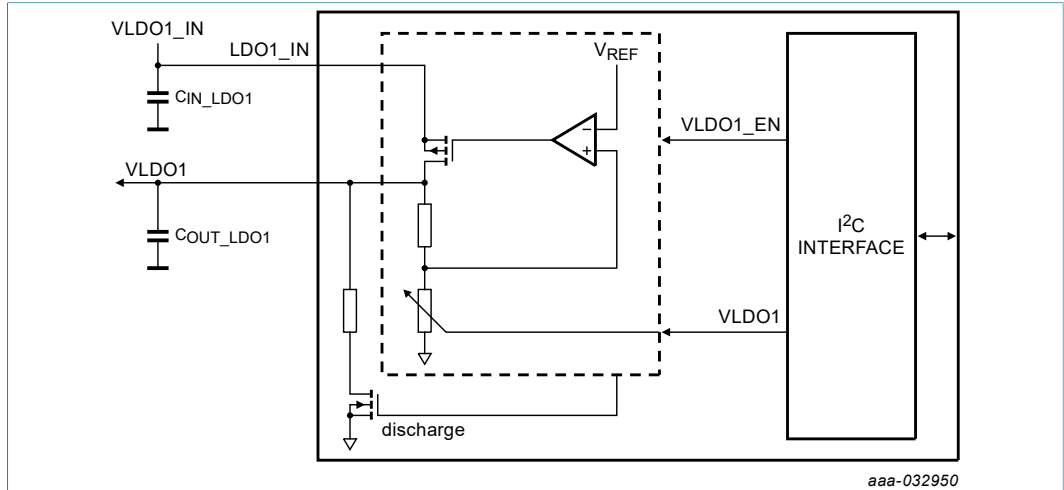


Figure 27. LDO1 block diagram

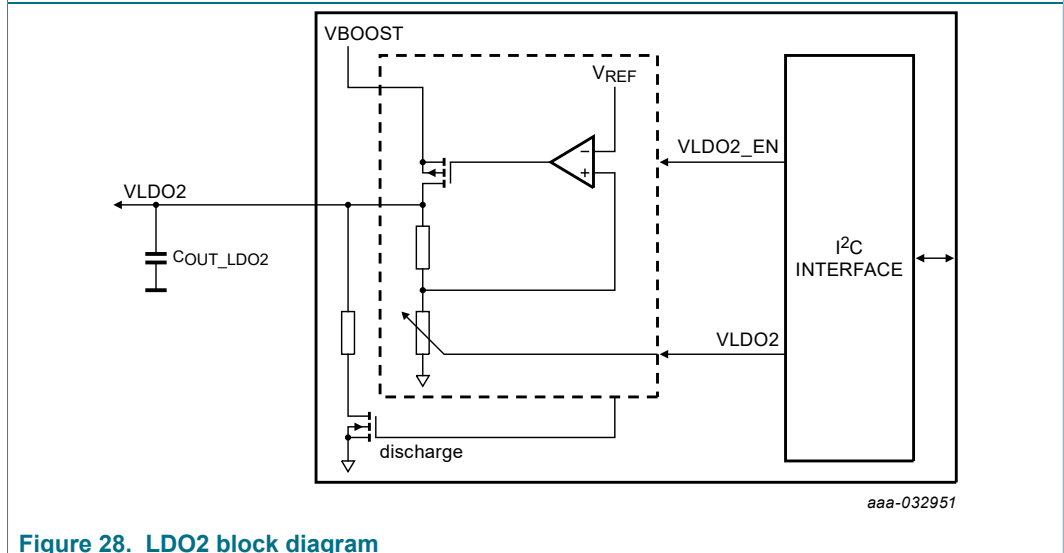


Figure 28. LDO2 block diagram

24.3 LDO1 and LDO2 electrical characteristics

Table 73. LDO1 and LDO2 electrical characteristics

$T_A = -40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$, unless otherwise specified. $VSUP = VSUP_UVH$ to 36 V, unless otherwise specified. All voltages referenced to ground.

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------------------------|--|-----|-----|-----|--------------------|
| V_{LDO12_IN} | Input voltage range | 2.5 | — | 6.5 | V |
| V_{LDO12} | Output voltage (OTP_VLDO1V[2:0] and OTP_LDO2V[2:0] bits) 1.1 V, 1.2 V, 1.6 V, 1.8 V, 2.5 V, 2.8 V, 3.3 V, 5.0 V | 1.1 | — | 5.0 | V |
| $V_{LDO12_ACC_150}$ | Output voltage accuracy, 150 mA current capability | -2 | — | +2 | % |
| $V_{LDO12_ACC_400}$ | Output voltage accuracy, 400 mA current capability | -3 | — | +3 | % |
| $V_{LDO12_DROP_150}$ | Minimum voltage drop for 150 mA current capability | 0.5 | — | — | V |
| $V_{LDO12_DROP_400}$ | Minimum voltage drop for 400 mA current capability | 1.0 | — | — | V |
| C_{IN_LDO1} | Input capacitor (close to LDO1_IN pin) | 1.0 | — | — | μF |
| $C_{OUT_LDO12_150}$ | Output capacitor, 150 mA current capability | 4.7 | — | 10 | μF |
| $C_{OUT_LDO12_400}$ | Output capacitor, 400 mA current capability | 6.8 | — | 10 | μF |
| C_{OUT_LDO12} | Output decoupling capacitor | 0.1 | — | — | μF |
| $V_{LDO12_LTR_150}$ | Transient load regulation (from 10 mA to 150 mA in 2.0 μs) | -4 | — | +4 | % |
| $V_{LDO12_LTR_400}$ | Transient load regulation (from 10 mA to 400 mA in 4.0 μs) | -5 | — | +5 | % |
| V_{LDO12_LR} | Line regulation | — | — | 0.5 | % |
| $V_{LDO12_ILIM_150}$ | Current limitation, 150 mA current capability (OTP_LDO1ILIM and OTP_LDO2ILIM bits) | 200 | 280 | 500 | mA |
| $V_{LDO12_ILIM_400}$ | Current limitation, 400 mA current capability (OTP_LDO1ILIM and OTP_LDO2ILIM bits) | 430 | 560 | 800 | mA |
| $V_{LDO12_SOFT_START}$ | Soft start (enable to 90 %) | — | 1.0 | 1.3 | ms |
| $V_{LDO12_STARTUP}$ | Overshoot at startup | — | — | 2 | % |
| R_{LDO12_DISCH} | Discharge resistance (when LDO1,2 is disabled) | 10 | 20 | 60 | Ω |
| TSD_{LDO12} | Thermal shutdown threshold | 160 | — | — | $^{\circ}\text{C}$ |
| TSD_{LDO12_HYST} | Thermal shutdown threshold hysteresis | — | 9 | — | $^{\circ}\text{C}$ |
| T_{LDO12_TSD} | Thermal shutdown filtering time | 3 | 5 | 8 | μs |

25 Clock management

25.1 Clock description

The clock management block is made of the internal oscillator, the Phase Locked Loop (PLL) and multiple dividers. This block manages the clock generation for the internal digital state machines, the switching regulators, and the external clock synchronization.

The internal oscillator is running at 20 MHz by default after startup. The frequency is programmable by I2C and a spread spectrum feature can be activated by I2C to reduce the emission of the oscillator fundamental frequency.

VPRE switching frequency is coming from CLK2 (455 kHz) or CLK1 (2.22 MHz). BUCK1,2,3 and BOOST switching frequency is coming from CLK1 (2.22 MHz). The switching regulators can be synchronized with an external frequency coming from FIN pin. A dedicated watchdog monitoring is implemented to verify and report the correct FIN frequency range. Different clocks can be sent to FOUT pin to synchronize an external IC or for diagnostic.

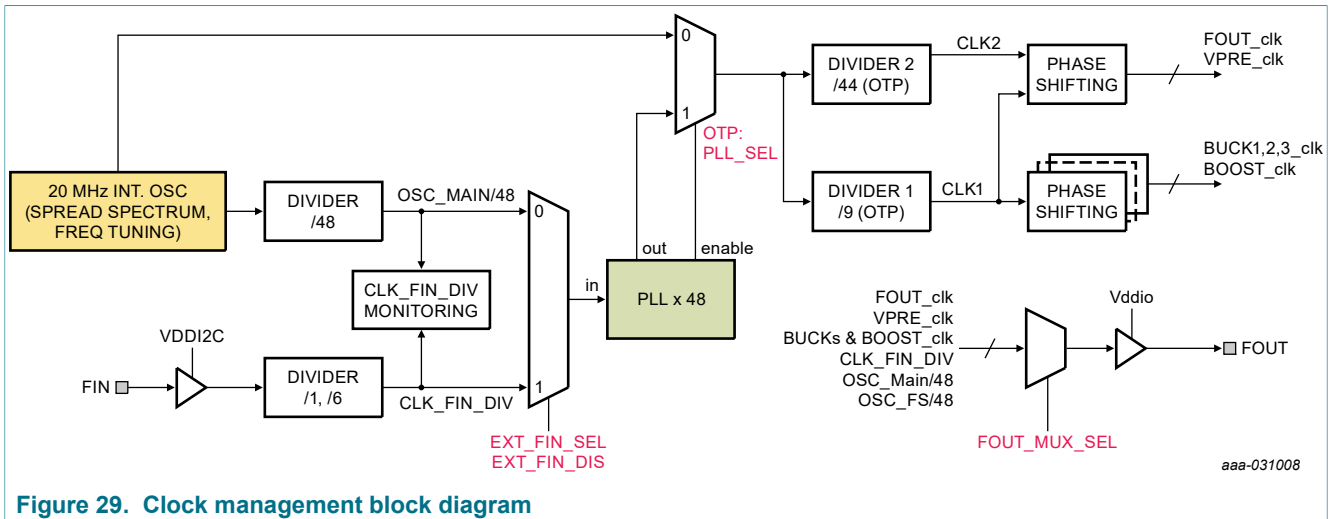


Figure 29. Clock management block diagram

25.2 Phase shifting

The clocks of the switching regulators (VPRE_clk, BOOST_clk, BUCK1_clk, BUCK2_clk and BUCK3_clk) can be delayed in order to avoid all the regulators to turn ON at the same time to reduce peak current and improve EMC performance.

Each clock of each regulator can be shifted from 1 to 7 clock cycles of CLK running at 20 MHz what corresponds to 50 ns. The phase shift configuration is done by OTP configuration using OTP_VPRE_ph[2:0], OTP_VBST_ph[2:0], OTP_BUCK1_ph[2:0], OTP_BUCK2_ph[2:0], and OTP_BUCK3_ph[2:0].

VPRE and BUCK3 have a peak current detection architecture. The PWM synchronizes the turn ON of the high-side switch. BUCK1 and BUCK2 have a valley current detection architecture. The PWM synchronizes the turn ON of the low-side switch.

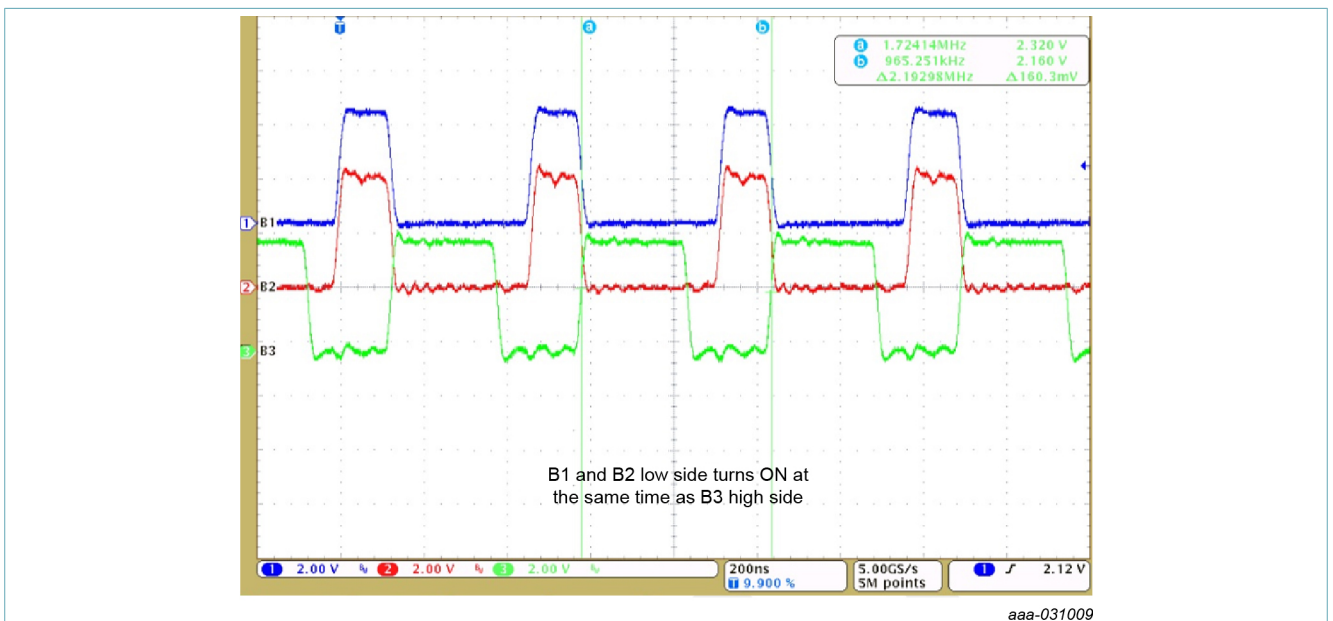


Figure 30. BUCK1,2,3_clk = 2.22 MHz without clock phase shifting

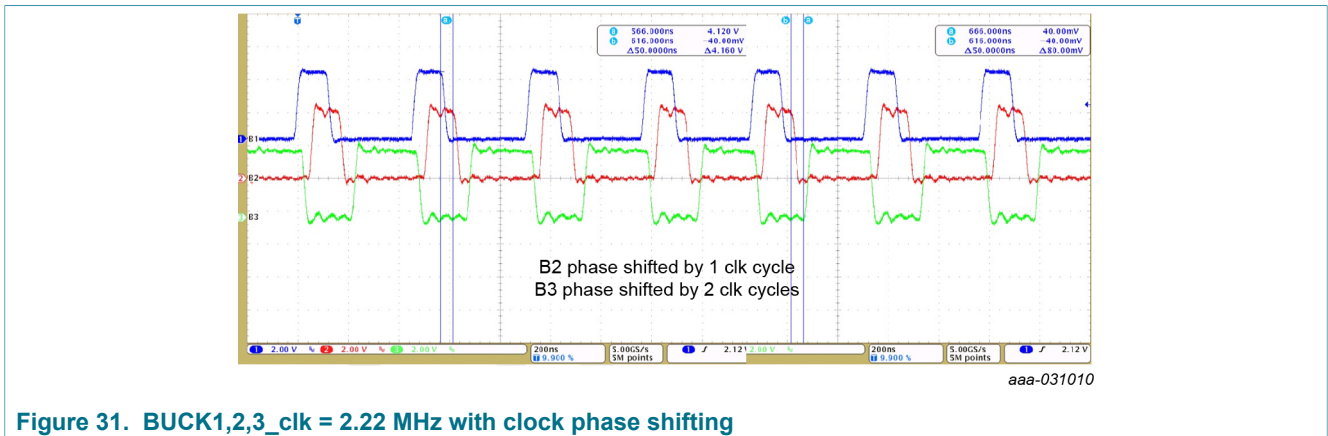


Figure 31. BUCK1,2,3_clk = 2.22 MHz with clock phase shifting

25.3 Manual frequency tuning

The internal oscillator frequency, 20 MHz by default, can be programmed from 16 MHz to 24 MHz with 1.0 MHz frequency step by I2C. The oscillator functionality is guaranteed for frequency increment of one step at a time in either direction, with a minimum of 10 μ s between two steps. For any unused code of the CLK_TUNE [3:0] bits, the internal oscillator is set at the default 20 MHz frequency.

To change the internal oscillator frequency from 20 MHz to 24 MHz, four I2C commands are required with 10 μ s wait time between each command (21 MHz – wait 10 μ s – 22 MHz – wait 10 μ s – 23 MHz – wait 10 μ s – 24 MHz). To change the internal oscillator frequency from 24 MHz to 16 MHz, eight I2C commands are required with 10 μ s wait time between each command (23 MHz – wait 10 μ s – 22 MHz – wait 10 μ s – 21 MHz – wait 10 μ s – 20 MHz – wait 10 μ s – 19 MHz – wait 10 μ s – 18 MHz – wait 10 μ s – 17 MHz – wait 10 μ s – 16 MHz).

Table 74. Manual frequency tuning configuration

| CLK_TUNE [3:0] | Oscillator frequency [MHz] |
|-----------------|----------------------------|
| 0000 (default) | 20 |
| 0001 | 21 |
| 0010 | 22 |
| 0011 | 23 |
| 0100 | 24 |
| 1001 | 16 |
| 1010 | 17 |
| 1011 | 18 |
| 1100 | 19 |
| Reset condition | POR |

25.4 Spread spectrum

The internal oscillator can be modulated with a triangular carrier frequency of 23 kHz or 94 kHz with ± 5 % deviation range around the oscillator frequency. The spread spectrum feature can be activated by I2C with the MOD_EN bit and the carrier frequency can be selected by I2C with the MOD_CONF bit. By default, the spread spectrum is disabled.

The spread spectrum and the manual frequency tuning functions cannot be used at the same time.

The main purpose of the spread spectrum is to improve the EMC performance by spreading the energy of the internal oscillator and VPRE frequency on VBAT frequency spectrum. It is recommended to select 23 kHz carrier frequency when VPRE is configured at 455 kHz and 94 kHz when VPRE is configured at 2.2 MHz for the best performance.

25.5 External clock synchronization

To synchronize the switching regulators with an external frequency coming from FIN pin, the PLL is enabled with OTP_PLL_SEL bit. The FIN pin accepts two ranges of frequency depending on the divider selection to always have CLK clock at the output of the PLL in the working range of the digital blocks from 16 MHz to 24 MHz. When FIN_DIV = 0, the input frequency range must be between 333 kHz and 500 kHz. When FIN_DIV = 1, the input frequency range must be between 2.0 MHz and 3.0 MHz.

After the FIN clock divider configuration with FIN_DIV bit, the FIN clock is routed to the PLL input with EXT_FIN_SEL bit. The CLK clock changes from the internal oscillator to FIN external clock with EXT_FIN_SEL bit. So, the configuration procedure is FIN_DIV first, then apply FIN and finally set EXT_FIN_SEL.

If FIN is out of range, CLK clock moves back to the internal oscillator and reports the error using the CLK_FIN_DIV_OK bit. When FIN comes back in the range, the configuration procedure described above is executed again.

The FOUT pin can be used to synchronize an external device with the VR5500. The frequency sent to FOUT is selected by I2C with the FOUT_MUX_SEL [3:0] bits.

Table 75. FOUT multiplexer selection

| FOUT_MUX_SEL [3:0] | FOUT multiplexer selection |
|--------------------|--|
| 0000 (default) | No signal, FOUT is low |
| 0001 | VPRE_clk |
| 0010 | BOOST_clk |
| 0011 | BUCK1_clk |
| 0100 | BUCK2_clk |
| 0101 | BUCK3_clk |
| 0110 | FOUT_clk (CLK1 or CLK2 selected with FOUT_CLK_SEL bit) |
| 0111 | OSC_MAIN/48 (when PLL is enabled by OTP) |
| 1000 | OSC_FS/48 |
| 1001 | CLK_FIN_DIV |
| Others | No signal, FOUT is low |
| Reset condition | POR |

25.6 Electrical characteristics

Table 76. Electrical characteristics

$T_A = -40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$, unless otherwise specified. $VSUP = VSUP_UVH$ to 36 V, unless otherwise specified. All voltages referenced to ground.

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------------------------------|---|-------------------------------|--------|-------------------------------|---------------|
| 20 MHz internal oscillator | | | | | |
| $F_{20\text{MHz}}$ | Oscillator nominal frequency (programmable) | — | 20 | — | MHz |
| $F_{20\text{MHz_ACC}}$ | Oscillator accuracy | -6 | — | +6 | % |
| $T_{20\text{MHz_step}}$ | Oscillator frequency tuning step transition time | — | 10 | — | μs |
| Spread spectrum | | | | | |
| FSS_{MOD} | Spread spectrum frequency modulation (MOD_CONF I2C configuration) | — | 23 | — | kHz |
| | | — | 94 | — | kHz |
| FSS_{RANGE} | Spread spectrum range (around the nominal frequency) | -5 | — | +5 | % |
| Clock synchronization (FIN) | | | | | |
| $V_{\text{FIN_IN}}$ | Input voltage range | — | VDDI2C | — | V |
| $DC_{\text{FIN_FOUT}}$ | FIN and FOUT duty cycle | 40 | 50 | 60 | % |
| FIN_{RANGE} | FIN input frequency range (FIN_DIV I2C configuration) | 333 | 417 | 500 | kHz |
| | | 2.25 | 2.5 | 2.75 | MHz |
| FIN_{VIL} | FIN low-voltage threshold | $0.3 \times V_{\text{DDI2C}}$ | — | — | V |
| FIN_{VIH} | FIN high-voltage threshold | — | — | $0.7 \times V_{\text{DDI2C}}$ | V |
| FIN_{HYST} | FIN hysteresis | 0.1 | — | — | V |
| FIN_{IPD} | FIN internal pull-down current source | 7 | 10 | 13 | μA |
| FIN_{DLY} | FIN input buffer propagation delay | — | — | 8 | ns |
| $FIN_{\text{ERR_LONG}}$ | CLK_FIN_DIV monitoring, long deviation detection | 5 | — | — | μs |
| $FIN_{\text{ERR_SHORT}}$ | CLK_FIN_DIV monitoring, short deviation detection | — | — | 1.5 | μs |
| FIN_{TLOST} | Time to switch to internal oscillator when FIN is lost | — | — | 3 | μs |
| Clock synchronization (FOUT) | | | | | |
| $V_{\text{FOUT_OUT}}$ | Output voltage range | — | VDDIO | — | V |
| FOUT_{VOL} | FOUT low-voltage threshold at 2.0 mA | — | — | 0.5 | V |
| FOUT_{VOH} | FOUT high-voltage threshold at -2.0 mA | $V_{\text{DDIO}} - 0.5$ | — | — | V |
| I_{FOUT} | 3-state leakage current ($V_{\text{DDIO}} = 5.0\text{ V}$) | -1.0 | — | 1.0 | μA |
| $\text{FOUT}_{\text{TRISE}}$ | FOUT rise time (from 20 % to 80 % of VDDIO, $C_{\text{out}} = 30\text{ pF}$) | — | — | 20 | ns |
| $\text{FOUT}_{\text{TFALL}}$ | FOUT fall time (from 80 % to 20 % of VDDIO, $C_{\text{out}} = 30\text{ pF}$) | — | — | 20 | ns |
| $\text{PLL}_{\text{TLOCK}}$ | PLL lock time | — | — | 90 | μs |
| PLL_{TSET} | PLL settling time (from EXT_FIN_DIS enable to $\pm 1\%$ of output frequency) | — | — | 125 | μs |

26 Analog multiplexer: AMUX

26.1 Functional description

The AMUX pin delivers 32 analog voltage channels to the MCU ADC input. The voltage channels delivered to AMUX pin can be selected by I2C. The maximum AMUX output voltage range is VDDIO. External Rs/Cout components are required for the buffer stability.

26.2 Block diagram

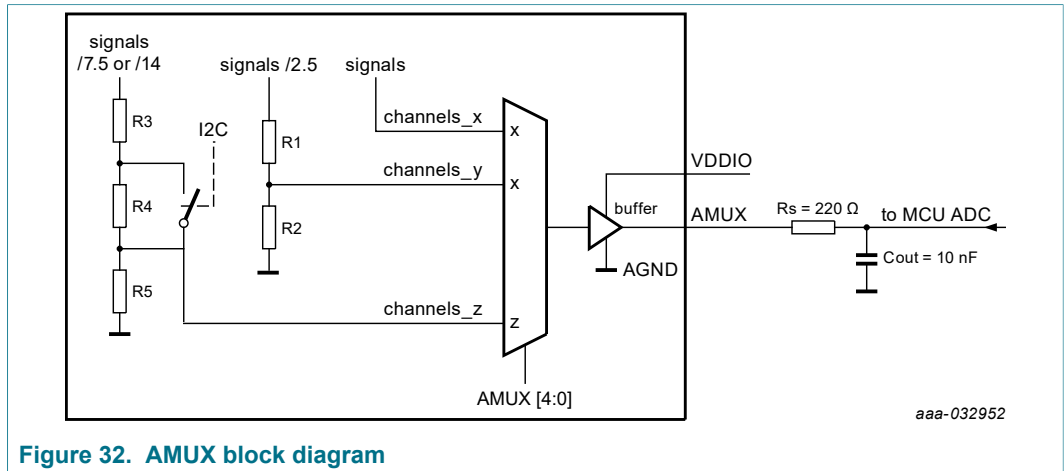


Figure 32. AMUX block diagram

26.3 AMUX channel selection

Table 77. AMUX output selection

| AMUX[4:0] | Signal selection for AMUX output |
|-------------------------|--|
| 0 0000 (default) | GND |
| 0 0001 | VDDIO voltage |
| 0 0010 | Temperature sensor : $T(^{\circ}\text{C}) = [(V_{\text{AMUX}} - V_{\text{TEMP25}}) / V_{\text{TEMP_COEFF}}] + 25$ |
| 0 0011 | Bandgap main: 1.0 V \pm 1 % |
| 0 0100 | Bandgap fail-safe: 1.0 V \pm 1 % |
| 0 0101 | VBUCK1 voltage |
| 0 0110 | VBUCK2 voltage |
| 0 0111 | VBUCK3 voltage divided by 2.5 |
| 0 1000 | VPRE voltage divided by 2.5 |
| 0 1001 | VBOOST voltage divided by 2.5 |
| 0 1010 | VLDO1 voltage divided by 2.5 |
| 0 1011 | VLDO2 voltage divided by 2.5 |
| 0 1100 | VBOS voltage divided by 2.5 |
| 0 1101 | Reserved |
| 0 1110 | VSUP1 voltage divided by 7.5 or 14 (I2C configuration with bit RATIO) |

| AMUX[4:0] | Signal selection for AMUX output |
|-----------|---|
| 0 1111 | WAKE1 voltage divided by 7.45 or 13.85 (I2C configuration with bit RATIO) |
| 1 0000 | WAKE2 voltage divided by 7.45 or 13.85 (I2C configuration with bit RATIO) |
| 1 0001 | Vana: internal main analog voltage supply: 1.6 V \pm 2 % |
| 1 0010 | Vdig: internal main digital voltage supply: 1.6 V \pm 2 % |
| 1 0011 | Vdig_fs: internal fail-safe digital voltage supply: 1.6 V \pm 2 % |
| 1 0100 | PSYNC voltage |
| Others | Same as default value (00000): GND |

26.4 AMUX electrical characteristics

Table 78. AMUX electrical characteristics

$T_A = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$, unless otherwise specified. $VSUP = VSUP_UVH$ to 36 V, unless otherwise specified. All voltages referenced to ground.

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------------------|---|--|----------------------------|--|----------------------|
| V_{AMUX_VDDIO} | Minimum VDDIO operating voltage for AMUX | 3.2 | — | — | V |
| V_{AMUX_IN} | Input voltage range for VSUP, WAKE1, WAKE2 <ul style="list-style-type: none"> Ratio 7.45 and 7.5 Ratio 13.85 and 14 | 2.25 4.2 | — — | 22.5 42 | V |
| I_{AMUX} | Output buffer current capability | — | — | 2.0 | mA |
| V_{AMUX_OFF} | Offset voltage (Iout = 1.0 mA) | -7 | — | +7 | mV |
| V_{AMUX_RATIO} | Ratio accuracy <ul style="list-style-type: none"> Ratio 1 Ratio 2.5 Ratio 7.5 for VSUP1 Ratio 7.45 for WAKE12 Ratio 14 for VSUP1 Ratio 13.85 for WAKE12 | -0.5 -1.5 -2.0 -2.0 -2.0 -2.0 | — — — — — — | 0.5 1.5 2.0 2.0 2.0 2.0 | % |
| V_{AMUX_BRIDGE} | VSUP1, WAKE1, WAKE2 resistor bridge | 0.75 | 1.5 | 3 | M Ω |
| V_{TEMP25} | Temperature sensor voltage at 25 $^\circ\text{C}$ | 2.01 | 2.07 | 2.12 | V |
| V_{TEMP_COEFF} | Temperature sensor coefficient | -6.25 | -6 | -5.75 | mV/ $^\circ\text{C}$ |
| T_{AMUX_SET} | Settling time (from 10 % to 90 % of V_{DDIO} , $R_s = 220\ \Omega$, $C_{out} = 10\ \text{nF}$) | — | — | 10 | μs |
| R_s | Output resistor | — | 220 | — | Ω |
| C_{out} | Output capacitor | — | 10 | — | nF |

26.5 1.8 V MCU ADC input use case

VR5500 AMUX buffer is referenced to VDDIO, 3.3 V, or 5.0 V. In case the MCU requires a 1.8 V ADC input voltage, an external resistor bridge R1/R2 can be added in between AMUX output and ADC input as shown in [Figure 33](#). It is recommended to use 0.1 % resistor accuracy to limit the conversion error impact.

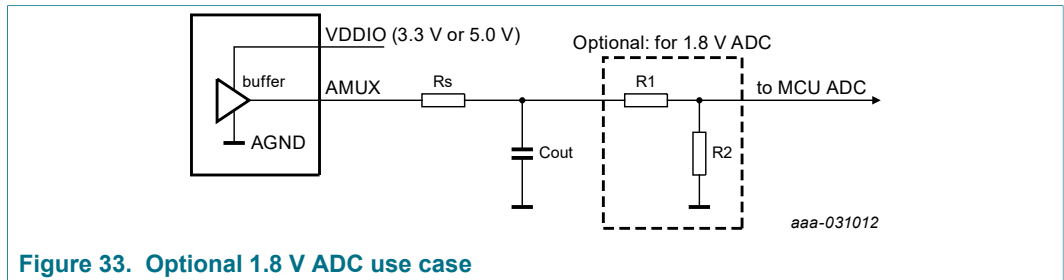


Figure 33. Optional 1.8 V ADC use case

The total resistor bridge value (R1 + R2) shall consume between min 10x ADC input current and max 1 mA at AMUX output to neither disturb the AMUX output buffer nor the ADC input. A good estimate is to calculate the resistor bridge value for 200 µA current consumption at VDDIO = 3.3 V.

Target R1 + R2 = 20 kΩ

For VDDIO = 3.3 V, $R2 / (R1 + R2) = 1.8 / 3.3 = 0.545$

After calculation, R2 = 11 kΩ and R1 = 9.3 kΩ

27 I/O interface pins

27.1 WAKE1, WAKE2

WAKE pins are used to manage the internal biasing of the device and the main state machine transitions.

- When WAKE1 or WAKE2 is > WAKE12_{VIH}, the internal biasing is started and the equivalent digital state is '1'
- When WAKE1 or WAKE2 is < WAKE12_{VIL}, the equivalent digital state is '0'
- When WAKE1 and WAKE2 are < WAKE12_{AVIL}, the internal biasing is stopped if the device was in Standby mode

WAKE1 and WAKE2 are level based wake-up input signals with analog measurement capability through AMUX. WAKE1 can be, for example, connected to a switched VBAT (KL 15 line) and WAKE2 to the wake-up output of a CAN or FlexRay transceiver. When a WAKE pin is used as a global pin, a C-R-C protection is required (see [Section 29 "Application information"](#)).

Table 79. WAKE1, WAKE2 electrical characteristics

T_A = -40 °C to 125 °C, unless otherwise specified. V_{SUP} = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

| Symbol | Parameter | Min | Typ | Max | Unit |
|------------------------|--|-----|-----|-----|------|
| WAKE12 _{AVIL} | Analog low input voltage threshold | 1.0 | — | — | V |
| WAKE12 _{VIL} | Digital low input voltage threshold | 2.0 | — | — | V |
| WAKE12 _{VIH} | Digital high input voltage threshold | — | — | 4.0 | V |
| I _{WAKE12} | Input current leakage at WAKE12 = 36 V | — | — | 100 | µA |
| | Input current leakage at WAKE12 = 60 V | — | — | 300 | µA |
| T _{WAKE12} | Filtering time | 50 | 70 | 100 | µs |

27.2 INTB

INTB is an open drain output pin with internal pull up to VDDIO. This pin generates a pulse when an internal interrupt occurs to inform the MCU. Each interrupt can be masked by setting the corresponding inhibit interrupt bit in M_INT_MASK registers.

Table 80. INTB electrical characteristics

$T_A = -40\text{ °C}$ to 125 °C , unless otherwise specified. $VSUP = VSUP_UVH$ to 36 V, unless otherwise specified. All voltages referenced to ground.

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------------------|--|-----|-----|-----|------|
| INTB _{PULL-up} | Internal pull-up resistor to VDDIO | 5.5 | 10 | 15 | kΩ |
| INTB _{VOL} | Low output level threshold (I = 2.0 mA) | — | — | 0.5 | V |
| INTB _{PULSE} | Pulse duration (without manual frequency tuning) | 90 | 100 | 110 | μs |

Table 81. List of interrupts from main logic

| Interrupt main | Description |
|----------------|---------------------------------------|
| VSUP_UV7 | VSUP undervoltage 7.0 V |
| VSUP_UVH | VSUP undervoltage high |
| VSUP_UVL | VSUP undervoltage low |
| VBOS_UVH | VBOS undervoltage high |
| VPRE_OC | VPRE overcurrent |
| VPRE_FB_OV | VPRE overvoltage protection |
| VPRE_UVH | VPRE undervoltage high |
| BUCK1_TSD | BUCK1 overtemperature shutdown event |
| BUCK1_OC | BUCK1 overcurrent |
| BUCK2_TSD | BUCK2 over temperature shutdown event |
| BUCK2_OC | BUCK2 overcurrent |
| BUCK3_TSD | BUCK3 overtemperature shutdown event |
| BUCK3_OC | BUCK3 overcurrent |
| BOOST_TSD | BOOST overtemperature shutdown event |
| VBOOST_OV | BOOST overvoltage |
| VBOOST_UVH | BOOST undervoltage high |
| LDO1_TSD | LDO1 overtemperature shutdown event |
| LDO1_OC | LDO1 overcurrent |
| LDO2_TSD | LDO2 overtemperature shutdown event |
| LDO2_OC | LDO2 overcurrent |
| WAKE1 | WAKE1 transition |
| WAKE2 | WAKE2 transition |
| COM | I2C communication error |

Table 82. List of interrupts from fail-safe logic

| Interrupt fail-safe | Description |
|---------------------|--------------------------------|
| VCOREMON_OV | VCOREMON overvoltage detected |
| VCOREMON_UV | VCOREMON undervoltage detected |
| VDDIO_OV | VDDIO overvoltage detected |
| VDDIO_UV | VDDIO undervoltage detected |
| VMON1_OV | VMON1 overvoltage detected |
| VMON1_UV | VMON1 undervoltage detected |

27.3 PSYNC for two VR5500

PSYNC function allows to manage complex startup sequence with multiple power management ICs like two VR5500 (OTP_PSYNC_CFG = 0) or one VR5500 plus one PF82 (OTP_PSYNC_CFG = 1). This function is enabled with the OTP_PSYNC_EN bit.

When PSYNC is used to synchronize two VR5500, PSYNC pins of each device shall be connected together and pulled up to VBOS pin of the VR5500 master device as shown in Figure 34. In this configuration, VR5500 #1 state machine stops before VR5500 #1_VPRE starts and waits for VR5500 #2 to synchronize VR5500#2_VPRE start.

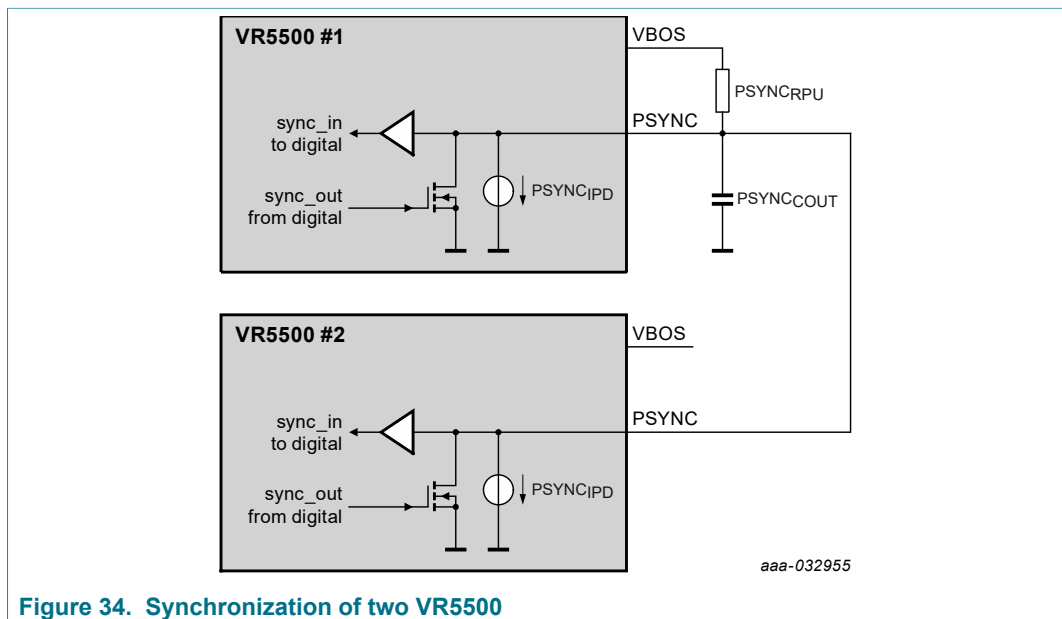
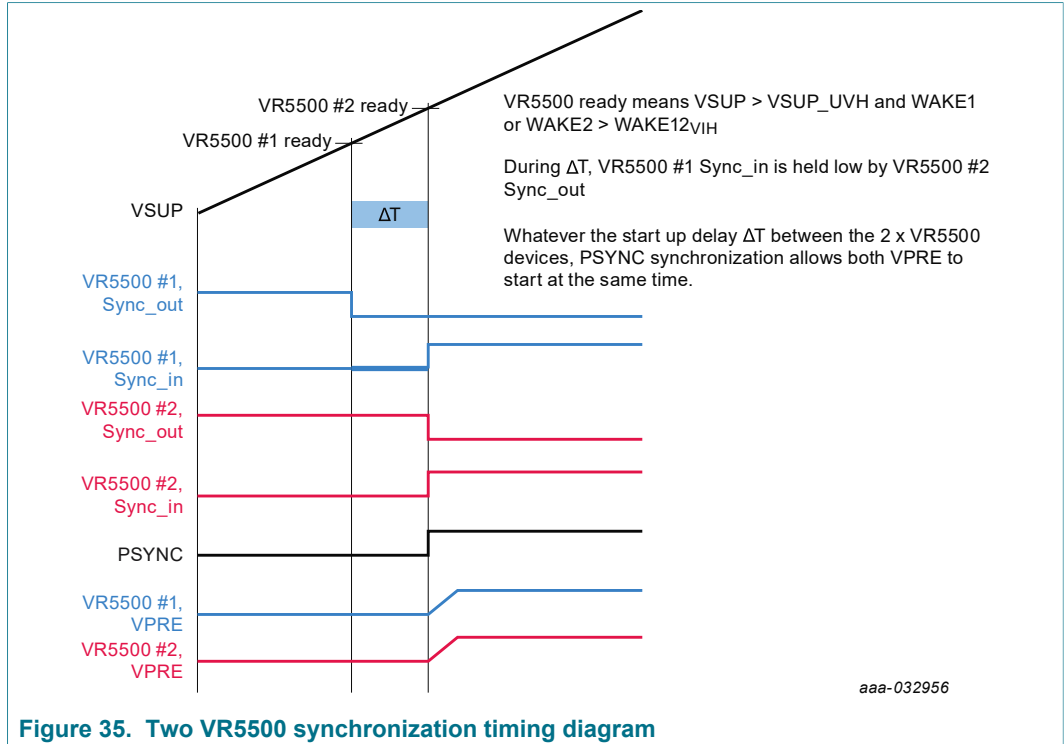


Figure 34. Synchronization of two VR5500

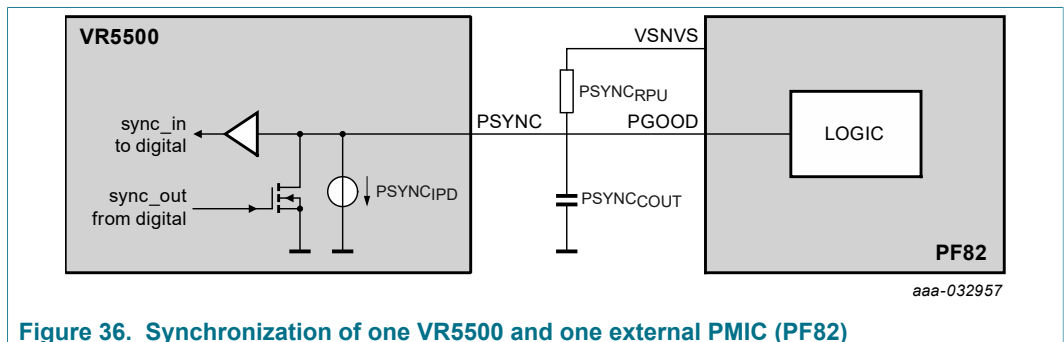


27.4 PSYNC for VR5500 and external PMIC

When PSYNC is used to synchronize one VR5500 and one external PMIC, PSYNC pin of VR5500 is connected to PGOOD pin of the external PMIC.

When the external PMIC is PF82 from NXP, it can be pulled up to VSNVS pin of PF82. In this configuration, VR5500 state machine stops after VPRE starts and waits for the PGOOD pin of the external PMIC to be released to continue its own power sequencing. It allows to synchronize the power up sequence of both devices.

During power-down sequence, VR5500 should wait for the external PMIC power-down sequence completion before turning OFF VPRE (VPRE is powering the external PMIC). OTP_VPRE_off_dly bit is configured to extend VPRE turn OFF delay from 250 μs default value to 32 ms.



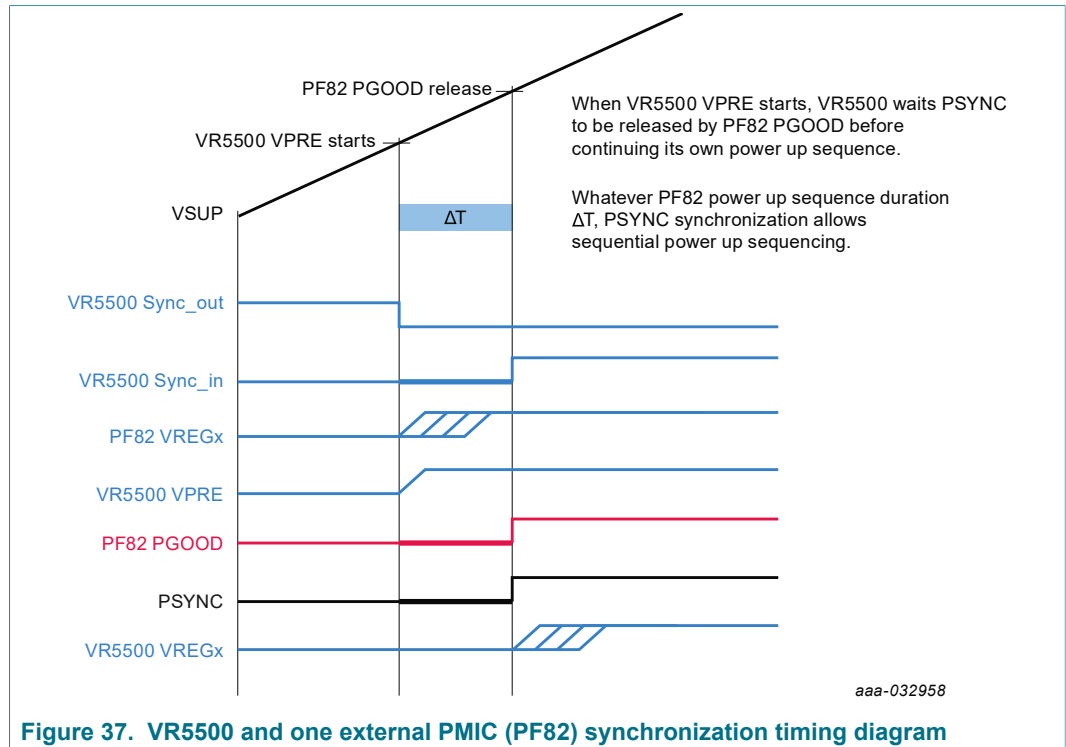


Figure 37. VR5500 and one external PMIC (PF82) synchronization timing diagram

Table 83. PSYNC electrical characteristics

$T_A = -40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$, unless otherwise specified. $VSUP = VSUP_UVH$ to 36 V , unless otherwise specified. All voltages referenced to ground.

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------------------|---|-----|-----|-----|------|
| PSYNC _{VIL} | Low-level input voltage threshold | 1.0 | — | — | V |
| PSYNC _{VIH} | High-level input voltage threshold | — | — | 2.0 | V |
| PSYNC _{HYST} | Hysteresis | 0.1 | — | — | V |
| PSYNC _{VOL} | Low-level output threshold (I = 2.0 mA) | — | — | 0.5 | V |
| PSYNC _{IPD} | Internal pull down current source | 7.0 | 10 | 13 | μA |
| PSYNC _{RPU} | External pull up resistor to VBOS | — | 10 | — | kΩ |
| PSYNC _{COUT} | External decoupling capacitor | — | 0.1 | — | μF |
| PSYNC _{TFB} | Feedback filtering time | 6.0 | 10 | 15 | μs |

28 I2C interface

28.1 I2C interface overview

The VR5500 uses an I2C interface following the high-speed mode definition up to 3.4 Mbit/s. I2C interface protocol requires a device address for addressing the target IC on a multi-device bus. The VR5500 has two device address: one to access the main logic and one to access the fail-safe logic. These two I2C addresses are set by OTP.

The I2C interface is using a dedicated power input pin VDDI2C and it is compatible with 1.8 V / 3.3 V input supply. Timing, diagrams, and further details can be found in the NXP I²C specification UM10204 rev6.

Table 84. I2C message arrangement

| | | | | | | | | | | | | | | | | |
|----------------|---------|---------|---------|---------|---------|--------|------------|------------------|--------|---------|--------|--------|--------|--------|--------|--|
| B39 | B38 | B37 | B36 | B35 | B34 | B33 | B32 | B31 | B30 | B29 | B28 | B27 | B26 | B25 | B24 | |
| ID_6-0 | | | | | | | 0 | 0 | 0 | Adr_5-0 | | | | | | |
| Device address | | | | | | | Read/Write | Register address | | | | | | | | |
| B23 | B22 | B21 | B20 | B19 | B18 | B17 | B16 | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | |
| Data_15 | Data_14 | Data_13 | Data_12 | Data_11 | Data_10 | Data_9 | Data_8 | Data_7 | Data_6 | Data_5 | Data_4 | Data_3 | Data_2 | Data_1 | Data_0 | |
| Data MSB | | | | | | | Data LSB | | | | | | | | | |
| | | | | | | | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | | |
| | | | | | | | CRC_7 | CRC_6 | CRC_5 | CRC_4 | CRC_3 | CRC_2 | CRC_1 | CRC_0 | | |
| | | | | | | | CRC_7 | CRC_6 | CRC_5 | CRC_4 | CRC_3 | CRC_2 | CRC_1 | CRC_0 | | |

28.2 Device address

The VR5500 has two device address: one to access the Main logic and one to access the Fail-safe logic.

| | | | | | | |
|-----|-----|-----|-----|-----|-----|------|
| B39 | B38 | B37 | B36 | B35 | B34 | B33 |
| 0 | 1 | OTP | OTP | OTP | OTP | M/FS |

The I2C addresses have the following arrangement:

- Bit 39: 0
- Bit 38: 1
- Bit 37 to 34: OTP value
- Bit 33: 0 to access the main logic, 1 to access the fail-safe logic

28.3 Cyclic redundant check

An 8 bit CRC is required for each Write and Read I2C command. Computation of a cyclic redundancy check is derived from the mathematics of polynomial division, modulo two.

The CRC polynomial used is $x^8+x^4+x^3+x^2+1$ (identified by 0x1D) with a SEED value of hexadecimal '0xFF'

The following table shows an example of CRC encoding HW implementation:

CRC calculation using XOR:

$$\begin{aligned}
 \text{CRC}_7 &= \text{XOR} (\text{B38, B35, B32, B31, B24, B23, B22, B20, B17, B13, B12, B11, 1, 1, 1}) \\
 \text{CRC}_6 &= \text{XOR} (\text{B37, B34, B23, B22, B21, B19, B16, B12, B11, B10, 1, 1}) \\
 \text{CRC}_5 &= \text{XOR} (\text{B39, B36, B33, B30, B29, B22, B21, B20, B18, B15, B11, B10, B9, 1, 1, 1}) \\
 \text{CRC}_4 &= \text{XOR} (\text{B39, B38, B35, B32, B29, B28, B21, B20, B19, B17, B14, B10, B9, B8, 1, 1, 1, 1}) \\
 \text{CRC}_3 &= \text{XOR} (\text{B37, B35, B34, B32, B28, B27, B24, B23, B22, B19, B18, B17, B16, B12, B11, B9, B8, 1, 1, 1, 1}) \\
 \text{CRC}_2 &= \text{XOR} (\text{B39, B38, B36, B35, B34, B33, B32, B27, B26, B24, B21, B20, B18, B16, B15, B13, B12, B10, B8, 1,1,1,1,1,1,1}) \\
 \text{CRC}_1 &= \text{XOR} (\text{B37, B34, B33, B26, B25, B24, B22, B19, B15, B14, B13, B9, 1, 1, 1}) \\
 \text{CRC}_0 &= \text{XOR} (\text{B39, B36, B33, B32, B25, B24, B23, B21, B18, B14, B13, B12, B8, 1, 1, 1, 1})
 \end{aligned}$$

CRC results examples:

- Main I2C device address: 0x20
- Fail-safe I2C device address: 0x21

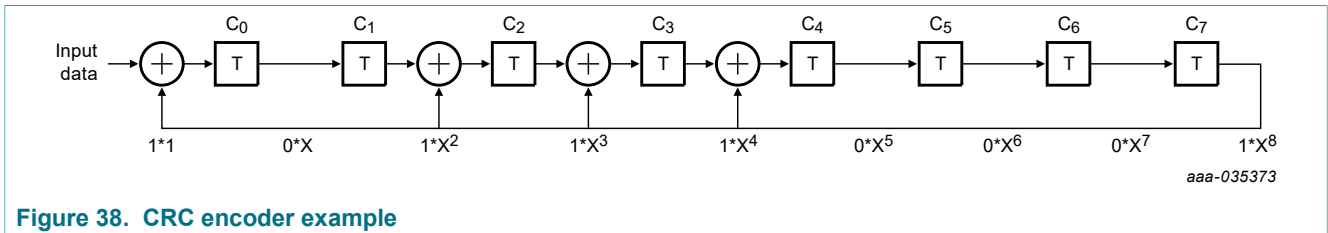


Figure 38. CRC encoder example

Table 85. CRC results example

| Device address, R/W, 8 bit (Hex) | 00, Register address, 8 bit (Hex) | Data MSB, 8 bit (Hex) | Data LSB, 8 bit (Hex) | CRC, 8 bit |
|----------------------------------|-----------------------------------|-----------------------|-----------------------|------------|
| 0x40 | 0x02 | 0x00 | 0x00 | 0x31 |
| 0x42 | 0x01 | 0xD0 | 0x0D | 0x8C |

28.4 I2C electrical characteristics

Table 86. I2C electrical characteristics

$T_A = -40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$, unless otherwise specified. $VSUP = VSUP_UVH$ to 36 V, unless otherwise specified. All voltages referenced to ground.

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------------|--|------------------------|-----|------------------------|------|
| VDDI2C | I2C interface power input | 1.62 | 1.8 | 1.98 | V |
| | | 2.97 | 3.3 | 3.63 | V |
| F_{SCL} | SCL clock frequency | — | — | 3.4 | MHz |
| $I2C_{VIL}$ | SCL, SDA low-level input voltage threshold | $0.3 \times V_{DDI2C}$ | — | — | V |
| $I2C_{VIH}$ | SCL, SDA high-level input voltage threshold | — | — | $0.7 \times V_{DDI2C}$ | V |
| SDA_{VOL} | Low-level output voltage at SDA pin ($I = 20\text{ mA}$) | — | — | 0.4 | V |
| C_{I2C} | Input capacitance at SCL / SDA | — | — | 10 | pF |
| t_{SPSCL} | SCL pulse width filtering time, when 50 ns filter selected (fast speed, fast speed plus) | 50 | — | 150 | ns |
| t_{SPSDA} | SDA pulse width filtering time, when 50 ns filter selected (fast speed, fast speed plus) | 50 | — | 150 | ns |
| t_{SPHSCL} | SCL pulse width filtering time, when 10 ns filter selected (high speed) | 10 | — | 25 | ns |
| t_{SPHSDA} | SDA pulse width filtering time, when 10 ns filter selected (high speed) | 10 | — | 25 | ns |

29 Application information

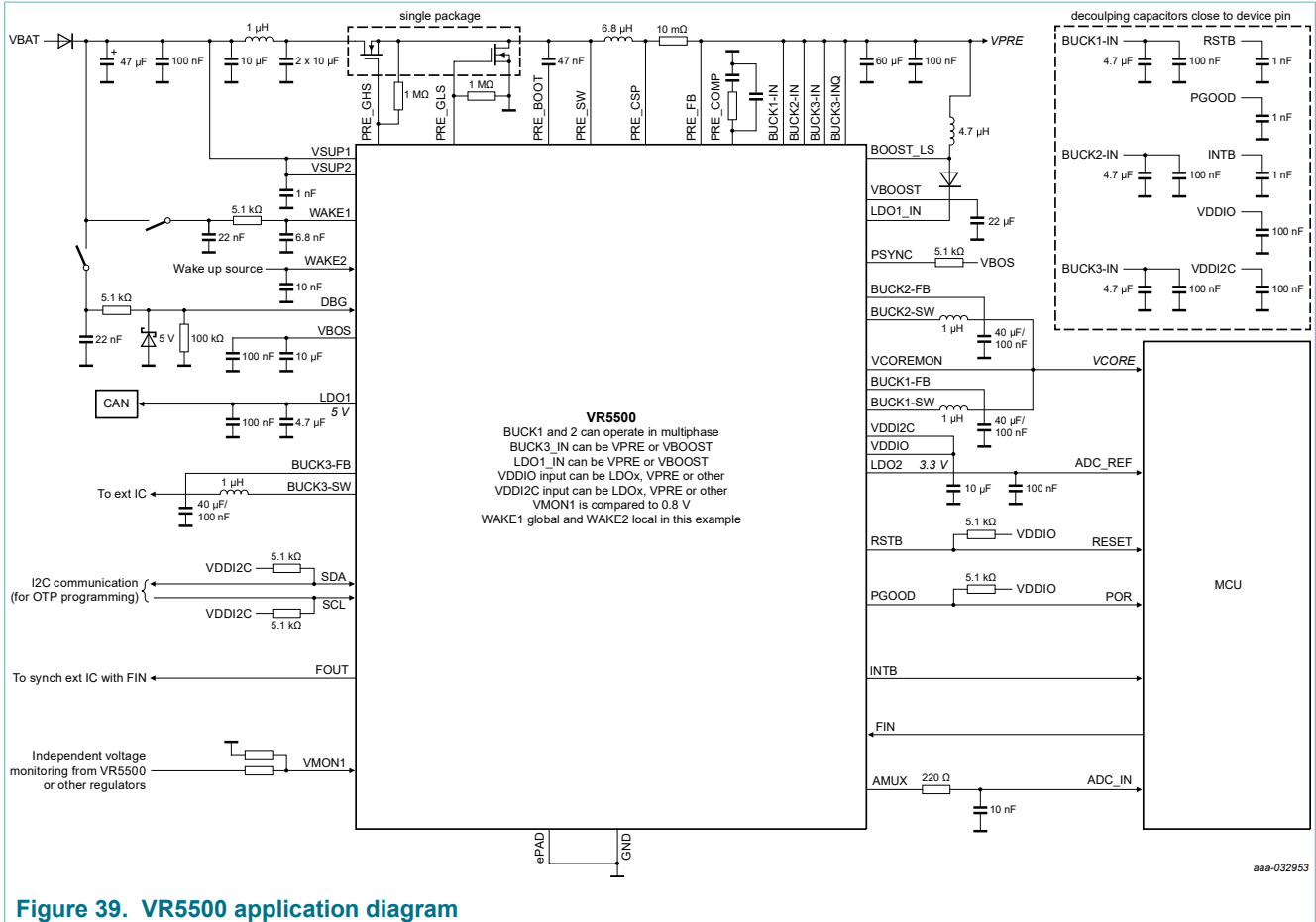


Figure 39. VR5500 application diagram

30 Fail-safe domain description

30.1 Functional description

The fail-safe domain is electrically independent and physically isolated. The fail-safe domain is supplied by its own reference voltages and current, has its own oscillator.

The fail-safe domain and the dedicated pins are represented in [Figure 40](#):

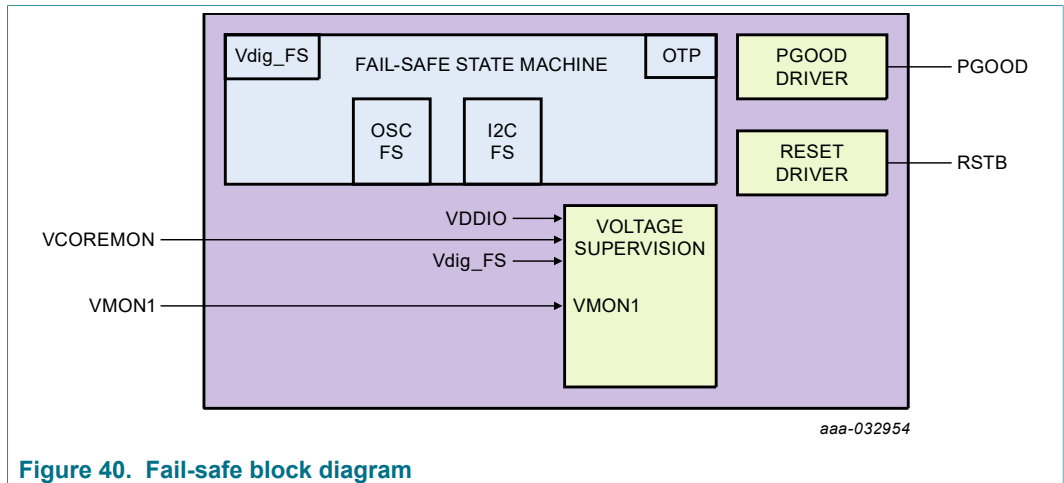


Figure 40. Fail-safe block diagram

30.2 Voltage supervisor

The voltage supervisor is in charge of overvoltage and undervoltage monitoring of VCOREMON, VDDIO and VMON1 input pins. When an overvoltage occurs on a VR5500 regulator monitored by one of these pins, the associated VR5500 regulator is switched off till the fault is removed. The voltage monitoring is active as soon as FS_ENABLE=1 and UV/OV flags are then reported accordingly.

30.2.1 VCOREMON monitoring

VCOREMON input pin is dedicated to BUCK1 or BUCK1 and BUCK2, in case of multiphase operation. When overvoltage or undervoltage fault is detected, the fail-safe reaction on RSTB is configurable with the VCOREMON_OV/UV_FS_IMPACT[1:0] bits during the INIT_FS phase.

Table 87. VCOREMON error impact configuration

| VCOREMON_OV_FS_IMPACT[1:0] | VCOREMON OV impact on RSTB |
|----------------------------|----------------------------|
| 00 | No effect on RSTB |
| 01 | Reserved |
| 1x (default) | RSTB is asserted |
| Reset condition | POR |

| VCOREMON_UV_FS_IMPACT[1:0] | VCOREMON UV impact on RSTB |
|----------------------------|----------------------------|
| 00 | No effect on RSTB |
| 01 (default) | No effect on RSTB |
| 1x | RSTB is asserted |
| Reset condition | POR |

Table 88. VCOREMON electrical characteristics

$T_A = -40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$, unless otherwise specified. $VSUP = VSUP_UVH$ to 36 V , unless otherwise specified. All voltages referenced to ground.

| Symbol | Parameter | Min | Typ | Max | Unit |
|------------------|---|-----|------|-----|---------------|
| VCOREMON_OV_min | Overvoltage threshold minimum | — | +4.5 | — | % |
| VCOREMON_OV_max | Overvoltage threshold maximum | — | +12 | — | % |
| VCOREMON_OV_step | Overvoltage threshold step (OTP_VCOREOVTH[7:0] bits) | — | +0.5 | — | % |
| VCOREMON_OV_acc | Overvoltage threshold accuracy | -2 | — | 2 | % |
| TCOREMON_OV | Overvoltage filtering time (OTP_VCORE_OV_DGLT bit) | 20 | 25 | 30 | μs |
| | | 40 | 45 | 50 | μs |
| VCOREMON_UV_min | Undervoltage threshold minimum | — | -4.5 | — | % |
| VCOREMON_UV_max | Undervoltage threshold maximum | — | -12 | — | % |
| VCOREMON_UV_step | Undervoltage threshold step (OTP_VCOREUVTH[7:0] bits) | — | -0.5 | — | % |
| VCOREMON_UV_acc | Undervoltage threshold accuracy | -2 | — | 2 | % |
| TCOREMON_UV | Undervoltage filtering time (OTP_VCORE_UV_DGLT[1:0] bits) | 2.5 | 5 | 7.5 | μs |
| | | 10 | 15 | 20 | μs |
| | | 20 | 25 | 30 | μs |
| | | 35 | 40 | 45 | μs |

30.2.2 Static voltage scaling (SVS)

A static voltage scaling function is implemented to allow the MCU to reduce the output voltage initially configured at start-up of BUCK1 (and BUCK2 if used in multiphase). The SVS configuration must be done in INIT_FS phase. The offset value is configurable by I2C with the SVS_OFFSET[4:0] bits and the exact complemented value shall be written in the NOT_SVS_OFFSET[4:0] bits.

Table 89. SVS offset configuration

| SVS_OFFSET[4:0] | NOT_SVS_OFFSET[4:0] | Offset applied to BUCK1 (and BUCK2 if used in multiphase) |
|-------------------------|---------------------|---|
| 0 0000 (default) | 1 1111 | 0 mV |
| 0 0001 | 1 1110 | -6.25 mV |
| ... | ... | -6.25 mV step per bit |
| 1 0000 | 0 1111 | -100 mV |
| Reset condition | POR | |

The BUCK1/2 output voltage transition starts when the NOT_SVS_OFFSET[4:0] I2C command is received and confirmed good. If the NOT_SVS_OFFSET[4:0] I2C command is not the exact opposite to the SVS_OFFSET[4:0] I2C command, the SVS procedure is not executed and the BUCK1 output voltage remains at its original value. The OV/UV threshold changes immediately when the NOT_SVS_OFFSET[4:0] I2C command is received and confirmed good. Therefore, the BUCK1 output voltage transition is done within TCOREMON_OV.

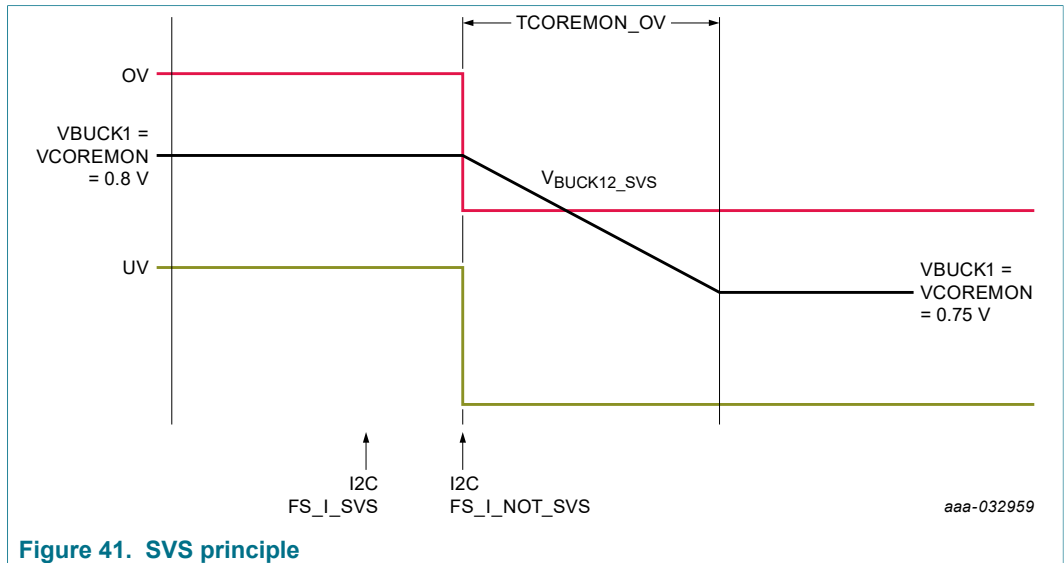


Figure 41. SVS principle

30.2.3 VDDIO monitoring

VDDIO input pin can be connected to VPRE, LDO1, LDO2, BUCK3, or an external regulator. The regulator connected to VDDIO must be at 3.3 V or 5.0 V to be compatible with overvoltage and undervoltage monitoring thresholds. In order to turn OFF the regulator in case of overvoltage detection, the configuration of which regulator is connected to VDDIO is done with OTP_VDDIO_REG_ASSIGN[2:0] bits. If an external regulator (not delivered by the VR5500) is connected to VDDIO, this regulator cannot be turned OFF, but the overvoltage flag is reported to the MCU which can take appropriate action. In all cases, the reaction on RSTB is configured with VDDIO_OV/UV_FS_IMPACT[1:0] bits.

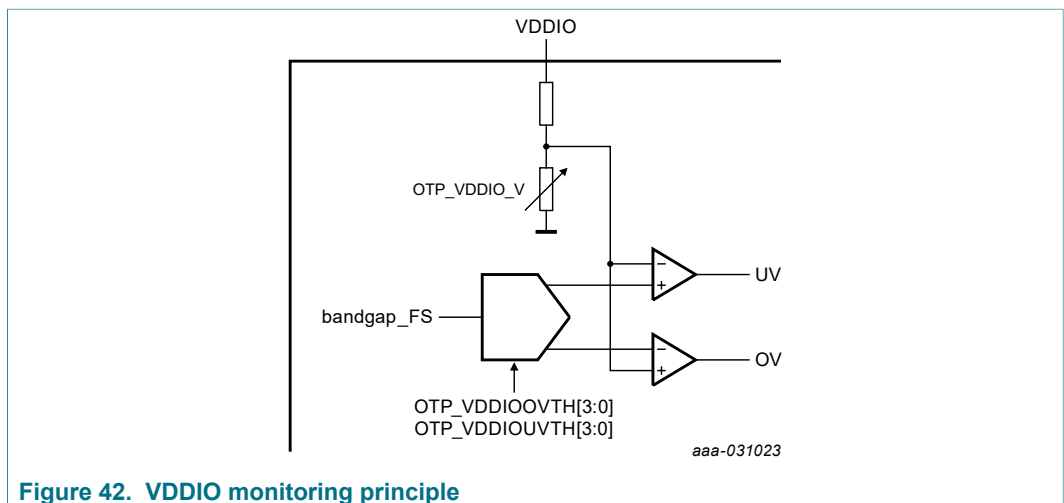


Figure 42. VDDIO monitoring principle

When overvoltage or undervoltage fault is detected, the fail-safe reaction on RSTB is configurable with the VDDIO_OV/UV_IMPACT[1:0] bits during the INIT_FS phase.

Table 90. VDDIO error impact configuration

| VDDIO_OV_FS_IMPACT[1:0] | VDDIO OV impact on RSTB |
|-------------------------|-------------------------|
| 00 | No effect on RSTB |
| 01 | Reserved |
| 1x (default) | RSTB is asserted |
| Reset condition | POR |

| VDDIO_UV_FS_IMPACT[1:0] | VDDIO UV impact on RSTB |
|-------------------------|-------------------------|
| 00 | No effect on RSTB |
| 01 (default) | No effect on RSTB |
| 1x | RSTB is asserted |
| Reset condition | POR |

Table 91. VDDIO electrical characteristics

$T_A = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$, unless otherwise specified. $VSUP = VSUP_UVH$ to 36 V, unless otherwise specified. All voltages referenced to ground.

| Symbol | Parameter | Min | Typ | Max | Unit |
|---------------|---|-----|------|-----|---------------|
| VDDIO_OV_min | Overvoltage threshold minimum | — | +4.5 | — | % |
| VDDIO_OV_max | Overvoltage threshold maximum | — | +12 | — | % |
| VDDIO_OV_step | Overvoltage threshold step (OTP_VDDIOOVTH[7:0] bits) | — | +0.5 | — | % |
| VDDIO_OV_acc | Overvoltage threshold accuracy | -2 | — | 2 | % |
| TVDDIO_OV | Overvoltage filtering time (OTP_VDDIO_OV_DGLT bit) | 20 | 25 | 30 | μs |
| | | 40 | 45 | 50 | μs |
| VDDIO_UV_min | Undervoltage threshold minimum | — | -4.5 | — | % |
| VDDIO_UV_max | Undervoltage threshold maximum | — | -12 | — | % |
| VDDIO_UV_step | Undervoltage threshold step (OTP_VDDIOUVTH[7:0] bits) | — | -0.5 | — | % |
| VDDIO_UV_acc | Undervoltage threshold accuracy | -2 | — | 2 | % |
| TVDDIO_UV | Undervoltage filtering time (OTP_VDDIO_UV_DGLT[1:0] bits) | 2.5 | 5 | 7.5 | μs |
| | | 10 | 15 | 20 | μs |
| | | 20 | 25 | 30 | μs |
| | | 35 | 40 | 45 | μs |

30.2.4 VMON1 monitoring

Each VMON1 monitoring feature is enabled by OTP. VMON1 input pin can be connected to VPRE, LDO1, LDO2, BUCK3, BUCK2 (in case BUCK2 is not used in multiphase), or even an external regulator. In order to turn OFF the regulator in case of Overvoltage detection, the configuration of which regulator is connected to VMON1 is done by I2C in the register M_VMON_REGx. If an external regulator (not delivered by the VR5500) is connected to VMON1, this regulator cannot be turned OFF, but the Overvoltage flag is reported to the MCU which can take appropriate action. In all cases, the fail-safe reaction on RSTB is configured with VMON1_OV/UV_FS_IMPACT[1:0] bits.

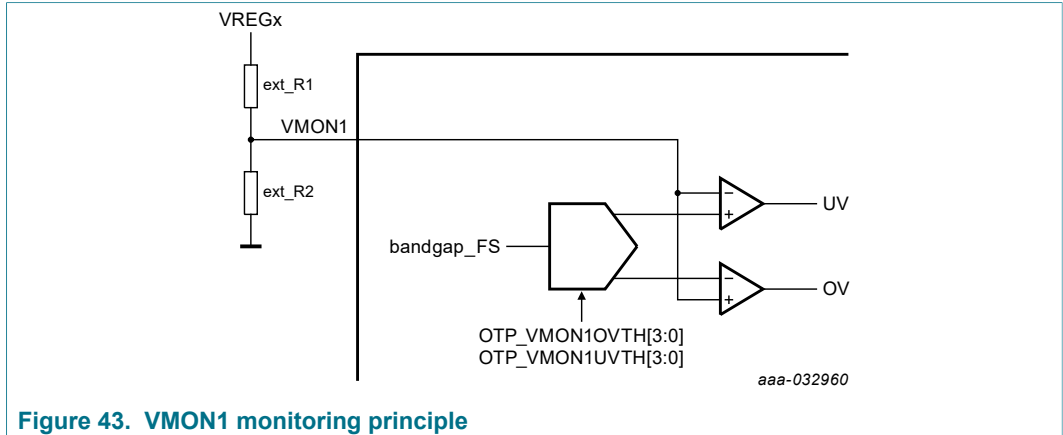


Figure 43. VMON1 monitoring principle

The external resistor bridge connected to VMON1 shall be calculated to deliver a middle point of 0.8 V. It is recommended to use ±1 % or less resistor accuracy. When overvoltage or undervoltage fault is detected, the fail-safe reaction on RSTB is configurable with the VMON1_OV/UV_FS_IMPACT[1:0] bits during the INIT_FS phase.

Table 92. VMON1 error impact configuration

| VMON1_OV_FS_IMPACT[1:0] | VMON1 OV impact on RSTB |
|-------------------------|-------------------------|
| 00 | No effect on RSTB |
| 01 | Reserved |
| 1x (default) | RSTB is asserted |
| Reset condition | POR |

| VMON1_UV_FS_IMPACT[1:0] | VMON1 UV impact on RSTB |
|-------------------------|-------------------------|
| 00 | No effect on RSTB |
| 01 (default) | No effect on RSTB |
| 1x | RSTB is asserted |
| Reset condition | POR |

Table 93. VMON1 (without ext resistor accuracy) electrical characteristics

T_A = -40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

| Symbol | Parameter | Min | Typ | Max | Unit |
|---------------|--|-----|------|-----|------|
| VMON1_OV_min | Overvoltage threshold minimum | — | +4.5 | — | % |
| VMON1_OV_max | Overvoltage threshold maximum | — | +12 | — | % |
| VMON1_OV_step | Overvoltage threshold step (OTP_VMON1OVTH[7:0] bits) | — | +0.5 | — | % |
| VMON1_OV_acc | Overvoltage threshold accuracy | -2 | — | 2 | % |
| TMON1_OV | Overvoltage filtering time (OTP_VMON1_OV_DGLT bit) | 20 | 25 | 30 | μs |
| | | 40 | 45 | 50 | μs |
| VMON1_UV_min | Undervoltage threshold minimum | — | -4.5 | — | % |
| VMON1_UV_max | Undervoltage threshold maximum | — | -12 | — | % |

| Symbol | Parameter | Min | Typ | Max | Unit |
|---------------|---|-----|------|-----|------|
| VMON1_UV_step | Undervoltage threshold step (OTP_VMON1UVTH[7:0] bits) | — | -0.5 | — | % |
| VMON1_UV_acc | Undervoltage threshold accuracy | -2 | — | 2 | % |
| TMON1_UV | Undervoltage filtering time (OTP_VMON1_UV_DGLT[1:0] bits) | 2.5 | 5 | 7.5 | μs |
| | | 10 | 15 | 20 | μs |
| | | 20 | 25 | 30 | μs |
| | | 35 | 40 | 45 | μs |
| VMON1_PD | Internal passive pull down | 1 | 2 | 4 | MΩ |

30.3 Fault management

30.3.1 Fault source and reaction

In normal operation when RSTB is released, the fault error counter is incremented when a fault is detected by the VR5500 fail-safe state machine. [Table 94](#) lists the faults and their impact on PGOOD and RSTB pins according to the device configuration. The faults that are configured to not assert RSTB will not increment the fault error counter. In that case, only the flags are available for MCU diagnostic.

Table 94. Application related fail-safe fault list and reaction

In Orange, the reaction is not configurable.

In Green, the reaction is configurable by OTP for PGOOD and I2C for RSTB during INIT_FS.

| Application-related fail-safe faults | FLT_ERR_CNT increment | RSTB assertion | PGOOD assertion |
|---------------------------------------|-----------------------|--------------------------|-----------------|
| VCOREMON_OV | +1 | VCOREMON_OV_FS_IMPACT[1] | OTP config |
| VDDIO_OV | +1 | VDDIO_OV_FS_IMPACT[1] | OTP config |
| VMON1_OV | +1 | VMON1_OV_FS_IMPACT[1] | OTP config |
| VCOREMON_UV | +1 | VCOREMON_UV_FS_IMPACT[1] | OTP config |
| VDDIO_UV | +1 | VDDIO_UV_FS_IMPACT[1] | OTP config |
| VMON1_UV | +1 | VMON1_UV_FS_IMPACT[1] | OTP config |
| External RESET (out of extended RSTB) | +1 | Yes (low externally) | No |
| RSTB pulse request by MCU | No | Yes | No |
| RSTB short to high | +1 | No (high externally) | No |
| REG_CORRUPT = 1 | +1 | No | No |
| OTP_CORRUPT = 1 | +1 | No | No |

If OTP_PGOOD_RSTB = '0' (default configuration), RSTB and PGOOD pins work independently according to [Table 94](#). If OTP_PGOOD_RSTB = '1', RSTB and PGOOD pins work concurrently and all the faults asserting RSTB will also assert PGOOD.

30.3.2 Fault error counter

The VR5500 integrates a configurable fault error counter which is counting the number of faults related to the device itself and also caused by external events. The fault error counter starts at level '1' after a POR or resuming from Standby. The final value of the fault error counter is used to transition in DEEP-FS mode. The maximum value of this

counter is configurable with the FLT_ERR_CNT_LIMIT[1:0] bits during the INIT_FS phase.

Table 95. Fault error counter configuration

| FLT_ERR_CNT_LIMIT[1:0] | Fault error counter max value configuration |
|------------------------|---|
| 00 | 2 |
| 01 (default) | 6 |
| 10 | 8 |
| 11 | 12 |
| Reset condition | POR |

30.4 PGOOD, RSTB

These two output pins have a hierarchical implementation in order to guarantee the safe state.

- PGOOD has the priority one. If PGOOD is asserted, RSTB is asserted.
- RSTB has the priority two. If RSTB is asserted, PGOOD may not be asserted.

30.4.1 PGOOD

PGOOD is an open-drain output that can be connected in the application to the PORB of the MCU. PGOOD requires an external pull-up resistor to VDDIO and a filtering capacitor to GND for immunity. An internal pull-down RPD ensures PGOOD low-level in Standby and Power down mode. VCOREMON, VDDIO, VMON1 can be assigned to PGOOD by OTP.

PGOOD is asserted low by the FS_LOGIC when any of the assigned regulators are in undervoltage or overvoltage. When PGOOD is asserted low, RSTB is also asserted low. An internal pull-up on the gate of the low-side MOS ensures PGOOD low-level in case of FS_LOGIC failure.

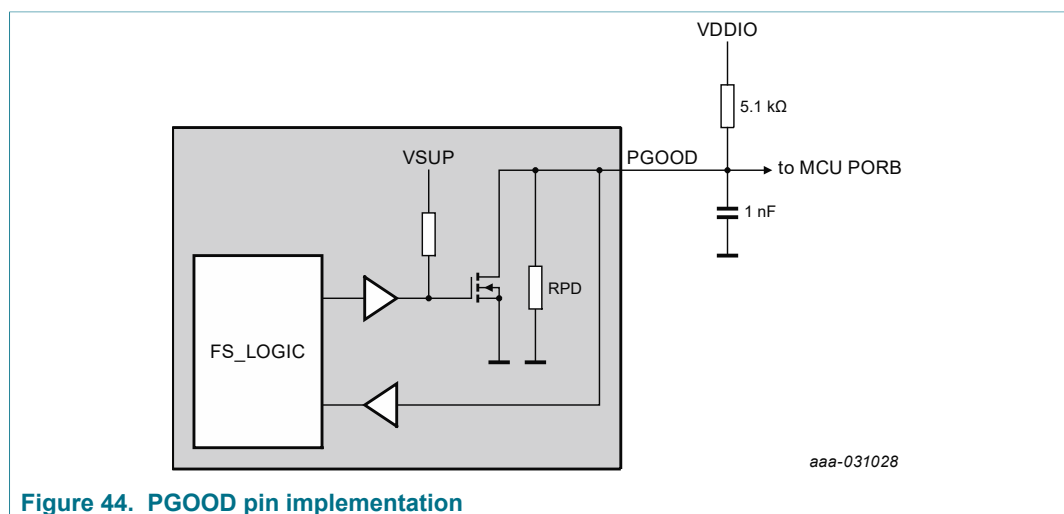


Figure 44. PGOOD pin implementation

Table 96. PGOOD electrical characteristics

$T_A = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$, unless otherwise specified. $VSUP = VSUP_UVH$ to 36 V, unless otherwise specified. All voltages referenced to ground.

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------------------|---------------------------------------|-----|-----|-----|------|
| PGOOD _{VIL} | Low-level input voltage threshold | 1.0 | — | — | V |
| PGOOD _{VIH} | High-level input voltage threshold | — | — | 2.0 | V |
| PGOOD _{HYST} | Input voltage hysteresis | 100 | — | — | mV |
| PGOOD _{VOL} | Low-level output voltage (I = 2.0 mA) | — | — | 0.5 | V |
| PGOOD _{RPD} | Internal pull-down resistor | 200 | 400 | 800 | kΩ |
| PGOOD _{ILIM} | Current limitation | 4.0 | — | 20 | mA |
| PGOOD _{TFB} | Feedback filtering time | 8.0 | — | 15 | μs |

30.4.2 RSTB

RSTB is an open-drain output that can be connected in the application to the RESET of the MCU. RSTB requires an external pull-up resistor to VDDIO and a filtering capacitor to GND for immunity. An internal pull-down RPD ensures RSTB low level in Standby and Power down mode. RSTB assertion depends on the device configuration during INIT_FS phase. An internal pull up on the gate of the low-side MOS ensures RSTB low level in case of FS_LOGIC failure. When RSTB is stuck low for more than RSTB_{T8S}, the device transitions in DEEP-FS mode.

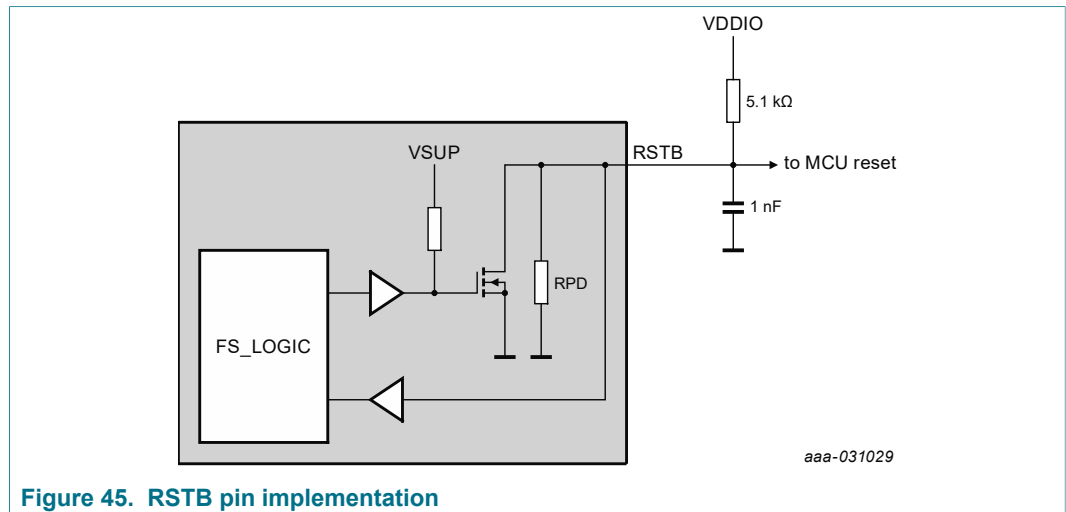


Figure 45. RSTB pin implementation

Table 97. RSTB electrical characteristics

$T_A = -40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$, unless otherwise specified. $VSUP = VSUP_UVH$ to 36 V, unless otherwise specified. All voltages referenced to ground.

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------------------------|--|-----|-----|-----|------|
| RSTB _{VIL} | Low-level input voltage threshold | 1.0 | — | — | V |
| RSTB _{VIH} | High-level input voltage threshold | — | — | 2.0 | V |
| RSTB _{HYST} | Input voltage hysteresis | 100 | — | — | mV |
| RSTB _{VOL} | Low-level output voltage (I = 2.0 mA) | — | — | 0.5 | V |
| RSTB _{RPB} | Internal pull-down resistor | 200 | 400 | 800 | kΩ |
| RSTB _{ILIM} | Current limitation | 4.0 | — | 20 | mA |
| RSTB _{TFB} | Feedback filtering time | 8.0 | — | 15 | μs |
| RSTB _{TSC} | Short to high filtering time | 500 | — | 800 | us |
| RSTB _{TLG} | Long pulse (configurable with RSTB_DUR bit) | 9.0 | — | 11 | ms |
| RSTB _{TST} | Short pulse (configurable with RSTB_DUR bit) | 0.9 | — | 1.1 | ms |
| RSTB _{T8S} | 8 second timer | 7.0 | 8.0 | 9.0 | s |
| RSTB _{TRELEASE} | Time to release RSTB from wake-up or POR with all regulators started in Slot 0 | — | 8.0 | — | ms |

31 Package information

VR5500 package is a QFN (sawn), thermally enhanced wettable flanks, 8 x 8 x 0.85 mm, 0.5 mm pitch, 56 pins. The assembly can be done at two different NXP assembly sites with slight wettable flank difference but sharing the same PCB footprint.

32 Package outline

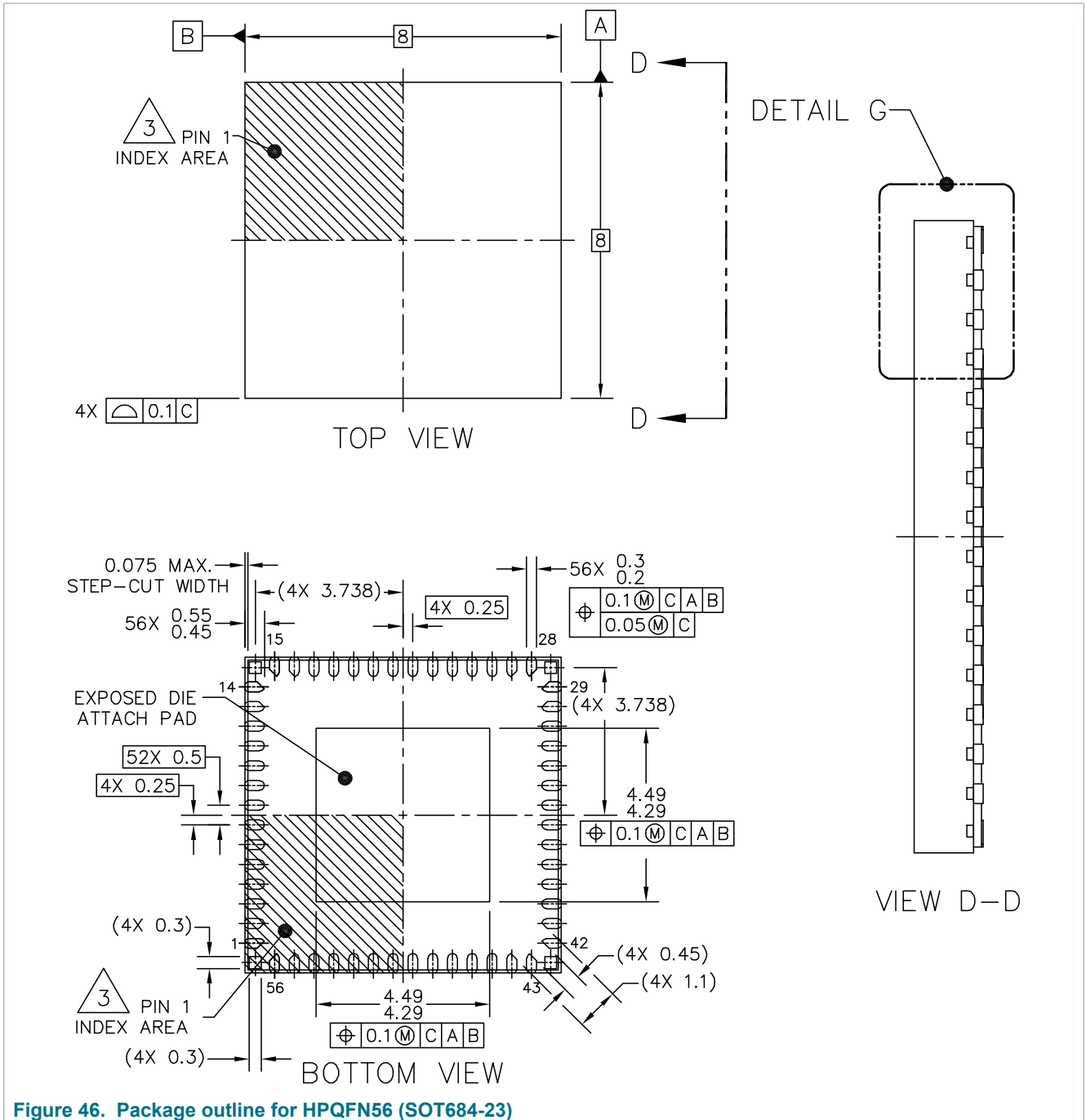


Figure 46. Package outline for HPQFN56 (SOT684-23)

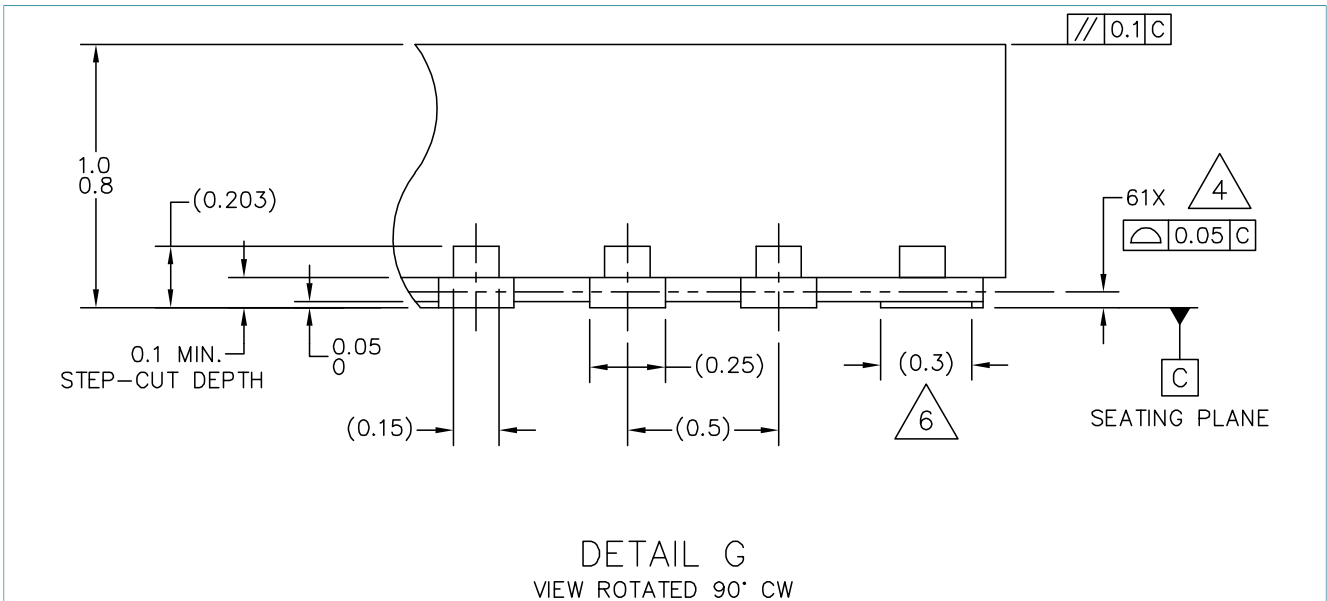


Figure 47. Package outline detail for HPQFN56 (SOT684-23)

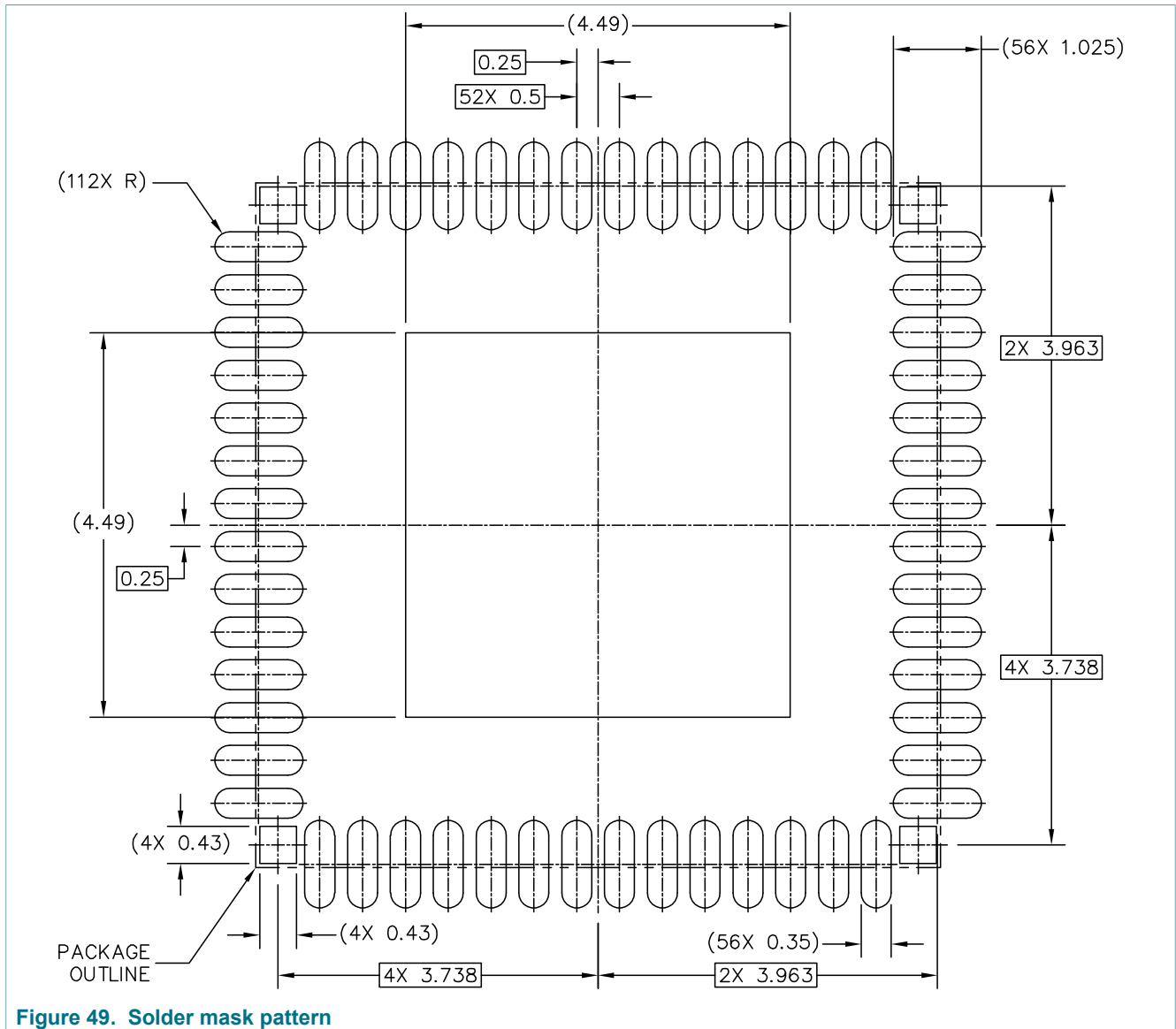
NOTES:

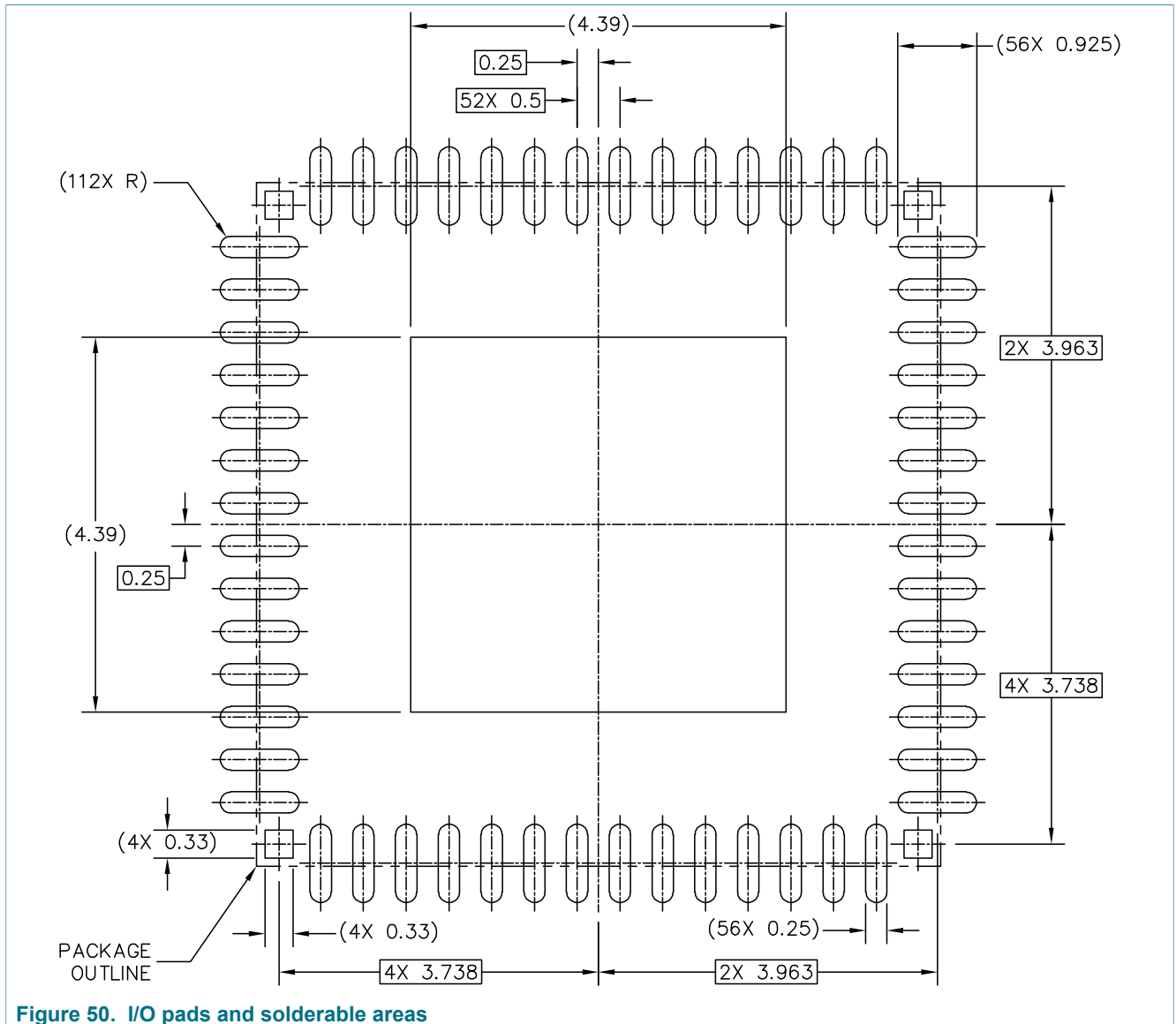
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS, DIE ATTACH FLAG AND CORNER NON-FUNCTIONAL PADS.
5. MIN. METAL GAP SHOULD BE 0.25 MM.
6. ANCHORING PADS.

Figure 48. Package outline notes for HPQFN56 (SOT684-23)

33 Layout and PCB guidelines

33.1 Landing pad information





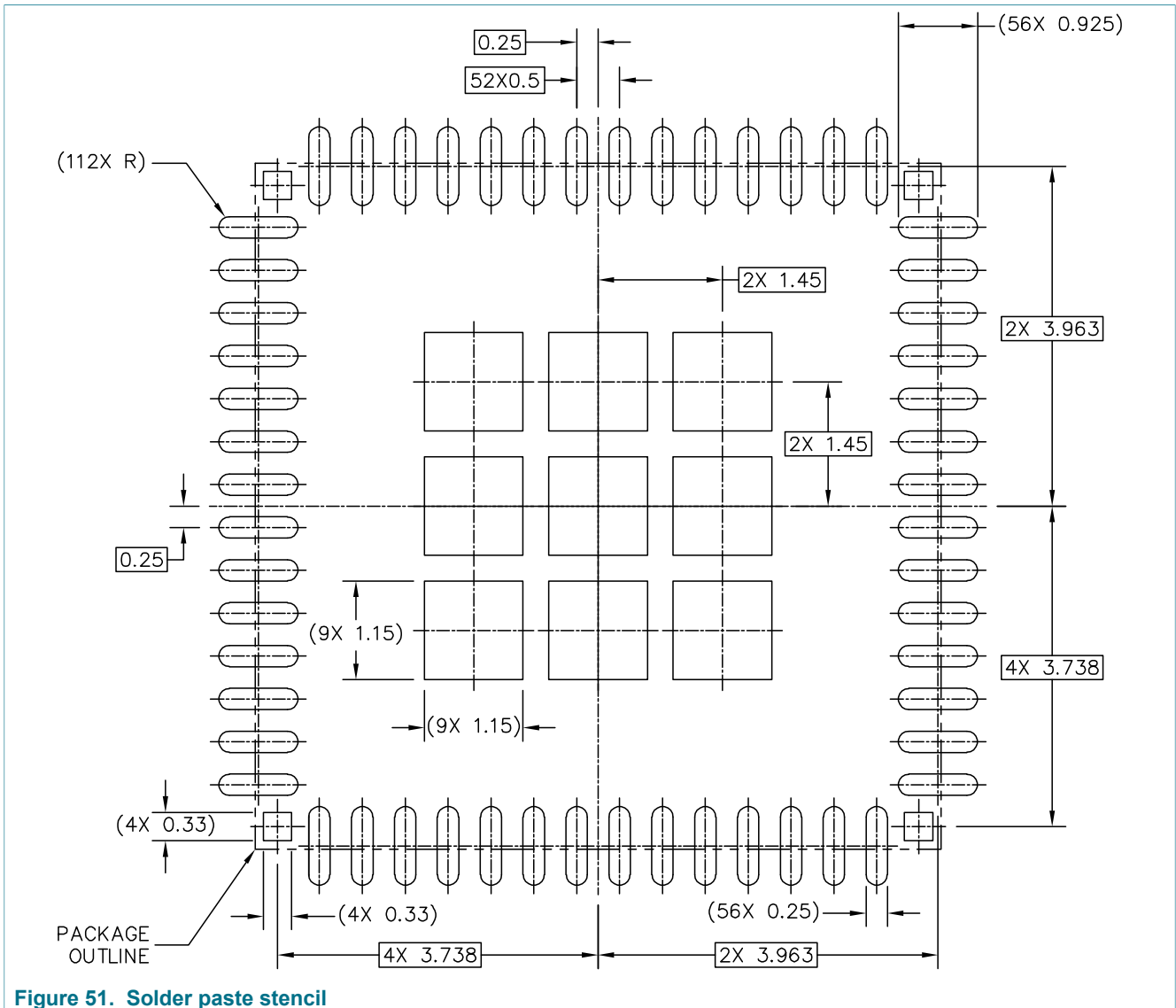


Figure 51. Solder paste stencil

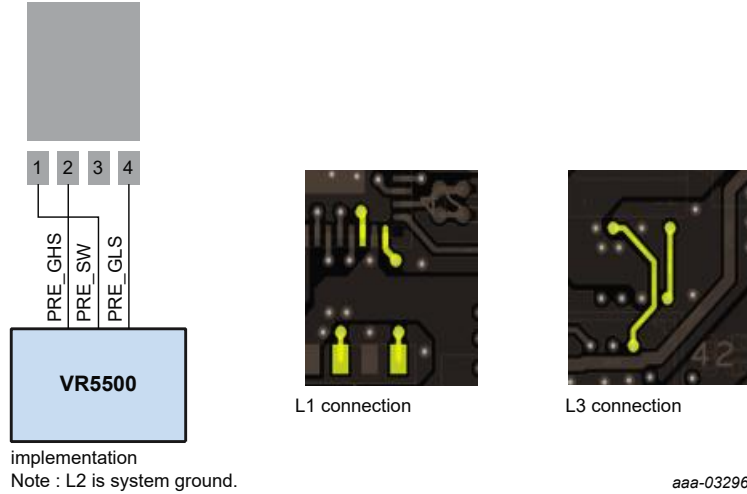
33.2 Component selection

- SMPS input and output capacitors shall be chosen with low ESR (ceramic or MLCC type of capacitors). X7R ceramic type is preferred. Input decoupling capacitors shall be placed as close as possible to the device pin. Output capacitor voltage rating shall be selected to be 3x the voltage output value to minimize the DC bias degradation.
- SMPS inductors shall be shielded with ISAT higher than maximum inductor peak current.

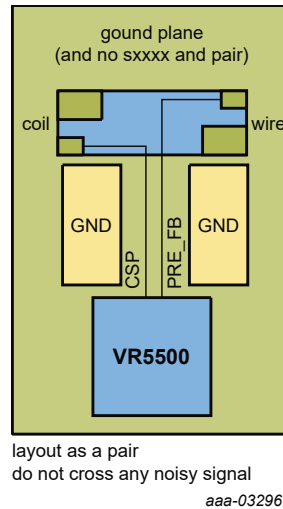
33.3 VPRE

- Inductor charging and discharging current loop is designed as small as possible.
- Input decoupling capacitors are placed close to the high-side drain transistor pin.
- The boot strap capacitor is placed close to the device pin using wide and short track to connect to the external low-side drain transistor.

- PRE_GLS, PRE_GHS and PRE_SW tracks is wide and short and should not cross any sensitive signal (current sensing, for example).



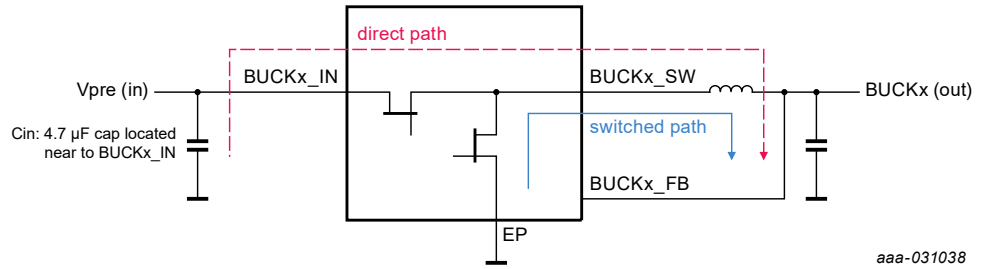
- PRE_FB used as voltage feedback and current sense shall be connected to R_{SHUNT} and routed as a pair with CSP.



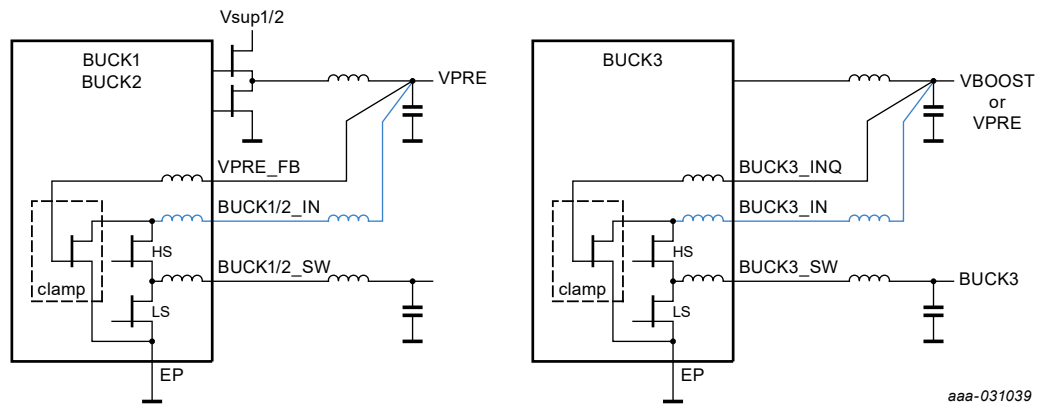
- The external transistor thermal shape should be in the range of 25 x 25 mm for optimum R_{th}.
- The LFPK56 application note can give better insight: <http://assets.nexperia.com/documents/application-note/AN10874.pdf>

33.4 VBUCKx

- Inductor charging and discharging current loop is designed as small as possible.



- Input decoupling capacitors is placed close to BUCKx_IN pins.
- BUCK3_FB and BUCK3_INQ pins shall be tied to the same capacitor, VPRE, or VBOOST output capacitor depending on BUCK3_IN supply selected (in the blue path below, the coil is parasitic from track on the PCB). In the package, the coil is parasitic from the bonding.



34 EMC compliance

The VR5500 EMC performance is verified against BISS generic IC EMC test specification version 2.0 from 07.2012 and FMC1278 electromagnetic compatibility specification for electrical/electronic components and subsystems from 2016 with the following specific conditions:

- Conducted emission: IEC 61967-4
 - Global pins: VBAT (Vsup1 and Vsup2), WAKE1/2, 150 Ohm method, 12-M level
 - Local pins: VPFE, BUCK1/2/3, LDO1/2, VBOOST, 150 Ohm method, 10-K level
- Conducted immunity: IEC 62132-4
 - Global pins: VBAT (Vsup1 and Vsup2), 36 dBm, Class A (no state change on RSTB, PGOOD, and all regulators in spec)
 - Global pins: WAKE1, WAKE2, 30 dBm, Class A (no state change on RSTB, PGOOD, and all regulators in spec)
 - Local pins: RSTB, PGOOD, VDDIO, VDDI2C, VBOS, 12 dBm, Class A (no state change on RSTB, PGOOD, and all regulators in spec)
 - Supply pins: VPFE, BUCK1/2/3, LDO1/2, 12 dBm, Class A (no state change on RSTB, PGOOD, and all regulators in spec)
- Radiated emission: FMC1278 from July 2015
 - Compliance with FMC1278 RE310 Level 2 requirement in Normal mode

- Radiated immunity: FMC1278 from July 2015
 - Injection level per FMC1278 RI112 Level 2 requirement in Normal mode,
 - Injection level per FMC1278 RI112 Level 2 requirement in Normal mode,
 - No wake up when injecting FMC1278 RI112 Level 2 requirement in Standby mode

Table 98. Regulators setup for the EMC tests

| | | |
|-------|---------------------|----------|
| VPRE | Output voltage | 3.3 V |
| | Switching frequency | 455 kHz |
| | Output current | 3 A |
| BUCK1 | Output voltage | 1.25 V |
| | Switching frequency | 2.22 MHz |
| | Output current | 1.2 A |
| BUCK2 | Output voltage | 0.8 V |
| | Switching frequency | 2.22 MHz |
| | Output current | 1.2 A |
| BUCK3 | Output voltage | 2.3 V |
| | Switching frequency | 2.22 MHz |
| | Output current | 1.2 A |
| BOOST | Output voltage | 5 V |
| | Switching frequency | 2.22 MHz |
| | Output current | 275 mA |
| LDO1 | Output voltage | 2.5 V |
| | Output current | 75 mA |
| LDO2 | Output voltage | 1.1 V |
| | Output current | 200 mA |

35 References

- [1] **VR5500_PDTCALC**^[1] — VPRE compensation network calculation and power dissipation tool (Excel file)
- [2] **VR5500_OTP_Mapping**^[1] — OTP programming configuration (Excel file)
- [3] **VR5500_VPRE_Simplis_Model**^[1] — Simplis model for stability and transient simulations
- [4] **Schematic**^[1] — Reference schematic in Cadence and PDF formats
- [5] **Layout**^[1] — Reference layout in Cadence format
- [6] **EVB**^[1] — Evaluation board (EVB)
- [7] **FlexGUI**^[1] — Graphical user interface to be used with the EVB

[1] Contact NXP sales representative.

36 Revision history

Table 99. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---------------|---|------------------------|---------------|--------------|
| VR5500 v.6.0 | 20200129 | Product data sheet | 201912015I | VR5500 v.5.0 |
| Modifications | <ul style="list-style-type: none"> Global: deleted "SPI" references Section 15: corrected typo (deleted R/W SPI column) | | | |
| VR5500 v.5.0 | 20191218 | Product data sheet | 201912015I | VR5500 v.4.0 |
| Modifications | <ul style="list-style-type: none"> Global: changed document status from "Preliminary" to "Product" | | | |
| VR5500 v.4.0 | 20191216 | Preliminary data sheet | 201912015I | VR5500 v.3.0 |
| Modifications | <ul style="list-style-type: none"> Global: multiple formatting and wording updates Table 1: added OTP ID Table 2: updated ground pin description Table 4: added values for BUCKx_SW and updated min value for DC voltage (replaced -1.0 by -0.3) Table 5: updated T_A and T_J description (added "Grade1") Table 7: updated T_{DBG} values and unit Table 8, Table 12: replaced "GOTOSTBY" by "GoToSTBY" Table 19: updated description for RATIO Table 26: updated reset value for Bit 22 and Bit 23 (replaced 0 by 1) Table 54: updated reset value for Bit 17 and Bit 22 (replaced 0 by 1) Table 64: updated OTP_CFG_BUCK1_2 and OTP_CFG_BUCK2_2 register description (replaced 2.6 A by Reserved) Table 65: updated OTP_CFG_UVOV_3 register description Table 66, Table 67, Table 70, Table 76, Table 72, Table 71: updated parameters Figure 8: replaced "WAKE1" by "WAKE1/2" Section 10: updated description for charged device model Section 11: updated assumptions and description (replaced "V_{FPRE_SW}" by "F_{PRE_SW}") Section 20.5: updated description and values in Table 68 Section 20.6: updated Figure 14 Section 22.6: updated Figure 22 Section 23.5: updated Figure 26 Section 25.1: replaced "VPRE switching frequency is coming from CLK2 (455 kHz)" by "VPRE switching frequency is coming from CLK2 (455 kHz) or CLK1 (2.22 MHz)" Section 27.4: updated figure title and description Section 28.3: enhanced description (added Figure 38 and Table 85) Section 30.4.1, Section 30.4.2: updated current limiting parameters Section 33.3, Section 33.4: updated description | | | |
| VR5500 v.3.0 | 20190522 | Preliminary data sheet | - | VR5500 v.2.0 |
| Modifications | <ul style="list-style-type: none"> Global: deleted safety references throughout the document Section 30: updated section title (replaced "Functional safety" by "Fail-safe domain description") | | | |
| VR5500 v.2.0 | 20190415 | Preliminary data sheet | - | VR5500 v.1.0 |
| Modifications | <ul style="list-style-type: none"> Global: changed document status from Objective to Preliminary Table 1: replaced MC by PC Table 4: added parameters for BUCKx_IN Section 10: updated description Section 11: updated Figure 4, assumptions, and description Section 15: renamed column R/W to R/W SPI and added a column R/W I2C Table 64: replaced CLK_DIV1 by 2.22 MHz Table 64: updated the value and description for OTP_CFG_CLOCK_4 register bit 3 (replaced 0 by 1 and 2.22 MHz by 455 kHz) Section 20.1: replaced "$V_{SUP} = V_{PRE} / (T_{PRE_ON_MIN} \times V_{PRE_SW})$" by "$V_{SUP} = L_{PI_DCR} \times I_{PRE} + V_{PRE_UVL} / D_{MAX}$ with $D_{MAX} = 1 - (V_{PRE_SW} \times T_{PRE_OFF_MIN})$" Figure 14: deleted 2.22 MHz curves | | | |
| VR5500 v.1.0 | 20190221 | Objective data sheet | - | - |

37 Legal information

37.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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