42V Quad, Gangable, Synchronous, Monolithic Step-Down Regulator

FEATURES

- Silent Switcher®2 Architecture
  - Ultralow EMI Emissions
  - Optional Spread Spectrum Modulation
- Two High Voltage Synchronous Buck Regulators
  - 3V to 42V Input Voltage Range
  - Output Currents Up to 2.5A per Channel
  - Channels May Be Connected in Parallel Using a Single Inductor
- Two Low Voltage Synchronous Buck Regulators
  - 3V to 8V Input Voltage Range
  - Output Currents Up to 4A per Channel
  - Channels May Be Connected in Parallel Using a Single Inductor
- 12µA I_Q All Channels Active and No-Load
- Flexible Supply Sequencing and Control
- Adjustable and Synchronizable: 350kHz to 3MHz
- Available in 36-Lead LQFN (5mm × 6mm)
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Automotive Systems
- Industrial Controls and Power Supplies

DESCRIPTION

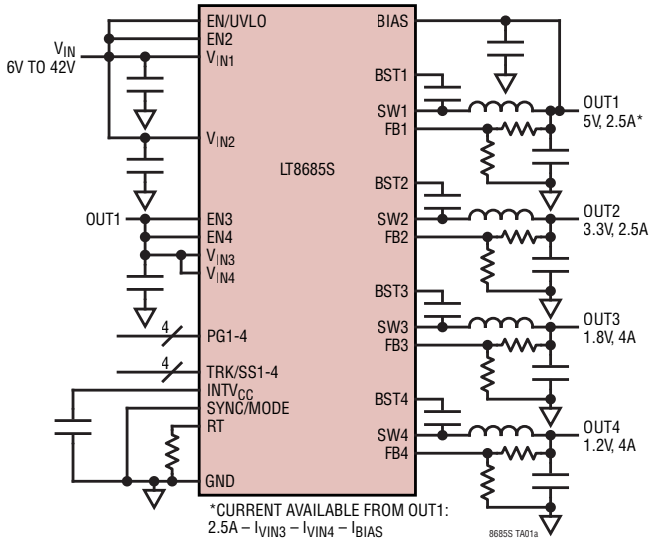
The LT®8685S is a highly flexible, four channel, current mode, monolithic regulator able to power a wide range of automotive and industrial applications while occupying minimal board space.

The LT8685S combines two 42V capable 2.5A buck regulators with two 8V capable 4A buck regulators. The two 42V regulators may be combined to provide up to 5A of output current using a single inductor. Similarly, the two 8V regulators may be combined to provide up to 8A of output current using a single inductor. Individual channel enable, track/soft-start and power good pins provide flexible power supply sequencing and control. The LT8685S features a Silent Switcher 2 architecture, plus selectable spread spectrum mode, to provide ultralow EMI/EMC emissions while delivering high efficiency at high switching frequencies.

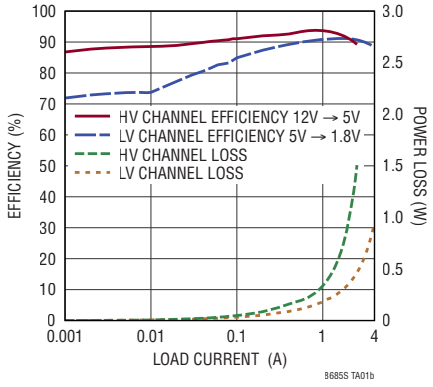
The LT8685S incorporates thermal shutdown and individual channel cycle-by-cycle current limit for short circuit protection and robust operation.

TYPICAL APPLICATION

42V Input, Quad Output 2MHz Step-Down Regulator



Efficiency and Loss



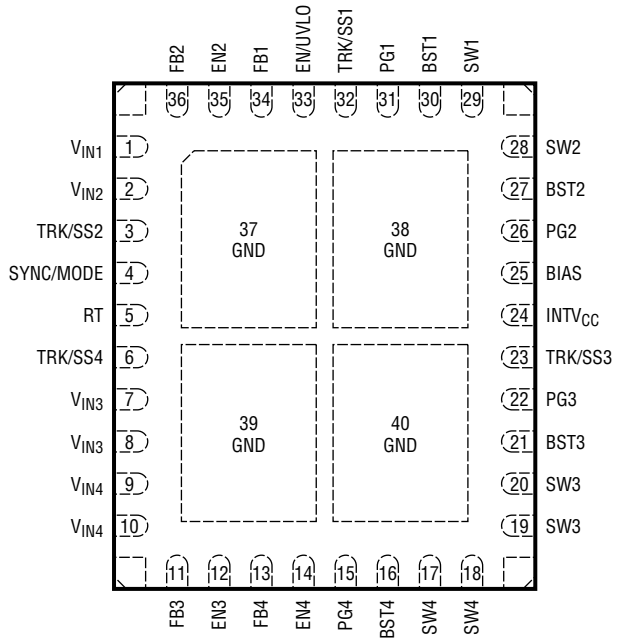
Rev. 0

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN1}, V_{IN2} ..... –0.3V to 42V
V_{IN3}, V_{IN4} ..... –0.3V to 10V
EN/UVLO, EN2, EN3, EN4.....42V
PG1, PG2, PG3, PG4, SYNC/MODE.....6V
BIAS..... –0.3V to 14V
FB1, FB2, FB3, FB4.....4V
TRK/SS1, TRK/SS2, TRK/SS3, TRK/SS4.....4V
Operating Junction Temperature (Notes 2, 3)
LT8685SR.....–40°C to 150°C
Storage Temperature Range .....–65°C to 150°C
Maximum Reflow (Package Body)
Temperature.....260°C

PIN CONFIGURATION



LQFN PACKAGE
36-LEAD (5mm × 6mm × 0.95mm)

T_{JMAX} = 150°C, θ_{JA} = 19°C/W, θ_{JC_top} = 18.3°C/W, θ_{JC_bottom} = 5.4°C/W
EXPOSED PAD (PINS 37 TO 40) MUST BE SOLDERED TO PCB GND

NOTE:
1) θ VALUES ARE DETERMINED BY SIMULATION PER JESD51 CONDITIONS;
2) θ_{JA} VALUE IS OBTAINED WITH DEMO BOARD.

ORDER INFORMATION

PART NUMBER	TAPE AND REEL	PAD OR BALL FINISH	PART MARKING		PACKAGE TYPE*	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
			DEVICE	FINISH CODE			
LT8685SRV#PBF	LT8685SRV#TRPBF	Au (RoHS)	8685S	e4	LQFN (Laminate Package with QFN Footprint)	3	–40°C to 150°C
AUTOMOTIVE PRODUCTS**							
LT8685SRV#WPBF	LT8685SRV#WTRPBF	Au (RoHS)	8685S	e4	LQFN (Laminate Package with QFN Footprint)	3	–40°C to 150°C

- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Tape and reel specifications.
- Parts ending with PBF and RoHS are WEEE compliant.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

*The LT8685S package has the same dimensions as a standard 5mm × 6mm QFN package.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN1} = V_{IN2} = 12V, V_{IN3} = V_{IN4} = 5V, f_{SW} = 2MHz unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Current, Shutdown				0.5	1.5	µA
Total Operating Input Current, Burst	V_{OUT1} = V_{BIAS} = 5V, V_{OUT2} = 3.3V, V_{OUT3} = 1.8V, V_{OUT4} = 1.2V, $V_{SYNC/MODE}$ = 0V, No Load			12		µA
Total Operating Input Current, Pulse-Skipping	V_{OUT1} = 5V, V_{OUT2} = 3.3V, V_{OUT3} = 1.8V, V_{OUT4} = 1.2V, $V_{SYNC/MODE}$ = Floating, No Load			1100		µA
Switching Frequency	R_{RT} = 154k R_{RT} = 22.6k R_{RT} = 13.7k	● ● ●	0.28 1.8 2.65	0.35 2 3	0.45 2.25 3.4	MHz MHz MHz
SYNC Threshold Voltage	V_{IL} V_{IH}	● ●	 1.5		0.4	V V
SYNC/MODE Pin Input Current	$V_{SYNC/MODE}$ = 6V			75		µA
Internal V_{CC} Regulator				3.4		V
Internal V_{CC} Undervoltage Lockout	Falling		2.3	2.4	2.5	V
BIAS Pin Threshold				4.5		V
Channels 1 to 2						
Minimum Input Voltage (CH1 Only)		●		2.8	3	V
Feedback Reference Voltage		●	0.786	0.8	0.812	V
Feedback Input Current		●	–100	0	100	nA
V_{FB1}, V_{FB2} Line Regulation	V_{VIN1} = 3V to 42V			0.01		%/V
Peak Current Limit			4.2	4.8	5.4	A
Power FET On-resistance Main Switch (Top) Synchronous Switch (Bottom)	 I_{SW1}, I_{SW2} = 0.1A I_{SW1}, I_{SW2} = 0.1A			 210 110		 mΩ mΩ
EN/UVLO Threshold	EN/UVLO Falling	●	0.78	0.8	0.82	V
EN/UVLO Hysteresis				100		mV
EN/UVLO Input Current	V_{EN}/UVLO = 42V		–250	0	250	nA
EN2 Threshold	EN2 Falling	●	0.78	0.81	0.84	V
EN2 Hysteresis				50		mV
EN2 Input Current	V_{EN2} = 42V		–250	0	250	nA
Pgood Upper Threshold Offset from V_{FB1}, V_{FB2}	V_{FB1}, V_{FB2} Rising	●	4.5	7.5	10	%
Pgood Lower Threshold Offset from V_{FB1}, V_{FB2}	V_{FB1}, V_{FB2} Falling	●	–10	–7.5	–4.5	%
Pgood Hysteresis				1.2		%
Pgood Leakage	V_{PG1}, V_{PG2} = 6V		–250	0	250	nA
Pgood Pull-Down Resistance	V_{PG1}, V_{PG2} = 0.1V			500	1200	Ω
TRK/SS1, TRK/SS2 Pull-Up Current	$V_{TRK/SS1}$, $V_{TRK/SS2}$ = 0V			2		µA
Channels 3 to 4						
Feedback Reference Voltage		●	0.688	0.7	0.712	V
Feedback Input Current		●	–100	0	100	nA
V_{FB3}, V_{FB4} Line Regulation	V_{VIN1} = 3V to 42V			0.01		%/V
Peak Current Limit			7	8.2	9.4	A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN1} = V_{IN2} = 12V, V_{IN3} = V_{IN4} = 5V, f_{SW} = 2MHz unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power FET On-resistance Main Switch (Top) Synchronous Switch (Bottom)	 I_{SW3}, I_{SW4} = 0.1A I_{SW3}, I_{SW4} = 0.1A			 45 25		 mΩ mΩ
EN3, EN4 Threshold	EN3, EN4 Falling	●	0.78	0.81	0.84	V
EN3, EN4 Hysteresis				50		mV
EN3, EN4 Input Current	V_{EN3}, V_{EN4} = 42V		–250	0	250	nA
Pgood Upper Threshold Offset from V_{FB3}, V_{FB4}	V_{FB3}, V_{FB4} Rising	●	4.5	7.5	10	%
Pgood Lower Threshold Offset from V_{FB3}, V_{FB4}	V_{FB3}, V_{FB4} Falling	●	–10	–7.5	–4.5	%
Pgood Hysteresis				1.2		%
Pgood Leakage	V_{PG3}, V_{PG4} = 6V		–250	0	250	nA
Pgood Pull-Down Resistance	V_{PG3}, V_{PG4} = 0.1V			500	1200	Ω
TRK/SS3, TRK/SS4 Pull-Up Current	$V_{TRK/SS3}$, $V_{TRK/SS4}$ = 0V			2		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

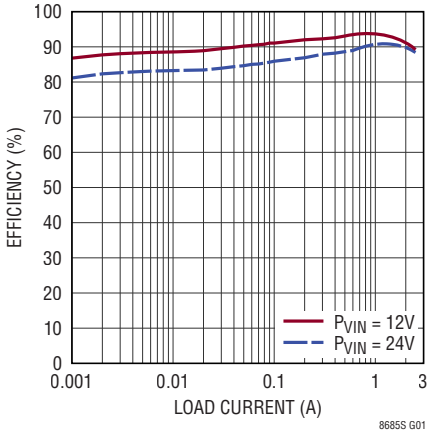
Note 2: The LT8685SR is specified over the –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: This IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

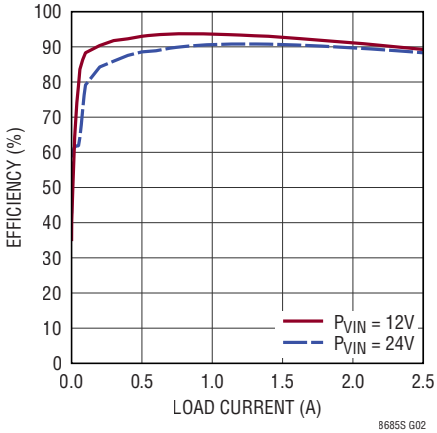
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. V_{IN1} = V_{IN2} = 12V, V_{IN3} = V_{IN4} = 3.3V, f_{SW} = 2MHz unless otherwise noted.

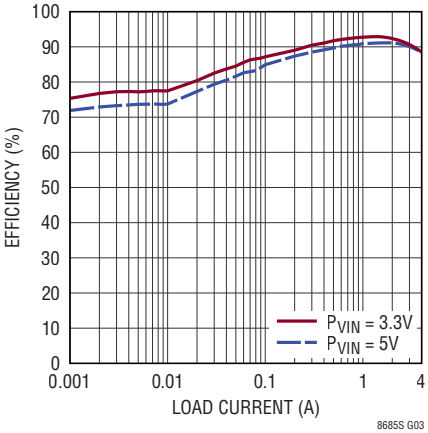
HV Channel Efficiency vs Load
V_{OUT} = 5V, Burst Mode® Operation



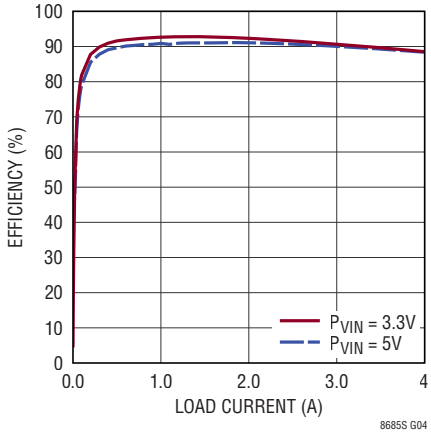
HV Channel Efficiency vs Load
V_{OUT} = 5V, Pulse Skip Mode



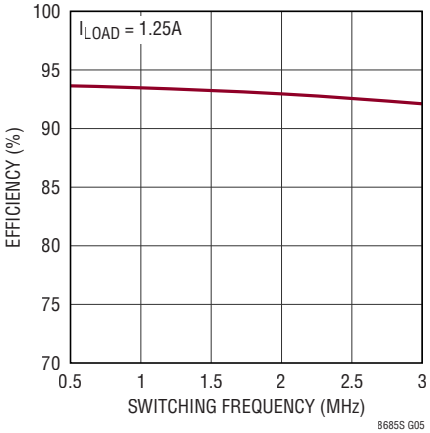
LV Channel Efficiency vs Load
V_{OUT} = 1.8V, Burst Mode Operation



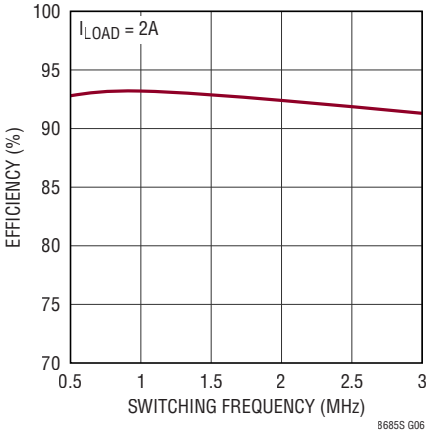
LV Channel Efficiency vs Load
V_{OUT} = 1.8V, Pulse Skip Mode



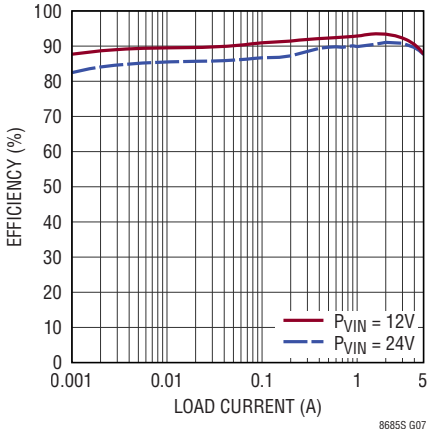
HV Channel Efficiency vs
Frequency V_{OUT} = 5V, Burst Mode
Operation



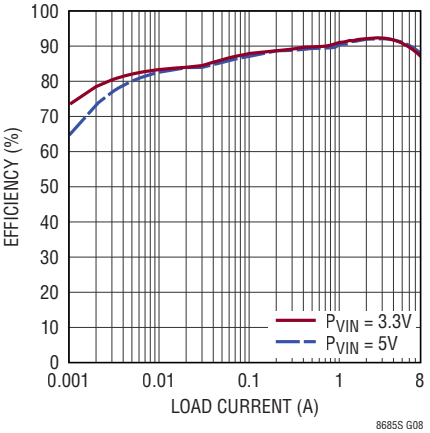
LV Channel Efficiency vs
Frequency V_{OUT} = 1.8V, Burst
Mode Operation



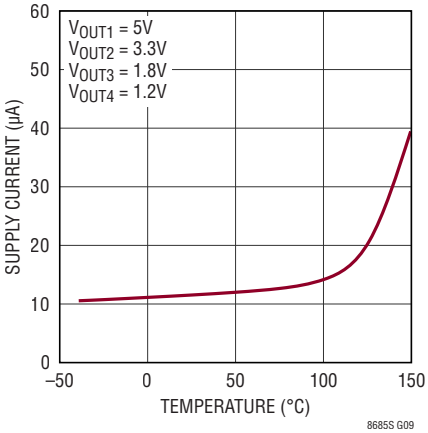
HV Channel Efficiency vs Load
CH1 and CH2 Shared V_{OUT} = 5V,
Burst Mode Operation



LV Channel Efficiency vs Load
CH3 and CH4 Shared V_{OUT} = 1.8V,
Burst Mode Operation



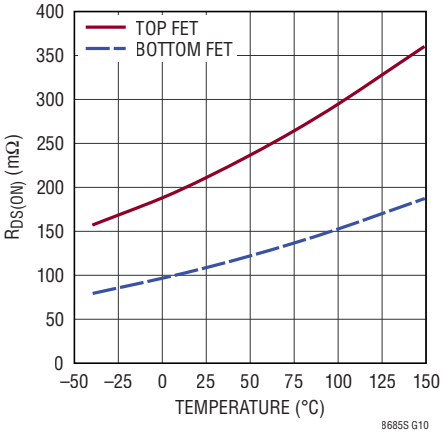
No-Load Supply Current vs
Temperature, Burst Mode Operation



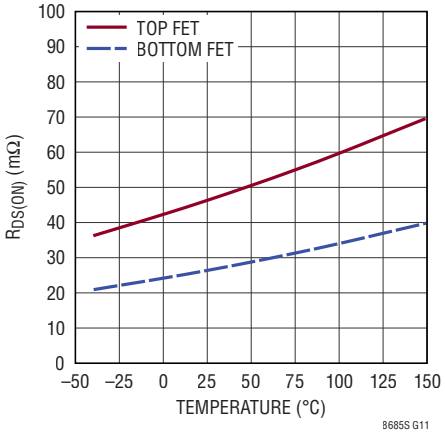
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. V_{IN1} = V_{IN2} = 12V, V_{IN3} = V_{IN4} = 3.3V, f_{SW} = 2MHz unless otherwise noted.

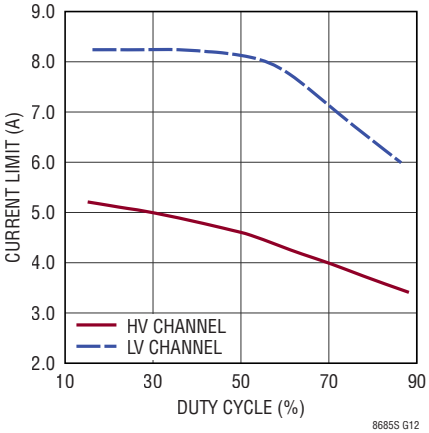
HV Channel $R_{DS(ON)}$ vs Temperature



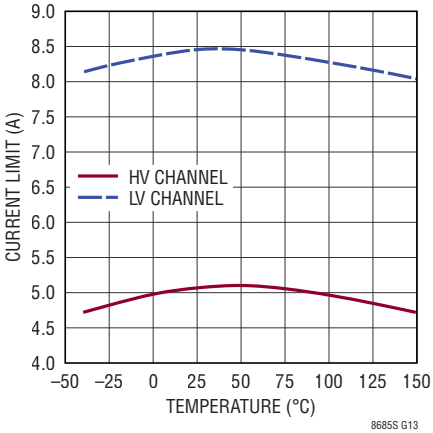
LV Channel $R_{DS(ON)}$ vs Temperature



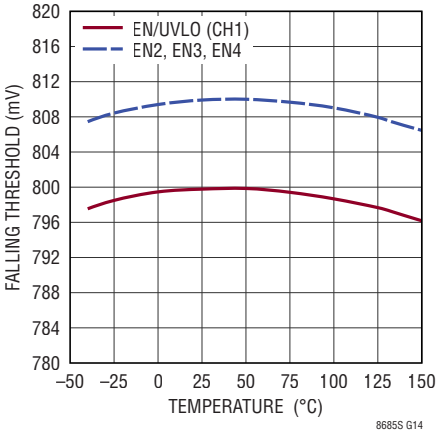
Top FET Current Limit vs Duty Cycle



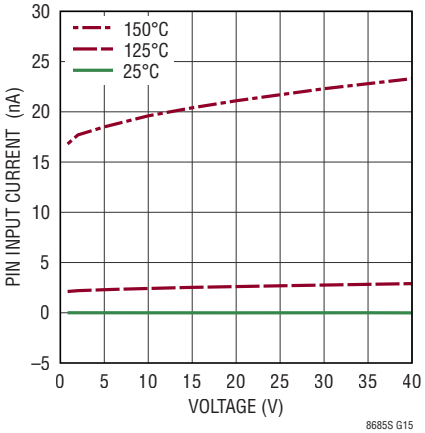
Top FET Current Limit vs Temperature



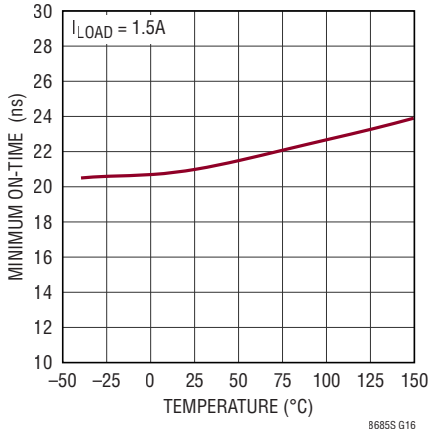
Enable Pin Falling Threshold vs Temperature



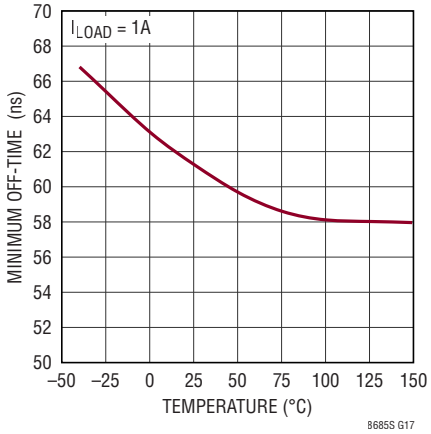
Enable Pin Current vs Voltage and Temperature



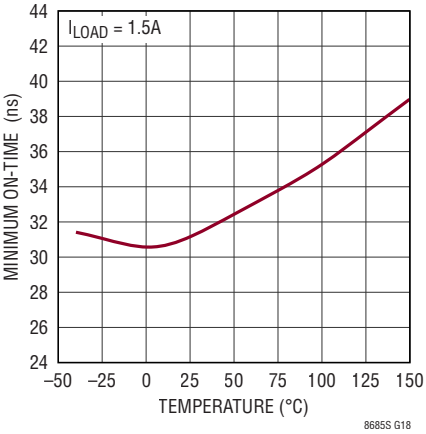
HV Channel Minimum On-Time vs Temperature



HV Channel Minimum Off-Time vs Temperature



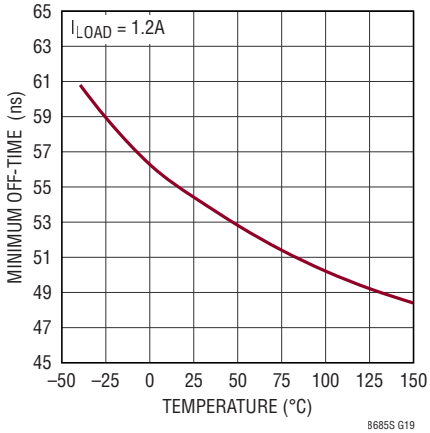
HV Channel Minimum On-Time vs Temperature, CH1 and CH2 Shared



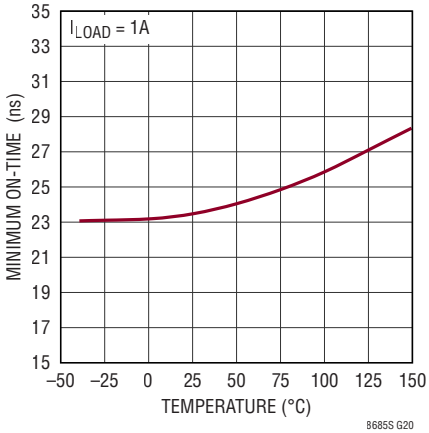
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. V_{IN1} = V_{IN2} = 12V, V_{IN3} = V_{IN4} = 3.3V, f_{SW} = 2MHz unless otherwise noted.

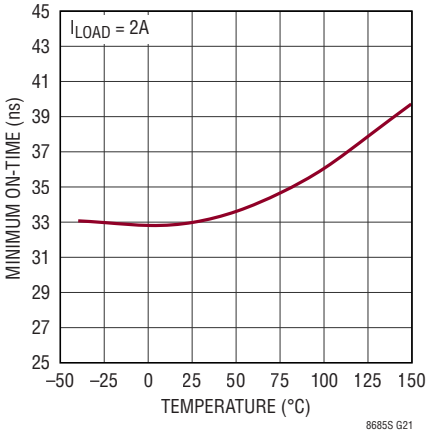
HV Channel Minimum Off-Time vs Temperature, CH1 and CH2 Shared



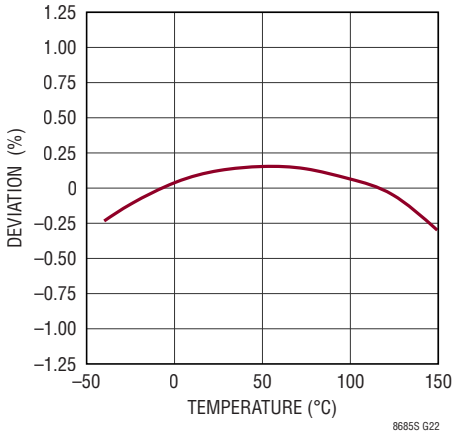
LV Channel Minimum On-Time vs Temperature



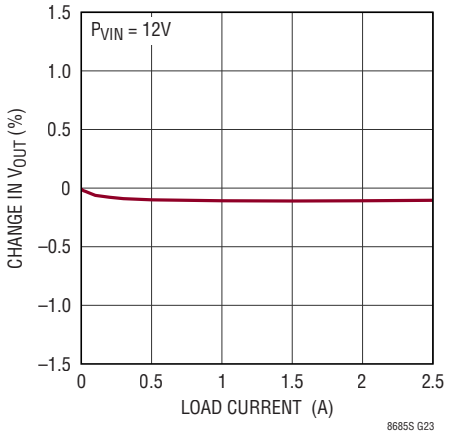
LV Channel Minimum On-Time vs Temperature, CH3 and CH4 Shared



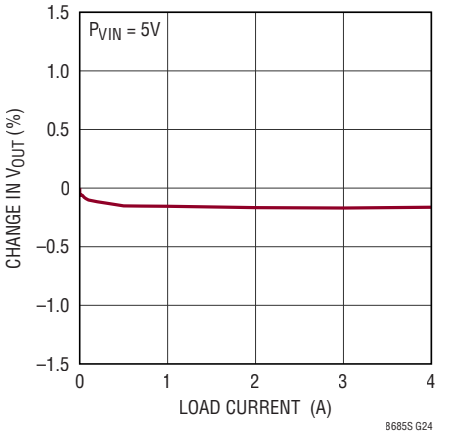
Reference Voltage Variation vs Temperature



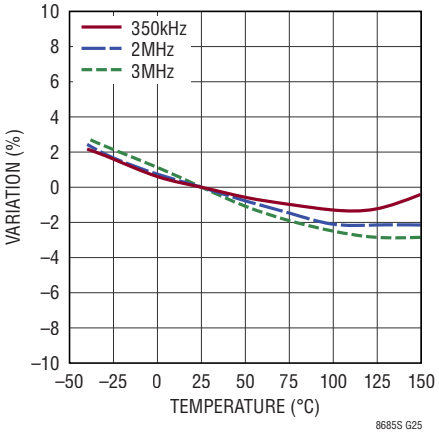
HV Channel Load Regulation



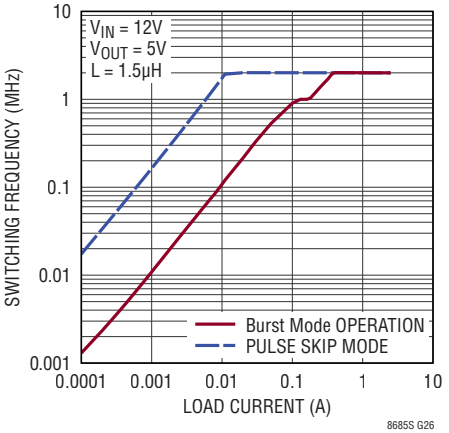
LV Channel Load Regulation



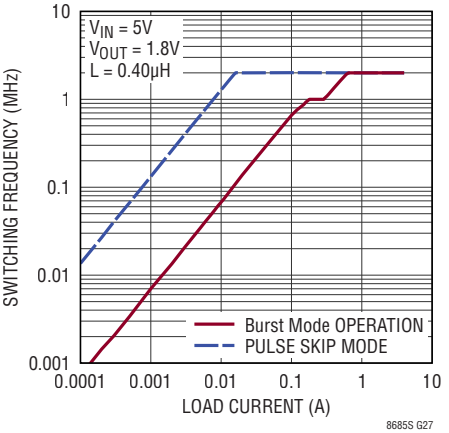
Switching Frequency vs Temperature



HV Channel Switching Frequency vs Load, R_T = 22.6kΩ



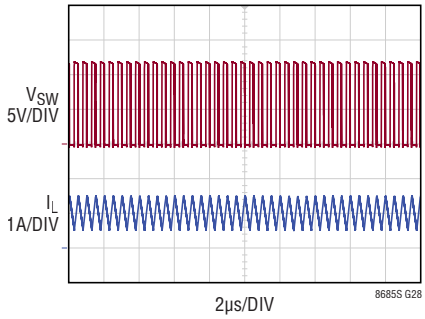
LV Channel Switching Frequency vs Load, R_T = 22.6kΩ



TYPICAL PERFORMANCE CHARACTERISTICS

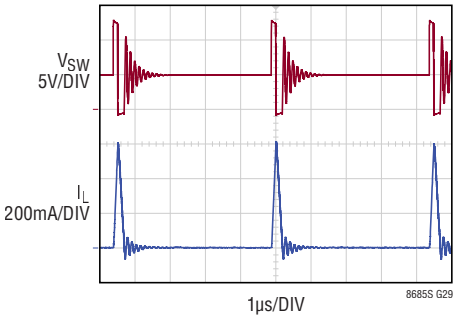
T_A = 25°C. V_{IN1} = V_{IN2} = 12V, V_{IN3} = V_{IN4} = 3.3V, f_{SW} = 2MHz unless otherwise noted.

Switching Waveform Continuous Full Frequency Operation



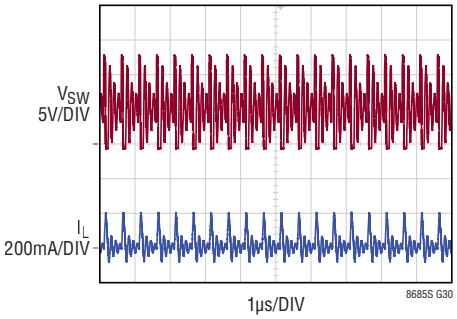
$12V_{IN}$ TO $5V_{OUT}$ AT 1A
SYNC_MODE = GND

Switching Waveform Burst Mode Operation



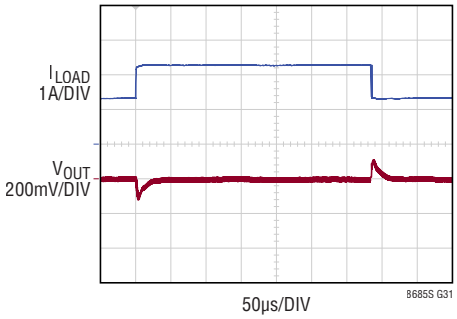
$12V_{IN}$ TO $5V_{OUT}$ AT 20mA
SYNC_MODE = GND

Switching Waveform Pulse Skipping Operation



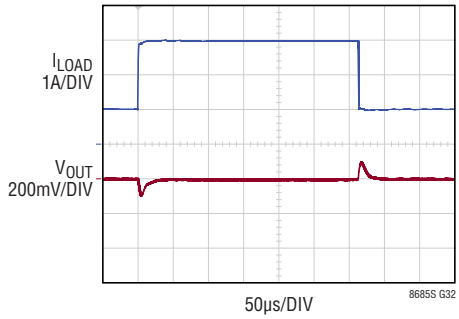
$12V_{IN}$ TO $5V_{OUT}$ AT 20mA
SYNC_MODE = FLOATING

HV Channel Load Step



1.25A TO 2.25A STEP
$5V_{OUT}$
C_{OUT} = 47µF
Burst Mode, f_{SW} = 2MHz

LV Channel Load Step

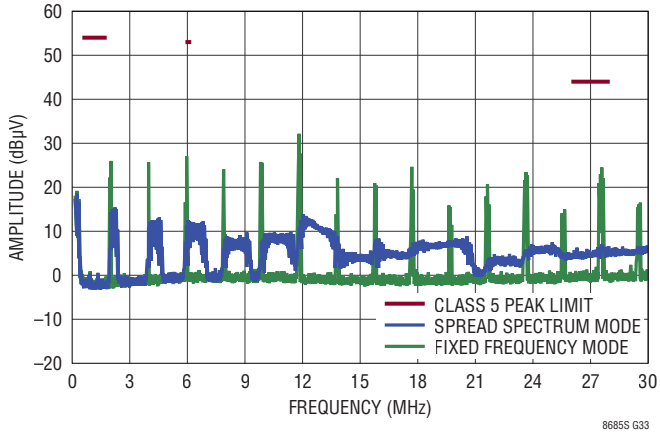


1A TO 3A STEP
$1.8V_{OUT}$
C_{OUT} = 47µF ×2
Burst Mode, f_{SW} = 2MHz

TYPICAL PERFORMANCE CHARACTERISTICS

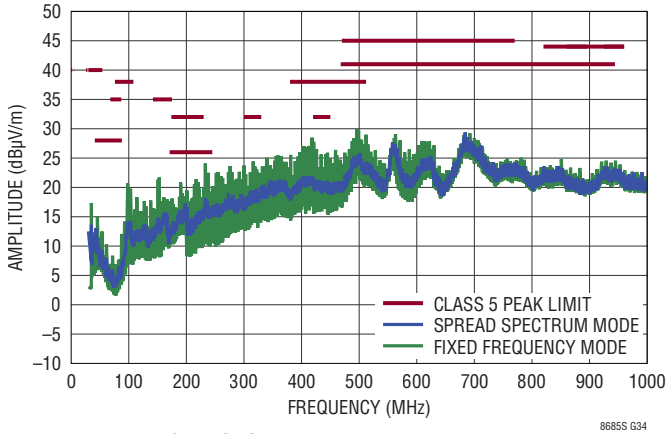
T_A = 25°C. V_{IN1} = V_{IN2} = 12V, V_{IN3} = V_{IN4} = 3.3V, f_{SW} = 2MHz unless otherwise noted.

Conducted EMI Performance



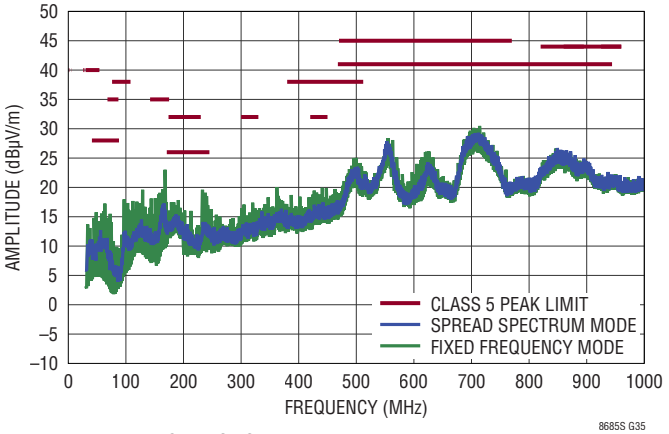
EVAL-LT8685S DEMO BOARD
(WITH EMI FILTER INSTALLED)
V_{EMI} = 14V, V_{OUT1} = 5V, V_{OUT2} = 3.3V, V_{OUT3} = 1.8V, V_{OUT4} = 1.2V
I_{OUT1} = I_{VIN3} + I_{VIN4} + I_{BIAS}, I_{OUT2} = 1A, I_{OUT3} = I_{OUT4} = 4A, f_{SW} = 2MHz

Radiated EMI Performance – Vertical Polarization (CISPR25 Radiated Emission Test with Class 5 Peak Limits)



EVAL-LT8685S DEMO BOARD
(WITH EMI FILTER INSTALLED)
V_{EMI} = 14V, V_{OUT1} = 5V, V_{OUT2} = 3.3V, V_{OUT3} = 1.8V, V_{OUT4} = 1.2V
I_{OUT1} = I_{VIN3} + I_{VIN4} + I_{BIAS}, I_{OUT2} = 1A, I_{OUT3} = I_{OUT4} = 4A, f_{SW} = 2MHz

Radiated EMI Performance – Horizontal Polarization (CISPR25 Radiated Emission Test with Class 5 Peak Limits)



EVAL-LT8685S DEMO BOARD
(WITH EMI FILTER INSTALLED)
V_{EMI} = 14V, V_{OUT1} = 5V, V_{OUT2} = 3.3V, V_{OUT3} = 1.8V, V_{OUT4} = 1.2V
I_{OUT1} = I_{VIN3} + I_{VIN4} + I_{BIAS}, I_{OUT2} = 1A, I_{OUT3} = I_{OUT4} = 4A, f_{SW} = 2MHz

PIN FUNCTIONS

V_{IN1} (Pin 1): Channel 1 and Internal $INTV_{CC}$ Regulator Power Supply Input. This pin should be closely decoupled to ground with a low ESR capacitor of value 2.2µF or greater.

V_{IN2} (Pin 2): Channel 2 Power Supply Input. This pin should be closely decoupled to ground with a low ESR capacitor of value 2.2µF or greater. This pin must be shorted to V_{IN1} when channel 2 is combined with channel 1.

SYNC/MODE (Pin 4): Mode Selection and External Synchronization Input Pin. This pin places all active LT8685S channels into high efficiency Burst Mode operation when tied to ground. Tie this pin to ground with a 26k (5% tolerance or better) resistor to enable high efficiency Burst Mode with spread spectrum modulation. Float this pin to enable pulse-skipping mode. Tie this pin to $INTV_{CC}$ to enable pulse-skipping mode with spread-spectrum modulation. When this pin is driven by an external clock source, the LT8685S will synchronize its switching frequency to that of the external clock and operate in pulse-skipping mode. Channels 1 to 4 clock phases default to 0°, 180°, 270°, and 90° respectively when operating independently. When combining channels, the master channel determines the operating phase. See the Applications Information section for more detail.

RT (Pin 5): Switching Frequency Program Pin. Connect an external resistor from this pin to ground to program the LT8685S switching frequency from 350kHz to 3MHz. When using external clock synchronization, an R_T resistor must be selected to match the nominal incoming clock frequency. See the Applications Information section for more detail.

V_{IN3} (Pins 7, 8): Channel 3 Power Supply Input. When driven from another LT8685S channel, the required decoupling capacitance for this pin is largely satisfied by the output capacitance of the driving channel. In this scenario, a low ESR capacitor of value 1µF or greater located close to the V_{IN3} pin is generally sufficient. If driven from an external source, this pin should be closely decoupled with a low ESR capacitor of value 4.7µF or greater.

V_{IN4} (Pins 9, 10): Channel 4 Power Supply Input. When driven from another LT8685S channel, the required decoupling capacitance for this pin is largely satisfied by the output capacitance of the driving channel. In this scenario, a low ESR capacitor of value 1µF or greater located close to the V_{IN4} pin is generally sufficient. If driven from an external source, this pin should be closely decoupled with a low ESR capacitor of value 4.7µF or greater. This pin must be shorted to V_{IN3} when channel 4 is combined with channel 3.

FB3 (Pin 11): Channel 3 Output Voltage Feedback Pin. Channel 3 regulates this pin to a precision, internal, 0.7V reference voltage. Connect this pin to the appropriate resistor divider network to program the desired output voltage.

FB4 (Pin 13): Channel 4 Output Voltage Feedback Pin. Channel 4 regulates this pin to a precision, internal, 0.7V reference voltage. Connect this pin to the appropriate resistor divider network to program the desired output voltage. When this pin is tied to $INTV_{CC}$, channel 4 is combined with channel 3 to create a single output channel with increased output current capability. See the Applications Information section for more detail.

$INTV_{CC}$ (Pin 24): Internal Regulator Output Pin. This regulator provides the supply current for the power FET driver circuits and internal control circuitry. This pin should be decoupled to ground with a low ESR ceramic capacitor of value 4.7µF. This capacitor should be placed close to the $INTV_{CC}$ pin with a low impedance connection to the exposed pad ground. This supply is not intended as a power supply output. Do not connect external circuitry to this pin.

BIAS (Pin 25): External Regulator Input Pin. The internal regulator, $INTV_{CC}$, will draw current from this supply instead of V_{IN1} when BIAS is tied to a voltage higher than 4.5V and V_{VIN1} is greater than V_{BIAS} + 1V. Connecting this pin to a high efficiency supply, such as an LT8685S output channel regulating to 5V, improves overall efficiency by reducing the on-chip power consumption that would normally result when drawing current from V_{IN1}. When used, this pin should be decoupled to ground with

PIN FUNCTIONS

a low ESR ceramic capacitor of value 0.1µF or greater. When driven by another LT8685S channel, the required decoupling capacitance may be satisfied with the output capacitance of the driving channel. When not used, tie this pin to ground.

SW1, SW2, SW3, SW4 (Pin 29, Pin 28, Pins 19 - 20, Pins 17 - 18): Channel Switch Pins. These pins are the outputs of each corresponding channel's internal power switches. When channels are operating independently, connect each SW pin to the corresponding channel's inductor and boost capacitor. When combining channels, tie the combined channel's SW pins together with a low impedance connection. SW traces on the PCB should be kept short for best efficiency and EMI performance.

BST1, BST2, BST3, BST4 (Pin 30, Pin 27, Pin 21, Pin 16): Channel Boost Pins. These pins provide a drive voltage, higher than the supply voltage, to the gate of each channel's top power switch.

PG1, PG2, PG3, PG4 (Pin 31, Pin 26, Pin 22, Pin 15): Open-Drain Power Good Output Pins. Each channel's PG pin is pulled to ground when the voltage at the corresponding FB pin is not within ±7.5% of the internal reference. PG becomes high impedance once the voltage at the corresponding FB pin returns to within ±6% of the internal reference. PG outputs for enabled channels are valid for V_{IN1} voltages greater than 3V. PG outputs are pulled low for channels which are not enabled. When channels are combined, the dependent (slave) channel's PG pin should be open.

TRK/SS1, TRK/SS2, TRK/SS3, TRK/SS4 (Pin 32, Pin 3, Pin 23, Pin 6): Output Tracking and Soft-Start Pins. These pins allow user control of output voltage ramp rate during startup. A TRK/SSx voltage below the internal reference forces the channel to regulate the FBx pin to equal the TRK/SSx voltage. When TRK/SSx is above internal reference, the tracking function is disabled and the internal reference resumes control of the error amplifier. An internal 2µA pull-up current from $INTV_{CC}$ on this pin allows a capacitor to program output voltage slew rate. When channels are combined, the dependent (slave) channel's TRK/SS pin should be open.

EN/UVLO (Pin 33): Channel 1 Enable and Undervoltage Lockout Pin. The LT8685S is in low power shutdown when this pin is below 0.4V regardless of the state of the remaining LT8685S enable pins. A voltage above 0.9V (rising) enables LT8685S operation and channel 1. A precision threshold at 0.8V (falling) allows this pin to be used as an input undervoltage lockout by connecting a resistor divider between V_{IN1} and ground.

FB1 (Pin 34): Channel 1 Output Voltage Feedback Pin. Channel 1 regulates this pin to a precision, internal, 0.8V reference voltage. Connect this pin to the appropriate resistor divider network to program the desired output voltage.

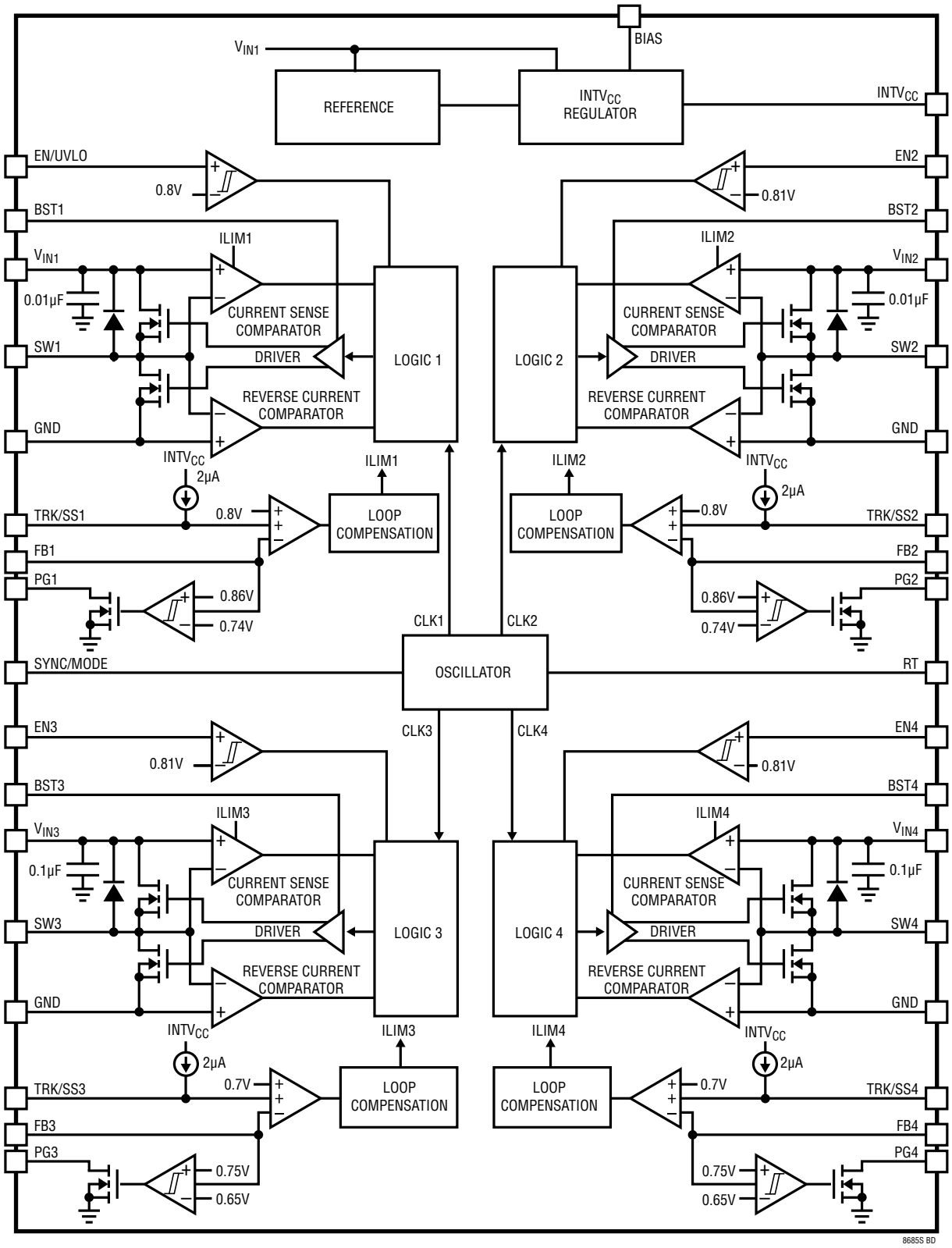
EN2, EN3, EN4 (Pin 35, Pin 12, Pin 14): Channel Enable Pins. Each LT8685S channel is active when the voltage on its corresponding enable pin is above 0.9V (rising). A precision threshold at 0.81V (falling) allows each enable pin to act as a programmable undervoltage lockout by connecting a resistor divider between the corresponding input supply and ground. When channels are combined, the dependent (slave) channel's EN pin should be connected to the enable pin of the controlling (master) channel.

FB2 (Pin 36): Channel 2 Output Voltage Feedback Pin. Channel 2 regulates this pin to a precision, internal, 0.8V reference voltage. Connect this pin to the appropriate resistor divider network to program the desired output voltage. When this pin is tied to $INTV_{CC}$, channel 2 is combined with channel 1 to create a single output channel with increased output current capability. See the Application Section for more detail.

GND (Exposed Pad Pins 37 - 40): Ground Pins. These pins must be soldered to the PCB to provide low impedance electrical contact to ground and good thermal contact to the PCB. See the Applications Information section for more detail.

CORNER PINS: These pins are for mechanical support only and can be tied anywhere on the PCB, typically ground.

BLOCK DIAGRAM



OPERATION

The LT8685S is a 42V input capable quad, monolithic, step-down regulator which incorporates Analog Device's 2nd generation Silent Switcher technology to allow fast switching edges for high efficiency at high switching frequency, while simultaneously achieving good EMI/EMC performance.

Channels 1 and 2 are designed to provide output currents up to 2.5A each from an input supply voltage as high as 42V. Channels 3 and 4 are designed to provide output currents up to 4A each from an input supply voltage as high as 8V. Higher output currents can be achieved by combining channels with a single inductor. For example, channels 1 and 2 can be combined using a single inductor to provide a regulated output up to 5A. Channels 3 and 4 can be combined using a single inductor to provide a regulated output up to 8A. Independent V_{IN} pins allow for the output of one channel to supply the input of the other channels.

START-UP

When enabled by setting the EN/UVLO voltage above its threshold, the LT8685S $INTV_{CC}$ regulator charges its output capacitor to supply the internal chip circuitry. Setting the EN/UVLO above 0.9V (rising) will enable the channel 1 regulator. Setting the EN/UVLO voltage below the UVLO threshold will put the part in low power shutdown mode regardless of the state of the other enable pins.

Channels 2, 3 and 4 are enabled by setting their respective enable pins above 0.9V (rising). When combining channels, connect the enable pin of the slave channel to that of the controlling channel. See Combining Channels in the Applications Information section for further detail.

BUCK REGULATOR OPERATION

Each channel is a monolithic, synchronous step-down regulator that operates from an independent V_{IN} pin. The internal top power MOSFET is turned on at the beginning of each oscillator cycle and turned off when the current flowing through the top MOSFET reaches a level determined by the error amplifier. The error amplifier measures the output voltage through an external resistor divider tied to the FB pin to control the peak current in the top switch. The reference of the error amplifier is determined by the lower of the internal reference and the voltage at its soft-start (TRK/SSx) pin. While the top MOSFET is off, the bottom MOSFET is turned on for the remainder of the oscillator cycle or until the inductor current starts to reverse. In current overload conditions the bottom MOSFET will remain on and the next clock cycle will be delayed until the switch current is reduced.

PRECISION ENABLE PINS

When driven below 0.4V, the EN/UVLO pin will place the LT8685S into low power shutdown mode. A voltage on the EN/UVLO pin above 0.9V (rising) will enable channel 1 operation. Channels 2, 3 and 4 are also activated by driving their respective EN2, EN3 and EN4 pins above 0.9V (rising).

A precision threshold of 0.8V (falling) allows the EN/UVLO to be used as an input undervoltage lockout by connecting a resistor divider between V_{IN1} and ground. Similarly, a precision threshold of 0.81V allows EN2, EN3, and EN4 to also be used as input undervoltage lockouts. See the Applications Information section for more detail.

POWER GOOD COMPARATORS

Each channel has a power good comparator with an open-drain output that pulls its PG pin low when its feedback voltage is more than 7.5% above or below the reference voltage. The PG pin is released when the feedback pin is within 6% of the reference voltage. The PG outputs are not valid until $INTV_{CC}$ rises to 2.7V.

SWITCHING FREQUENCY

Each channel operates from a clock provided by an internal oscillator whose frequency is determined by an external resistor connected from the RT pin to ground. By selecting the appropriate external resistor value, the switching frequency may be configured from 350kHz to 3MHz. See the Applications Information section for further frequency selection information.

The oscillator generates four clock phases. When operating independently, the relative phases of the channels are

OPERATION

0° for CH1, 180° for CH2, 270° for CH3 and 90° for CH4. Multiphase operation reduces input current ripple amplitude while increasing the ripple frequency resulting in lower required input capacitance. When combining channels, the master channel phase determines the combined channel's clock phase.

MODE SELECTION AND SYNCHRONIZATION

The LT8685S offers two primary operating modes, Burst Mode and Pulse Skipping Mode, plus the option to select frequency spread-spectrum for each. In pulse skipping mode, all switching cycles remain aligned to the internal clock. Further, full switching frequency is maintained to lower load currents than Burst Mode. Conversely, Burst Mode reduces input current at low load currents, thereby achieving higher low load efficiency than Pulse Skipping Mode. Selecting spread-spectrum results in frequency modulation of the programmed clock frequency to reduce EMI/EMC emissions. When selected, the clock frequency will vary between the programmed frequency and the programmed frequency plus approximately 20%.

The SYNC/MODE pin is used to select the desired operating mode. To select low ripple, high efficiency Burst Mode, connect the SYNC/Mode pin to ground. Alternatively, connect a 26k (5% tolerance or better) resistor to enable low ripple high efficiency Burst Mode operation with spread spectrum. To select pulse skipping mode, float the SYNC/MODE pin, or to enable pulse skipping with spread spectrum connect the SYNC/MODE pin to $INTV_{CC}$.

Finally, the LT8685S may be synchronized to an external clock source by driving the SYNC/MODE pin with a clock signal that has a minimum high voltage of 1.5V and maximum low voltage of 0.4V. The minimum required pulse width is 100ns for a high pulse and 100ns for a low pulse. When syncing, the R_T resistor should be chosen to set the LT8685S switching frequency close to the synchronization frequency. The LT8685S will operate in pulse-skipping mode while synchronized to an external clock.

$INTV_{CC}$ REGULATOR

The $INTV_{CC}$ regulator supplies internal LT8685S circuitry. The current draw will depend on the operating frequency, the higher the switching frequency, the greater the current drawn from $INTV_{CC}$. The regulator is supplied by V_{IN1} at start-up, but it will draw its supply current from BIAS if the BIAS voltage is above 4.5V and V_{IN1} is greater than V_{BIAS} + 1V. If the BIAS pin is connected to a switching regulator channel it will improve efficiency, reduce on-chip power dissipation and lower the required current. The $INTV_{CC}$ regulator may be used to configure other input pins and output pull-ups related to the LT8685S. It should not be used to connect to any components not related to the LT8685S to avoid unexpected interactions.

APPLICATIONS INFORMATION

The LT8685S combines four buck converters to provide a flexible system supply that can be configured to generate two to four regulated outputs while occupying minimal board space.

PRECISION UNDERVOLTAGE LOCKOUT

The accurate 0.8V threshold (falling) of the EN/UVLO pin enables a programmable LT8685S undervoltage lockout feature realized by connecting an external resistor divider between the V_{IN1} input supply pin and the EN/UVLO pin. An EN/UVLO logic low input turns off all channels regardless of the state of EN2, EN3, and EN4 pins.

The LT8685S UVLO divider circuit is shown in Figure 1. The UVLO threshold is given by:

$$V_{(LT8685S\_UVLO)} = \frac{R_{UV1} + R_{UV2}}{R_{UV2}} \bullet 0.8V$$

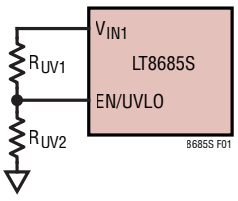


Figure 1. LT8685S UVLO Resistor Divider Connection

APPLICATIONS INFORMATION

Similar to the EN/UVLO pin, the accurate 0.81V reference of the EN2, EN3 and EN4 pins enables a programmable undervoltage lockout feature for each corresponding channel, realized by connecting an external resistor divider between the respective channel's input supply pin and its EN pin.

The individual channel UVLO divider circuit is shown in Figure 2. The threshold is given by:

$$V_{(CHAN\_UVLO)} = \frac{R_{UV1} + R_{UV2}}{R_{UV2}} \bullet 0.81V$$

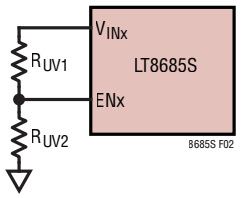


Figure 2. Individual Channel UVLO Resistor Divider Connection

SWITCHING FREQUENCY

Each channel operates from a clock provided by an internal oscillator whose frequency is determined by an external resistor connected from the RT pin to ground. By selecting the appropriate external resistor value, the switching frequency may be programmed from 350kHz to 3MHz.

Table 1 shows the recommended value of the R_T resistor for some common switching frequencies.

Table 1. Switching Frequency (f_{SW}) vs R_T Value

SWITCHING FREQUENCY (MHz)	R_T (kΩ)
0.35	154
0.5	107
0.75	69
1	49.9
1.25	39
1.5	32
1.75	26.4
2	22.6
2.25	19.6
2.5	17.2
2.75	15.4
3	13.7

The following equation approximates the values shown in Table 1.

$$R_T = \frac{55.4}{f_{SW} - 0.002} - 5$$

Where f_{SW} is in MHz, and R_T is in kΩ. The RT pin is sensitive to noise so the resistor should be placed close to the LT8685S and away from noise sources.

The oscillator generates four clock phases. When operating independently, the relative phases of the channels are 0° for CH1, 180° for CH2, 270° for CH3 and 90° for CH4. When combining channels, the master channel phase determines the combined channel's clock phase.

COMBINING CHANNELS

The LT8685S provides the ability to combine multiple regulators to create a single regulator capable of greater output current using a single inductor.

The allowed channel combinations are given in Table 2.

Table 2. Allowed Channel Combinations

	CONFIGURATION	NUMBER OF INDEPENDENT REGULATORS
1	1, 2, 3, 4	4
2	1, 2, 3 + 4	3
3	1 + 2, 3, 4	3
4	1 + 2, 3 + 4	2

When combining, the lowest numbered channel assumes control of the combined regulators. For example, with channel 1 and channel 2 combined, channel 1 assumes control (master) and channel 2 becomes dependent (slave). A feedback network is connected only to the master channel to program the combined regulator output voltage. The slave channel's feedback pin must be connected to $INTV_{CC}$.

Combined channels must have a low impedance connection between their respective V_{IN} pins, SW pins, and BST pins. Only a single inductor is connected to the combined SW pins. Though combined channels' BST pins are connected together, each channel should retain their individual boost capacitors.

APPLICATIONS INFORMATION

A simplified application schematic showing sharing between channels 1 and 2 as well as channels 3 and 4 is given in Figure 3.

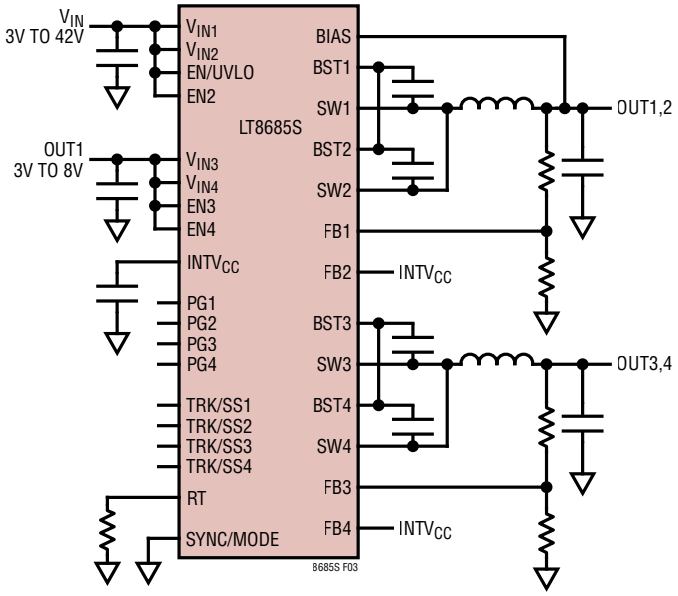


Figure 3. Simplified Schematic of Channel Sharing

REVERSE INPUT PROTECTION

In some applications, such as battery charging or battery backup applications, an LT8685S channel output may be held high when its input is made to either float or is grounded. If the input to the channel is floated, and the LT8685S is enabled, then the LT8685S's internal circuitry will pull its quiescent current through the SW pin. If the input is floated, and the LT8685S is disabled, then the SW pin current will drop to less than 1µA. If the input is grounded, an input protection diode is required to prevent reverse current from the output, through the top power FET body diode (shown in the Block Diagram), out of the V_{INx} pin to the grounded input.

BUCK REGULATOR COMPONENT SELECTION

Setting the Output Voltages

The output voltages of the buck channels are set with a resistor divider from the output to the related FBx pin as shown in Figure 4.

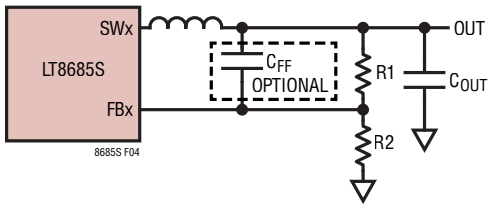


Figure 4. Feedback Resistor Divider

The value of R2 is best selected first as this establishes how much current is in the resistor divider network calculated as based on I = V_{REF}/R2 where V_{REF} is the internal channel reference voltage. The current should be chosen such that it is not influenced by anticipated leakage or noise. R1 can then be calculated from:

$$R1 = R2 \bullet \left(\frac{V_{OUTx}}{V_{REF}} - 1 \right)$$

C_{FF} can optionally be used to improve the transient response and stability of the internally compensated feedback loops. The values shown in the Typical Applications section will provide a good starting point for selecting C_{FF}, though careful evaluation of regulator stability should be made to ensure adequate design margin.

For the LT8685S's 42V input capable channels the maximum allowed programmed output voltage is 14V.

When the 8V input capable channels are combined (channels 3 and 4), the maximum allowed programmed output voltage is 4V.

Operating Frequency and Input Voltage Range

Each buck regulator's, minimum on-time, $t_{ON(MIN)}$, and minimum off-time, $t_{OFF(MIN)}$, impose limitations on the achievable duty cycle range and operating frequency. For buck regulators, the duty cycle is calculated as:

$$D = \frac{V_{OUTx}}{V_{INx}}$$

Further, the minimum duty cycle achievable at a given operating frequency is calculated as:

$$D_{MIN} = t_{ON(MIN)} \bullet f_{SW}$$

where f_{SW} is the programmed operating frequency.

APPLICATIONS INFORMATION

The maximum duty cycle achievable at a given operating frequency is calculated as:

$$D_{MAX} = 1 - (t_{OFF(MIN)} \bullet f_{SW})$$

Combining these equations, the minimum V_{IN} voltage while regulating at full frequency is

$$V_{VINx(MIN)} = \frac{V_{OUTx}}{1-\left(t_{OFF(MIN)} \bullet f_{SW}\right)}$$

Below $V_{VINx(MIN)}$ the buck regulator will enter dropout, and the top switch will stay on longer than a clock cycle. While operating in dropout, the buck regulator's output voltage will be below the programmed value.

The maximum V_{IN} voltage while regulating at full frequency is

$$V_{VINx(MAX)} = \frac{V_{OUTx}}{t_{ON(MIN)} \bullet f_{SW}}$$

If the $V_{VINx(MAX)}$ given above is exceeded during regulation, the buck regulator will skip switch-on cycles to maintain regulation.

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the inductor ripple current. More specifically, the inductor ripple current decreases with higher inductor value or higher operating frequency according to the following equation:

$$\Delta I_L = \left(\frac{V_{OUT}}{f_{SW} \bullet L}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where ΔI_L = inductor ripple current (A), f_{SW} = switching frequency (Hz), L = inductor value (H), and V_{IN} is the nominal input voltage rating. A trade-off between component size, efficiency and operating frequency can be seen from this equation. Accepting larger values of ΔI_L allows the use of lower value inductors but results in greater core loss in the inductor, greater ESR loss in the output capacitor, and larger output ripple.

The inductor value should be chosen to give a peak-to-peak ripple current ΔI_L of between 35% and 45% of the rated channel output current at the nominal input voltage. Note, the rated channel output current is 2.5A for channels 1 and 2, and 4A for channels 3 and 4. Channels 1 and 2 have a rating of 5A when combined, and channels 3 and 4 have a rating of 8A when combined. Rearranging the equation above, select the inductor value according to:

$$L = \left(\frac{V_{OUT}}{f_{SW} \bullet \Delta I_L}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating that is greater than the maximum expected output load of the application. In addition, for best efficiency the inductor series resistance should be as small as possible, and the core material should be intended for the application switching frequency.

The saturation current rating of the inductor must be higher than the load plus half the ripple current. This peak inductor current can be computed per the following equation:

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

where $I_{OUT(MAX)}$ is the maximum output current for a given application.

The optimum inductor for a given application may differ from the one indicated by this design guide. Careful evaluation of the application circuit should be completed with the chosen inductor to ensure adequate design margin.

Input Capacitor Selection

Buck, or step-down, converters draw current from the input supply in pulses with very fast rise and fall times. An input capacitor is required to reduce the resultant voltage ripple at the input and minimize EMI. For this function, a ceramic X7R or X5R bypass capacitor should be placed between each buck regulator's V_{IN} pin and ground. To be most effective, the input capacitor must have low impedance at the switching frequency and an adequate ripple current rating.

APPLICATIONS INFORMATION

The worst-case ripple current occurs when V_{OUT} is one-half V_{IN}. Under this condition, the ripple current is:

$$I_{CIN(RMS)} = \frac{I_{OUT}}{2}$$

Reasonable starting values for the input capacitance are 2.2µF for channels 1 and 2 and 2.2µF for channels 3 and 4.

When combining channels, the shared channel V_{IN} pins must be connected together, and the input capacitor should be chosen based on the total current supplied by the combined channels.

Output Capacitor Selection

The output capacitor performs two functions. First, it filters the inductor current to generate an output with low voltage ripple. Second, it stores energy to minimize droop and overshoot during transient loads. Because the LT8685S buck converters are able to operate at a high frequency, required output capacitance is minimal. The internally compensated current mode control loops are stable without requiring a minimum series resistance (ESR) in the output capacitor. Therefore, ceramic capacitors may be used and will result in very low output ripple.

An estimate for the output ripple is as follows for a given capacitor type:

$$V_{RIPPLE} = \frac{\Delta I_L}{8 \bullet f_{SW} \bullet C_{OUT}}$$

for ceramic capacitors, and

$$V_{RIPPLE} = \Delta I_L \bullet ESR$$

for aluminum or tantalum capacitors. V_{RIPPLE} is the peak-to-peak output ripple, f_{SW} is the switching frequency in MHz, ΔI_L is the peak-to-peak ripple current in the inductor, C_{OUT} is the output capacitor value in µF and ESR is the output capacitor effective series resistance.

The low ESR and small size of ceramic capacitors make them the preferred type for LT8685S applications. However, not all ceramic capacitors are the same. Many of the higher value capacitors use dielectrics with high temperature and voltage coefficients. Y5V and Z5U types lose a large fraction of their capacitance with applied voltage and at temperature extremes. Because loop stability, transient response ripple and EMI depend on the value of the input and output capacitors, it is best to use X5R (max 85°C), X7R (max 125°C) or X8R (max 150°C) capacitors depending on the operating temperature range.

Electrolytic capacitors are also an option. The ESRs of most aluminum electrolytic capacitors are too large to deliver low output ripple. Tantalum, as well as newer, lower ESR organic electrolytic capacitors intended for power supply use are suitable. Choose a capacitor with a low enough ESR for the required output ripple. Because the volume of the capacitor determines its ESR, both the size and value will be larger than a ceramic capacitor that would give similar ripple performance.

The Typical Applications section provides a reasonable starting point for output capacitor values. Careful evaluation of each application must be made to ensure adequate design margin.

Boost Capacitor Selection

Connecting a capacitor between each channel's BST and SW pins creates an internal approximately 3.4V supply used to drive the internal power devices. For most applications, choosing a 0.1µF ceramic capacitor for this function works well.

Although the SW and BST pins of combined channels are connected at the board level to drive a single inductor, for robust operation, each of the combined channels must have its own boost capacitor connected between their respective BST and SW pins.

Output Voltage Tracking and Soft-Start

The LT8685S's programmable channel soft-start feature, which controls the output voltage ramp time during startup, combined with channel power good (PG) and enable (EN) functions, supports flexible startup sequencing and control. In addition, the soft-start feature can be used to reduce input surge current and prevent output voltage overshoot. To program the output voltage

APPLICATIONS INFORMATION

soft-start time, connect a capacitor between the channel's TRK/SS pin and ground according to:

$$t_{SS} = \frac{C_{SS} \bullet V_{REF}}{2\mu A}$$

where 2µA is the TRK/SS pull-up current, C_{SS} is the value of the capacitor in Farads, and V_{REF} is 0.8V for CH1 and CH2, 0.7V for CH3 and CH4.

The channel TRK/SSx pins are pulled down through approximately 300kΩ, which will discharge the external soft-start capacitor when the part is shut down or during certain fault conditions.

For output voltage tracking, the channel TRK/SS pin can be driven by an external voltage source. More specifically, when driven with a voltage between 0V and the internal reference level, the TRK/SS pin will override the internal reference input to the error amplifier thus regulating the FB voltage to that present on the TRK/SS pin. When TRK/SS is above the reference level, tracking is disabled, and the feedback voltage will regulate to the internal reference voltage.

When combining channels, slave channel TRK/SS pins should be open.

Power Good Comparators

Each LT8685S channel has a power good comparator with an open drain output pin, PGx. Each PG pin is pulled low when the corresponding feedback voltage is either above or below its reference voltage by more than 7.5%. See the Electrical Characteristics table for more information on each channel's power good thresholds. All PG pins will be pulled low when the part is shut down. Individual channel PG pins will be pulled low when their corresponding EN pin is low.

When combining channels, only the master channel PG pins are valid. Slave PG pins should be open.

PCB LAYOUT

The LT8685S is specifically designed to minimize EMI/EMC emissions and to maximize efficiency when switching at high frequencies.

For proper operation and minimum EMI, care must be taken during printed circuit board layout. A recommended board layout is available with the latest LT8685S demo board. Some general guidelines are available in the remainder of this section.

Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer and connect the exposed GND pad to this layer. The exposed pad ground connection should be made with the maximum number of vias possible to reduce thermal and electrical impedance to the board ground. For best performance, maximize unbroken board ground planes in the vicinity of the LT8685S.

The SW and BST nodes should be made as small as possible to minimize noise coupling to sensitive traces. Minimize traces connecting to the RT and all FB pins and provide ground shielding as needed to minimize noise coupling to these sensitive nodes.

For each buck regulator, place input bypass capacitors close to the V_{INx} pins with a low impedance connection to the exposed pad through the ground plane mentioned above.

The recommended layer use for a 4-layer board is:

Layer 1 (Components): use 2oz (70µm) copper. Unbroken high frequency/high current routing, including SW and BST node routing, plus inductor, input, and output capacitor placement. Ground fill on the remainder.

Layer 2 (Internal): Unbroken ground plane.

Layer 3 (Internal): Signal routing with ground plane on remainder.

Layer 4 (Bottom): Use 2oz (70µm) copper. Use for remaining signal routing with ground fill on the remainder.

THERMAL CONSIDERATIONS

The exposed pad is the path for conducting heat from the silicon die to the PC board and the surrounding air. For good heat conduction, thermal vias should be placed under the device to conduct heat down to internal ground planes and the back side of the board. Multiple small vias work better than a few large ones as the copper plating of

APPLICATIONS INFORMATION

the via is a much better conductor than the solder which may or may not fill the via volume. The planes will distribute heat over a large area.

Power dissipated within the LT8685S will result in a junction temperature rise beyond the ambient temperature in proportion to the package thermal resistance, θ_{JA} (°C/W). The power dissipation within the LT8685S can be estimated from an efficiency measurement by calculating the total power loss, then subtracting power loss in components external to the LT8685S, such as inductor DCR loss. The maximum operating junction temperature is then estimated by multiplying the estimated LT8685S power loss by the package θ_{JA} and summing the result with the maximum application ambient temperature.

A good board design can achieve a θ_{JA} of 17 °C/W. If the calculation of maximum junction temperature indicates the LT8685S will operate near or above the allowed junction temperature, more precise thermal modelling may be required or design changes must be made to reduce the die junction temperature. Design changes may include reducing V_{VINx}, reducing f_{SW}, or reducing the operating load current. Load current reduction may be achieved with either direct load current reduction or reducing the duty cycle or duration over which the maximum load current occurs. Die junction temperature can also be reduced by lowering the ambient temperature or the addition of air flow. Figure 5 shows the approximate allowable on-chip power dissipation for a given ambient temperature using a θ_{JA} =17 °C/W.

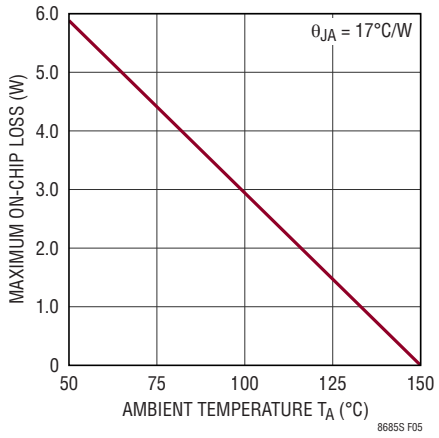
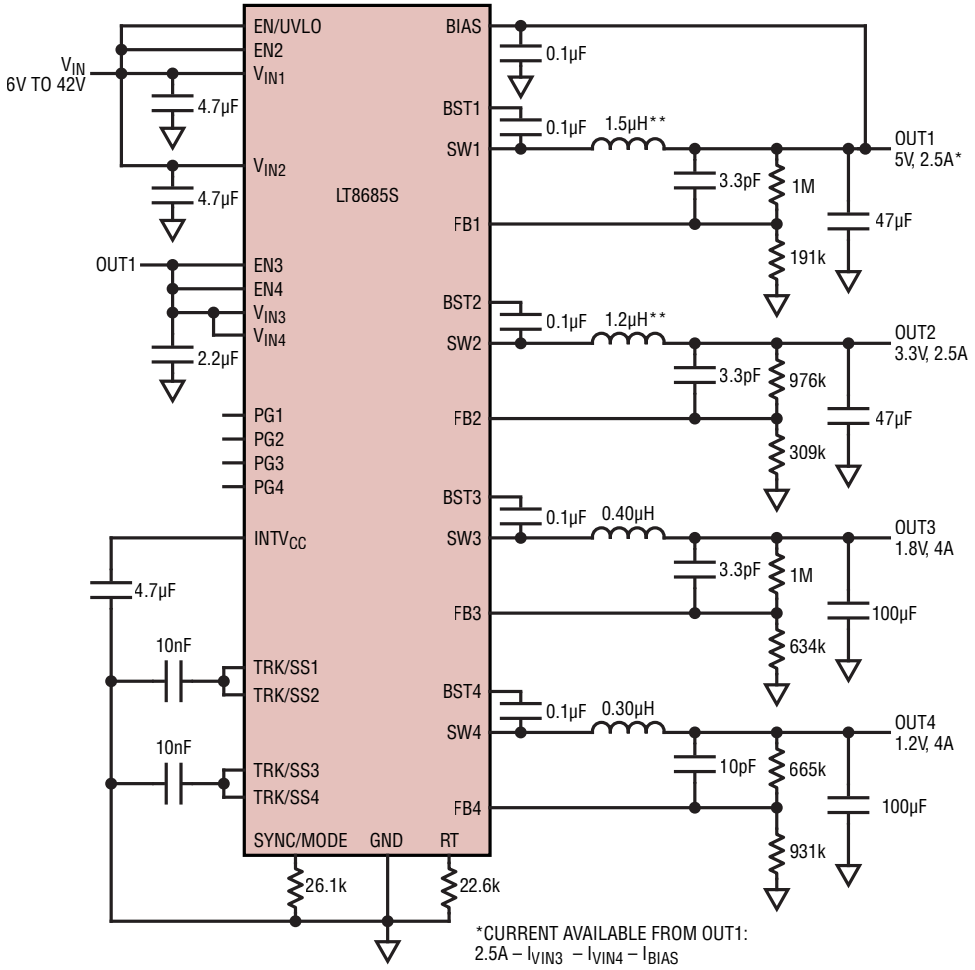


Figure 5. Maximum Loss vs Ambient Temperature

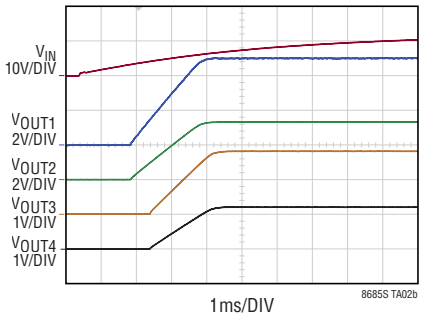
The LT8685S contains an internal thermal shutdown feature that will stop switching if the die temperature rises to approximately 177°C. Switching will resume when the temperature falls approximately 5°C. This feature is not production tested and is intended as a failsafe only.

TYPICAL APPLICATIONS

42V Input, Quad Output 2MHz Step-Down Regulator with Spread Spectrum and Ratiometric Output Start-Up (Details of Front Page Application)



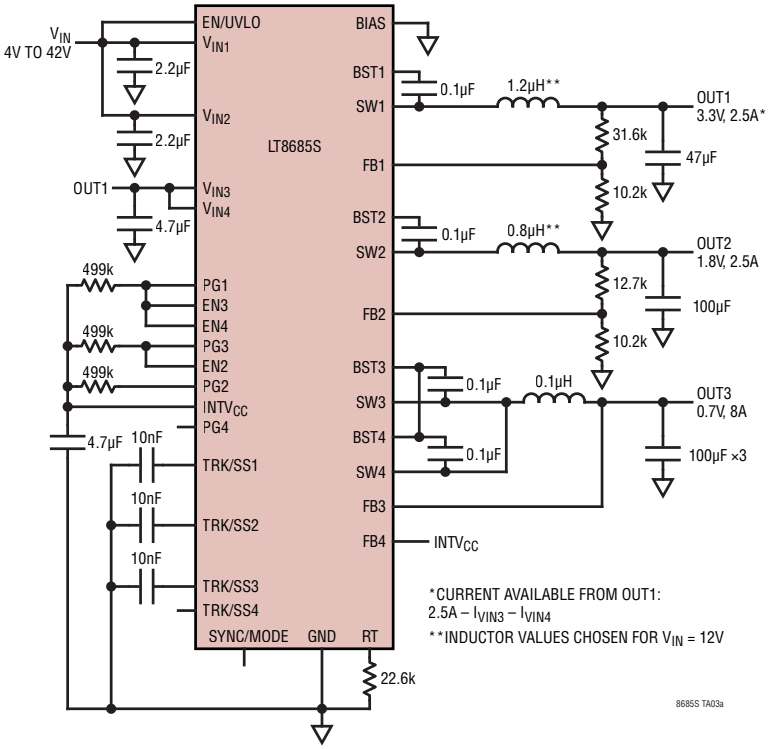
Startup Sequence



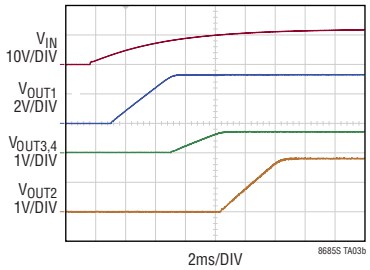
STARTUP SEQUENCE:
V_{IN} HIGH ENABLES HV CHANNELS
HV CHANNELS TRACK RATIOMETRICALLY
V_{OUT1} HIGH ENABLES LV CHANNELS
LV CHANNELS TRACK RATIOMETRICALLY

TYPICAL APPLICATIONS

Compact Microcontroller Power Supply with Supply Sequencing

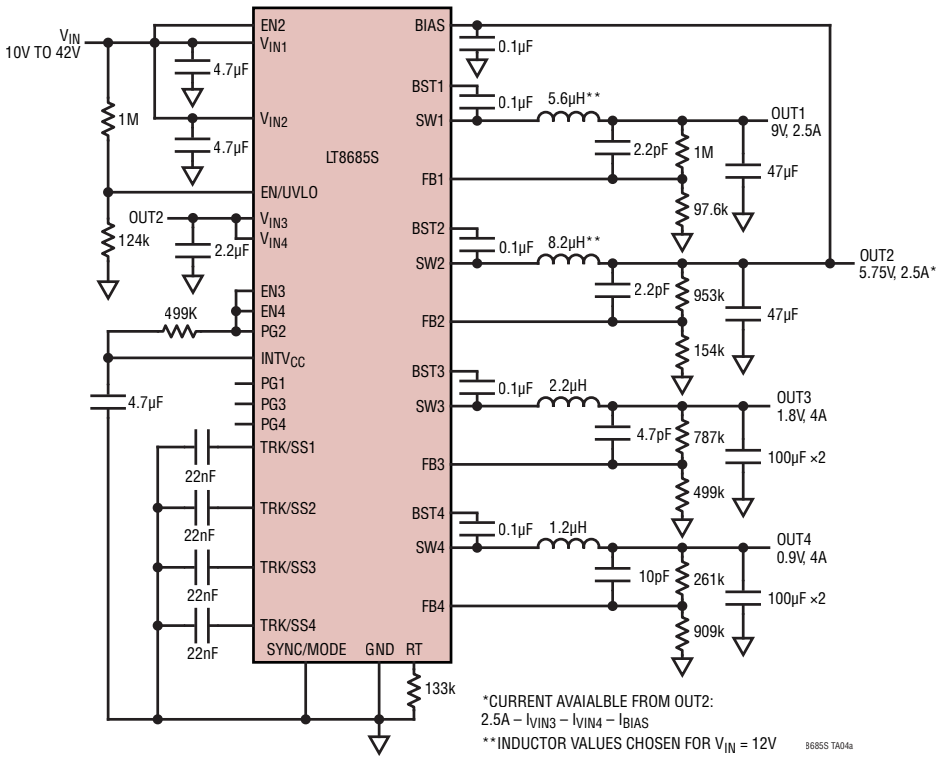


Startup Sequencing

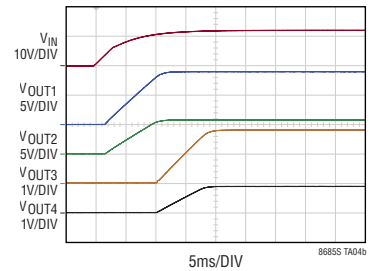


STARTUP SEQUENCE:
V_{IN} HIGH ENABLES OUT1
V_{OUT1} IN REGULATION ENABLES OUT3,4
$V_{OUT3,4}$ IN REGULATION ENABLES OUT2

High Efficiency Quad Output Regulator Suitable for Driving Multiple LDO's or Remote Circuitry



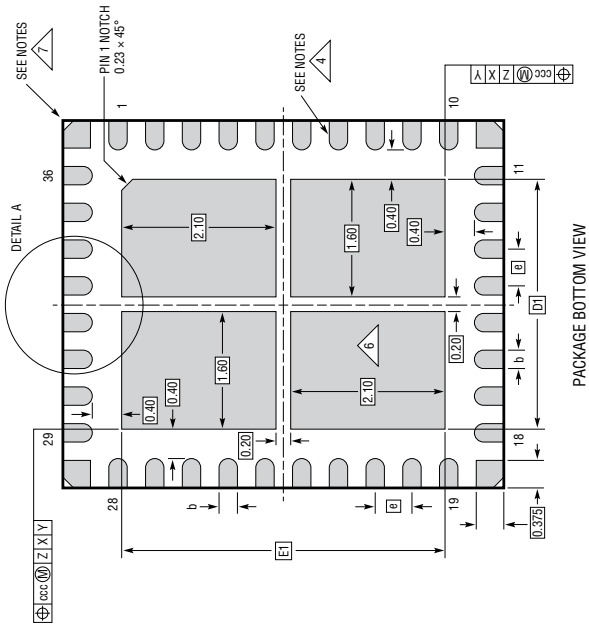
Startup Sequencing



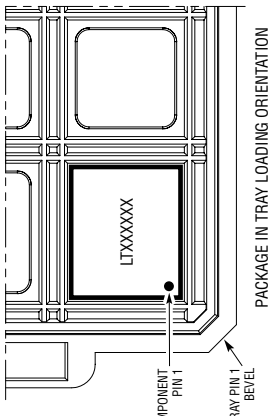
STARTUP SEQUENCE:
V_{IN} HIGH ENABLES OUT1 AND OUT2
V_{OUT2} IN REGULATION ENABLES OUT3 AND OUT4

PACKAGE DESCRIPTION

LQFN Package
36-Lead (5mm × 6mm × 0.95mm)
(Reference LTC DWG # 05-08-7056 Rev Ø)

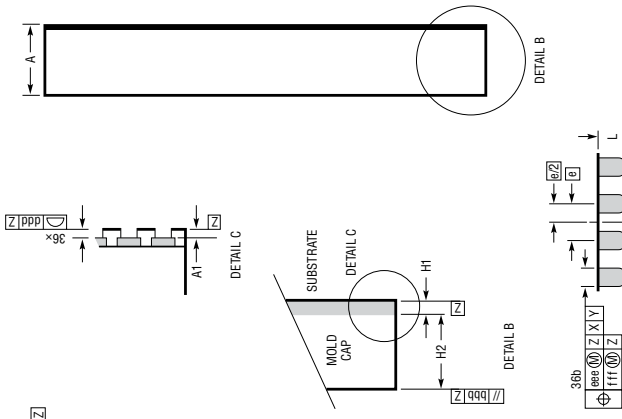


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
6. THE EXPOSED HEAT FEATURE IS SEGMENTED AND ARRANGED IN A MATRIX FORMAT. IT MAY HAVE OPTIONAL CORNER RADII ON EACH SEGMENT
7. CORNER SUPPORT PAD CHAMFER IS OPTIONAL

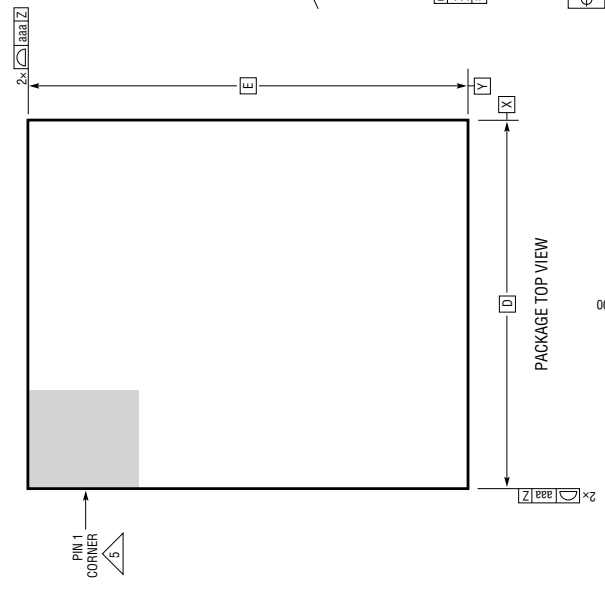


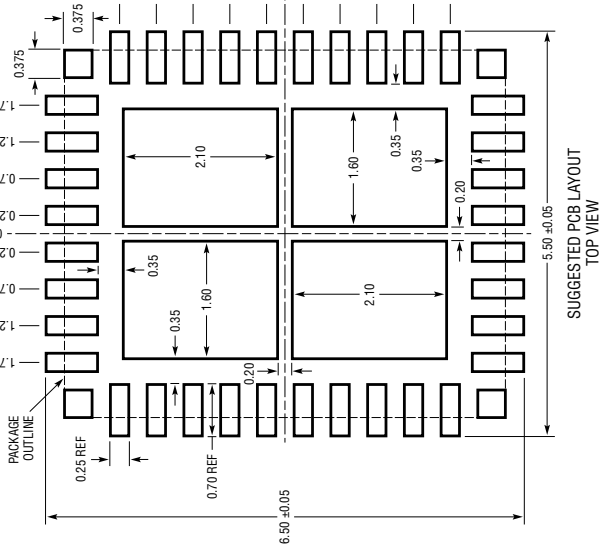
PACKAGE IN TRAY LOADING ORIENTATION

LQFN 36 1020 REV Ø



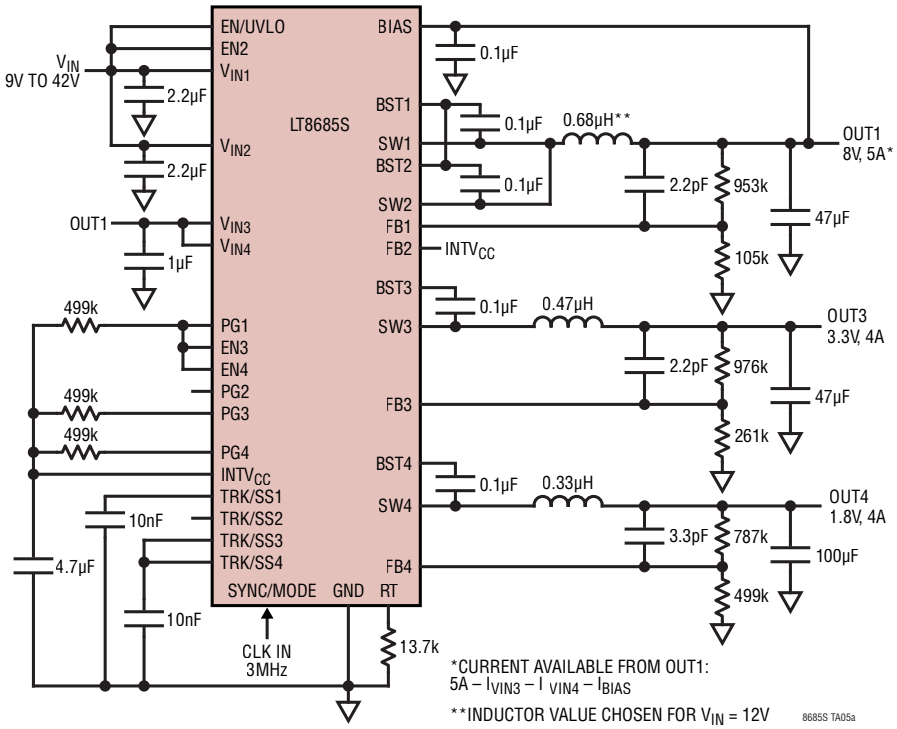
DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	0.85	0.95	1.05	
A1			0.04	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		5.00		
E		6.00		
D1		3.40		
E1		4.40		
e		0.50		
H1		0.25 REF		SUBSTRATE THK
H2		0.70 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	



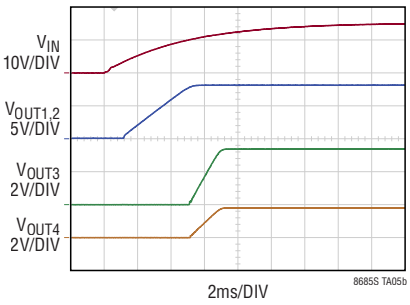


TYPICAL APPLICATION

Triple Output, 3MHz Step-Down Regulator with Sequenced Ratiometric Start-Up



Startup Sequencing



1A LOAD PER OUTPUT
STARTUP SEQUENCE:
VIN HIGH ENABLES OUT1,2
$V_{OUT1,2}$ IN REGULATION ENABLES OUT3 AND OUT4
V_{OUT3} AND V_{OUT4} SOFT-START RATIOMETRICALLY

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8601	42V, 94% Efficiency, 2.2MHz Triple Output (1.5A + 2.5A + 1.8A) Synchronous Micropower Step-Down DC/DC Converter with I_Q = 30µA	V_{IN}: 3V to 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 30µA, I_{SD} < 25µA, 6mm × 6mm QFN-40 Package
LT8602	42V, Quad Output (2.5A + 1.5A + 1.5A + 1.5A) 95% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 25µA	V_{IN}: 3V to 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 25µA, I_{SD} < 25µA, 6mm × 6mm QFN-40 Package
LT8603	42V, Low I_Q, Quad Output Triple Monolithic Buck Converter and Boost Controller	V_{IN}: 3V to 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 25µA, I_{SD} < 25µA, 6mm × 6mm QFN-40 Package