

3 Half-Bridge Gate-Drive IC

FAN7888



SOIC-20, 300 mils
CASE 751BJ-01

Description

The FAN7888 is a monolithic three half-bridge gate-drive IC designed for high-voltage, high-speed driving MOSFETs and IGBTs operating up to +200 V.

onsemi's high-voltage process and common-mode noise canceling technique provide stable operation of high-side drivers under high-dv/dt noise circumstances.

An advanced level-shift circuit allows high-side gate driver operation up to $V_S = -9.8$ V (typical) for $V_{BS} = 15$ V.

The UVLO circuits prevent malfunction when V_{DD} and V_{BS} are lower than the specified threshold voltage.

Output drivers typically source/sink 350 mA / 650 mA, respectively, which is suitable for three-phase half-bridge applications in motor drive systems.

Features

- Floating Channel for Bootstrap Operation to +200 V
- Typically 350 mA / 650 mA Sourcing/Sinking Current Driving Capability for All Channels
- 3 Half-Bridge Gate Driver
- Extended Allowable Negative V_S Swing to -9.8 V for Signal Propagation at $V_{BS} = 15$ V
- Matched Propagation Delay Time Maximum: 50 ns
- 3.3 V and 5 V Input Logic Compatible
- Built-in Shoot-Through Prevention Circuit for All Channels with 270 ns Typical Dead Time
- Built-in Common Mode dv/dt Noise Canceling Circuit
- Built-in UVLO Functions for All Channels
- This Device is Pb-Free, Halide Free and is RoHS Compliant

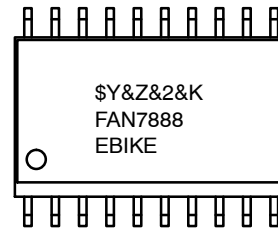
Applications

- Battery Based Motor Applications (E-bike, Power Tool)
- 3-Phase Motor Inverter Driver

Related Resources

- [AN-6076](#) – Design and Application Guide of Bootstrap Circuit for High-Voltage Gate-Drive IC
- [AN-9052](#) – Design Guide for Selection of Bootstrap Components
- [AN-8102](#) – Recommendations to Avoid Short Pulse Width Issues in HVIC Gate Driver Applications

MARKING DIAGRAM



- \$Y = Logo
- &Z = Assembly Plant Code
- &2 = 2-Digit Date Code
- &K = 2-Digits Lot Run Traceability Code
- FAN7888 = Specific Device Code
- EBIKE = 3rd Line Marking

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

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TYPICAL APPLICATION CIRCUIT

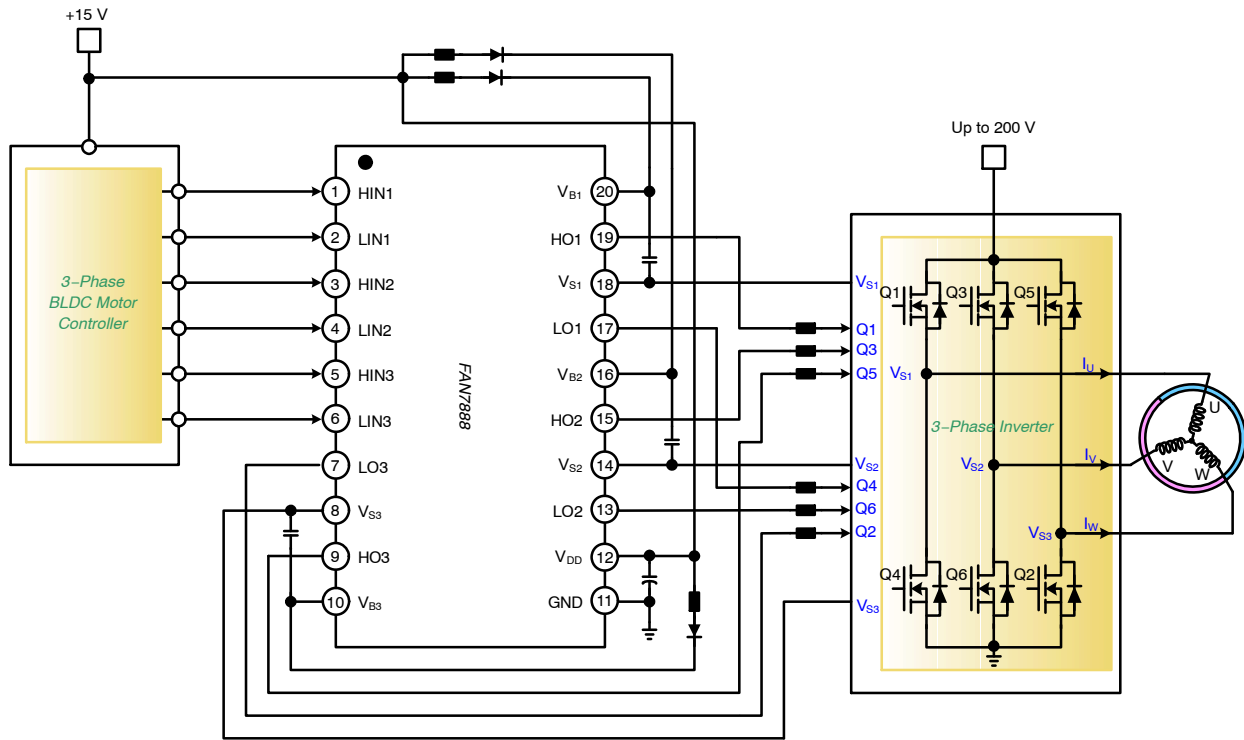


Figure 1. 3-Phase BLDC Motor Drive Application

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INTERNAL BLOCK DIAGRAM

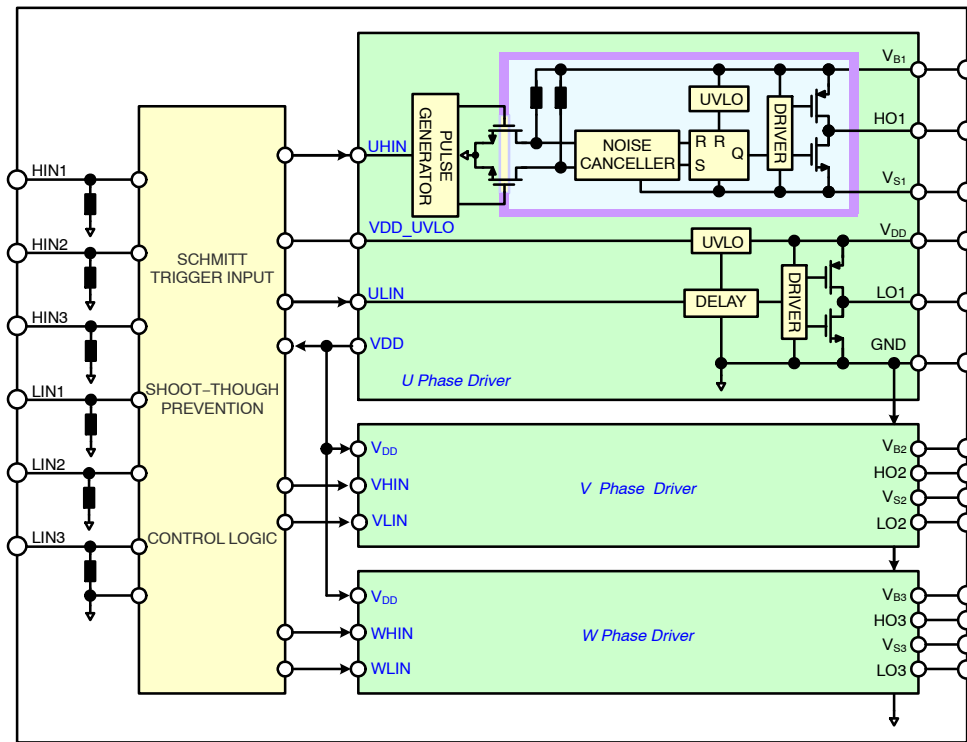


Figure 2. Functional Block Diagram

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PIN CONFIGURATION

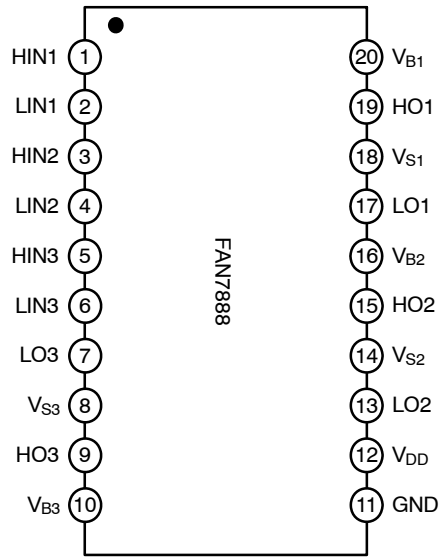


Figure 3. Pin Configuration (Top View)

PIN DEFINITIONS

| Pin No. | Name | Description |
|---------|------|--|
| 1 | HIN1 | Logic input 1 for high-side gate 1 driver |
| 2 | LIN1 | Logic input 1 for low-side gate 1 driver |
| 3 | HIN2 | Logic input 2 for high-side gate 2 driver |
| 4 | LIN2 | Logic input 2 for low-side gate 2 driver |
| 5 | HIN3 | Logic input 3 for high-side gate 3 driver |
| 6 | LIN3 | Logic input 3 for low-side gate 3 driver |
| 7 | LO3 | Low-side gate driver 3 output |
| 8 | VS3 | High-side driver 3 floating supply offset voltage |
| 9 | HO3 | High-side driver 3 gate driver output |
| 10 | VB3 | High-side driver 3 floating supply voltage |
| 11 | GND | Ground |
| 12 | VDD | Logic and all low-side gate drivers power supply voltage |
| 13 | LO2 | Low-side gate driver 2 output |
| 14 | VS2 | High-side driver 2 floating supply offset voltage |
| 15 | HO2 | High-side driver 2 gate driver output |
| 16 | VB2 | High-side driver 2 floating supply voltage |
| 17 | LO1 | Low-side gate driver 1 output |
| 18 | VS1 | High-side driver 1 floating supply offset voltage |
| 19 | HO1 | High-side driver 1 gate driver output |
| 20 | VB1 | High-side driver 1 floating supply voltage |

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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

| Symbol | Parameter | Min | Max | Unit |
|----------------------|---|---------------------------|---------------------------|------|
| V _B | High-Side Floating Supply Voltage of V _{B1,2,3} | -0.3 | 225.0 | V |
| V _S | High-Side Floating Supply Offset Voltage of V _{S1,2,3} | V _{B1,2,3} - 25 | V _{B1,2,3} + 0.3 | V |
| V _{HO1,2,3} | High-Side Floating Output Voltage | V _{S1,2,3} - 0.3 | V _{B1,2,3} + 0.3 | V |
| V _{DD} | Low-Side and Logic-fixed Supply Voltage | -0.3 | 25.0 | V |
| V _{LO1,2,3} | Low-Side Output Voltage | -0.3 | V _{DD} + 0.3 | V |
| V _{IN} | Logic Input Voltage (HIN1,2,3 and LIN1,2,3) | -0.3 | V _{DD} + 0.3 | V |
| dV _S /dt | Allowable Offset Voltage Slew Rate | - | 50 | V/ns |
| P _D | Power Dissipation (Note 1) (Note 2) (Note 3) | - | 1.47 | W |
| θ _{JA} | Thermal Resistance, Junction-to-ambient | - | 85 | °C/W |
| T _J | Junction Temperature | - | +150 | °C |
| T _{STG} | Storage Temperature | -55 | +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR-4 glass epoxy material).
2. Refer to the following standards:
 JESD51-2: Integral circuits thermal test method environmental conditions – natural convection.
 JESD51-3: Low effective thermal conductivity test board for leaded surface-mount packages.
3. Do not exceed P_D under any circumstances.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|----------------------|---|--------------------------|--------------------------|------|
| V _{B1,2,3} | High-Side Floating Supply Voltage | V _{S1,2,3} + 10 | V _{S1,2,3} + 20 | V |
| V _{S1,2,3} | High-Side Floating Supply Offset Voltage | 6 - V _{DD} | 200 | V |
| V _{DD} | Supply Voltage | 10 | 20 | V |
| V _{HO1,2,3} | High-Side Output Voltage | V _{S1,2,3} | V _{B1,2,3} | V |
| V _{LO1,2,3} | Low-Side Output Voltage | GND | V _{DD} | V |
| V _{IN} | Logic Input Voltage (HIN1,2,3 and LIN1,2,3) | GND | V _{DD} | V |
| T _A | Ambient Temperature | -40 | +125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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ELECTRICAL CHARACTERISTICS (V_{BIAS} (V_{DD} , $V_{BS1,2,3}$) = 15.0 V, T_A = 25°C, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to GND. The V_O and I_O parameters are referenced to GND and $V_{S1,2,3}$ and are applicable to the respective outputs LO1,2,3 and HO1,2,3.)

| Symbol | Characteristics | Condition | Min | Typ | Max | Unit |
|--------|-----------------|-----------|-----|-----|-----|------|
|--------|-----------------|-----------|-----|-----|-----|------|

LOW-SIDE POWER SUPPLY SECTION

| | | | | | | |
|----------------|--|------------------------------------|-----|-----|-----|---------|
| I_{QDD} | Quiescent V_{DD} Supply Current | $V_{LIN1,2,3} = 0$ V or 5 V | – | 160 | 350 | μ A |
| $I_{PDD1,2,3}$ | Operating V_{DD} Supply Current for each Channel | $f_{LIN1,2,3} = 20$ kHz, rms Value | – | 500 | 900 | μ A |
| V_{DDUV+} | V_{DD} Supply Under-Voltage Positive-Going Threshold | $V_{DD} =$ Sweep, $V_{BS} = 15$ V | 7.2 | 8.2 | 9.0 | V |
| V_{DDUV-} | V_{DD} Supply Under-Voltage Negative-Going Threshold | $V_{DD} =$ Sweep, $V_{BS} = 15$ V | 6.8 | 7.8 | 8.5 | V |
| V_{DDHYS} | V_{DD} Supply Under-Voltage Lockout Hysteresis | $V_{DD} =$ Sweep, $V_{BS} = 15$ V | – | 0.4 | – | V |

BOOTSTRAPPED POWER SUPPLY SECTION

| | | | | | | |
|----------------|--|------------------------------------|-----|-----|-----|---------|
| $I_{QBS1,2,3}$ | Quiescent V_{BS} Supply Current for each Channel | $V_{HIN1,2,3} = 0$ V or 5 V | – | 50 | 120 | μ A |
| $I_{PBS1,2,3}$ | Operating V_{BS} Supply Current for each Channel | $f_{HIN1,2,3} = 20$ kHz, rms Value | – | 400 | 800 | μ A |
| V_{BSUV+} | V_{BS} Supply Under-Voltage Positive-going Threshold | $V_{DD} = 15$ V, $V_{BS} =$ Sweep | 7.2 | 8.2 | 9.0 | V |
| V_{BSUV-} | V_{BS} Supply Under-Voltage Negative-going Threshold | $V_{DD} = 15$ V, $V_{BS} =$ Sweep | 6.8 | 7.8 | 8.5 | V |
| V_{BSHYS} | V_{BS} Supply Under-Voltage Lockout Hysteresis | $V_{DD} = 15$ V, $V_{BS} =$ Sweep | – | 0.4 | – | V |
| I_{LK} | Offset Supply Leakage Current | $V_{B1,2,3} = V_{S1,2,3} = 200$ V | – | – | 10 | μ A |

GATE DRIVER OUTPUT SECTION

| | | | | | | |
|----------|---|---|-----|------|------|----|
| V_{OH} | High-Level Output Voltage, $V_{BIAS}-V_O$ | $I_O=20$ mA | – | – | 1.0 | V |
| V_{OL} | Low-Level Output Voltage, V_O | $I_O=20$ mA | – | – | 0.6 | V |
| I_{O+} | Output HIGH Short-Circuit Pulsed Current (Note 4) | $V_O = 0$ V, $V_{IN} = 5$ V with PW < 10 μ s | 250 | 350 | – | mA |
| I_{O-} | Output LOW Short-Circuit Pulsed Current (Note 4) | $V_O = 15$ V, $V_{IN} = 0$ V with PW < 10 μ s | 500 | 650 | – | mA |
| V_S | Allowable Negative V_S Pin Voltage for IN Signal Propagation to H_O | | – | –9.8 | –7.0 | V |

LOGIC INPUT SECTION (HIN, LIN)

| | | | | | | |
|-----------|---------------------------------------|----------------|-----|-----|-----|------------|
| V_{IH} | Logic “1” Input Voltage | | 2.5 | – | – | V |
| V_{IL} | Logic “0” Input Voltage | | – | – | 1.0 | V |
| I_{IN+} | Logic “1” Input Bias Current | $V_{IN} = 5$ V | – | 25 | 50 | μ A |
| I_{IN-} | Logic “0” Input Bias Current (Note 4) | $V_{IN} = 0$ V | – | – | 2.0 | μ A |
| R_{IN} | Input Pull-Down Resistance | | 100 | 200 | 300 | k Ω |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. This parameter is guaranteed by design.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{BIAS} (V_{DD} , $V_{BS1,2,3}$) = 15.0 V, $V_{S1,2,3} =$ GND, $C_{Load} = 1000$ pF unless otherwise specified.)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|-----------|--|--------------------|-----|-----|-----|------|
| t_{ON} | Turn-on Propagation Delay | $V_{S1,2,3} = 0$ V | – | 130 | 220 | ns |
| t_{OFF} | Turn-off Propagation Delay | $V_{S1,2,3} = 0$ V | – | 150 | 240 | ns |
| t_R | Turn-on Rise Time | | – | 50 | 120 | ns |
| t_F | Turn-off Fall Time | | – | 30 | 80 | ns |
| MT1 | Turn-on Delay Matching $t_{ON(H)} - t_{OFF(L)}$ | | – | – | 50 | ns |
| MT2 | Turn-off Delay Matching $t_{OFF(H)} - t_{ON(L)}$ | | – | – | 50 | ns |
| DT | Dead Time | | 100 | 270 | 440 | ns |
| MDT | Dead-time Matching $t_{DT1} - t_{DT2}$ | | – | – | 60 | ns |

TYPICAL CHARACTERISTICS

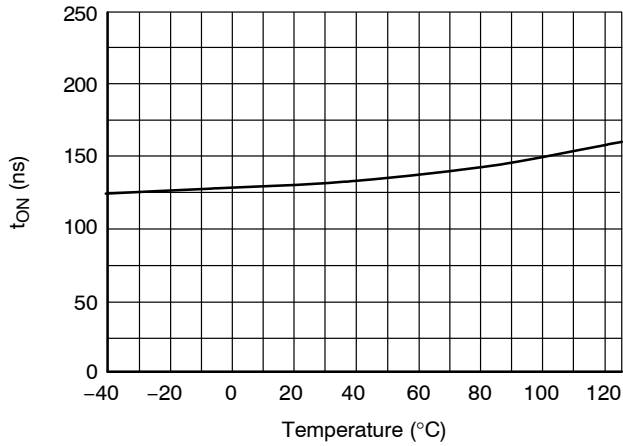


Figure 4. Turn-on Propagation Delay vs. Temperature

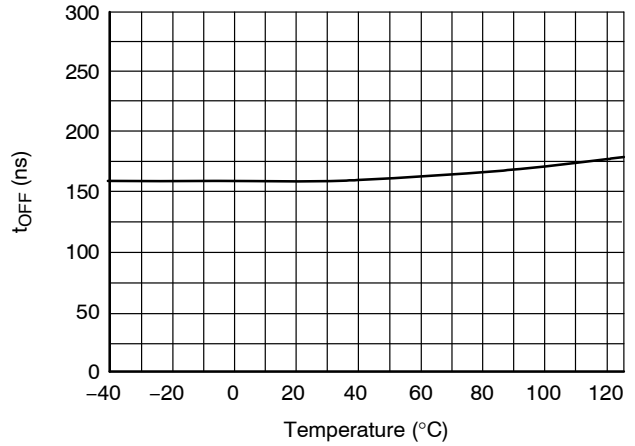


Figure 5. Turn-off Propagation Delay vs. Temperature

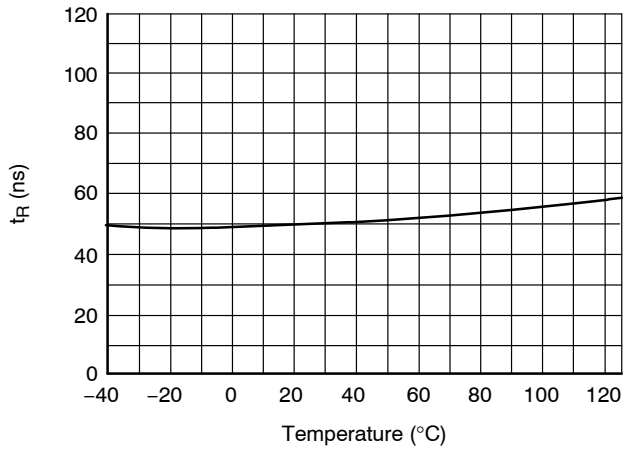


Figure 6. Turn-on Rise Time vs. Temperature

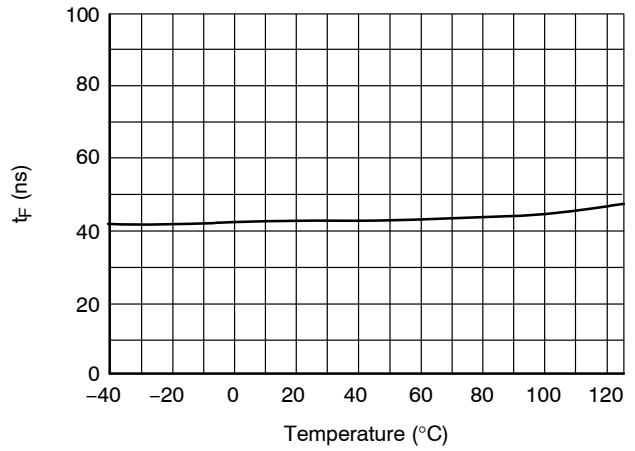


Figure 7. Turn-off Fall Time vs. Temperature

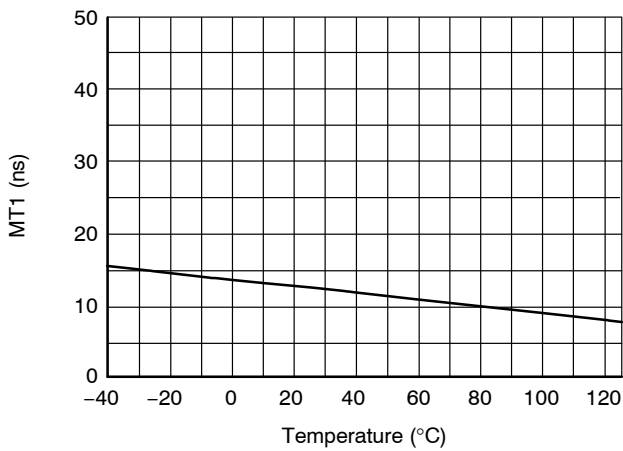


Figure 8. Turn-on Delay Matching vs. Temperature

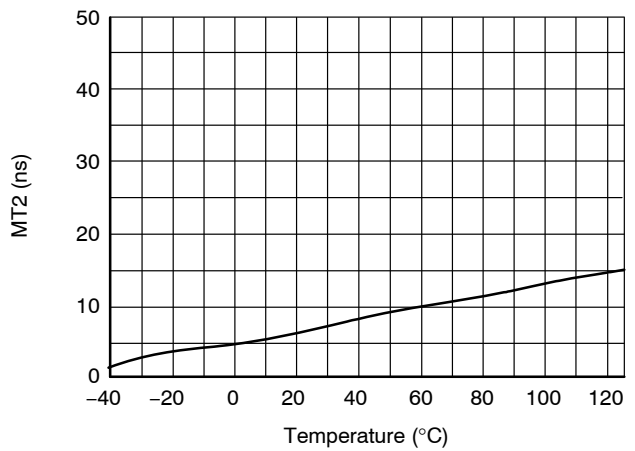


Figure 9. Turn-off Delay Matching vs. Temperature

TYPICAL CHARACTERISTICS (continued)

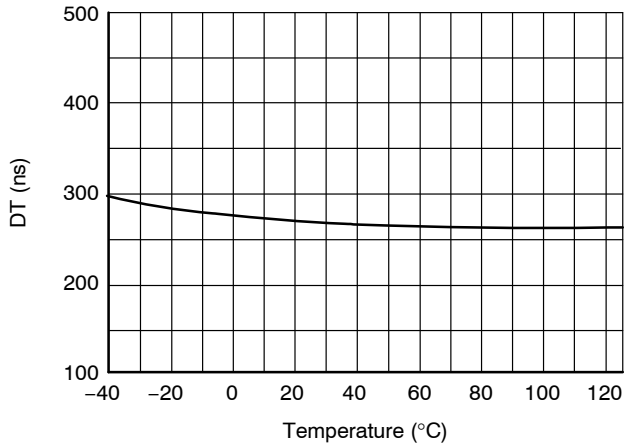


Figure 10. Dead Time vs. Temperature

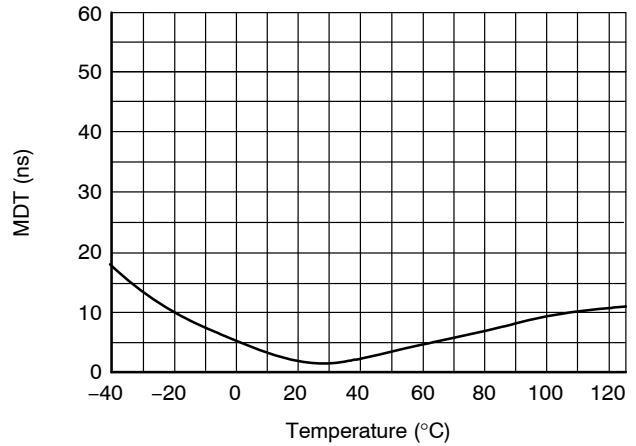


Figure 11. Dead-Time Matching vs. Temperature

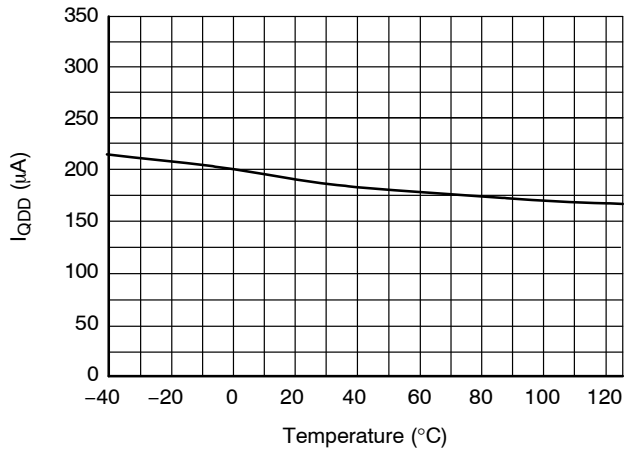


Figure 12. Quiescent V_{DD} Supply Current vs. Temperature

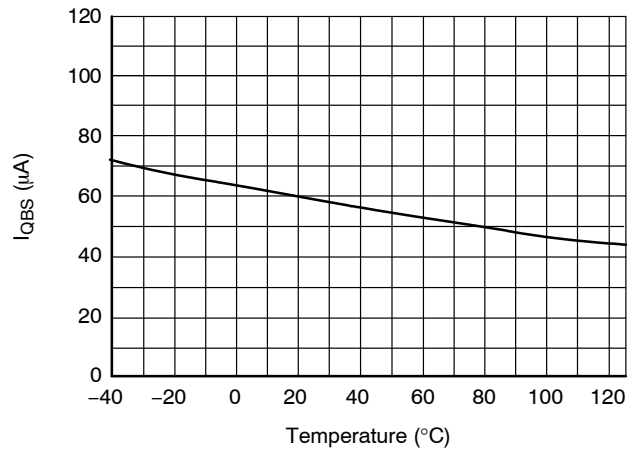


Figure 13. Quiescent V_{BS} Supply Current vs. Temperature

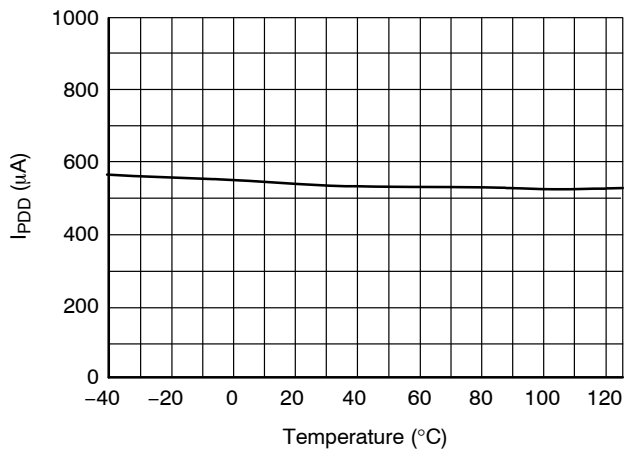


Figure 14. Operating V_{DD} Supply Current vs. Temperature

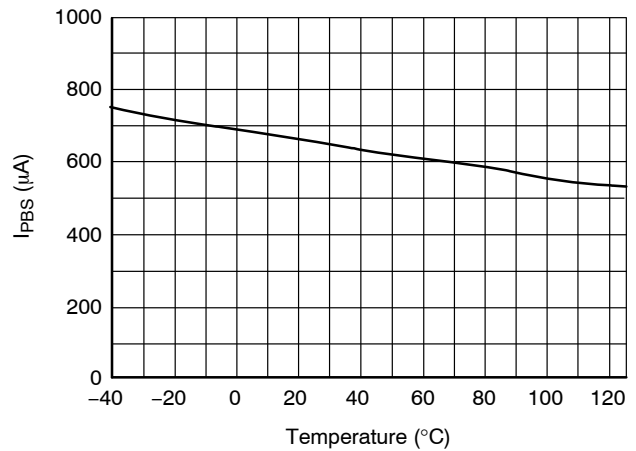


Figure 15. Operating V_{BS} Supply Current vs. Temperature

TYPICAL CHARACTERISTICS (continued)

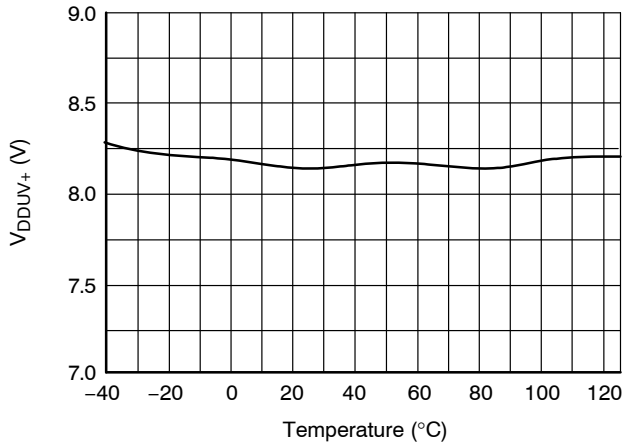


Figure 16. V_{DD} UVLO+ vs. Temperature

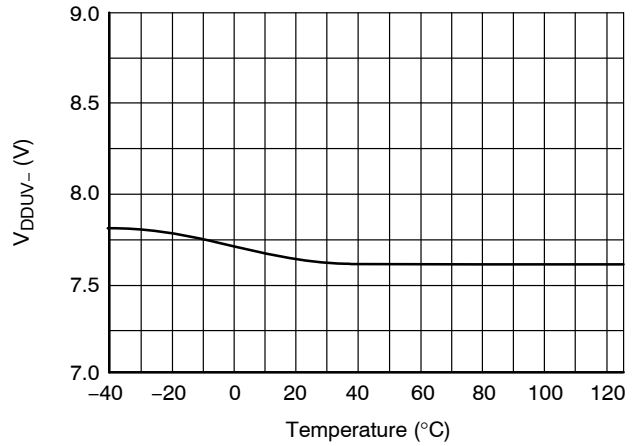


Figure 17. V_{DD} UVLO- vs. Temperature

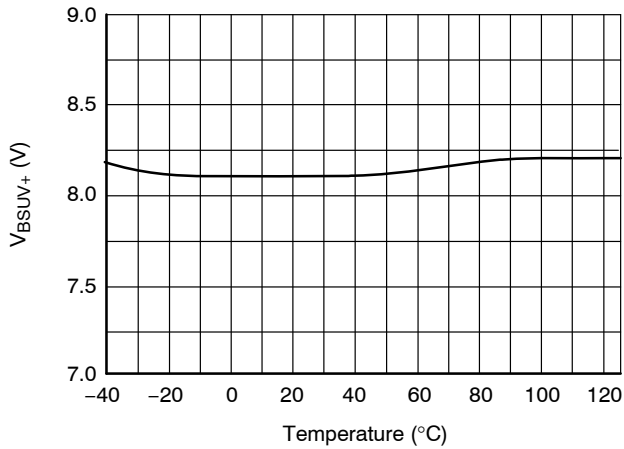


Figure 18. V_{BS} UVLO+ vs. Temperature

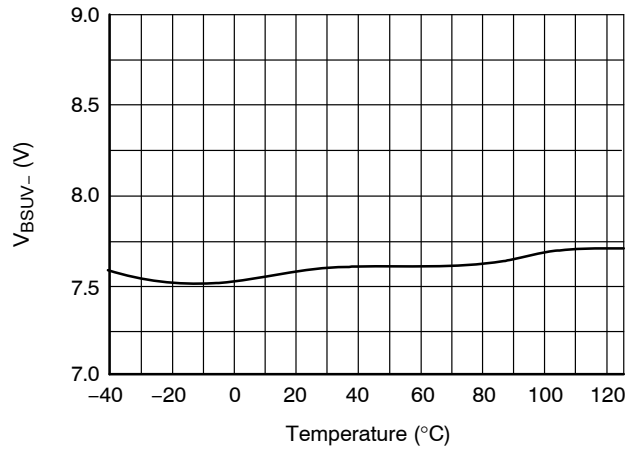


Figure 19. V_{BS} UVLO- vs. Temperature

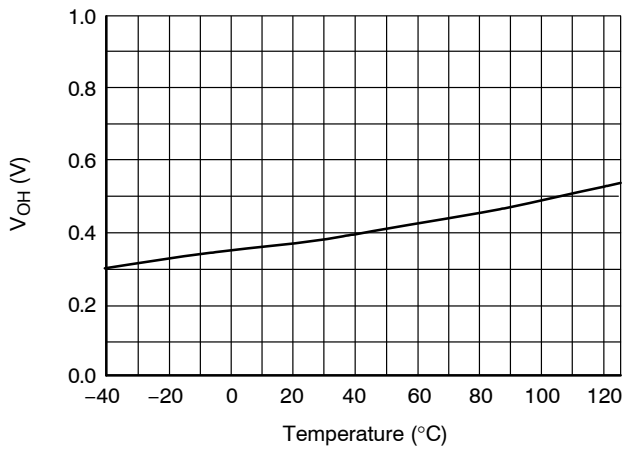


Figure 20. High-Level Output Voltage vs. Temperature

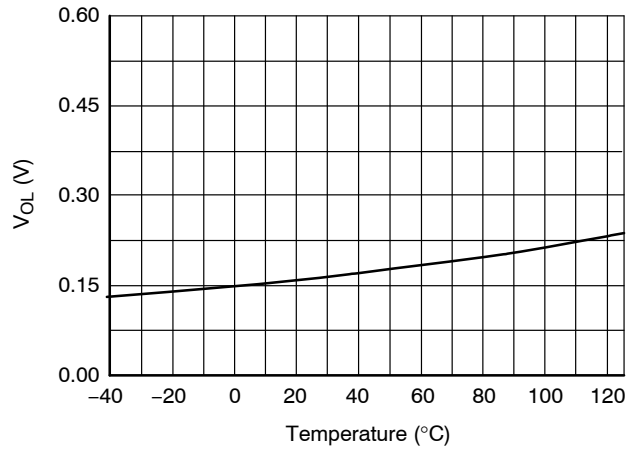


Figure 21. Low-Level Output Voltage vs. Temperature

TYPICAL CHARACTERISTICS (continued)

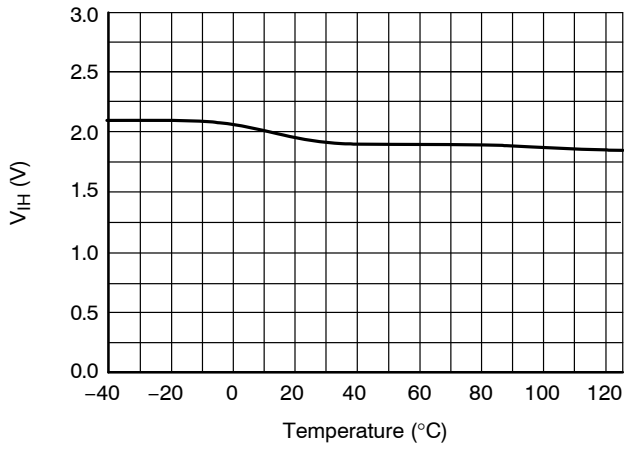


Figure 22. Logic High Input Voltage vs. Temperature

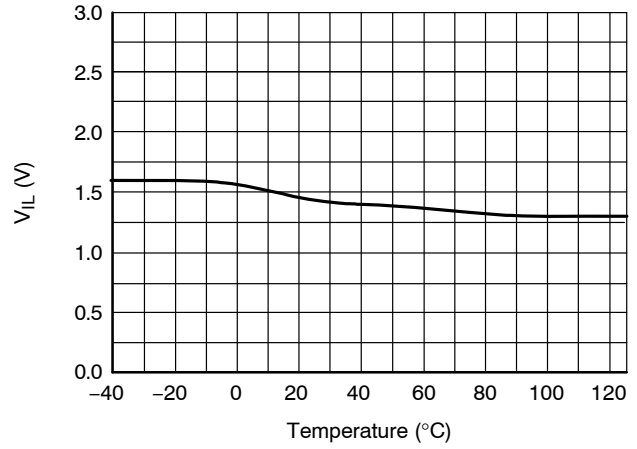


Figure 23. Logic Low Input Voltage vs. Temperature

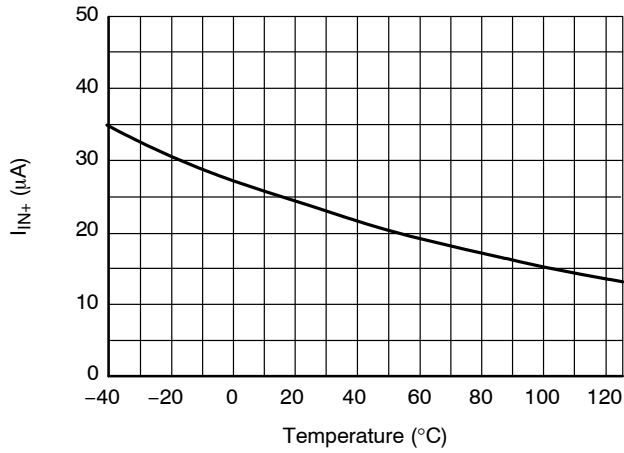


Figure 24. Logic Input High Bias Current vs. Temperature

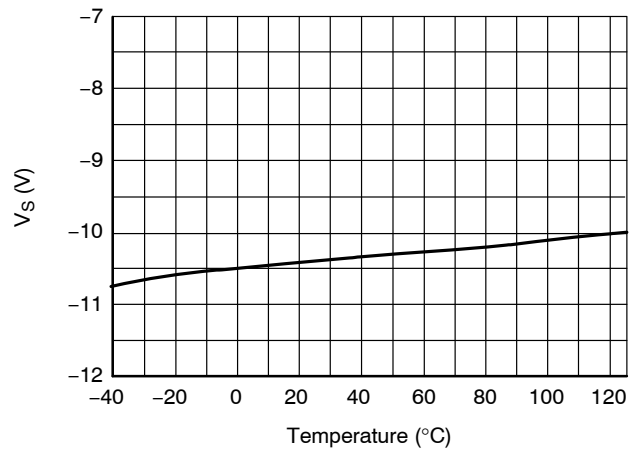


Figure 25. Allowable Negative V_S Voltage vs. Temperature

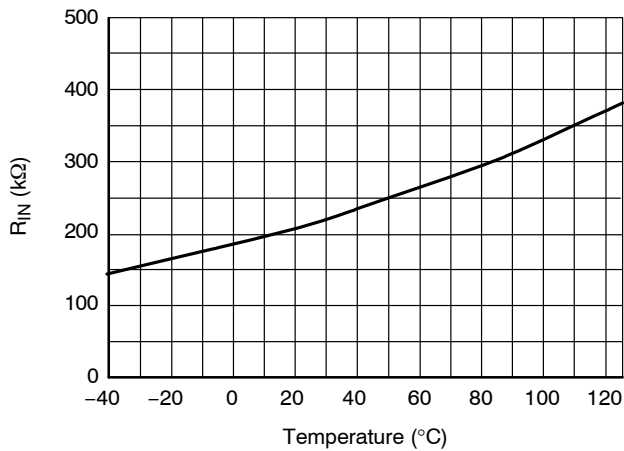


Figure 26. Input Pull-down Resistance vs. Temperature

APPLICATION INFORMATION

Protection Function

Under-Voltage Lockout (UVLO)

The high- and low-side drivers include under-voltage lockout (UVLO) protection circuitry for each channel that monitors the supply voltage (V_{DD}) and bootstrap capacitor voltage ($V_{BS1,2,3}$) independently. It can be designed prevent malfunction when V_{DD} and $V_{BS1,2,3}$ are lower than the specified threshold voltage. The UVLO hysteresis prevents chattering during power supply transitions.

Shoot-Through Prevention Function

The FAN7888 has shoot-through prevention circuitry monitoring the high- and low-side control inputs. It can be designed to prevent outputs of high and low side from turning on at same time, as shown Figure 27 and 28.

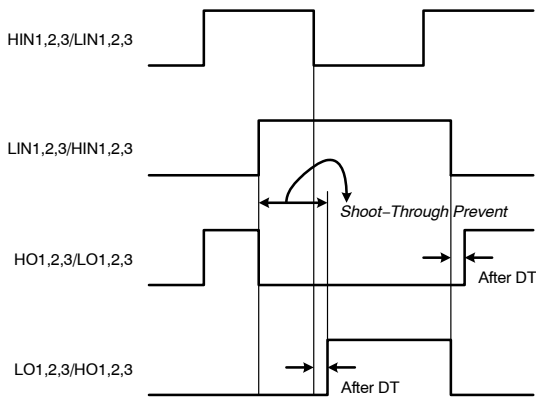


Figure 27. Waveforms for Shoot-Through Prevention

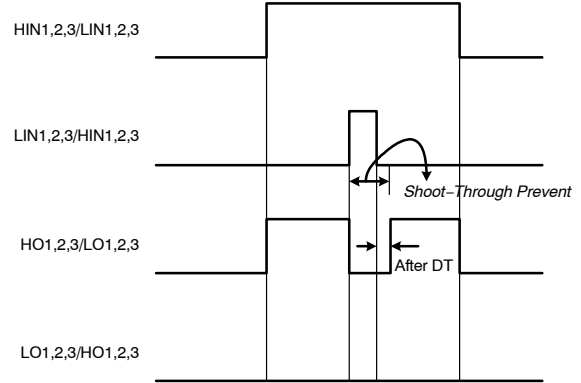


Figure 28. Waveforms for Shoot-Through Prevention

Operational Notes

The FAN7888 is a three half-bridge gate driver with internal, typical 270 ns dead-time for the three-phase brushless DC (BLDC) motor drive system, as shown in Figure 1.

Figure 29 shows a switching sequence of 120° electrical commutation for a three-phase BLDC motor drive system. The waveforms are idealized: they assumed that the generated back EMF waveforms are trapezoidal with flat tops of sufficient width to produce constant torque when the line currents are perfectly rectangular, 120° electrical degrees, with the switching sequence as shown in Figure 29. The operating waveforms of the wye-connection reveal that repeat every 60 electrical degrees, with each 60° segment being “commutated” to another phase, as shown in Figure 29.

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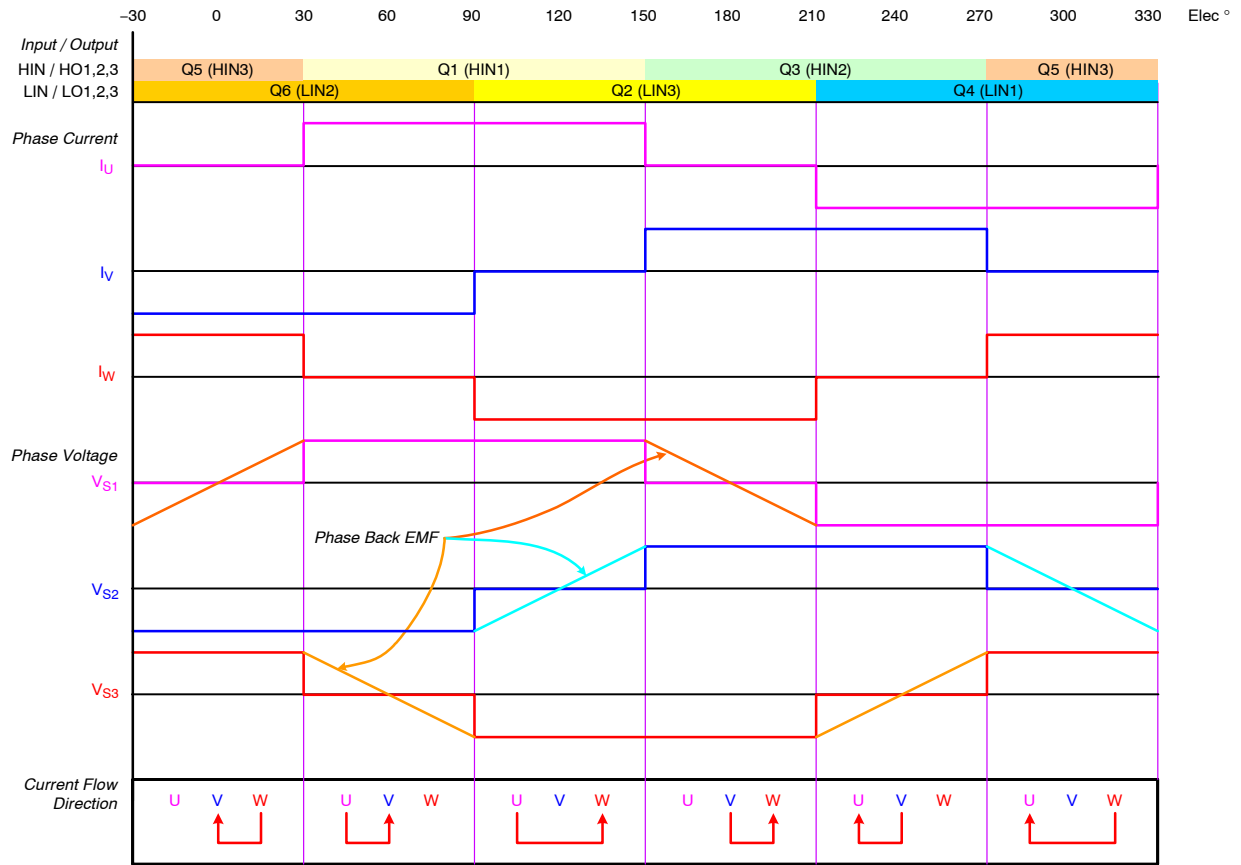


Figure 29. 120° Commutation Operation Waveforms for 3-Phase BLDC Motor Application

SWITCHING TIME DIAGRAM

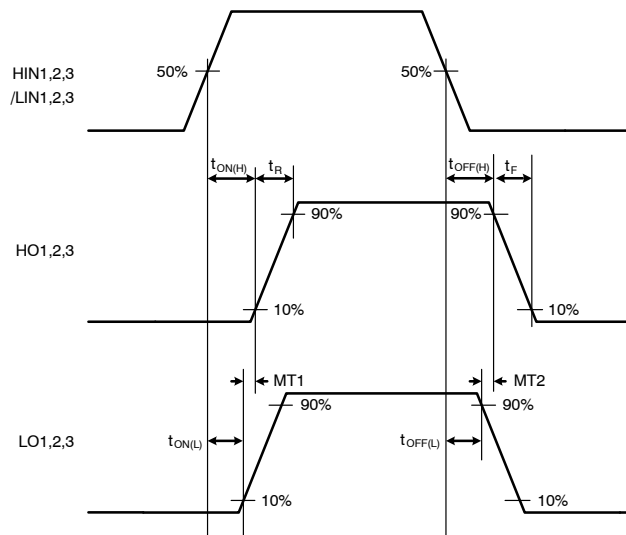


Figure 30. Switching Time Definition

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ORDERING INFORMATION

| Part Number | Package | Operating Temperature Range | Shipping [†] |
|-------------|---|-----------------------------|-----------------------|
| FAN7888MX | SOIC-20, 300 mils (Pb-Free, Halide Free) | -40°C to +125°C | 1000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

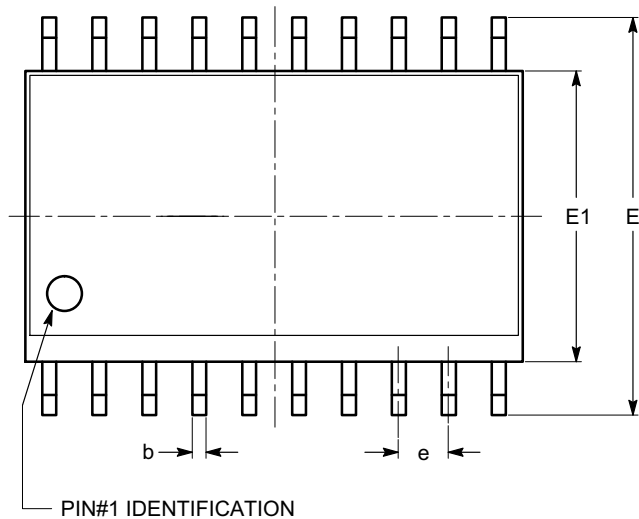
PACKAGE DIMENSIONS

ON Semiconductor®



SOIC-20, 300 mils
CASE 751BJ-01
ISSUE O

DATE 19 DEC 2008



TOP VIEW

| SYMBOL | MIN | NOM | MAX |
|------------|----------|-------|-------|
| A | 2.36 | 2.49 | 2.64 |
| A1 | 0.10 | | 0.30 |
| A2 | 2.05 | | 2.55 |
| b | 0.31 | 0.41 | 0.51 |
| c | 0.20 | 0.27 | 0.33 |
| D | 12.60 | 12.80 | 13.00 |
| E | 10.01 | 10.30 | 10.64 |
| E1 | 7.40 | 7.50 | 7.60 |
| e | 1.27 BSC | | |
| h | 0.25 | | 0.75 |
| L | 0.40 | 0.81 | 1.27 |
| θ | 0° | | 8° |
| $\theta 1$ | 5° | | 15° |



SIDE VIEW



END VIEW

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-013.

| | | |
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