National Semiconductor

October 2003

LP3945/LP3946
Battery Charge Management System

General Description

The LP3945 and LP3946 are complete charge management systems that safely charge and maintain a Li-Ion battery or a four-cell Ni-MH (LP3945 only) battery pack. The LP3945 offers the flexibility of programming charge current, battery regulation voltage (4.1V/4.2V), battery type (Li-Ion/Ni-MH), and End Of Charge (EOC) termination through the use of I^2C interface. On the LP3946, these parameters are programmed at the factory per customer specification.

The pass transistor, charge current sensing resistor and charge current setting resistors are all integrated inside the LP3945 and LP3946. This eliminates the use of external components and significantly reduces design time and board space.

The LP3945 and LP3946 operate in four modes: prequalification, constant current, constant voltage and maintenance modes. The LP3945 features Ni-MH charging mode as well. The charger has under-voltage and over-voltage protection as well as an internal 5.6 hr timer to prevent overcharging the battery. There are two open drain outputs for status indication. An internal amplifier readily converts the charge current into a voltage. Also, the charger can operate in an LDO mode providing up to 1 Amp to the load.

Features

- Integrated pass transistor
- Does not require external charge current setting or sensing resistors
- I^2C interface (LP3945 only) — programmable charge current, EOC current and battery regulation voltage
- Near-depleted battery preconditioning
- Built-in 5.6 hour timer
- Under voltage and over voltage lockout on adaptor
- Charge status indicators
- Charge current monitor analog output
- LDO mode operation can source 1 amp
- Continuous over current/temperature protection

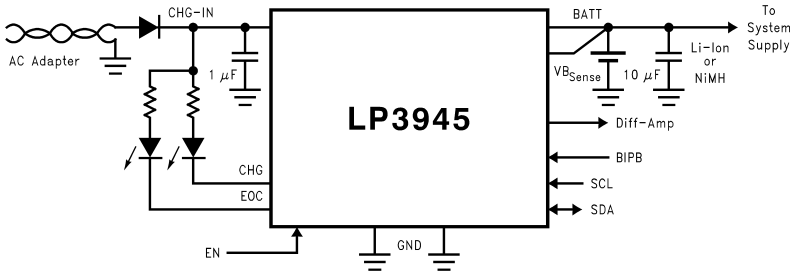
Key Specifications

- 1% charger voltage accuracy over $0^\circ C \le T_J \le 85^\circ C$
- 4.5V to 6.0V input voltage range
- LLP package power dissipation: 2.7W at $T_A = 25^\circ C$

Applications

- Cellular phones
- PDAs
- Digital cameras
- USB powered devices
- Programmable current sources

Typical Application Circuit



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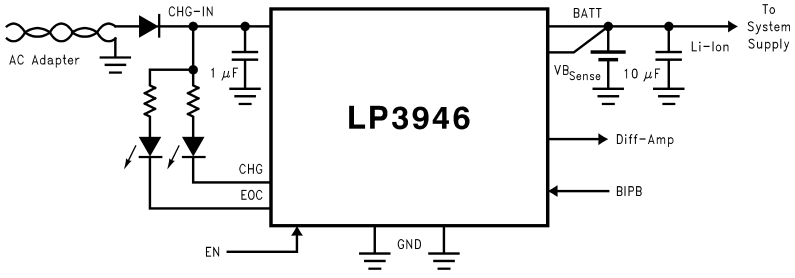

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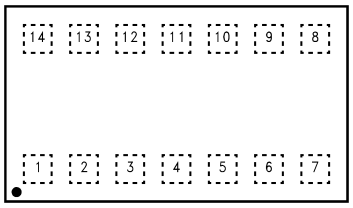
LP3945/LP3946 LLP14 Package Drawing



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(TOP VIEW)
See NS Package Number LDA14A

LP3945/LP3946 Pin Description

Pin #	LP3945	LP3946	Description
1	EN	EN	Charger Enable Input. Internally pulled high to CHG-IN pin.
2	SCL	GND	Serial Interface Clock Input for LP3945. Ground in LP3946.
3	SDA	GND	Serial Interface DATA Input/Output for LP3945. Ground in LP3946.
4	BATT	BATT	Battery supply input terminal. Must have 10 µF ceramic capacitor to GND.
5	V_{BG}	V_{BG}	Bandgap Voltage Reference (1.225V). Factory test point. Must be left floating.
6	VB_{SENSE}	VB_{SENSE}	Battery Voltage Sense connected to the + terminal of the battery.
7	GND	GND	Digital Ground
8	Diff-Amp	Diff-Amp	Charge current monitoring differential amplifier output. Voltage output representation of the charge current.
9	BIPB	BIPB	Battery in Place Bar. Input signal to indicate presence/absence of the battery. Internally pulled high to CHG-IN. Pulled low by the Battery ID resistor. Absence of the ID resistor (BIPB signal high) indicates no battery. Pulling BIPB pin high sets the device to LDO mode.
10	EOC	EOC	Active Low Open Drain Output to drive Green LED. Active when wall adaptor is connected and battery is fully charged. Regardless of the battery chemistry, this signal is available whenever a battery is attached.
11	GND	GND	Analog Ground
12	CHG	CHG	Active Low Open Drain Output to drive Red LED. Active when wall adaptor is connected and battery is being charged. Regardless of the battery chemistry, this signal is available whenever a battery is attached.
13	StopModeEN	StopModeEN	For normal operation, this pin must be left floating. Pulling this pin to ground will bypass the 5.6 Hrs safety timer in constant current mode. See "StopModeEN PIN" Section for more detail. **WARNING! Disabling the timer is not a recommended operating condition since it disables the safety timer function. User must provide protection against continuously charging a defective battery.**
14	CHG-IN	CHG-IN	Charger input from a regulated, current limited power source. Must have a 1 µF ceramic capacitor to GND.

Ordering Information

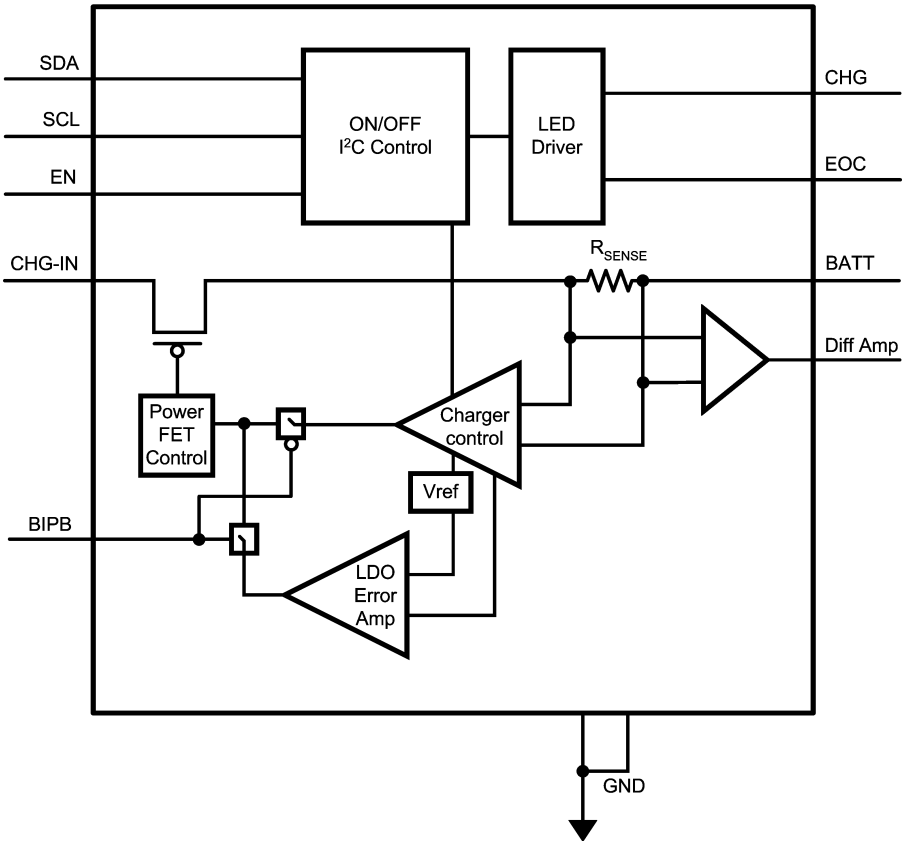
LP3945 supplied as 1000 units Tape and Reel	LP3945 supplied as 4500 units Tape and Reel	Package Marking
LP3945ILD	LP3945ILDX	L00011B

LP3946 supplied as 1000 units Tape and Reel	LP3946 supplied as 4500 units Tape and Reel	Package Marking
LP3946ILD	LP3946ILDX	L00030B

The LP3946 has default values of I_{CHG}=500mA, V_{BATT}=4.1V and EOC=0.1C. For other default options, please contact National Semiconductor Sales Office.

Block Diagram

LP3945 Functional Block Diagram



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Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

CHG-IN	−0.3V to +6.5V
BATT, VB_{SENSE}, SDA, SCL, EOC, CHG, EN, BIPB, StopModeEN	−0.3V to +6V
Junction Temperature	150˚C
Storage Temperature	−65˚C to +150˚C
Power Dissipation (Note 3)	1.76W
ESD (Note 4)	
Human Body Model	2kV
Machine Model	200V

Operating Ratings (Notes 1, 2)

CHG-IN	3.0V to 6.0V
EN, BIPB, StopModeEN	0V to (V_{CHG-IN}+0.3V)
Junction Temperature, T_J	−40˚C to +125˚C
Operating Temperature, T_A	−40˚C to +85˚C
Thermal Resistance, θ_{JA}	37˚C/W
Maximum Power Dissipation (T_A = 85˚C, (Note 5))	1.08W

Electrical Characteristics

Unless otherwise noted, V_{CHG-IN} = 5V, V_{BATT} = 4V, C_{CHG-IN} = 1µF, C_{BATT} = 10µF. Typical values and limits appearing in normal type apply for T_J = 25˚C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40˚C to +85˚C. (Notes 6, 7, 8)

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
V_{CC} SUPPLY						
V_{CHG-IN}	Input Voltage Range			**4.5**	**6**	V
	Operating Range	Battery Connected		**4.5**	**6**	
I_{BATT}	Battery Leakage Current	$V_{CHG-IN} \leq 4V$	2		**20**	µA
		EOC = Low, adaptor connected, V_{BATT} = 4.1V	50		**150**	µA
$V_{OK-TSHD}$	Adapter OK Trip Point (CHG-IN)	V_{CHG-IN} - V_{BATT} (Rising)	60			mV
		V_{CHG-IN} - V_{BATT} (Falling)	50			mV
$V_{UVLO-TSHD}$	Under Voltage Lock-out Trip Point	V_{CHG-IN} (Rising)	4.15	**3.8**	**4.5**	V
		V_{CHG-IN} (Falling)	3.95	**3.6**	**4.3**	V
$V_{OVLO-TSHD}$	Over Voltage Lock-out Trip Point	V_{CHG-IN} (Rising)	5.9			V
		V_{CHG-IN} (Falling)	5.7			
	Thermal Shutdown Temperature	(Note 7)	160			˚C
	Thermal Shutdown Hysteresis		20			˚C
BATTERY CHARGER—Li ION MODE (MODE = LOW)						
I_{CHG}	Fast Charge Current Range			**500**	**950**	mA
	Fast Charge Current Accuracy			**−10**	**+10**	%
	Programmable Charging Current Step		50			mA
$I_{PRE-CHG}$	Pre-Charge Current	V_{BATT} = 2V		**50**	**65**	mA
I_{EOC}	End Of Charge Current Accuracy	For I_{EOC} = 0.1C, 0.15C or 0.2C		**+20**	**−20**	%
V_{BATT}	Battery Regulation Voltage (For 4.1V Cell) (Default State)	T_J = 0˚C to +85˚C, I_{CHARGE} = 10 mA, Mode = Low	4.1	**4.059**	**4.141**	V
		T_J = −40˚C to +85˚C, I_{CHARGE} = 10 mA, Mode = Low	4.1	**4.038**	**4.162**	
	Battery Regulation Voltage (For 4.2V Cell)	T_J = 0˚C to +85˚C, I_{CHARGE} = 10 mA, Mode = Low	4.2	**4.158**	**4.242**	
		T_J = −40˚C to +85˚C, I_{CHARGE} = 10 mA, Mode = Low	4.2	**4.137**	**4.263**	
V_{CHG-Q}	Full Charge Qualification Threshold	V_{BATT} Rising, Transition from Pre-Charge to Full Current	3.0			V

Electrical Characteristics (Continued)

Unless otherwise noted, V_{CHG-IN} = 5V, V_{BATT} = 4V, C_{CHG-IN} = 1µF, C_{BATT} = 10µF. Typical values and limits appearing in normal type apply for T_J = 25˚C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40˚C to +85˚C. (Notes 6, 7, 8)

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
BATTERY CHARGER—Li ION MODE (MODE = LOW)						
$V_{BAT-RST}$	Restart Threshold Voltage (For 4.1V Cell)	V_{BATT} Falling, Transition from EOC, to Pre-Qualification State	3.9	**3.77**	**4.02**	V
	Restart Threshold Voltage (For 4.2V Cell)	V_{BATT} Falling, Transition from EOC, to Pre-Qualification State	4.00	**3.86**	**4.12**	
R_{SENSE}	Internal Current Sense Resistance	(Note 7)	120			mΩ
	Internal Current Sense Resistor Load Current	(Note 7)			**1.2**	A
$ICHG_{MON}$	Diff-Amp Output	I_{CHG} = 50 mA	0.583			V
		I_{CHG} = 500 mA	1.333			
		I_{CHG} = 950 mA	2.090			
t_{EOC}	Time to EOC State	0˚C to +85˚C (Note 7)	5.625	**4.78**	**6.42**	Hrs
		−40˚C to +85˚C (Note 7)	5.625	**4.5**	**6.75**	
BATTERY CHARGER—NI-MH MODE (MODE = HIGH, LP3945 ONLY)						
$V_{BATT-MAX}$	Battery Over Voltage Protection	(Charging Current Decreases to 0 mA when V_{BATT} is above this Voltage), V_{CHG-IN} = 5.6V	5.4	**5.292**	**5.508**	V
LDO MODE (BIPB=HIGH)						
V_{OUT}	Output Voltage Regulation	I_{LOAD}=50mA	4.10			V
		I_{LOAD}=950mA	4.06			
LOGIC LEVELS						
V_{IL}	Low Level Input Voltage	EN			**0.4**	V
V_{IH}	High Level Input Voltage	EN		**2.0**		V
I_{IL}	Enable Pin Input Current	EN = LOW		**−10**	**+10**	µA
		EN = HIGH		**−5**	**+5**	

Electrical Characteristics, I²C Interface (LP3945 Only)

Unless otherwise noted, V_{CHG-IN} = 5V, V_{BATT} = 4V. Typical values and limits appearing in normal type apply for T_J = 25˚C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40˚C to +85˚C. (Notes 6, 7, 8)

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
V_{IL}	Low Level Input Voltage	SDA & SCL		**0.4**	**0.3 V_{DD}**	V
V_{IH}	High Level Input Voltage	SDA & SCL		**0.7 V_{DD}**	**V_{DD} +0.5**	V
V_{OL}	Low Level Output Voltage	SDA & SCL		**0**	**0.2 V_{DD}**	V
V_{HYS}	Schmitt Trigger Input Hysteresis	SDA & SCL		**0.1 V_{DD}**		V
F_{CLK}	Clock Frequency				**400**	kHz
t_{HOLD}	Hold Time Repeated START Condition	(Note 7)		**0.6**		µs
t_{CLK-LP}	CLK Low Period	(Note 7)		**1.3**		µs
t_{CLK-HP}	CLK High Period	(Note 7)		**0.6**		µs
t_{SU}	Set-up Time Repeated START Condition	(Note 7)		**0.6**		µs
$t_{DATA-HOLD}$	Data Hold Time	(Note 7)		**300**		ns
$t_{DATA-SU}$	Data Set-up Time	(Note 7)		**100**		ns
t_{SU}	Set-up Time for STOP Condition	(Note 7)		**0.6**		µs

Electrical Characteristics, I²C Interface (LP3945 Only) (Continued)

Unless otherwise noted, V_{CHG-IN} = 5V, V_{BATT} = 4V. Typical values and limits appearing in normal type apply for T_J = 25˚C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40˚C to +85˚C. (Notes 6, 7, 8)

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
t_{TRANS}	Maximum Pulse Width of Spikes that must be Suppressed by the Input Filter of both DATA & CLK signals.	(Note 7)	50			ns

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula

$$P = (T_J — T_A)/\theta_{JA}, \quad (1)$$

where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. The 1.76W rating appearing under Absolute Maximum Ratings results from substituting the Absolute Maximum junction temperature, 150˚C, for T_J, 85˚C for T_A, and 37˚C/W for θ_{JA}. More power can be dissipated safely at ambient temperature below 85˚C. Less power can be dissipated safely at ambient temperatures above 85˚C. The Absolute Maximum power dissipation can be increased by 27 mW for each degree below 85˚C, and it must be de-rated by 27 mW for each degree above 85˚C.

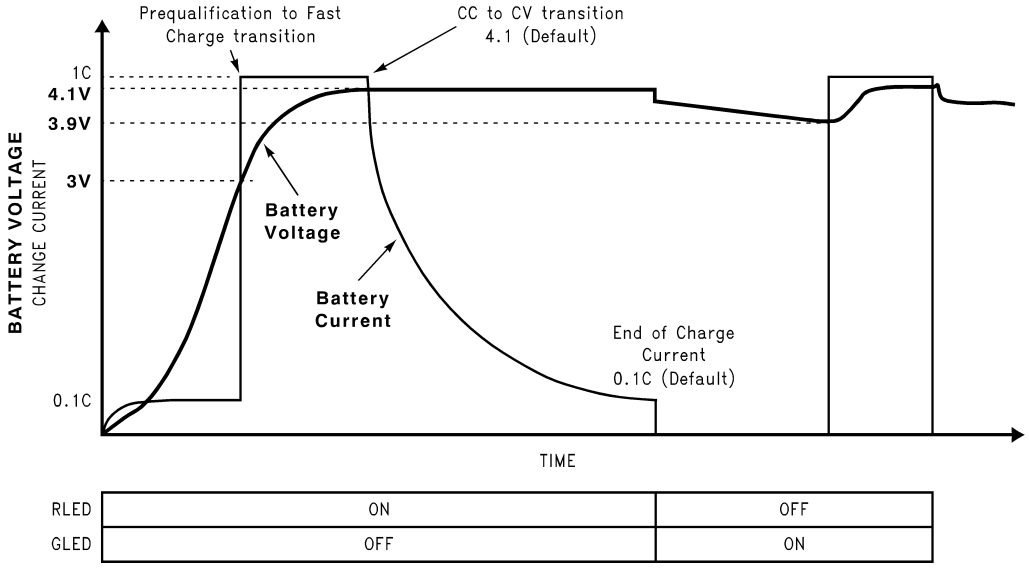
Note 4: The human-body model is 100 pF discharged through 1.5 kΩ. The machine model is 0Ω in series with 220pF

Note 5: Like the Absolute Maximum power dissipation, the maximum power dissipation for operation depends on the ambient temperature. The 1.08W rating appearing under Operating Ratings results from substituting the maximum junction temperature for operation, 125˚C, for T_J, 85˚C for T_A, and 37˚C/W for θ_{JA} into (1) above. More power can be dissipated at ambient temperatures below 85˚C. Less power can be dissipated at ambient temperatures above 85˚C. The maximum power dissipation for operation can be increased by 27 mW for each degree below 85˚C, and it must be de-rated by 27 mW for each degree above 85˚C.

Note 6: All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production with T_J = 25˚C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Note 7: Guaranteed by design.

Note 8: LP3945 and LP3946 are not intended as a Li-Ion battery protection device, battery used in this application should have an adequate internal protection.



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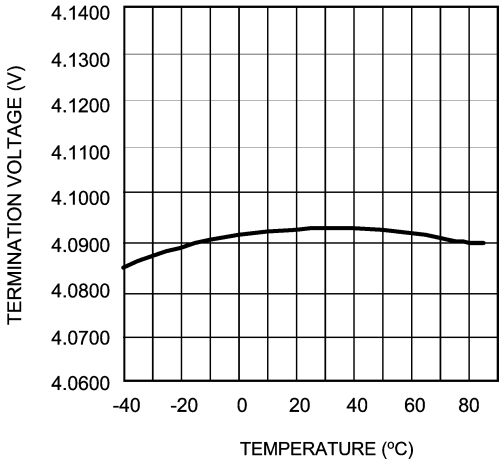
The end of charge current threshold default setting is at 0.1C, this threshold can be set to 0.15 or 0.2 by the controller (see bit chart for detail).

Li-Ion Charging Profile

Typical Performance Characteristics

Unless otherwise specified, T_A = 25˚C, V_{CHG-IN} = 5V.

4.1V Termination Voltage vs Temperature



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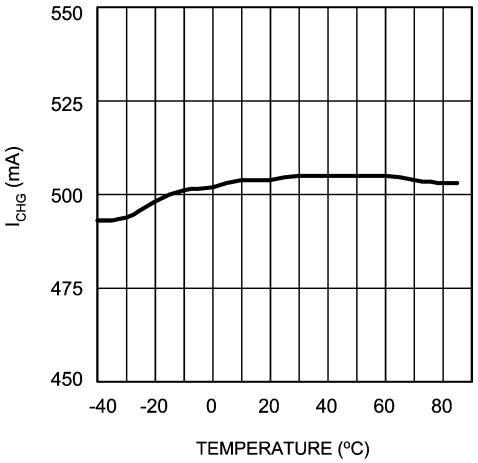
500mA vs Temperature



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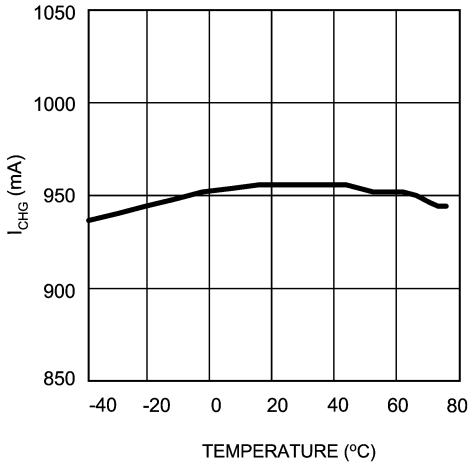
950mA vs Temperature



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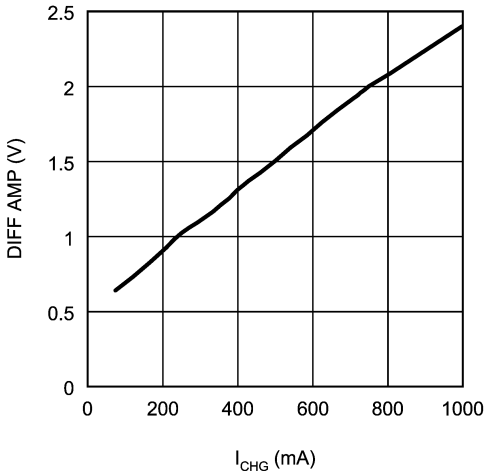
I_{CHG} vs Diff Amp



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Application Notes

LP3945 CHARGER OPERATION

The LP3945 is a complete battery charger with I²C interface. Charge cycle is initiated with wall adaptor insertion. If the wall adaptor voltage appearing on the CHG-IN pin meets under-voltage ($V_{UVLO-TSHD}$), over-voltage ($V_{OVLO-TSHD}$), and the Adaptor OK signal is detected, then pre-conditioning process begins (see *Figure 1*). In pre-qualification cycle, a safe current level, less than 65 mA, is pumped into the battery while the voltage across the battery terminals is measured. Once this voltage exceeds 3.0V, the controller will initiate constant current fast charge cycle. During this cycle, the 5.6 hr safety timer is started and charge current is increased to I_{CHG}. The default value for I_{CHG} is set during manufacturing to 500 mA but it is user programmable from 500 mA to 950 mA in 50 mA step. The programmed current is determined by battery type and manufacturers' recommendation.

If safety timer times out during constant current cycle, charging will be terminated if StopModeEN pin is pulled high. If it is pulled low, device will proceed to operate in maintenance mode and have to be interrupted externally. This is not a recommended mode of operation. Disabling the 5.6hr timer can potentially expose the battery to prolong charge cycle and damage the battery. If StopModeEN feature is used, user must protect the battery from exposure to prolong charge cycle.

As the battery is charged during constant current mode, the voltage across pack terminal increases until it reaches 4.1V (or 4.2V). As soon as pack terminal exceeds 4.1V (or 4.2V), controller starts operating in constant voltage mode by applying regulated V_{BATT} voltage across the battery terminal. During this cycle, charge current, I_{CHG}, continues to decrease with time and when it drops below 0.1C (by default), the EOC signal is activated indicating successful completion of the charge cycle. The "C" term in 0.1C is the programmed I_{CHG}. For example, 0.1C of 700mA is 70mA, and 0.2C of 700mA is 140mA. EOC current can be programmed to 0.1C, 0.15C, or 0.2C. The default value is 0.1C. After completing the full charge cycle, controller will start maintenance cycle where battery pack voltage is monitored continuously. If during the maintenance cycle, pack voltage drops below 3.9V, charge cycle will be initiated providing that the wall adaptor is plugged in and is alive.

Ni-MH charge mode (LP3945 only), which is a constant voltage mode charging, can be selected by setting the "mode" bit to HIGH via the I²C interface.

The LP3945 with I²C programming allows maximum flexibility in selecting charge current, battery regulation voltage (4.1V or 4.2V), EOC current and battery type (Li Ion or Ni-MH). The LP3945 operates in default mode during power up. See the "I²C Interface" section for more detail.

LP3946 CHARGER OPERATION

The LP3946 is a simpler version of the LP3945. It does not have any I²C interface, thus the device operates on default setting. The values in **BOLD** in *Table 1* are the default settings. Default settings can be set at the factory to customer's specifications. For other options, please contact a National Semiconductor sales office.

The LP3946 charges only Li Ion type battery.

TABLE 1. LP3946 Performance Options

Battery Voltage Regulation (V)	End of Charge Current Threshold (mA)	Charge Current (mA)
4.1	**0.1C**	**500**
4.2	0.15C	550
	0.20C	600
		650
		700
		750
		800
		850
		900
		950

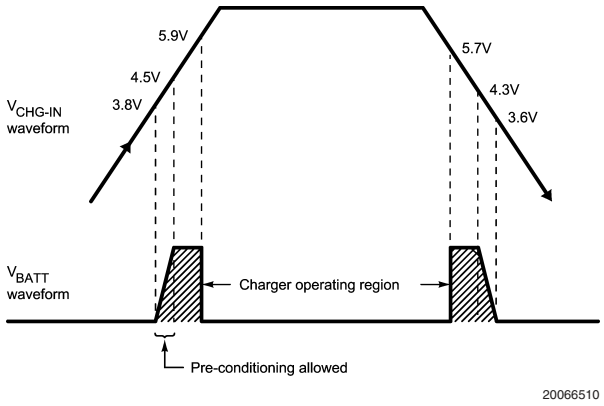


FIGURE 1. Charger Power Up and Power Down Waveform

Application Notes (Continued)

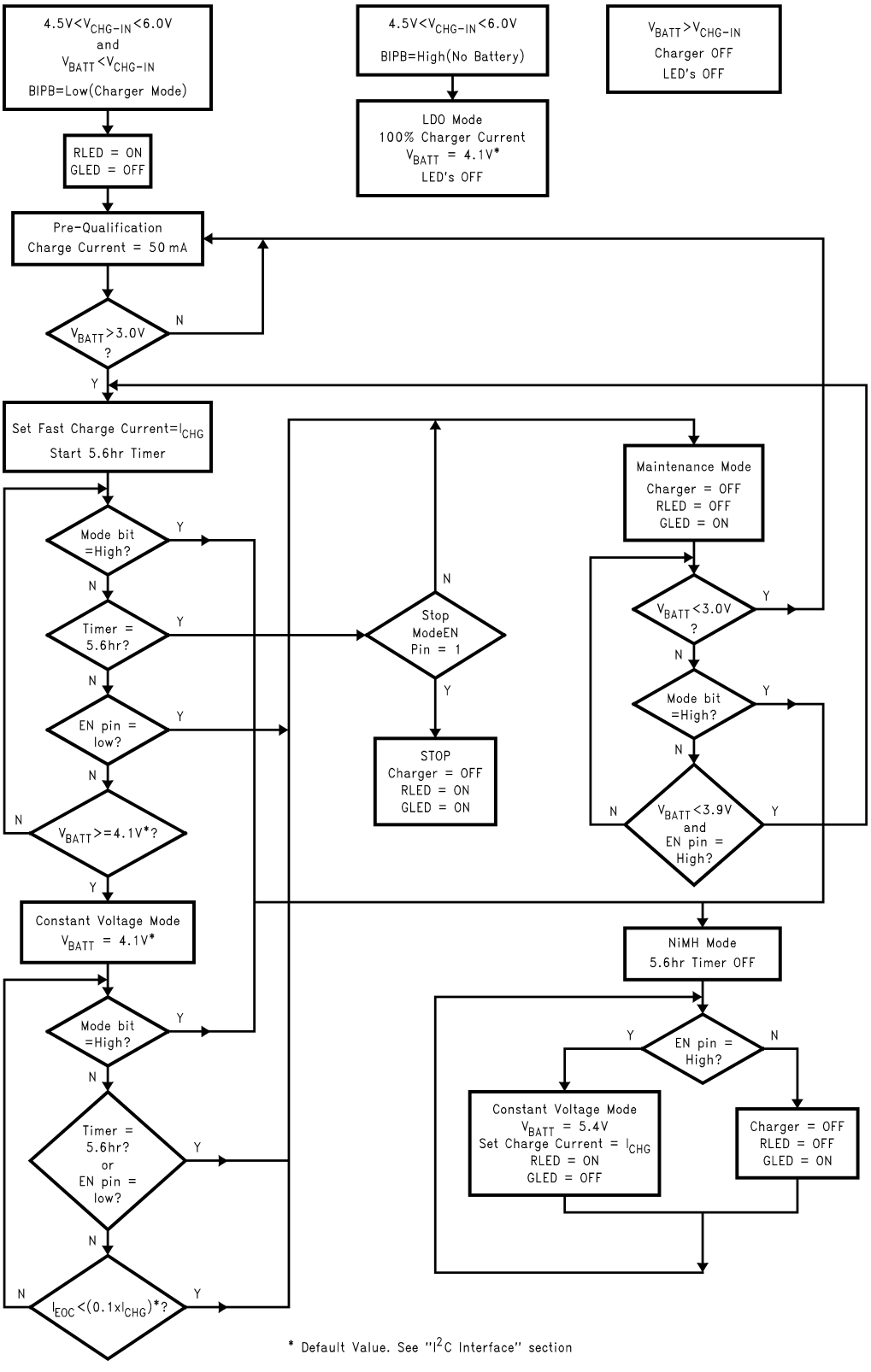


FIGURE 2. LP3945 Charger Flow Chart

Application Notes (Continued)

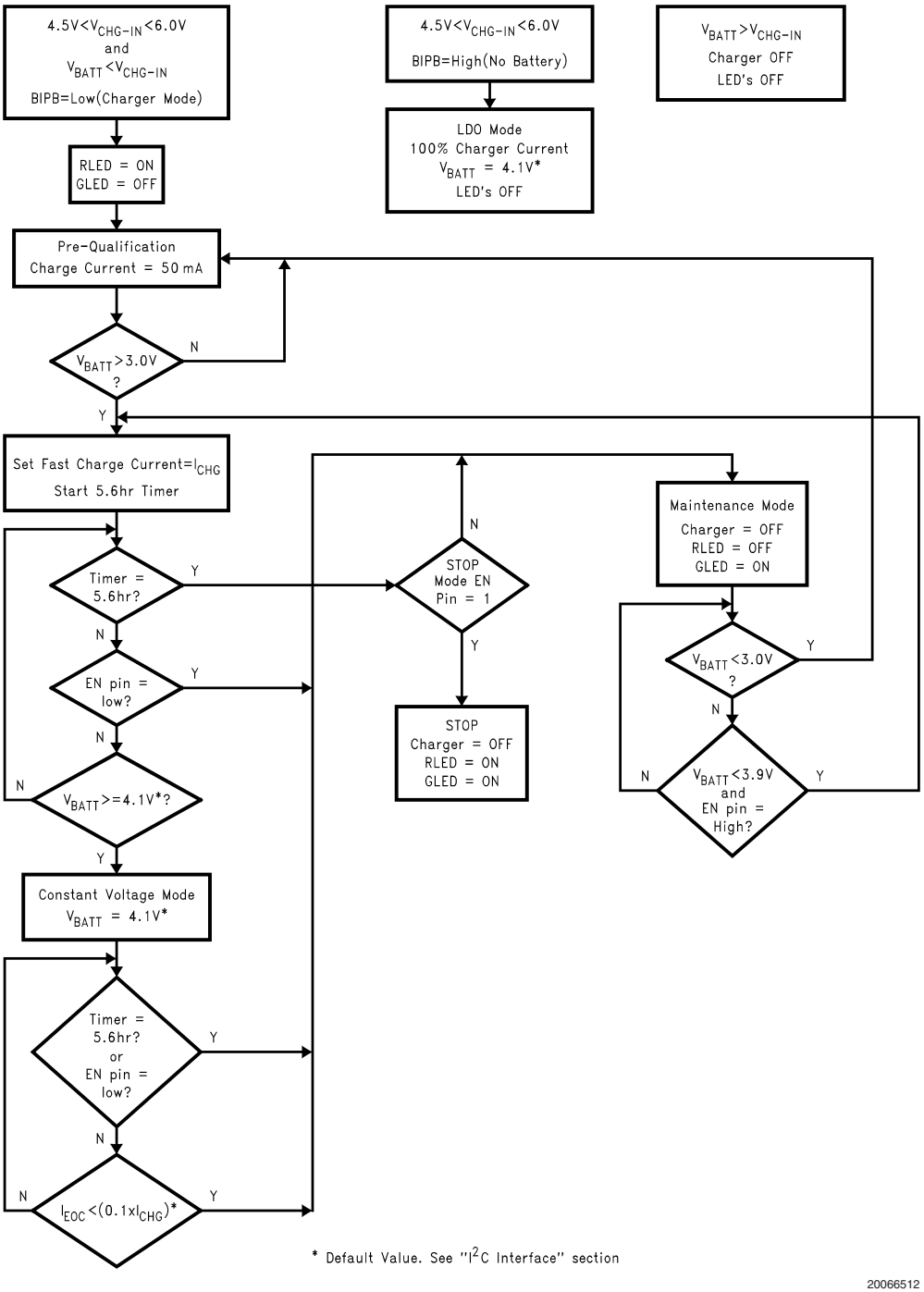


FIGURE 3. LP3946 Charger Flow Chart

Application Notes (Continued)

CHARGE CURRENT SELECTION

The LP3945 and LP3946 are designed to provide a charge current ranging from 500 mA to 950 mA, in 50 mA resolution, to support batteries with different capacity ratings. No external resistor is required to set the charge current in the LP3945 and LP3946. This entirely eliminates design time, external component board space and stability issue.

The LP3945 uses the I^2C interface to program the charge current while the LP3946 has a pre-programmed charge current.

BATTERY VOLTAGE SELECTION

The battery voltage regulation is set to 4.1V during the manufacturing. The 4.2V option can be selected on LP3945 via the I^2C interface or set at the factory for LP3946.

The Ni-MH charge mode is only available in LP3945.

END OF CHARGE (EOC) CURRENT SELECTION

The EOC thresholds can be programmed to 0.1C, 0.15C and 0.2C in the LP3945. The default value is 0.1C, which provides the highest energy storage, but at the expense of longer charging time. On the other hand, 0.2C takes the least amount of charging time, but yields the least energy storage. The LP3946 has 0.1C as pre-programmed EOC threshold. 0.15C and 0.2C options are available upon request.

No EOC function is available during Ni-MH charge cycle. User must provide a reliable method for charge termination.

CHARGE CURRENT SENSE DIFFERENTIAL AMPLIFIER

The charge current is monitored across the internal 120 mΩ current sense resistor. The differential amplifier provides the analog representation of the charge current. Charge current can be calculated using the following equation:

$$I_{CHG} = \frac{(V_{DIFF} - 0.497)}{1.655}$$

Where voltage at Diff Amp output (V_{DIFF}) is in volt, and charge current (I_{CHG}) is in amps.

Monitoring the Diff Amp output during constant voltage cycle can provide an accurate indication of the battery charge status and the time remaining to EOC. This feature is particularly useful during Ni-MH charge cycle. The current sense circuit is operational in the LDO mode as well. It can be used to monitor the system current consumption during testing.

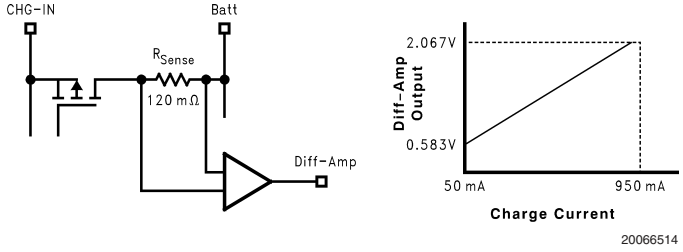


FIGURE 4. Charge Current Monitoring Circuit (Diff-Amp)

LED CHARGE STATUS INDICATORS

The LP3945 and LP3946 are equipped with two open drain outputs to drive a green LED and a red LED. These two LEDs work together in combinations to indicate charge status or fault conditions. *Table 2* shows all the conditions.

TABLE 2. LED Indicator Summary

Charger Status	RED LED	GREEN LED
Charger Off	OFF	OFF
Charging Li Ion Battery*	ON	OFF
Maintenance Mode	OFF	ON
Charging Li Ion Battery after Passing Maintenance Mode	OFF	ON
Charging Ni-MH in Constant Voltage Mode	ON	OFF
EN Pin = LOW	OFF	ON
LDO Mode	OFF	OFF
5.6 Hr Safety Timer Flag	ON	ON

*Charging Li Ion battery for the first time after V_{CHG-IN} insertion.

Application Notes (Continued)

BIPB PIN

BIPB pin is used to select between charger mode and LDO mode. It is pulled HIGH internally to the CHG-IN pin, which is the LDO mode. To select charger mode, this pin must be connected to ground directly or pulled to ground via the battery pack ID resistor. In the latter case, BIPB pin pulled LOW confirms battery connection. Alternatively, this pin can be pulled to LOW by the system micro-controller for added flexibility.

LDO MODE

The charger is in the LDO mode when the BIPB pin is left open or HIGH. This mode of operation is used primarily during system level testing of the handset to eliminate the need for battery insertion. **CAUTION:** battery may be damaged if device is operating in LDO mode with battery connected.

The internal power FET provides up to 1.2 amp of current at BATT pin in this mode. The LDO output is set to 4.1V. When operating at higher output currents, care must be taken not to exceed the package power dissipation rating. See "Thermal Performance of LLP Package" section for more detail.

EN PIN

The Enable pin is used to enable/disable the charger, in both charger mode and LDO mode, see *Figure 5* and *Figure 6*. The Enable pin is internally pulled HIGH to the CHG-IN pin. When the charger is disabled, it draws less than 4 µA of current.

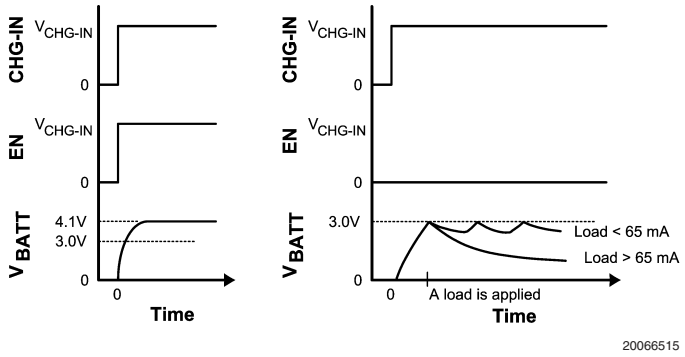


FIGURE 5. Power Up Timing Diagram in Charger Mode (BIPB = LOW)

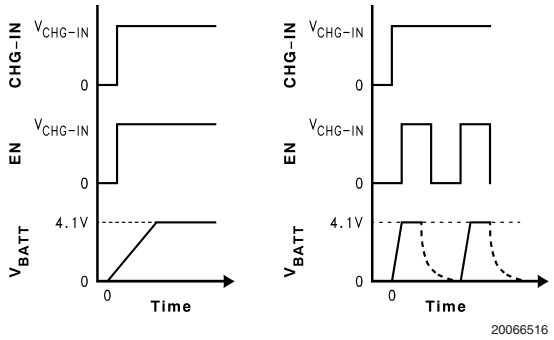


FIGURE 6. Power Up Timing Diagram in LDO Mode (BIPB = HIGH)

5.6 HR SAFETY TIMER IN CHARGER MODE

Both LP3945 and LP3946 have built-in 5.6 hr back up safety timer to prevent over-charging a Li Ion battery. The 5.6 hr timer starts counting when the charger enters constant current mode. It will turn the charger off when the 5.6 hr timer is up while the charger is still in constant current mode. In this case, both LEDs will turn on, indicating a fault condition.

In order for the 5.6 hr safety timer to function in the LP3945, pin 13 should be left floating. **CAUTION:** disabling the back up safety timer could create unsafe charging conditions. If disabled, user must provide external protection to prevent overcharging the battery.

StopModeEN PIN

To provide the flexibility of using an external back up timer, StopModeEN allows "bypassing" of the 5.6 hr safety timer. It is achieved by pulling pin 13 on the LP3945 to LOW. As indicated in the LP3945 Flow Chart, this feature works only in constant current mode with a Li Ion battery. Therefore, if a Li Ion battery is in constant current mode and the 5.6 hr timer times out, instead of the charger being turned off, it proceeds to maintenance mode.

This is not a recommended mode of operation. Disabling the 5.6 hr timer can potentially expose the battery to prolong charge cycle and damage the battery. If StopModeEn feature is used, user must protect the battery from exposure to prolong charge cycle. For normal operation, pin 13 should be left floating.

Application Notes (Continued)

NI-MH MODE (LP3945 ONLY)

Programming the "mode" bit to HIGH sets the LP3945 to Ni-MH mode and charges the battery in constant voltage mode until the battery voltage reaches 5.4V. Since each cell of the Ni-MH is 1.25V when fully charged, the LP3945 can only charge exactly four cells. Charging is terminated by the system micro-controller timer by monitoring the charge current. The system micro-controller reads the charge current value from the Diff Amp output. Charge current in Ni MH can be programed as in Li Ion mode, from 950 mA to 500 mA in 50 mA step. The 5.6 hr timer is disabled in Ni-MH mode.

I²C INTERFACE (LP3945 ONLY)

I²C interface is used in the LP3945 to program various parameters as shown in *Table 3*. The LP3945 operates on default settings during power up. Once programmed, the LP3945 retains the register data as long as the battery voltage is above 2.85V. *Table 4* shows the charge current and EOC current programming code.

Figures 7, 8 display I²C read/write format.

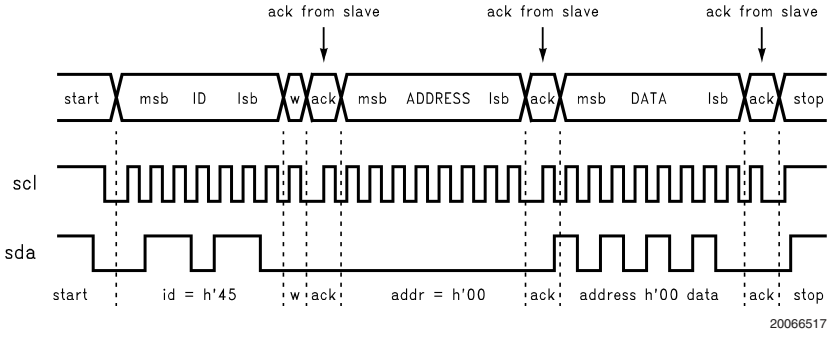
TABLE 3. LP3945 Serial Port Communication Address Code 7h'45

LP3945 Control and Data Codes									
Addrs	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
8'h00	Charger Register –1			Mode (0) = Li-Ion 1 = Ni-MH	Batt Voltage (0) = 4.1V 1 = 4.2V	Charger Current Code 3 (0)	Charger Current Code 2 (0)	Charger Current Code 1 (0)	Charger Current Code 0 (0)
8'h01	Charger Register –2				EOC (Green LED) R/O	Charging (Red LED) R/O	EOC Sel –1 (0)	EOC Sel –0 (1)	

Numbers in parentheses indicate default setting. "0" bit is set to low state, and "1" bit is set to high state. R/O — Read Only. All other bits are Read and Write.

TABLE 4. Charger Current and EOC Current Programming Code

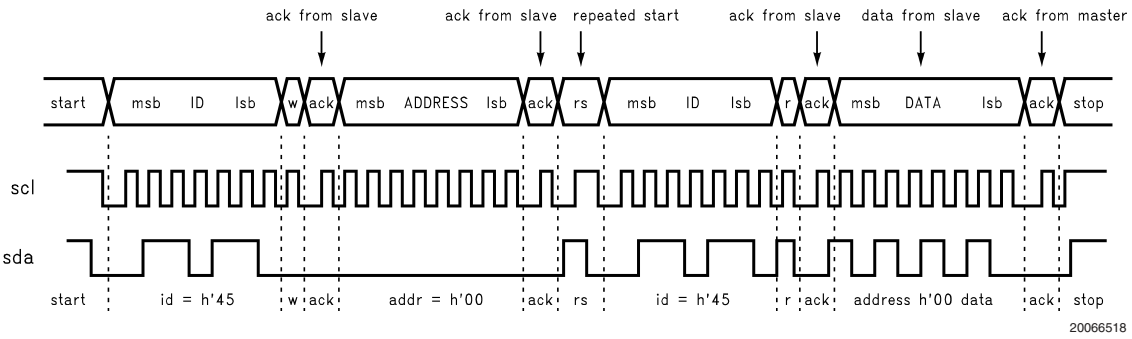
Data Code	Charger Current Selection Code I_{SET} (mA)	Data Code	End of Charge Current Selection Code
4h'00	**500**		
4h'01	550	2h'1	**0.1C**
4h'02	600	2h'2	0.15C
4h'03	650	2h'3	0.2C
4h'04	700		
4h'05	750		
4h'06	800		
4h'07	850		
4h'08	900		
4h'09	950		



w = write (sda = "0")
r = read (sda = "1")
ack = acknowledge (sda pulled down by either master or slave)
rs = repeated start

FIGURE 7. LP3945 (Slave) Register Write

Application Notes (Continued)



w = write (sda = "0")
r = read (sda = "1")
ack = acknowledge (sda pulled down by either master or slave)
rs = repeated start

FIGURE 8. LP3945 (Slave) Register Read

THERMAL PERFORMANCE OF LLP PACKAGE

The LP3945 and LP3946 are monolithic devices with integrated pass transistors. To enhance the power dissipation performance, the Leadless Lead frame Package, or LLP, is used. The LLP package is designed for improved thermal performance because of the exposed die attach pad at the bottom center of the package. It brings advantage to thermal performance by creating a very direct path for thermal dissipation. Compared to the traditional leaded packages where the die attach pad is embedded inside the mold compound, the LLP reduces a layer of thermal path.

The thermal advantage of the LLP package is fully realized only when the exposed die attach pad is soldered down to a thermal land on the PCB board and thermal vias are planted underneath the thermal land. Based on a LLP thermal measurement, junction to ambient thermal resistance (θ_{JA}) can be improved by as much as two times if a LLP is soldered on the board with thermal land and thermal vias than if not.

An example of how to calculate for LLP thermal performance is shown below:

$$\theta_{JA} = \frac{T_J - T_A}{P_D}$$

By substituting 37˚C/W for θ_{JA}, 125˚C for T_J and 70˚C for T_A, the maximum power dissipation allowed from the chip is 1.48W at T_A = 70˚C. If V_{CHG-IN} is at 5.0V and a 3.0V battery is being charged, then 740 mA of I_{CHG} can safely charge the battery. More power can be safely dissipated at ambient temperatures below 70˚C. Less power can be safely dissipated at ambient temperatures above 70˚C. The maximum power dissipation for operation can be increased by 27 mW for each degree below 70˚C, and it must be de-rated by 27 mW for each degree above 70˚C.

LAYOUT CONSIDERATION

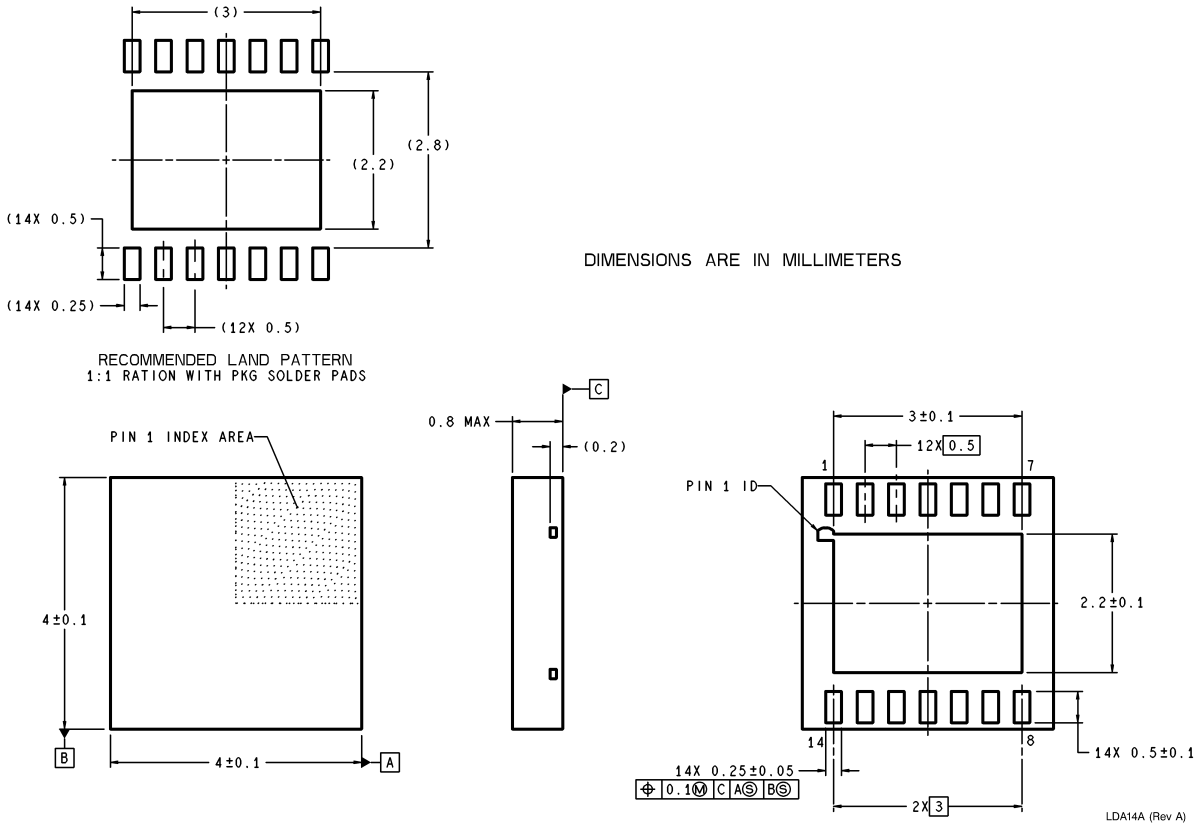
The LP3945 and LP3946 have exposed die attach pad located at the bottom center of the LLP package. It is imperative to create a thermal land on the PCB board when designing a PCB layout for the LLP package. The thermal land helps to conduct heat away from the die, and the land should be the same dimension as the exposed pad on the bottom of the LLP (1:1 ratio). In addition, thermal vias should be added inside the thermal land to conduct more heat away from the surface of the PCB to the ground plane. Typical pitch and outer diameter for these thermal vias are 1.27 mm and 0.33 mm respectively. Typical copper via barrel plating is 1 oz. although thicker copper may be used to improve thermal performance. The LP3945 and LP3946 bottom pad is connected to ground. Therefore, the thermal land and vias on the PCB board need to be connected to ground.

For more information on board layout techniques, refer to Application Note 1187 "Leadless Leadframe Package (LLP)". The application note also discuss package handling, solder stencil, and assembly.

LP3945 AND LP3946 EVALUATION BOARDS

The LP3945 and LP3946 evaluation boards and instruction manuals are available for order on National's website (www.national.com). The LP3945 evaluation board has on-board I^2C interface capability for more flexibility. Please visit National's website for more detail.

Physical Dimensions inches (millimeters) unless otherwise noted



NS Package Number LDA14A

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