# TSW6011EVM

This document outlines the basic steps and functions that are required for the proper operation of the TSW6011 evaluation module (EVM) system. The TSW6011EVM is a single RX channel board that can be used to demonstrate a TRF371125 integrated direct downconversion receiver interfacing to an ADS5282 octal analog-to-digital converter (ADC). This guide helps the user to evaluate the performance of various modes of operation of the TSW6011EVM. Throughout this document, the term *evaluation module* and the abbreviation *EVM* are synonymous with the TSW6011EVM.

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# 1 Overview

The TSW6011EVM board provides options to send an input RF signal directly to the TR371125 or through one or two low-noise amplifiers (LNAs) by moving two resistors. Additionally, there is an option to drive two of the ADCs with an external source. This source can be single-ended (board default through a transformer) or a differential signal (from a TRF3711xxEVM, for example). There also is an option to bypass the onboard oscillator with an external source. The EVM contains a TRF371125, an ADS5282 for data conversion, an FPGA for digital processing, a CDCE62005 for system clocks, and a DAC5672A to allow for data evaluation using just a spectrum analyzer.

## 1.1 EVM Frequency Configuration Options

The TR371125 device is inherently broadband; however, the radio frequency (RF) and local oscillator (LO) inputs require differential signals which are achieved with the use of RF baluns. This EVM can be configured with a different balun to facilitate operation in the desired band. The default configuration includes 2-GHz baluns for both inputs. Table 1 summarizes the TRF3711xx device frequency options and lists the recommended balun for each device.

**Table 1. TRF3711xx Device Frequencies and Recommended Baluns(1)**

| Frequency | Device | Recommended Balun |
|---|---|---|
| 700 MHz | TRF371125 | Murata LDB21897M05C |
| 880 MHz | TRF371125 | Murata LDB21881M05C |
| 940 MHz | TRF371125 | Murata LDB21942M05C |
| 1740 MHz | TRF371125, TRF371135 | Murata LDB211G8005C |
| 1950 MHz | TRF371125, TRF371135 | Murata LDB211G9005C |
| 2025 MHz | TRF371125, TRF371135 | Murata LDB211G9005C |
| 2500 MHz | TRF371125, TRF371135 | Murata LDB212G4005C |
| 3550 MHz | TRF371125, TRF371135 | Johanson 3600BL14M050E |
| 5400 MHz | TRF371135 | Johanson 5400BL15B050E |

(1) There is considerable overlap in the operating frequency range of the TRF3711xx family of devices. Refer to the specific device data sheet and compare performance parameters at the frequencies of interest to select the best part for a particular application.

## 1.2 TSW6011EVM Block Diagram

The TSW6011EVM system block diagram is shown in Figure 1.

The output data can be captured through the CMOS connector. This interface has an RC network on every data and clock signal to allow the user to plug an Agilent-style logic analyzer pod directly to the connector.

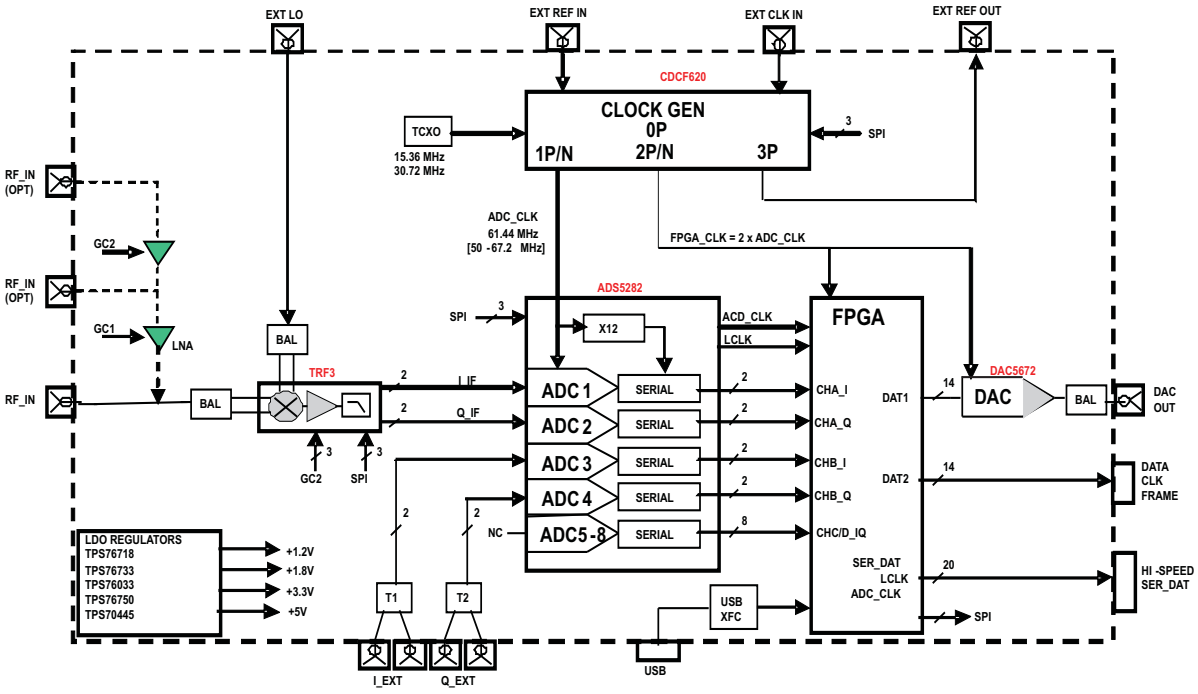


**Figure 1. TSW6011EVM System Block Diagram**

## 1.3 Digital Processing Block Functions

The FPGA receives the digital data from the ADC and converts it from serial to parallel format. The data then are split into two paths. One path converts the data back to unsigned serial data and determines which ADC output to route to the LVDS connector. The other path either bypasses or goes through the IQ Correction block. After IQ Correction processing, the data are interpolated by 2, processed through a finite impulse response (FIR) and then mixed to fs/4 (30.72 MHz). DAC sample rate is 122.88 MHz, and ADC sample rate is 61.44 MHz.

The FPGA allows the user to perform the following functions.

- Select the processing path between TRF3711 and SMA
- Enable or disable the LVDS and CMOS data outputs
- Enable or disable the IQ Correction algorithm
- Digital gain control by 0.5dB step
- Program ADC, PLL, and TRF371125 registers
- Enable or disable the DC offset compensation algorithm
- Set the LNA gain
- Provide attenuation setting for TRF371125

The FPGA digital processing block diagram is shown in Figure 2.

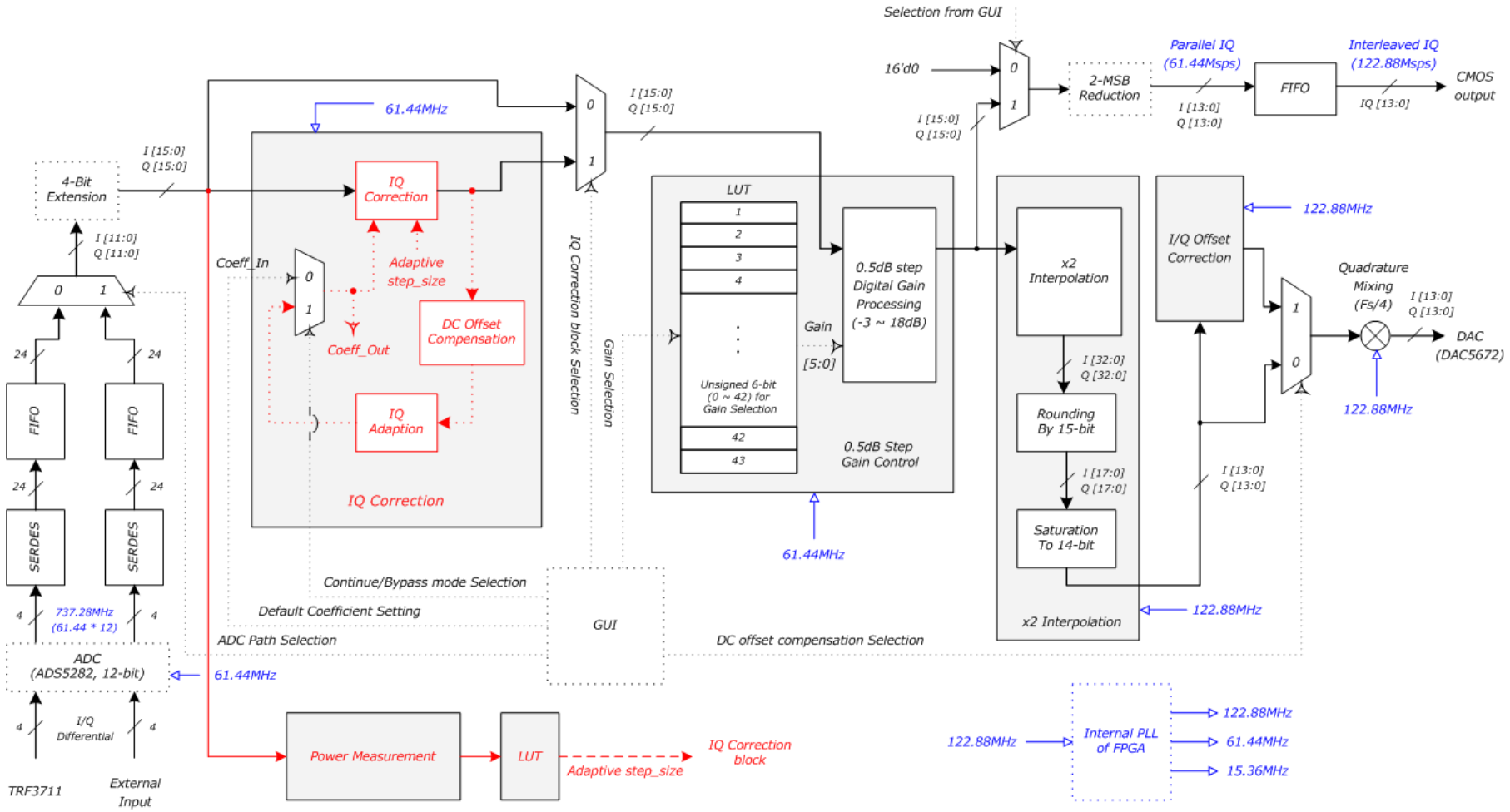


**Figure 2. FPGA Digital Processing Block Diagram**

# 2 Software Installation

## 2.1 Installation Instructions

Step 1. Download and install *TSW6011EVM GUI Installer* and *MCRinstaller.exe* on the web (www.ti.com/tool/tsw6011evm)

Step 2. To get started the GUI, double-click *TSW6011_control_panel.exe* in your target directory. You can set this directory during installation.

# 3 EVM Test Configuration

## 3.1 Test Equipment

The following equipment is required to operate the TSW6011:

- Signal generator for input signal (Agilent E4438C or equivalent)
- Signal generator for LO signal (Agilent E4438C or equivalent)
- Spectrum analyzer (Agilent E4440A or equivalent)
- Programming computer
- USB cable (provided)
- RF cables

## 3.2 Calibration

The RF cables must be good quality because of the high-frequency signals.

- Measure the insertion loss of the RF input cable and use this value to compensate for the desired input power.
- Measure the insertion loss of the LO input cable and use this value to compensate for the desired LO power.

**NOTE:** Approximately 1 dB of insertion loss for the input traces and balun is on the printed-circuit board (PCB).

# 4 Board Bring Up

## 4.1 Power Up

- Plug +6-VDC power supply to a 110-VAC to 120-VAC source and the output to J9. (See the board top-view drawing as shown in Figure 3.)

  Verify that the jumpers are configured as follows:

  JP1: Pins 1 and 2 (applies power to TR371125 Chip_EN input pin).

  JP2: Pins 2 and 3 (disables LNA power regulator U13).

  JP3: Pins 1 and 2 (enables USB to parallel interface device power regulator U21).

  SJP1: Pins 2 and 3 (selects SMA J1 to be the RF input source to the TRF371125).

  SJP2: Pins 1 and 2 (selects LNA U2 output).

  SJP3: Open (used to select source for LNA U2 GAIN_SEL input).

  SJP4: Pins 2 and 3 (enables primary reference source Y2 for the CDCE62005).

  SJP5: Open. (used to select source for LNA U8 GAIN_SEL input).

  SJP6: Pins 2 and 3 (selects CDCE62005 power down source).

  SJP7: Pins 1 and 2 (disables CDCE62005 AUX_IN source Y4).

  SJP8: Pins 1 and 2 (selects DAC5672 SLEEP input source).

  SJP9: Pins 1 and 2 (selects USB to parallel interface device power source).

  SJP10: Pins 2 and 3 (selects DAC5672 input clock source).
- Note that the following LE's are now illuminated:
  - D6: +6V power present
  - D1: CDC is locked to reference source
  - D10: USB powered up
  - D11: FPGA is configured
  - D7: TR371125 enabled
  - D3: DAC input data enabled
  - D12: DAC enabled

  (This is the board default power-up mode.)
- Plug the USB cable into the host PC and connector J7 on the TSW6011.
- When plugging in the USB cable for the first time, the user is be prompted to install the USB drivers.
  - When a pop-up screen opens, select *Continue Downloading*.
  - Follow the on-screen instructions to install the USB drivers.
  - If needed, the USB drivers can be accessed in the following directory: **C:\TSW6011GUI\FTD245_Drivers**

## 4.2 Basic RF Test

Follow these steps to perform a basic RF test.

Step 1. Inject a LO signal at J4 at a frequency of 2150 MHz at 0 dBm. Compensate for RF cable losses, including about 1 dB for input balun and transmission line losses.

Step 2. Since the board default configuration bypasses the two LNAs, inject an RF signal at J1 at 2153 MHz at –15 dBm. Compensate for cable loss, including about 1 dB for input transmission line losses and balun.

Step 3. Connect a spectrum analyzer to J6.

Step 4. Set up the spectrum analyzer as follows:

- Set span to 20 MHz
- Set center frequency to 30.72 MHz
- Set reference level to –10 dBm
- Set attenuation to 15 dB
- Set sweep time to 2.5 ms
- Set RBW to 300 kHz
- Set VBW to 1 MHz

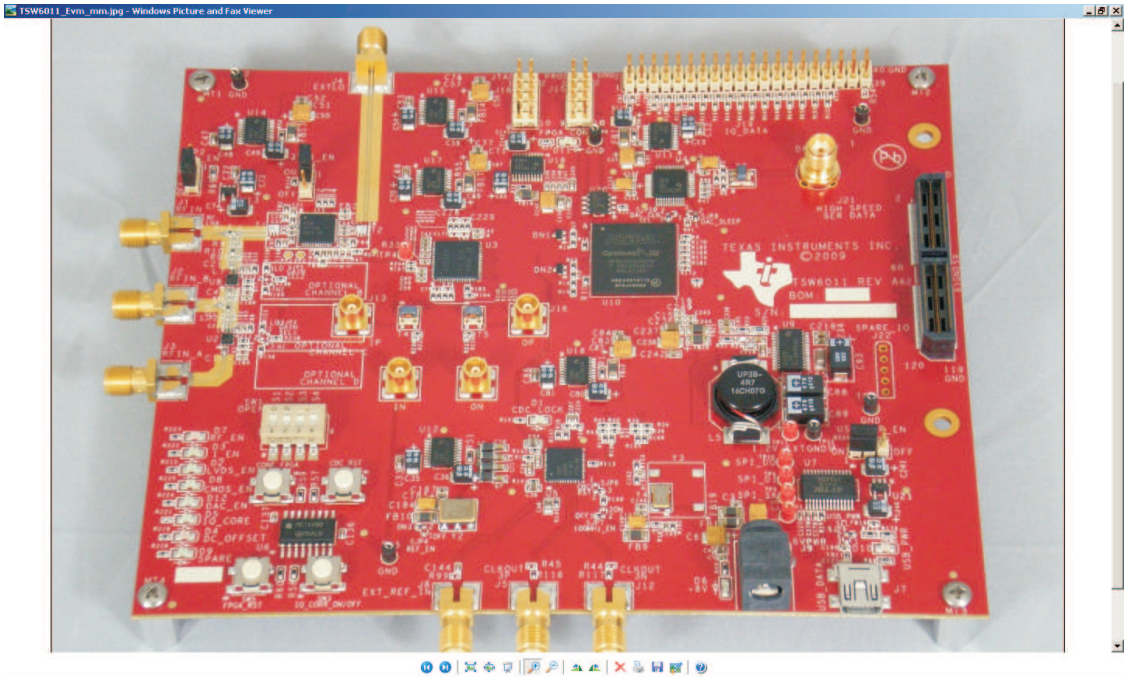


**Figure 3. TSW6011EVM Board Top View**

### 4.3 Software Operation

When the GUI first starts, the front control panel appears as shown in Figure 4.

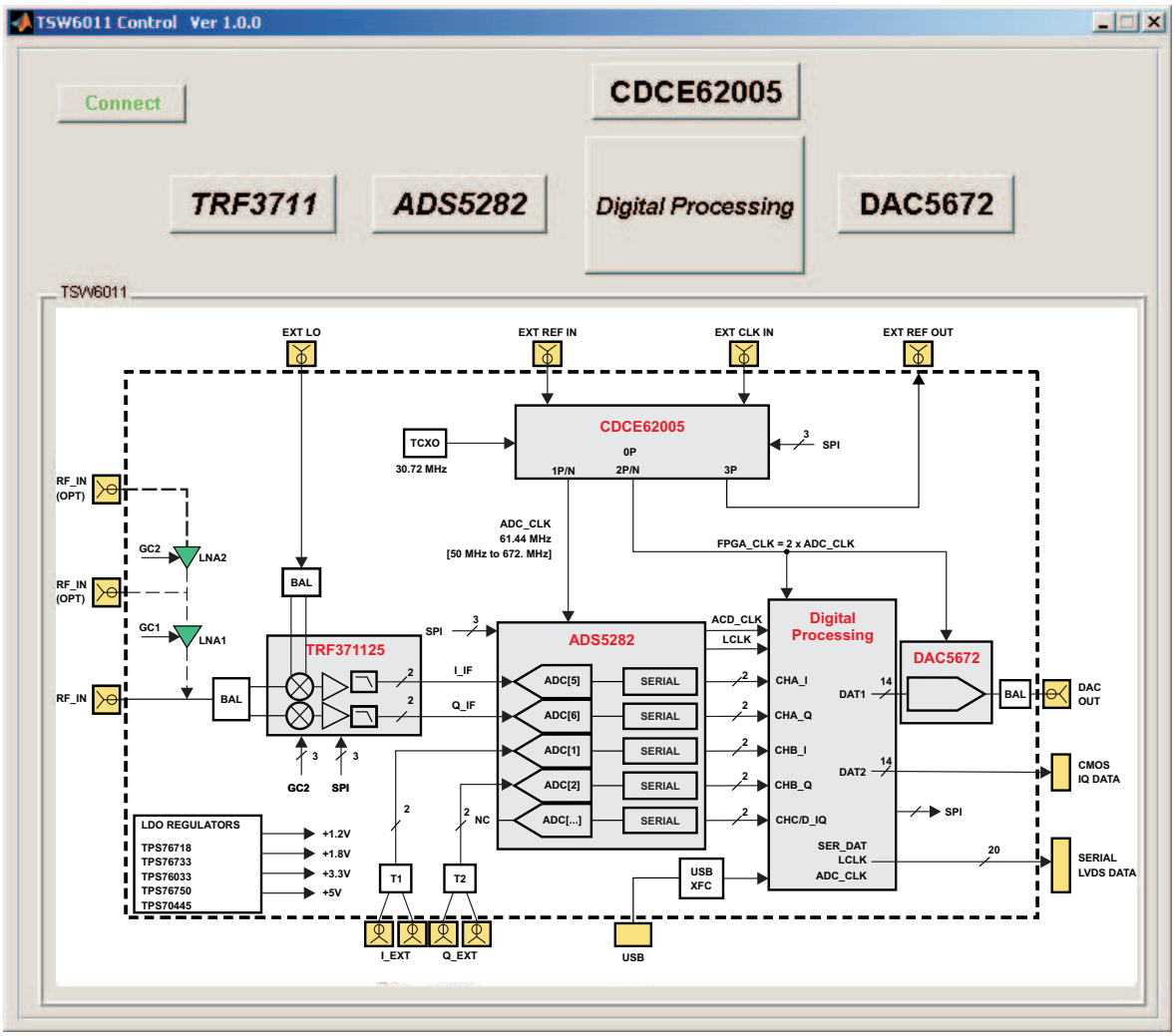


**Figure 4. TSW6011EVM Software GUI Front Panel**

To enable the GUI, the user must click on the button labeled **Connect** in the upper left-hand corner. If communication between the GUI and TSW6011 is successful, the button changes to display **Disconnect**. Clicking on this button again disconnects the GUI, and the button displays **Connect** once more. If there is a problem with the connection, an error message appears, as shown in Figure 5.


**Figure 5. GUI Communication Error**

If this message appears, make sure the USB cable is installed, the USB drivers are installed, and verify that the board is powered up. If this problem persists, unplug the USB cable from the EVM, then reconnect it. If this procedure does not correct the problem, close the GUI and reboot the host computer.

### 4.4 Device Initialization

- Click on the GUI button labeled **ADS5282**. This opens the ADS5282 control panel as shown in Figure 6.

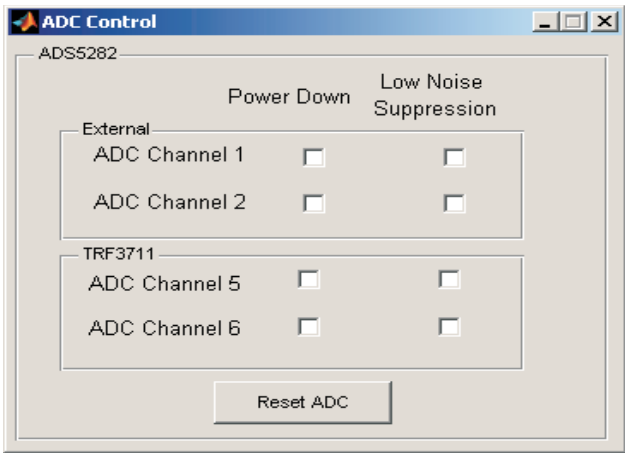


**Figure 6. ADS5282 Control Panel**

- When the control panel opens, the ADS5282 is initialized by the software automatically. The TSW6011 routes external signals from the SMAs to ADC channels 1 and 2. The TR371125 outputs are routed to channels 5 and 6. Channels 3, 4, 7, and 8 are not used. The following sequence is performed every time this GUI window is opened:
  - Reset the device.
  - Power up ADC Channels 1, 2, 5, and 6. Power down ADC channels 3, 4, 7, and 8.
  - Set the serial output stream to send MSB first.
  - Set the data format to twos complement.
  - Set the input clock to differential mode.
- To power down any of the four channels, click on the respective box in the *Power Down* column.
- To activate the respective channel Low Noise Suppression, click on the box.
- To issue a device reset, click on the **Reset ADC** button.
- Click on the ***X*** in the upper right-hand corner to close the panel.

Click on the **TRF3711** button of the GUI to open the TR371125 control panel as shown in Figure 7.

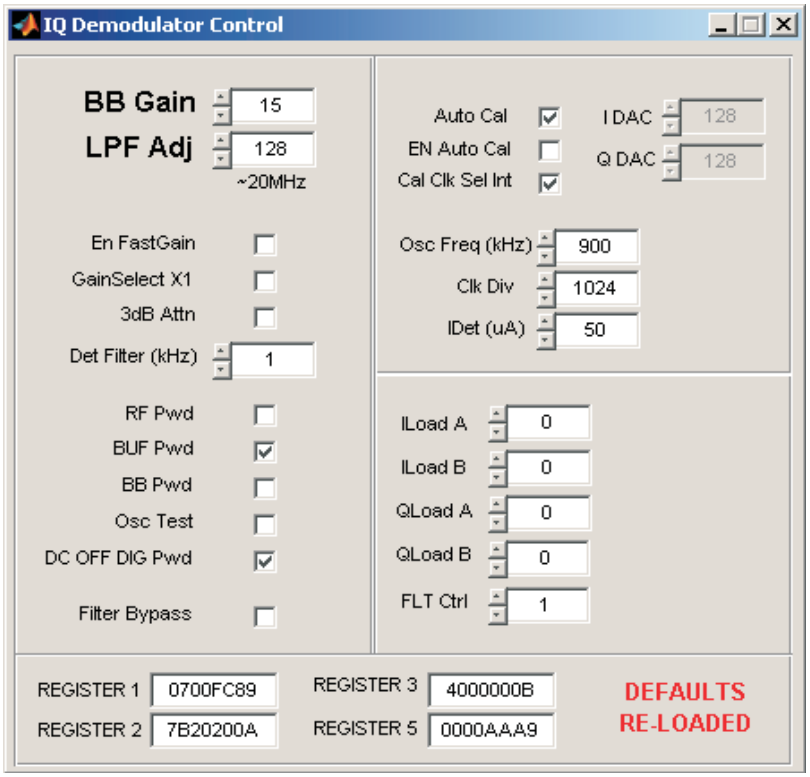


**Figure 7. TR371125 Control Panel**

- When the control panel opens, the TR371125 is initialized by the software automatically. The default settings are those shown in the control panel when it opens. Every time this panel is opened, the default values are loaded. This process is reported by the message in red: DEFAULTS RE-LOADED (as shown in Figure 7).
- Click on the **BB Gain** field and set the gain to 5.
- Click the **Filter Bypass** checkbox to bypass the TR371125 LPF internal filter.

After loading the TRF371125, the output spectrum now looks as shown in Figure 8.

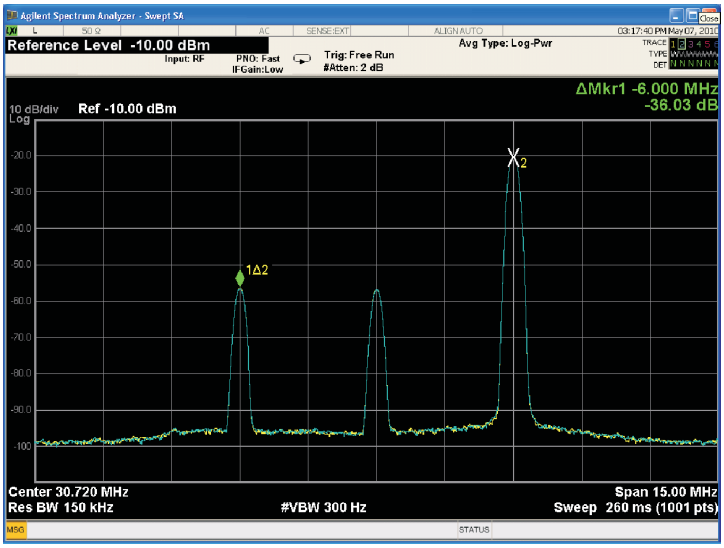


**Figure 8. Test Tone From DAC5672 Output**

- Click on the GUI button labeled **Digital Processing**. This opens a control panel that is shown in Figure 9.

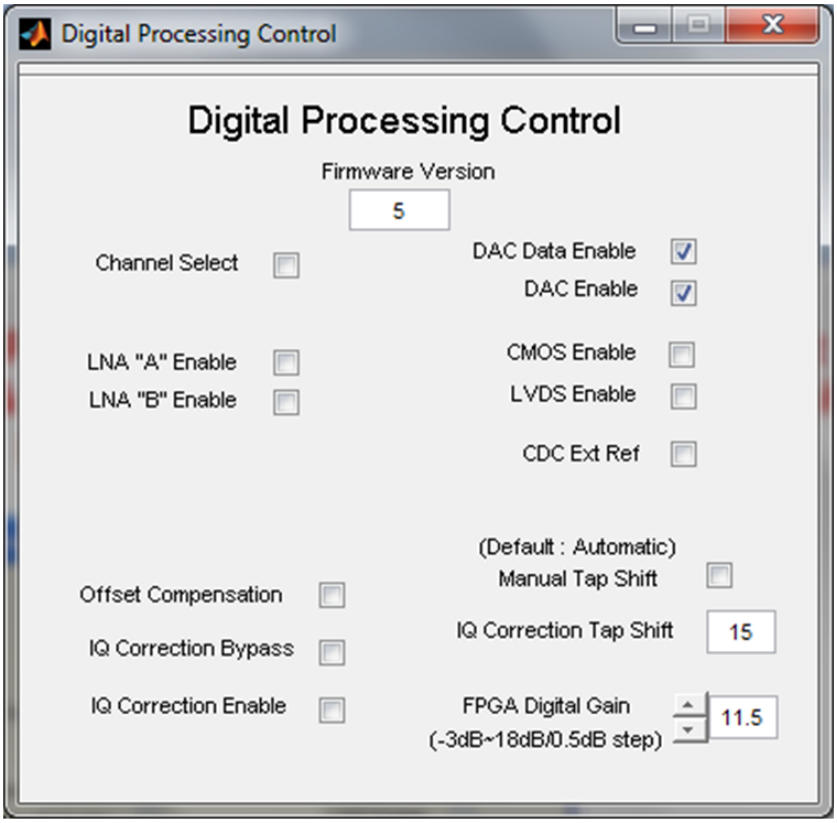


**Figure 9. Digital Processing Control Panel**

- The values selected in the control panel are the default values loaded at power up. The controls are defined as follows:

| | |
|---|---|
| Firmware Version: | Displays the version of the firmware loaded in the FPGA |
| Channel select: | When not selected, the output of the TR371125 is used by the digital processing path and sent to the DAC. When selected, the external SMA inputs are used by the digital processing path. |
| LNA "A" Enable: | When selected, places LNA U2 into low gain mode (–3 dB typ). When not selected, the LNA is in high gain mode (14.5 dB typ). |
| LNA "B" Enable: | When selected, places LNA U8 into low gain mode (–3 dB typ). When not selected, the LNA is in high gain mode (14.5 dB typ). |
| DAC Data Enable: | When selected, enables data through digital processing path to be routed to the DAC. When disabled, no data are routed to the DAC. |
| DAC Enable: | When selected, the DAC is enabled. When disabled, the DAC is in sleep mode. |
| CMOS Enable: | When selected, enables unprocessed data to be routed to the CMOS data connectors. When disabled, no data are routed to the connectors. |
| LVDS Enable: | When selected, enables unprocessed data to be routed to the LVDS connector. When disabled, no data are routed to the connector. |
| CDC Ext Ref: | Disabled. Currently not used. |
| IQ Correction Enable: | When selected, IQ Correction is enabled. When disabled, IQ Correction block is bypassed. |

| | |
|---|---|
| FPGA Digital Gain (0.5dB step): | This function compensates digital gain by 12 dB because there is 2-bit of headroom between ADS5282 (12-bit) and DAC5672 (14-bit). Digital gain can be controlled in 0.5 dB steps from -3 dB to 18 dB. For better signal quality such as EVM improvement, increase the digital dynamic range of the input signal to DAC5672. 11.5 dB of digital gain is recommended to avoid the input signal saturated to DAC5672. |
| OFFSET Compensation: | When selected, the DC offset compensation is enabled. When disabled, the DC offset compensation block is bypassed. |
| IQ Correction Tap Shift Avg: | Initial value is 13, which is coarse adaption. Users can choose the value of 18, which slows the adaption algorithm. |
| Manual Tap Shift: | This option is not recommended; however, it allows selection of a tap shift value ranging from 10 to 18. The tap shift value is automatically chosen inside the FPGA firmware based on input digital power. |
| IQ Correction Bypass: | When selected, IQ correction is bypassed and the output of ADS5282 goes into digital gain block. |

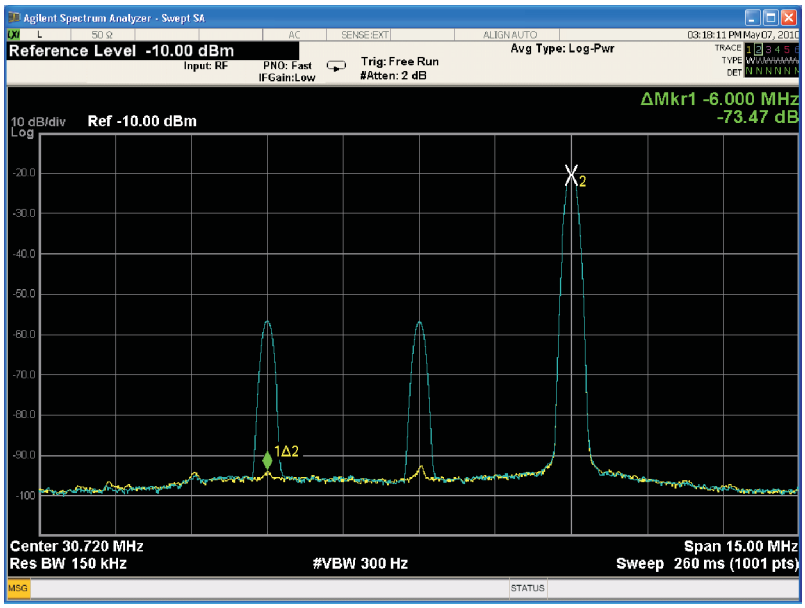


**Figure 10. Test Tone After IQ Correction and DC Offset Compensation**

The buttons labeled **CDCE62005** and **DAC5672** do not have control panel associations. The CDC is loaded at power up, and no internal registers are within the DAC5672. Contact TI if settings other than the default are required for the CDCE62005.

# 5 TR371125 Register Definitions

## 5.1 Register 1

- BB Gain: The PGA (Programmable Gain Amplifier) setting; range is 0 to 24.
- LPFAdj: Sets the bandwidth of the BB filters. Setting 0 is maximum bandwidth (~29.6 MHz); setting 254 is minimum (~ 1.27 MHz). See the product data sheet (SLWS219) for comprehensive curves.
- EN_FastGain: Enables the fast gain option to adjust PGA gain with external bits.
- Gain Select: Selects whether each bit in the fast gain control is either 1 dB or 2 dB.
- 3 dB Attn: Engages the 3-dB attenuator at the baseband output.
- Det Filter: Selects the internal detector filter used in dc offset calibration.
- RF Pwd: Enables SW controlled power down of RF stages inside device.
- BUF Pwd: Enables power down on test buffer for mixer output; default is powered down.
- Osc_Test: Enables dc offset oscillator to the Readback pin.
- DC_Off_DIG Pwd: Enables SW controlled power down of dc offset correction circuitry.

## 5.2 Register 2

- Auto Cal: Manual mode allows the dc offset DACs to be user configurable; Auto mode uses the internally stored values.
- En Auto Cal: When toggled, an Auto Cal is initiated. Note, Auto Cal must be in Auto mode.
- I/Q DAC: Shows the setting of the dc offset I and Q DAC when in Manual mode; range is 0 to 255
- Cal Clk Sel: Toggle between using an externally supplied SPI clock or internal oscillator clock.
- Osc. Freq: Selects the oscillator frequency for the internal clock.
- Clk Div: Sets the clock divider if the control clocks need to be slowed down. Value chosen in conjunction with Det Filter setting for optimal averaging.
- I Det: Selects the resolution of the I and Q DAC.

## 5.3 Register 3

- I/QLoadA/B: Selects the mixer gain for the differential BB paths. Typically, these registers do not need to be modified, but minor I/Q amplitude adjustments are allowed.
- Filter Ctrl: Trims the peaking response of the BB LPF response.
- Filter Bypass Engages the bypass feature of the BB LPF.

## 5.4 Register 5

- Mix GM Trim No adjustment of this register required
- Mix LO Trim No adjustment of this register required
- LO Trim No adjustment of this register required
- Mix Buff Trim No adjustment of this register required
- Filter Trim No adjustment of this register required
- Out Buff Trim No adjustment of this register required

The hex values in the Register # boxes are the actual values loaded into the TRF371125.

## A.1 LED Definitions

D1: CDC locked to reference
D6: +6V present
D10: USB device powered up
D11: FPGA configured
D7: TR371125 enabled
D3: DAC input data enabled
D12: DAC powered up
D4: DC Offset compensation enabled with blinking
D5: IQ Correction enabled with blinking

## A.2 Connector Descriptions

| Designator | Description |
|---|---|
| J1 | RF input. Bypasses both LNAs. |
| J2 | RF input to LNA #2. Bypasses LNA #1. |
| J3 | RF input to LNA #1. |
| J4 | TR371125 LO input source |
| J13 | ADC #1 analog input. Positive analog input when T4 is bypassed. |
| J14 | ADC #1 negative analog input when T4 is bypassed. |
| J16 | ADC #2 analog input. Positive analog input when T5 is bypassed. |
| J17 | ADC #2 negative analog input when T5 is bypassed. |
| J8 | External reference for CDCE62005. |
| J5 | Spare output from CDCE62005 |
| J12 | Spare output from CDCE62005 |
| J6 | DAC5672 output. |
| J21 | LVDS outputs. Mates with TSW1400 LVDS input connector. |
| J19 | CMOS output data. |
| J22 | Test connector. |
| J9 | +6-VDC input power connector. |
| J7 | USB connector. |
| J18 | FPGA JTAG connector. |
| J15 | FPGA PROM programming connector. |

## A.3 Jumper and Switch Descriptions

| Designator | Description | Default Position |
|---|---|---|
| SJP3 | Selects gain for LNA #1. Logic high sets typ gain to 14.5 dB. Logic low sets typ gain to –3.0 dB. | FPGA control (Low Gain) |
| SJP5 | Selects gain for LNA #2. Logic high sets typ gain to 14.5 dB. Logic low sets typ gain to –3.0 dB. | FPGA control (Low Gain) |
| SJP2 | LNA #1 bypass. Jumper 1-2 to use LNA #1, 2-3 to bypass LNA #1. | 1-2 |
| SJP1 | LNA #2 bypass. Jumper 1-2 to use LNA #1, 2-3 to bypass LNA #1. | 2-3 |
| JP1 | TR371125 enable. Installed to enable device. | 1-2 |
| SJP7 | CDCE62005 AUX oscillator power. Set to 1-2 to power down oscillator, 2-3 to power up. | 1-2 |
| SJP4 | CDCE62005 primary reference enable. Set to 1-2 to power down oscillator, 2-3 to power up. | 2-3 |
| SJP6 | CDCE62005 power down. Set to 2-3 to enable CDC, set to 1-2 for FPGA control of power down mode. | 2-3 |
| SJP10 | DAC5672 clock source. Set to 1-2 for CDCE62005, set to 2-3 for FPGA source. | 2-3 |
| SJP8 | DAC5672 sleep mode. Set to 1-2 for FPGA control, set to 2-3 to keep device active. | 1-2 |
| JP2 | LNA power enable. Set to 1-2 to enable LNA regulator, 2-3 to disable regulator. | 2-3 |
| JP3 | USB device power regulator enable. Set to 1-2 to enable regulator, 2-3 to disable. | 1-2 |
| SJP9 | USB device power select. Set to 1-2 to power device from onboard regulator, set to 2-3 to power device from USB connector. | 1-2 |
| SW1 | Spare dip switches. Currently not used. | |
| SW3 | Turn I/Q correction on/off. Currently not used | |
| SW4 | Not Used | |
| SW5 | FPGA Reset. Reset all FPGA registers. | |
| SW6 | CDC Reset | |

# REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Original (February, 2010) to A Revision** **Page**

- Changed device name in document title to correspond with product name ..... 1
- Revised *Overview* section ..... 2
- Added Table 1 ..... 2
- Updated Figure 1 for clarity ..... 3
- Updated Figure 4 for clarity ..... 8

**Changes from A Revision (March 2010) to B Revision** **Page**

- Deleted TRF311 Att and IQ Offset values from the list following Figure 9 ..... 11
- Added 4 values in the control panel ..... 11
- Deleted Section 6. Optional Configurations ..... 13
- Deleted LED definitions, D8, D2, D9 in Section A.1 ..... 14
- Changed D4 definition in Section A.1 ..... 14
- Added D5: IQ correction enabled with blinking in Section A.1 ..... 14

**Changes from B Revision (June 2010) to C Revision** **Page**

- Changed the first two sentences of second paragraph in Section 1.2 with new sentence ..... 2
- Deleted third paragraph of Section 1.2 ..... 2
- Deleted section 1.3 and replaced it with section 4.5. ..... 3
- Added new Figure 2 ..... 4
- Changed Added new Figure 9 ..... 11

**Changes from C Revision (March 2013) to D Revision** **Page**

- Deleted "6-VDC power supply (provided)" from the list in Section 3.1 ..... 5
- Changed From: "Plug one end of the provided +6-VDC power supply" To: "Plug +6-VDC power supply" in the list in Section 4.1 ..... 6

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      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      **CAUTION**

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      **FCC Interference Statement for Class A EVM devices**

      *NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

**FCC Interference Statement for Class B EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:*

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

**Concerning EVMs Including Radio Transmitters:**

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

**Concernant les EVMs avec appareils radio:**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

**Concerning EVMs Including Detachable Antennas:**

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

**Concernant les EVMs avec antennes détachables**

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

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4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

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