

NTTFS3A08PZ

Power MOSFET

-20 V, -15 A, Single P-Channel, μ 8FL

Features

- Ultra Low $R_{DS(on)}$ to Minimize Conduction Losses
- μ 8FL 3.3 x 3.3 x 0.8 mm for Space Saving and Excellent Thermal Conduction
- ESD Protection Level of 5 kV per JESD22-A114
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Battery Switch
- High Side Load Switch
- Optimized for Power Management Applications for Portable Products such as Media Tablets, Ultrabook PCs and Cellphones

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	-20	V	
Gate-to-Source Voltage	V_{GS}	± 8	V	
Continuous Drain Current $R_{\theta JA}$ (Note 1)		$T_A = 25^\circ\text{C}$	-15	A
		$T_A = 85^\circ\text{C}$	-11	
Power Dissipation $R_{\theta JA}$ (Note 1)	P_D	2.3	W	
Continuous Drain Current $R_{\theta JA} \leq 10$ s (Note 1)		$T_A = 25^\circ\text{C}$	-22	A
		$T_A = 85^\circ\text{C}$	-16	
Power Dissipation $R_{\theta JA} \leq 10$ s (Note 1)	P_D	4.9	W	
Continuous Drain Current $R_{\theta JA}$ (Note 2)		$T_A = 25^\circ\text{C}$	-9	A
		$T_A = 85^\circ\text{C}$	-7	
Power Dissipation $R_{\theta JA}$ (Note 2)	P_D	0.84	W	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM}	-46	A
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$	
ESD (HBM, JESD22-A114)	V_{ESD}	5000	V	
Source Current (Body Diode)	I_S	-3	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.

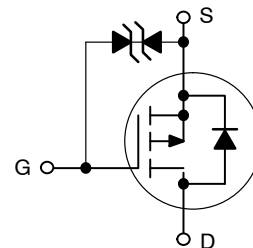


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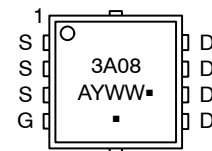
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
-20 V	6.7 m Ω @ -4.5 V	-15 A
	9.0 m Ω @ -2.5 V	

P-Channel MOSFET



WDFN8
(μ 8FL)
CASE 511AB

MARKING DIAGRAM



3A08 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTTFS3A08PZTAG	WDFN8 (Pb-Free)	1500 / Tape & Reel
NTTFS3A08PZTWG	WDFN8 (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTTFS3A08PZ

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	55	°C/W
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	148	
Junction-to-Ambient – ($t \leq 10$ s) (Note 3)	$R_{\theta JA}$	26	

3. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.

4. Surface-mounted on FR4 board using the minimum recommended pad size (40 mm², 1 oz. Cu).

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			6		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = -16\text{ V}$ $T_J = 25^\circ\text{C}$			-1	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 5\text{ V}$			± 5	μA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\ \mu\text{A}$	-0.4		-1.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			3.3		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -12\text{ A}$		4.9	6.7	m Ω
		$V_{GS} = -2.5\text{ V}, I_D = -10\text{ A}$		6.9	9.0	
Forward Transconductance	g_{FS}	$V_{DS} = -1.5\text{ V}, I_D = -8\text{ A}$		62		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = -10\text{ V}$		5000		pF
Output Capacitance	C_{oss}			600		
Reverse Transfer Capacitance	C_{rss}			540		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -8\text{ A}$		56		nC
Threshold Gate Charge	$Q_{G(TH)}$			2.0		
Gate-to-Source Charge	Q_{GS}			6.5		
Gate-to-Drain Charge	Q_{GD}			15.4		

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -8\text{ A}, R_G = 6.0\ \Omega$		13		ns
Rise Time	t_r			60		
Turn-Off Delay Time	$t_{d(off)}$			250		
Fall Time	t_f			170		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = -3\text{ A}$ $T_J = 25^\circ\text{C}$		-0.65	-1.0	V
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = -6\text{ A}$		207		ns
Charge Time	t_a			45		
Discharge Time	t_b			162		
Reverse Recovery Charge	Q_{RR}			234		

5. Pulse Test: pulse width = 300 μs , duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

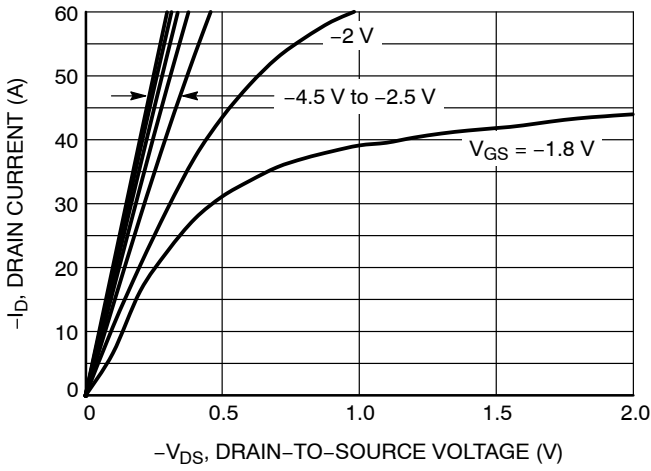


Figure 1. On-Region Characteristics

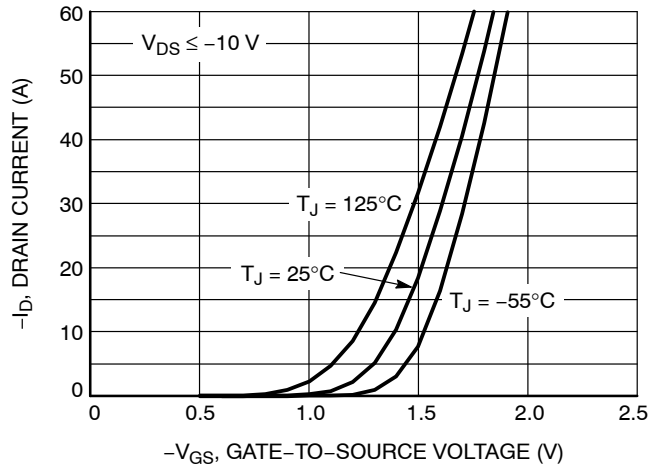


Figure 2. Transfer Characteristics

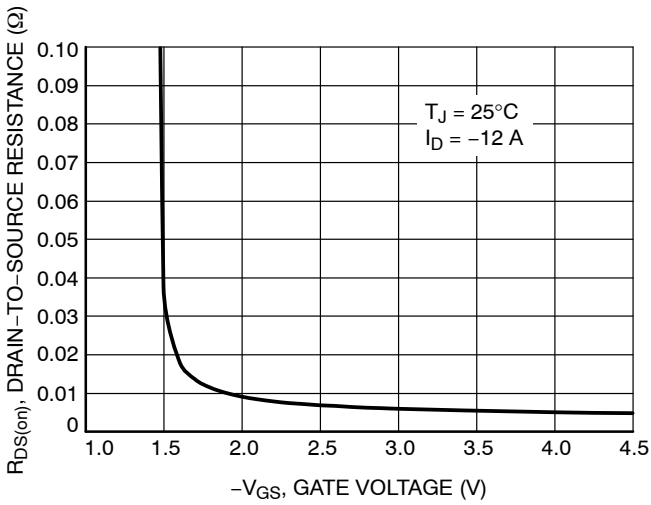


Figure 3. On-Resistance vs. Gate-to-Source Voltage

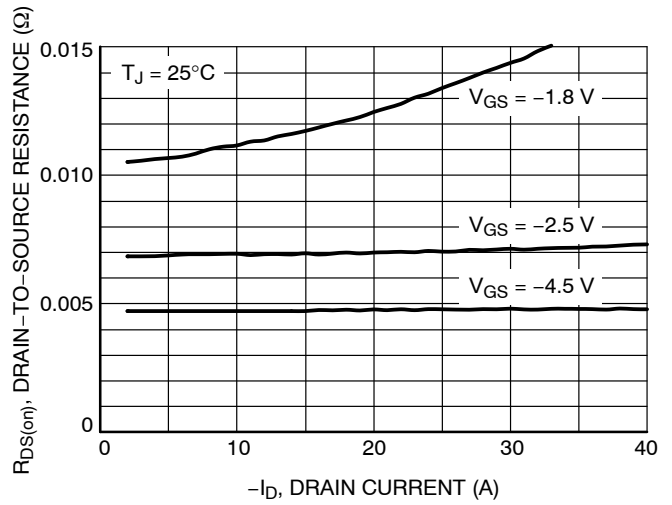


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

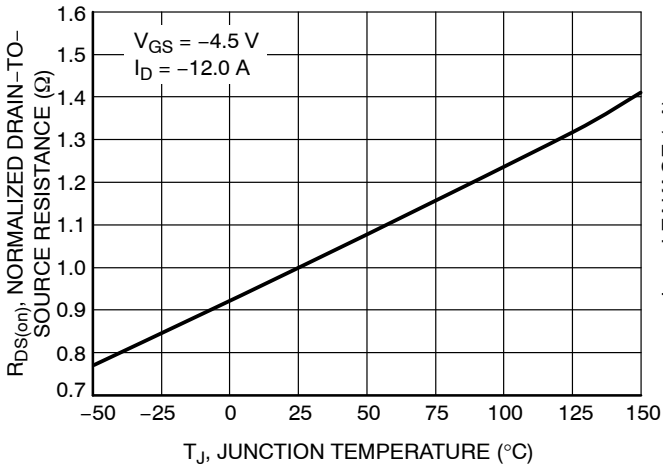


Figure 5. On-Resistance Variation with Temperature

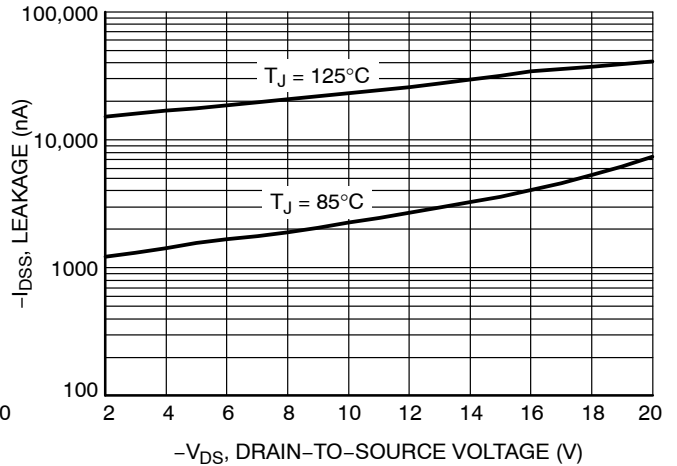


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

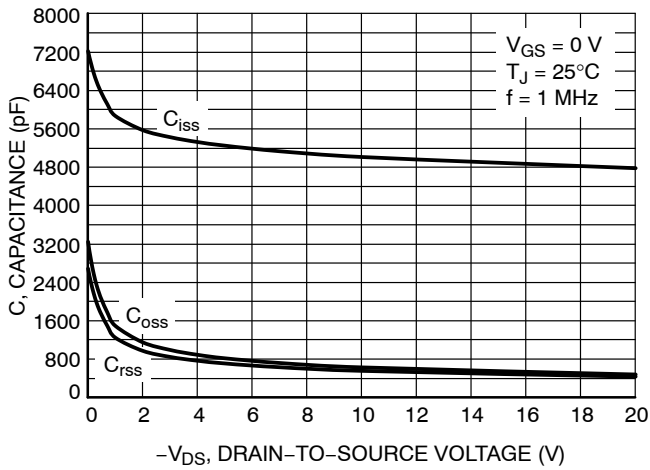


Figure 7. Capacitance Variation

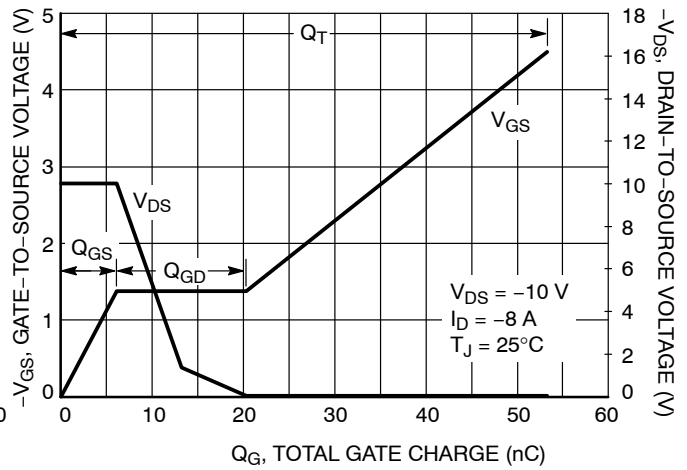


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

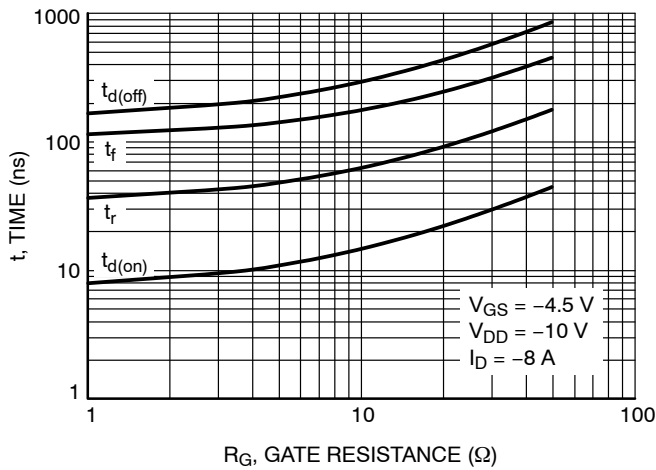


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

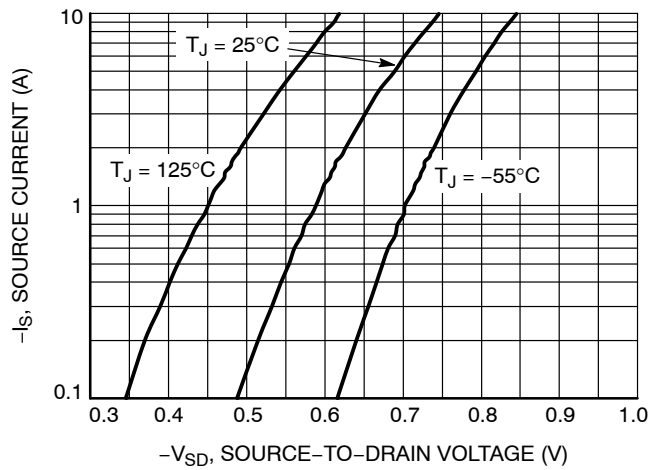


Figure 10. Diode Forward Voltage vs. Current

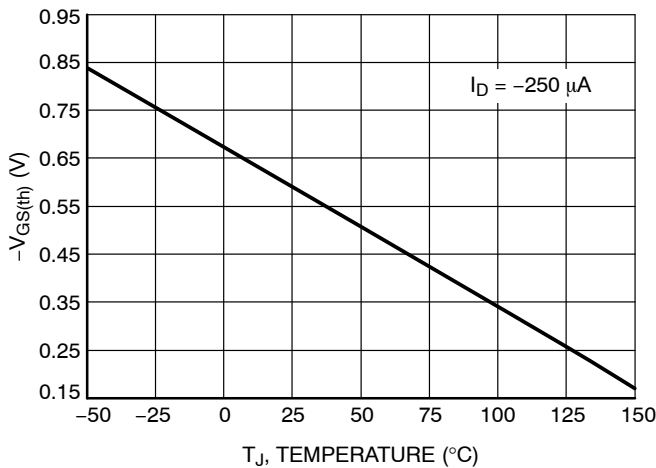


Figure 11. Threshold Voltage

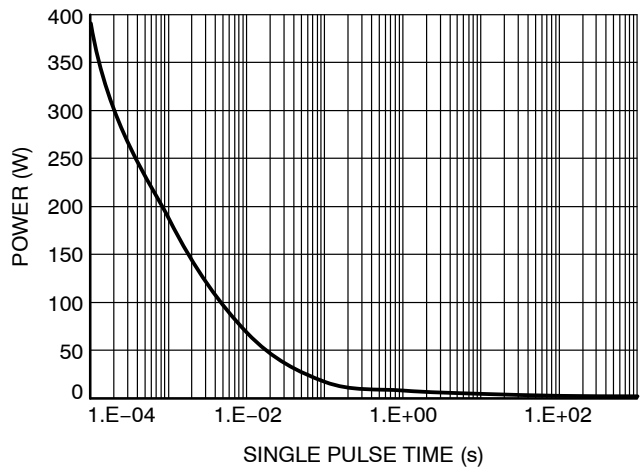


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS

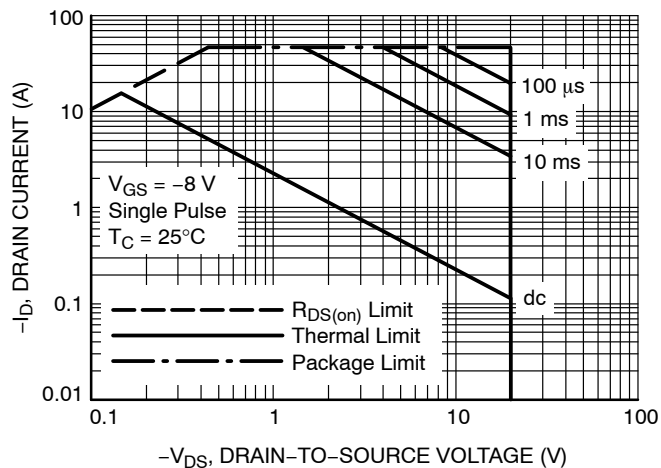


Figure 13. Maximum Rated Forward Biased Safe Operating Area

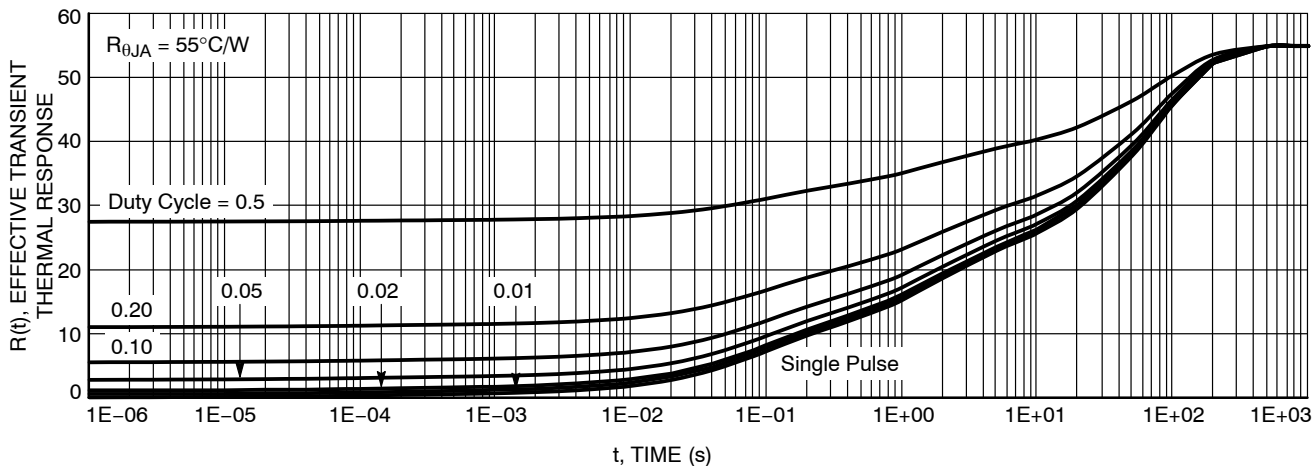


Figure 14. FET Thermal Response

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

WDFN8 3.3x3.3, 0.65P
CASE 511AB
ISSUE D

DATE 23 APR 2012



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30 BSC			0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30 BSC			0.130 BSC		
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e	0.65 BSC			0.026 BSC		
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0 °	---	12 °	0 °	---	12 °

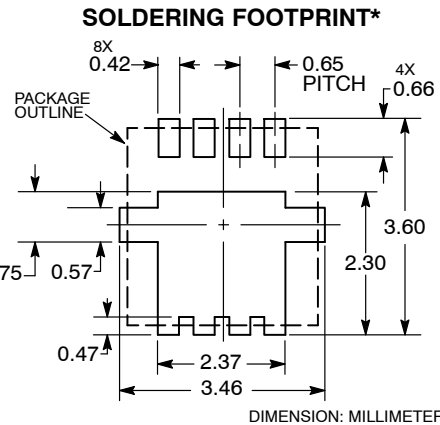


GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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