ADC12V170 12-Bit, 170 MSPS, 1.1 GHz Bandwidth A/D Converter with LVDS Outputs

Check for Samples: ADC12V170

FEATURES

- **1.1 GHz Full Power Bandwidth**
- **Internal Sample-and-Hold Circuit**
- **Internal Precision 1.0V Reference**
- **Single-Ended or Differential Clock Modes**
- **Clock Duty Cycle Stabilizer**
- **Dual +3.3V and +1.8V Supply Operation**
- **Power-Down and Sleep Modes**
- **Offset Binary or 2's Complement Output Data Format**
- **LVDS Outputs**
- **Pin-Compatible: ADC14V155**
- **48-Pin WQFN Package, (7x7x0.8mm, 0.5mm Pin-Pitch)**

APPLICATIONS

- **High IF Sampling Receivers**
- **Wireless Base Station Receivers**
- **Power Amplifier Linearization**
- **Multi-Carrier, Multi-Mode Receivers**
- **Test and Measurement Equipment**
- **Communications Instrumentation**
- **Radar Systems**

KEY SPECIFICATIONS

- **Resolution: 12 Bits**
- **Conversion Rate: 170 MSPS**
- **SNR (f_{IN} = 70 MHz): 67.2 dBFS (Typ)**
- **SFDR (f_{IN} = 70 MHz): 85.8 dBFS (Typ)**
- **ENOB (f_{IN} = 70 MHz): 10.9 Bits (Typ)**
- **Full Power Bandwidth: 1.1 GHZ (Typ)**
- **Power Consumption: 781 mW (Typ)**

DESCRIPTION

The ADC12V170 is a high-performance CMOS analog-to-digital converter with LVDS outputs. It is capable of converting analog input signals into 12-Bit digital words at rates up to 170 Mega Samples Per Second (MSPS). Data leaves the chip in a DDR (Dual Data Rate) format; this allows both edges of the output clock to be utilized while achieving a smaller package size. This converter uses a differential, pipelined architecture with digital error correction and an on-chip sample-and-hold circuit to minimize power consumption and the external component count, while providing excellent dynamic performance. A unique sample-and-hold stage yields a full-power bandwidth of 1.1 GHz. The ADC12V170 operates from dual +3.3V and +1.8V power supplies and consumes 781 mW of power at 170 MSPS.

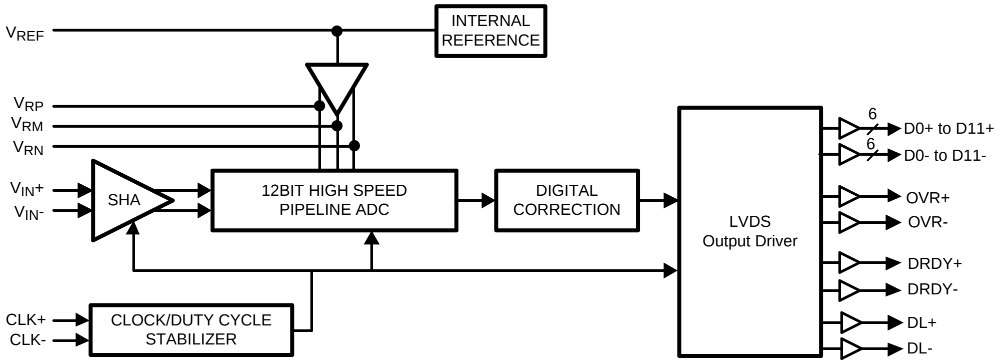
The separate +1.8V supply for the digital output interface allows lower power operation with reduced noise. A power-down feature reduces the power consumption to 15 mW while still allowing fast wake-up time to full operation. In addition there is a sleep feature which consumes 50 mW of power and has a faster wake-up time.

The differential inputs provide a full scale differential input swing equal to 2 times the reference voltage. A stable 1.0V internal voltage reference is provided, or the ADC12V170 can be operated with an external reference.

Clock mode (differential versus single-ended) and output data format (offset binary versus 2's complement) are pin-selectable. A duty cycle stabilizer maintains performance over a wide range of input clock duty cycles.

The ADC12V170 is pin-compatible with the ADC14V155. It is available in a 48-lead WQFN package and operates over the industrial temperature range of −40°C to +85°C.

Block Diagram



Connection Diagram

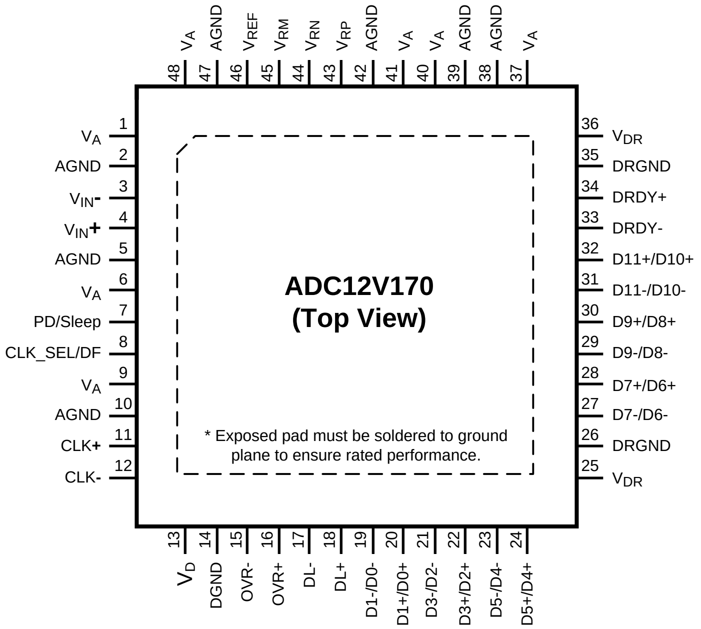
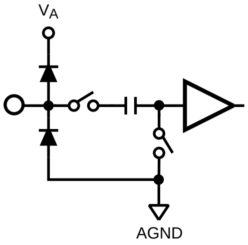
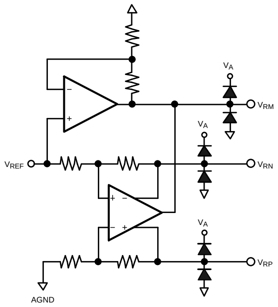
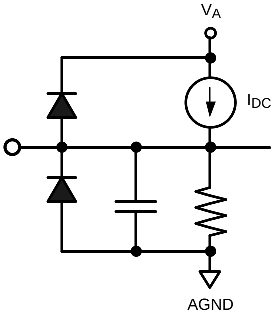
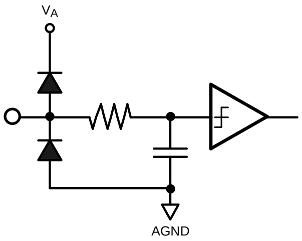
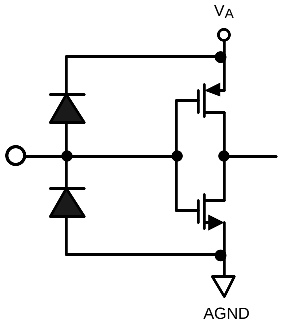
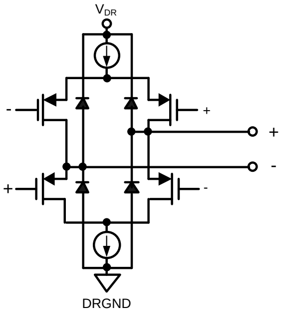


Figure 1. 48-Lead WQFN
See RHS0048A Package

PIN DESCRIPTIONS

Pin No.	Symbol	Equivalent Circuit	Description
		ANALOG I/O	
3	V_{IN}−		Differential analog input pins. The differential full-scale input signal level is two times the reference voltage with each input pin signal centered on a common mode voltage, V_{CM}.
4	V_{IN}+		
43	V_{RP}		These pins should each be bypassed to AGND with a low ESL (equivalent series inductance) 0.1 µF capacitor placed very close to the pin to minimize stray inductance. A 0.1 µF capacitor should be placed between V_{RP} and V_{RN} as close to the pins as possible, and a 10 µF capacitor should be placed in parallel. The 0.1 µFcapacitor should be as small as possible (preferably 0201). V_{RP} and V_{RN} should not be loaded. V_{RM} may be loaded to 1mA for use as a temperature stable 1.5V reference. It is recommended to use V_{RM} to provide the common mode voltage, V_{CM}, for the differential analog inputs, V_{IN}+ and V_{IN}−.
45	V_{RM}		
44	V_{RN}		
46	V_{REF}		This pin can be used as either the +1.0V internal reference voltage output (internal reference operation) or as the external reference voltage input (external reference operation). To use the internal reference, V_{REF} should be decoupled to AGND with a 0.1 µF, low equivalent series inductance (ESL) capacitor. In this mode, V_{REF} defaults as the output for the internal 1.0V reference. To use an external reference, overdrive this pin with a low noise external reference voltage. The input impedance looking into this pin is 9kΩ. Therefore, to overdrive this pin, the output impedance of the external reference source should be << 9kΩ. This pin should not be used to source or sink current. The full scale differential input voltage range is 2 * V_{REF}.
8	CLK_SEL/DF		This is a four-state pin controlling the input clock mode and output data format. CLK_SEL/DF = V_A, CLK+ and CLK− are configured as a differential clock input. The output data format is 2's complement. CLK_SEL/DF = (2/3)*V_A, CLK+ and CLK− are configured as a differential clock input. The output data format is offset binary. CLK_SEL/DF = (1/3)*V_A, CLK+ is configured as a single-ended clock input and CLK− should be tied to AGND. The output data format is 2's complement. CLK_SEL/DF = AGND, CLK+ is configured as a single-ended clock input and CLK− should be tied to AGND. The output data format is offset binary.
7	PD/Sleep		This is a three-state input controlling Power Down and Sleep modes. PD/Sleep = V_A, Power Down is enabled. In the Power Down state only the reference voltage circuitry remains active and power dissipation is reduced. PD/Sleep = V_A/2, Sleep mode is enabled. Sleep mode is similar to Power Down mode - it consumes more power but has a faster recovery time. PD/Sleep = AGND, Normal operation.

PIN DESCRIPTIONS (continued)

Pin No.	Symbol	Equivalent Circuit	Description
11	CLK+		The clock input pins can be configured to accept either a single-ended or a differential clock input signal. When the single-ended clock mode is selected through CLK_SEL/DF (pin 8), connect the clock input signal to the CLK+ pin and connect the CLK− pin to AGND. When the differential clock mode is selected through CLK_SEL/DF (pin 8), connect the positive and negative clock inputs to the CLK+ and CLK− pins, respectively. The analog input is sampled on the falling edge of the clock input.
12	CLK−		
DIGITAL I/O			
19 20 21 22 23 24 27 28 29 30 31 32	D1-/D0- D1+/D0+ D3-/D2- D3+/D2+ D5-/D4- D5+/D4+ D7-/D6- D7+/D6+ D9-/D8- D9+/D8+ D11-/D10- D11+/D10+		LVDS digital data output pins that make up the 12-Bit conversion result. The data is provided in a 2:1 multiplexed manner synchronous to DRDY+/-. The even bits should be captured with the rising edge of DRDY and the odd bits should be captured with the falling edge of DRDY. D0 is the LSB. D11 is the MSB.
15 16	OVR- OVR+		Over-Range Indicator. This LVDS output is set HIGH when the input amplitude goes outside the expected 12-Bit conversion range (0 to 4095).
33 34	DRDY+ DRDY-		Data Ready Strobe. This LVDS output is used to clock the output data. It has the same frequency as the sampling clock. One half of the data word is output with each edge of this signal - thus transferring a complete 12-bit word in each cycle of this clock. The even bits should be captured with the rising edge of DRDY and the odd bits should be captured with the falling edge of DRDY.
17, 18	DL-/DL+		LVDS low logic level.
ANALOG POWER			
1, 6, 9, 37, 40, 41, 48	V_A		Positive analog supply pins. These pins should be connected to a quiet +3.3V source and be bypassed to AGND with 0.01 µF and 0.1 µF capacitors located close to the power pins.
2, 5, 10, 38, 39, 42, 47, Exposed Pad	AGND		The ground return for the analog supply. Note: Exposed pad on bottom of package must be soldered to ground plane to ensure rated performance.
DIGITAL POWER			
13	V_D		Positive digital supply pin. This pin should be connected to a quiet +3.3V source and be bypassed to DGND with a 0.01 µF and 0.1 µF capacitor located close to the power pin.
14	DGND		The ground return for the digital supply.
25, 36	V_{DR}		Positive driver supply pin for the output drivers. This pin should be connected to a quiet voltage source of +1.8V and be bypassed to DRGND with 0.01 µF and 0.1 µF capacitors located close to the power pins.
26, 35	DRGND		The ground return for the digital output driver supply. These pins should be connected to the system digital ground, but not be connected in close proximity to the ADC's DGND or AGND pins. See Layout and Grounding for more details.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)(4)(5)

Supply Voltage (V_A, V_D)		−0.3V to 4.2V
Supply Voltage (V_{DR})		−0.3V to 2.35V
$\|V_A – V_D\|$		≤ 100 mV
Voltage on Any Input Pin (Not to exceed 4.2V)		−0.3V to (V_A +0.3V)
Voltage on Any Output Pin (Not to exceed 2.35V)		-0.3V to (V_{DR} +0.2V)
Input Current at Any Pin other than Supply Pins(6)		±5 mA
Package Input Current(6)		±50 mA
Max Junction Temp (T_J)		+150°C
Thermal Resistance (θ_{JA})		24°C/W
Package Dissipation at T_A = 25°C(7)		5.2W
ESD Rating	Human Body Model(8)	2000 V
	Machine Model(8)	200 V
	Charge Device Model	1000 V
Storage Temperature		−65°C to +150°C

(1) All voltages are measured with respect to GND = AGND = DGND = DRGND = 0V, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is ensured to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Converter Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.
(3) Soldering process must comply with Texas Instruments' Reflow Temperature Profile specifications. Refer to www.ti.com/packaging.
(4) Reflow temperature profiles are different for lead-free and non-lead-free packages.
(5) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(6) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or V_{IN} > V_A), the current at that pin should be limited to ±5 mA. The ±50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of ±5 mA to 10.
(7) The maximum allowable power dissipation is dictated by $T_{J,max}$, the junction-to-ambient thermal resistance, (θ_{JA}), and the ambient temperature, (T_A), and can be calculated using the formula $P_{D,max} = (T_{J,max} - T_A)/\theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions should always be avoided.
(8) Human Body Model is 100 pF discharged through a 1.5 kΩ resistor. Machine Model is 220 pF discharged through 0 Ω

Operating Ratings(1)(2)

Operating Temperature	−40°C ≤ T_A ≤ +85°C
Supply Voltage (V_A, V_D)	+3.0V to +3.6V
Output Driver Supply (V_{DR})	+1.6V to +2.0V
Clock Inputs (CLK+, CLK-)	−0.05V to (V_A + 0.05V)
Clock Duty Cycle	30/70 %
Analog Input Pins (V_{IN}+, V_{IN}-)	0V to 2.6V
Analog Input Common Mode (V_{CM})	1.4V to 1.6V
|AGND-DGND|	≤100mV

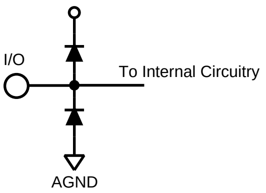
(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is ensured to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Converter Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.
(2) All voltages are measured with respect to GND = AGND = DGND = DRGND = 0V, unless otherwise specified.

Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply: V_{IN} = -1dBFS, AGND = DGND = DRGND = 0V, $V_A = V_D$ = +3.3V, V_{DR} = +1.8V, Internal V_{REF} = +1.0V, f_{CLK} = 170 MHz, $V_{CM} = V_{RM}$, C_L = 5 pF/pin, Single-Ended Clock Mode, Offset Binary Format. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C(1)(2)(3)(4)

Symbol	Parameter	Conditions	Typical(5)	Limits	Units (Limits)
STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes			**12**	Bits (min)
INL	Integral Non Linearity(6)	Full Scale Input	±0.5	**1.9**	LSB (max)
				-1.9	LSB (min)
DNL	Differential Non Linearity	Full Scale Input	±0.3	**1.0**	LSB (max)
				-1.0	LSB (min)
PGE	Positive Gain Error		+0.74	**3.30**	%FS (max)
				-2.10	%FS (min)
NGE	Negative Gain Error		-0.33	**2.10**	%FS (max)
				-2.85	%FS (min)
TC GE	Gain Error Tempco	−40°C ≤ T_A ≤ +85°C	+8.0		ppm/°C
V_{OFF}	Offset Error ($V_{IN}+ = V_{IN}-$)		−0.11	**0.75**	%FS (max)
				-0.95	%FS (min)
TC V_{OFF}	Offset Error Tempco	−40°C ≤ T_A ≤ +85°C	+0.5		ppm/°C
	Under Range Output Code		0	**0**	
	Over Range Output Code		4095	**4095**	
REFERENCE AND ANALOG INPUT CHARACTERISTICS					
V_{CM}	Common Mode Input Voltage		1.5		V
V_{RM}	Reference Ladder Midpoint Output Voltage	Maximum output load = 1 mA	1.5		V
C_{IN}	V_{IN} Input Capacitance (each pin to GND)(7)	V_{IN} = 1.5 Vdc ± 0.5 V (V_{CM}) (CLK LOW)	6		pF
		(CLK HIGH)	9		pF
V_{REF}	Reference Voltage(8)		1.00		V
	Reference Input Resistance		9		kΩ

(1) The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited per(4). However, errors in the A/D conversion can occur if the input goes above 2.6V or below GND as described in the Operating Ratings section.



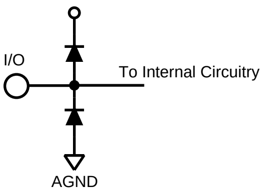
(2) To ensure accuracy, it is required that $|V_A–V_D| \le$ 100 mV and separate bypass capacitors are used at each power supply pin.
(3) With the test condition for V_{REF} = +1.0V ($2V_{P-P}$ differential input), the 12-Bit LSB is 488.3 µV.
(4) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or $V_{IN} > V_A$), the current at that pin should be limited to ±5 mA. The ±50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of ±5 mA to 10.
(5) Typical figures are at T_A = 25°C and represent most likely parametric norms at the time of product characterization. The typical specifications are not ensured.
(6) Integral Non Linearity is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive and negative full-scale.
(7) The input capacitance is the sum of the package/pin capacitance and the sample and hold circuit capacitance.
(8) Optimum performance will be obtained by keeping the reference input in the 0.9V to 1.1V range. The LM4051CIM3-ADJ (SOT-23 package) is recommended for external reference applications.

Dynamic Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply: V_{IN} = -1dBFS, AGND = DGND = DRGND = 0V, $V_A = V_D$ = +3.3V, V_{DR} = +1.8V, Internal V_{REF} = +1.0V, f_{CLK} = 170 MHz, $V_{CM} = V_{RM}$, C_L = 5 pF/pin, Single-Ended Clock Mode, Offset Binary Format. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C(1)(2)(3)(4)

Symbol	Parameter	Conditions	Typical(5)	Limits	Units (Limits)
DYNAMIC CONVERTER CHARACTERISTICS, A_{IN}= -1dBFS					
FPBW	Full Power Bandwidth	-1 dBFS Input, −3 dB Corner	1.1		GHz
SNR	Signal-to-Noise Ratio	f_{IN} = 10 MHz	67.9		dBFS
		f_{IN} = 70 MHz	67.2	**66.0**	dBFS
		f_{IN} = 150 MHz	67.1		dBFS
		f_{IN} = 250 MHz	66.9		dBFS
		f_{IN} = 400 MHz	65.4		dBFS
SFDR	Spurious Free Dynamic Range	f_{IN} = 10 MHz	85.0		dBFS
		f_{IN} = 70 MHz	85.8	**74.0**	dBFS
		f_{IN} = 150 MHz	85.0		dBFS
		f_{IN} = 250 MHz	83.0		dBFS
		f_{IN} = 400 MHz	71.6		dBFS
ENOB	Effective Number of Bits	f_{IN} = 10 MHz	11.0		Bits
		f_{IN} = 70 MHz	10.9	**10.5**	Bits
		f_{IN} = 150 MHz	10.8		Bits
		f_{IN} = 250 MHz	10.7		Bits
		f_{IN} = 400 MHz	10.3		Bits
THD	Total Harmonic Disortion	f_{IN} = 10 MHz	-82.7		dBFS
		f_{IN} = 70 MHz	-82.3	**-72.0**	dBFS
		f_{IN} = 150 MHz	-80.7		dBFS
		f_{IN} = 250 MHz	-79.6		dBFS
		f_{IN} = 400 MHz	-68.8		dBFS

(1) The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited per(4). However, errors in the A/D conversion can occur if the input goes above 2.6V or below GND as described in the Operating Ratings section.



(2) To ensure accuracy, it is required that $|V_A–V_D| \le$ 100 mV and separate bypass capacitors are used at each power supply pin.
(3) With the test condition for V_{REF} = +1.0V ($2V_{P-P}$ differential input), the 12-Bit LSB is 488.3 µV.
(4) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or $V_{IN} > V_A$), the current at that pin should be limited to ±5 mA. The ±50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of ±5 mA to 10.
(5) Typical figures are at T_A = 25°C and represent most likely parametric norms at the time of product characterization. The typical specifications are not ensured.

Dynamic Converter Electrical Characteristics (continued)

Unless otherwise specified, the following specifications apply: V_{IN} = -1dBFS, AGND = DGND = DRGND = 0V, V_A = V_D = +3.3V, V_{DR} = +1.8V, Internal V_{REF} = +1.0V, f_{CLK} = 170 MHz, V_{CM} = V_{RM}, C_L = 5 pF/pin, Single-Ended Clock Mode, Offset Binary Format. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \leq T_A \leq T_{MAX}$.** All other limits apply for T_A = 25°C(1)(2)(3)(4)

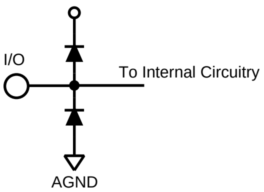
Symbol	Parameter	Conditions	Typical(5)	Limits	Units (Limits)
H2	Second Harmonic Distortion	f_{IN} = 10 MHz	-95.0		dBFS
		f_{IN} = 70 MHz	-88.4	**-77.0**	dBFS
		f_{IN} = 150 MHz	-87.4		dBFS
		f_{IN} = 250 MHz	-83.0		dBFS
		f_{IN} = 400 MHz	-71.6		dBFS
H3	Third Harmonic Distortion	f_{IN} = 10 MHz	-85.0		dBFS
		f_{IN} = 70 MHz	-86.8	**-74.0**	dBFS
		f_{IN} = 150 MHz	-85.0		dBFS
		f_{IN} = 250 MHz	-88.1		dBFS
		f_{IN} = 400 MHz	-73.7		dBFS
SINAD	Signal-to-Noise and Distortion Ratio	f_{IN} = 10 MHz	67.7		dBFS
		f_{IN} = 70 MHz	67.1	**65.1**	dBFS
		f_{IN} = 150 MHz	67.0		dBFS
		f_{IN} = 250 MHz	66.7		dBFS
		f_{IN} = 400 MHz	63.8		dBFS

Logic and Power Supply Electrical Characteristics

Unless otherwise specified, the following specifications apply: V_{IN} = -1 dBFS, AGND = DGND = DRGND = 0V, $V_A = V_D$ = +3.3V, V_{DR} = +1.8V, Internal V_{REF} = +1.0V, f_{CLK} = 170 MHz, $V_{CM} = V_{RM}$, C_L = 5 pF/pin, Single-Ended Clock Mode, Offset Binary Format. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \leq T_A \leq T_{MAX}$.** All other limits apply for T_A = 25°C(1)(2)(3)(4)

Symbol	Parameter	Conditions	Typical(5)	Limits	Units (Limits)
CLK INPUT CHARACTERISTICS					
$V_{IN(1)}$	Logical "1" Input Voltage	V_D = 3.6V		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	V_D = 3.0V		**0.8**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 3.3V	10		µA
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0V	−10		µA
C_{IN}	Input Capacitance		5		pF
DIGITAL OUTPUT CHARACTERISTICS (D0+/- to D11+/-, DRDY+/-, OVR+/-, DL+/-)					
V_{OD}	LVDS differential output voltage	See(6)	350	**250**	mV_{P-P} (min)
				450	mV_{P-P} (max)
V_{OS}	The common-mode voltage of the LVDS output	See(6)	1.22	**1.125**	V (min)
				1.375	V (max)
R_L	Intended Load Resistance		100		Ω
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	Full Operation	221	**289**	mA (max)
I_D	Digital Supply Current	Full Operation	15	**16**	mA (max)
I_{DR}	Digital Output Supply Current	Full Operation	31.5		mA
	Power Consumption	Excludes I_{DR}	781		mW
	Power Down Power Consumption		15		mW
	Sleep Power Consumption		50		mW

(1) The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited per(4). However, errors in the A/D conversion can occur if the input goes above 2.6V or below GND as described in the Operating Ratings section.



(2) To ensure accuracy, it is required that $|V_A–V_D| \leq$ 100 mV and separate bypass capacitors are used at each power supply pin.
(3) With the test condition for V_{REF} = +1.0V ($2V_{P-P}$ differential input), the 12-Bit LSB is 488.3 µV.
(4) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or $V_{IN} > V_A$), the current at that pin should be limited to ±5 mA. The ±50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of ±5 mA to 10.
(5) Typical figures are at T_A = 25°C and represent most likely parametric norms at the time of product characterization. The typical specifications are not ensured.
(6) This test parameter is ensured by design and characterization.

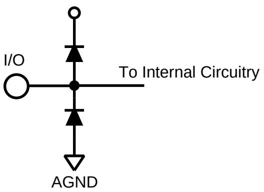
Timing and AC Characteristics

Unless otherwise specified, the following specifications apply: V_{IN} = -1dBFS, AGND = DGND = DRGND = 0V, $V_A = V_D$ = +3.3V, V_{DR} = +1.8V, Internal V_{REF} = +1.0V, f_{CLK} = 170 MHz, $V_{CM} = V_{RM}$, C_L = 5 pF/pin, Single-Ended Clock Mode, Offset Binary Format. Typical values are for T_A = 25°C. Timing measurements are taken at 50% of the signal amplitude. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C(1)(2)(3)(4)

Symbol	Parameter	Conditions	Typical(5)	Limits	Units (Limits)
	Maximum Clock Frequency			**170**	MHz (max)
	Minimum Clock Frequency			**5**	MHz (min)
	Clock High Time		2.7		ns
	Clock Low Time		2.7		ns
	Conversion Latency			**7.5**	Clock Cycles
t_{OD}	Output Delay of CLK to DATA	Relative to falling edge of CLK	3.8		ns
t_{DV}	Data Output Valid Time	Time output data is valid before the output edge of DRDY(6)	1.3	**0.9**	ns (min)
t_{DNV}	Data Output Not Valid Time	Time till output data is not valid after the output edge of DRDY(6)	1.3	**0.9**	ns (min)
t_{AD}	Aperture Delay		0.5		ns
	Aperture Jitter		0.08		ps rms
	Power Down Recovery Time	0.1 µF to GND on pins 43, 44; 10 µF and 0.1 µF between pins 43, 44; 0.1 µF and 10 µF to GND on pins 45, 46	3.0		ms
	Sleep Recovery Time	0.1 µF to GND on pins 43, 44; 10 µF and 0.1 µF between pins 43, 44; 0.1 µF and 10 µF to GND on pins 45, 46	100		µs

---

(1) The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited per(4). However, errors in the A/D conversion can occur if the input goes above 2.6V or below GND as described in the Operating Ratings section.



(2) To ensure accuracy, it is required that $|V_A – V_D| \le$ 100 mV and separate bypass capacitors are used at each power supply pin.

(3) With the test condition for V_{REF} = +1.0V ($2V_{P-P}$ differential input), the 12-Bit LSB is 488.3 µV.

(4) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or $V_{IN} > V_A$), the current at that pin should be limited to ±5 mA. The ±50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of ±5 mA to 10.

(5) Typical figures are at T_A = 25°C and represent most likely parametric norms at the time of product characterization. The typical specifications are not ensured.

(6) This test parameter is ensured by design and characterization.

Specification Definitions

APERTURE DELAY is the time after the falling edge of the clock to when the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

CLOCK DUTY CYCLE is the ratio of the time during one cycle that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

COMMON MODE VOLTAGE (V_{CM}) is the common DC voltage applied to both input terminals of the ADC.

CONVERSION LATENCY is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. Data for any given sample is available at the output pins the Pipeline Delay plus the Output Delay after the sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated as:

$$\text{Gain Error} = \text{Positive Full Scale Error} - \text{Negative Full Scale Error} \quad (1)$$

It can also be expressed as Positive Gain Error and Negative Gain Error, which are calculated as:

$$\text{PGE} = \text{Positive Full Scale Error - Offset Error NGE} = \text{Offset Error - Negative Full Scale Error} \quad (2)$$

INTEGRAL NON LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the intermodulation products to the total power in the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is $V_{FS}/2^n$, where “V_{FS}” is the full scale input voltage and “n” is the ADC resolution in bits.

LVDS DIFFERENTIAL OUTPUT VOLTAGE (V_{OD}) is the absolute value of the differnece between V_{DX+} and V_{DX-} outputs; each measured with respect to Ground.

LVDS OUTPUT OFFSET VOLTAGE (V_{OS}) is the midpoint between the DX+ and DX- pins' output voltages; i.e., $[V_{Dx+} + V_{DX-}]/2$.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC12V170 is ensured not to have any missing codes.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL SCALE ERROR is the difference between the actual first code transition and its ideal value of ½ LSB above negative full scale.

OFFSET ERROR is the difference between the two input voltages $[(V_{IN}+) – (V_{IN}-)]$ required to cause a transition from code 2047 to 2048.

OUTPUT DELAY is the time delay after the falling edge of the clock before the data update is presented at the output pins.

PIPELINE DELAY (LATENCY) See CONVERSION LATENCY.

POSITIVE FULL SCALE ERROR is the difference between the actual last code transition and its ideal value of 1½ LSB below positive full scale.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well the ADC rejects a change in the power supply voltage. PSRR is the ratio of the Full-Scale output of the ADC with the supply at the minimum DC supply limit to the Full-Scale output of the ADC with the supply at the maximum DC supply limit, expressed in dB.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$\mathrm{THD} = 20 \times \log \sqrt{\frac{f_2^{\,2} + \ldots + f_{10}^{\,2}}{f_1^{\,2}}} \tag{3}$$

where f_1 is the RMS power of the fundamental (output) frequency and f_2 through f_{10} are the RMS power of the first 9 harmonic frequencies in the output spectrum.

SECOND HARMONIC DISTORTION (2ND HARM) is the difference expressed in dB, between the RMS power in the input frequency at the output and the power in its 2nd harmonic level at the output.

THIRD HARMONIC DISTORTION (3RD HARM) is the difference, expressed in dB, between the RMS power in the input frequency at the output and the power in its 3rd harmonic level at the output.

Timing Diagram

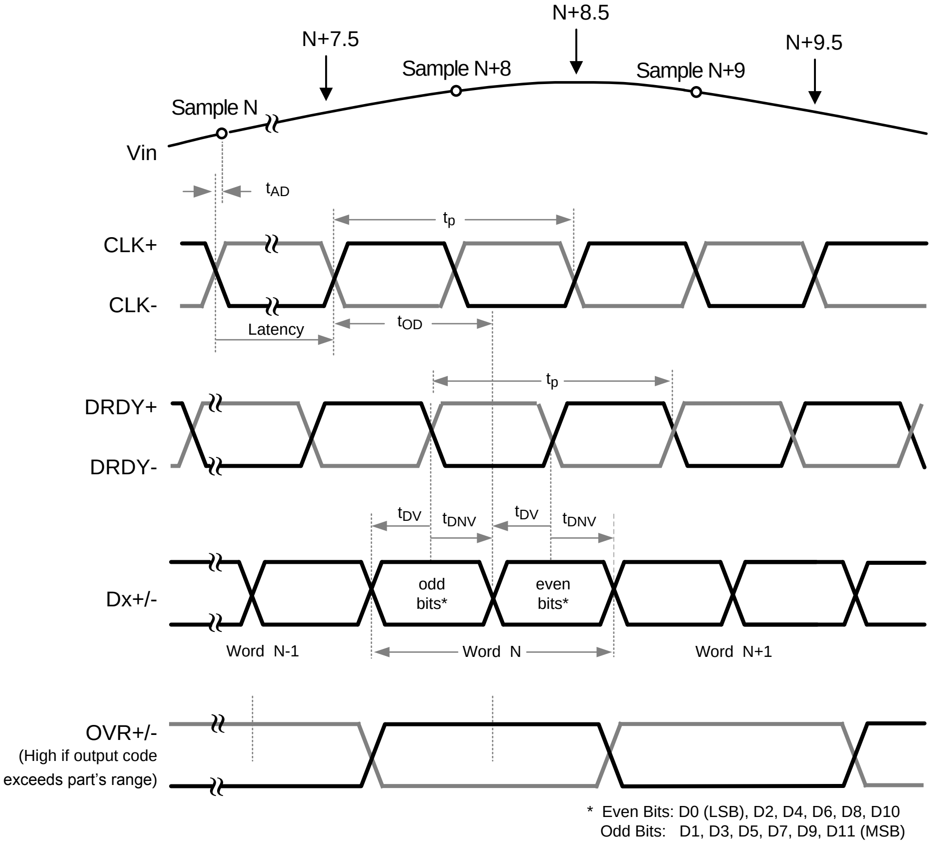


Figure 2. Output Timing

Transfer Characteristic

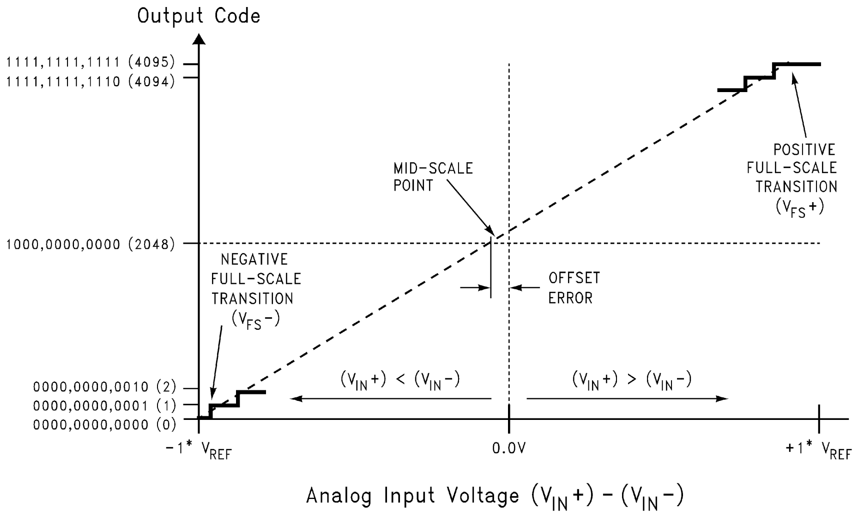


Figure 3. Transfer Characteristic (Offset Binary Format)

Typical Performance Characteristics, DNL, INL

Unless otherwise specified, the following specifications apply: V_{IN} = -1dBFS, AGND = DGND = DRGND = 0V, $V_A = V_D$ = +3.3V, V_{DR} = +1.8V, Internal V_{REF} = +1.0V, f_{CLK} = 170 MHz, $V_{CM} = V_{RM}$, C_L = 5 pF/pin, Single-Ended Clock Mode, Offset Binary Format. Typical values are for T_A = 25°C (1) (2) (3) (4)

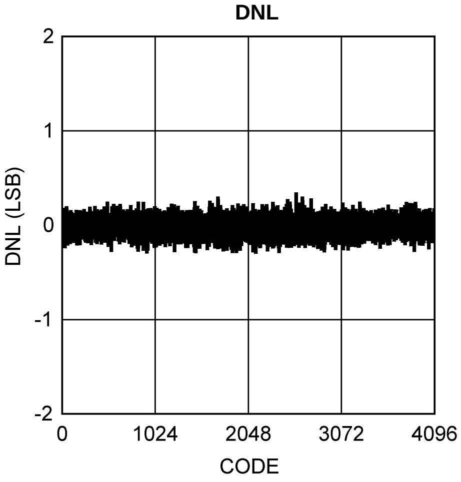


Figure 4.

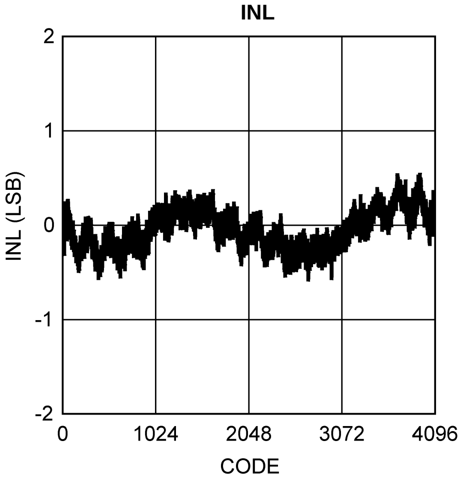
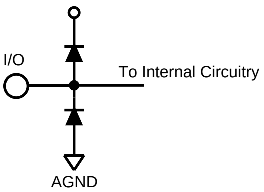


Figure 5.

(1) The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited per(4). However, errors in the A/D conversion can occur if the input goes above 2.6V or below GND as described in the Operating Ratings section.



(2) To ensure accuracy, it is required that $|V_A–V_D| \leq$ 100 mV and separate bypass capacitors are used at each power supply pin.

(3) With the test condition for V_{REF} = +1.0V ($2V_{P-P}$ differential input), the 12-Bit LSB is 488.3 µV.

(4) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or $V_{IN} > V_A$), the current at that pin should be limited to ±5 mA. The ±50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of ±5 mA to 10.

Typical Performance Characteristics, Dynamic Performance

Unless otherwise specified, the following specifications apply: V_{IN} = -1dBFS, AGND = DGND = DRGND = 0V, $V_A = V_D$ = +3.3V, V_{DR} = +1.8V, Internal V_{REF} = +1.0V, f_{CLK} = 170 MHz, f_{IN} = 70 MHz, $V_{CM} = V_{RM}$, C_L = 5 pF/pin, Single-Ended Clock Mode, Offset Binary Format. Typical values are for T_A = 25°C.

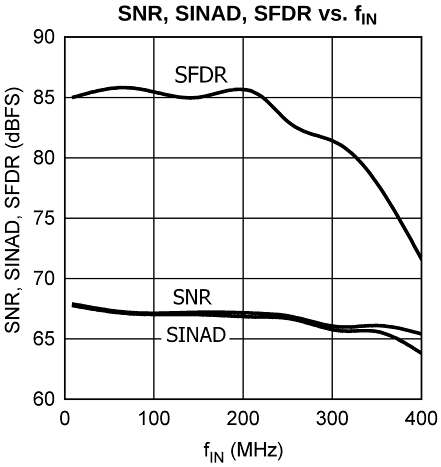


Figure 6.

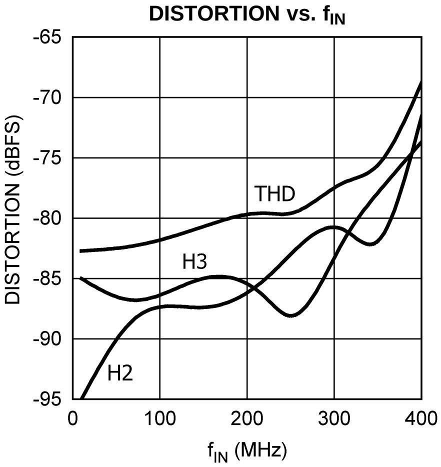


Figure 7.

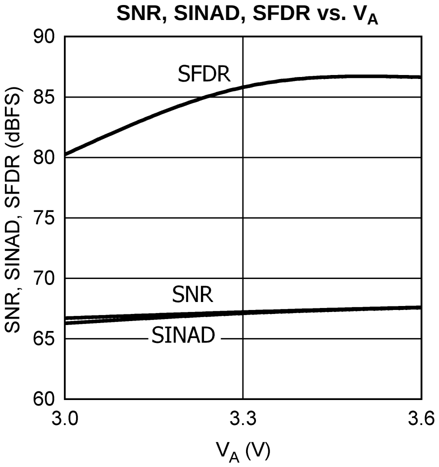


Figure 8.

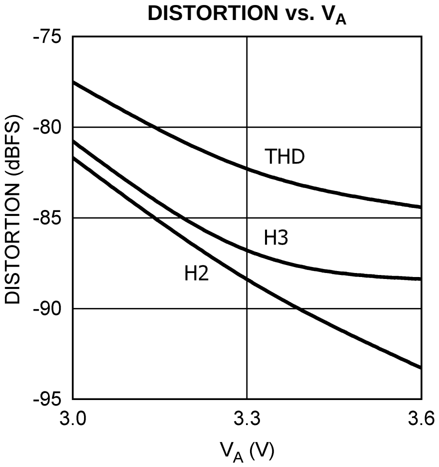


Figure 9.

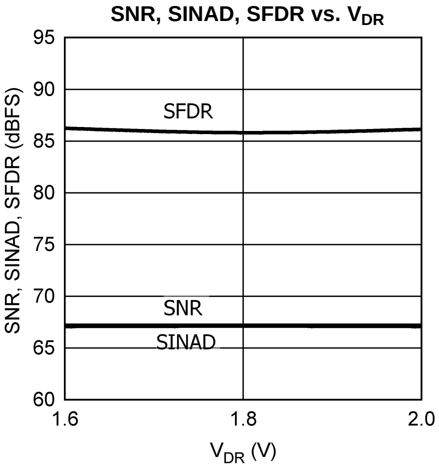


Figure 10.

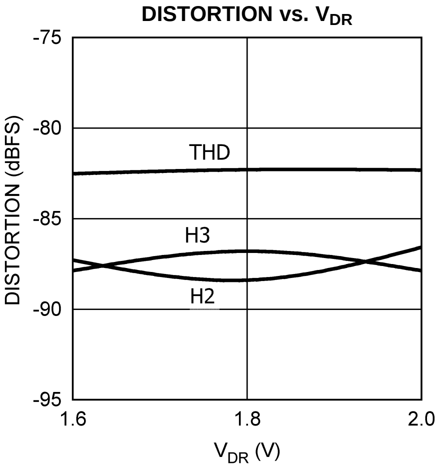


Figure 11.

Typical Performance Characteristics, Dynamic Performance (continued)

Unless otherwise specified, the following specifications apply: V_{IN} = -1dBFS, AGND = DGND = DRGND = 0V, V_A = V_D = +3.3V, V_{DR} = +1.8V, Internal V_{REF} = +1.0V, f_{CLK} = 170 MHz, f_{IN} = 70 MHz, V_{CM} = V_{RM}, C_L = 5 pF/pin, Single-Ended Clock Mode, Offset Binary Format. Typical values are for T_A = 25°C.

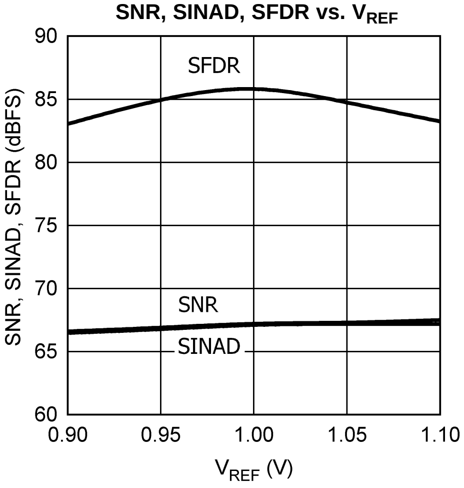


Figure 12.

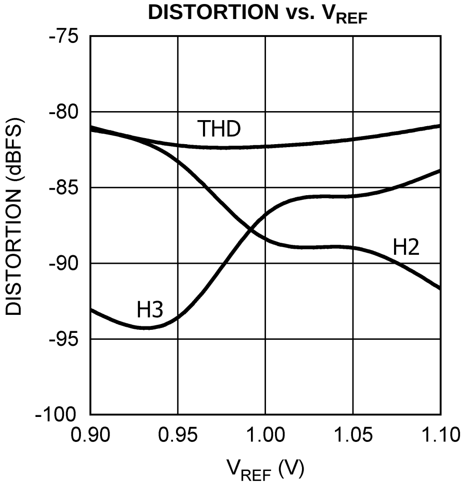


Figure 13.

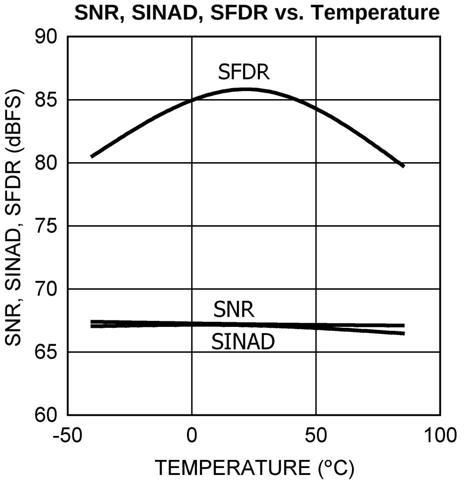


Figure 14.

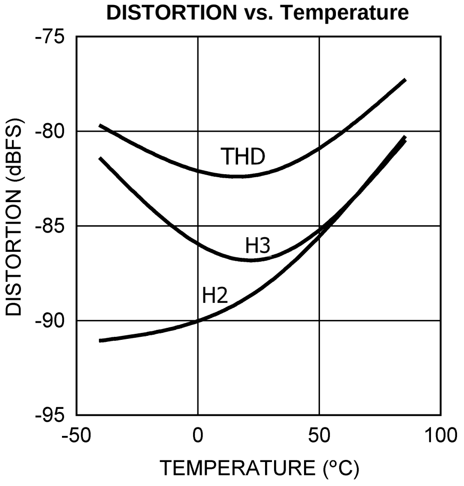


Figure 15.

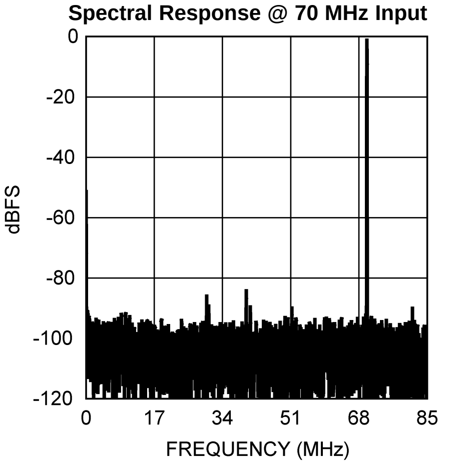


Figure 16.

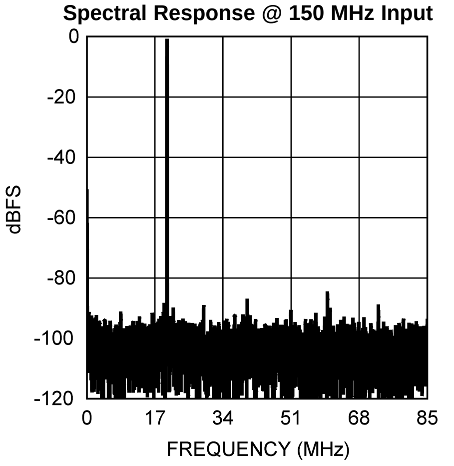


Figure 17.

Typical Performance Characteristics, Dynamic Performance (continued)

Unless otherwise specified, the following specifications apply: V_{IN} = -1dBFS, AGND = DGND = DRGND = 0V, V_A = V_D = +3.3V, V_{DR} = +1.8V, Internal V_{REF} = +1.0V, f_{CLK} = 170 MHz, f_{IN} = 70 MHz, V_{CM} = V_{RM}, C_L = 5 pF/pin, Single-Ended Clock Mode, Offset Binary Format. Typical values are for T_A = 25°C.

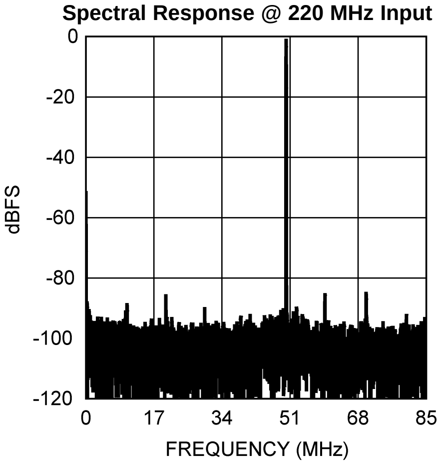

Spectral Response @ 220 MHz Input

Figure 18.

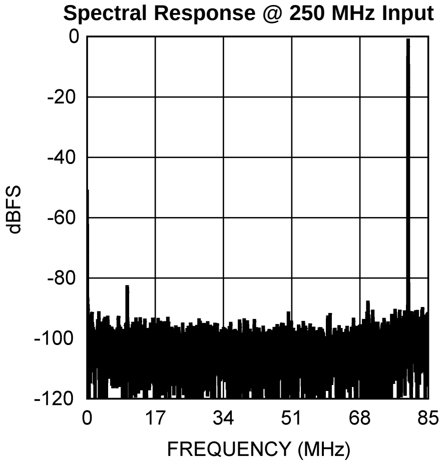

Spectral Response @ 250 MHz Input

Figure 19.

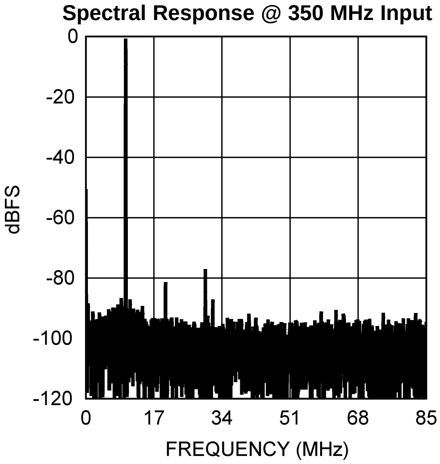

Spectral Response @ 350 MHz Input

Figure 20.

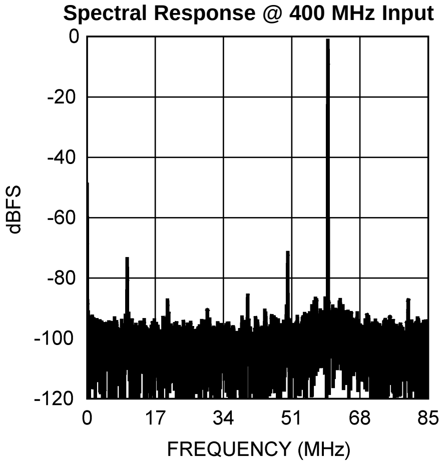

Spectral Response @ 400 MHz Input

Figure 21.

Functional Description

Operating on dual +3.3V and +1.8V supplies, the ADC12V170 digitizes a differential analog input signal to 12 bits, using a differential pipelined architecture with error correction circuitry and an on-chip sample-and-hold circuit to ensure maximum performance.

The user has the choice of using an internal 1.0V stable reference, or using an external reference. The ADC12V170 will accept an external reference between 0.9V and 1.1V (1.0V recommended) which is buffered on-chip to ease the task of driving that pin. The +1.8V output driver supply reduces power consumption and decreases the noise at the output of the converter.

The quad state function pin CLK_SEL/DF (pin 8) allows the user to choose between using a single-ended or a differential clock input and between offset binary or 2's complement output data format. The digital outputs are LVDS compatible signals that are clocked by a synchronous data ready output signal (DRDY pins 33, 34) at the same rate as the clock input. For the ADC12V170 the clock frequency can be between 5 MSPS and 170 MSPS (typical) with fully specified performance at 170 MSPS. The analog input is acquired at the falling edge of the clock and the digital data for a given sample is output on the falling edge of the DRDY signal and is delayed by the pipeline for 7.5 clock cycles. The odd data bits should be captured with the rising edge of DRDY and the even data bits should be captured with the falling edge of DRDY.

Power-down is selectable using the PD/Sleep pin (pin 7). A logic high on the PD/Sleep pin disables everything except the voltage reference circuitry and reduces the converter power consumption to 15 mW. When PD/Sleep is biased to $V_A/2$ the the chip enters sleep mode. In sleep mode everything except the voltage reference circuitry and its accompanying on chip buffer is disabled; power consumption is reduced to 50 mW. The ADC12V170's wake-up time is quicker from sleep mode than from power down mode. For normal operation, the PD/Sleep pin should be connected to the analog ground (AGND). A duty cycle stabilizer maintains performance over a wide range of clock duty cycles.

APPLICATIONS INFORMATION

OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC12V170:

$3.0V \leq V_A \leq 3.6V$

$V_D = V_A$

$V_{DR} = 1.8V$

$5\text{ MHz} \leq f_{CLK} \leq 170\text{ MHz}$

1.0V internal reference

$0.9V \leq V_{REF} \leq 1.1V$ (for an external reference)

$V_{CM} = 1.5V$ (from V_{RM})

Single Ended Clock Mode

ANALOG INPUTS

Signal Inputs

Differential Analog Input Pins

The ADC12V170 has one pair of analog signal input pins, $V_{IN}+$ and $V_{IN}-$, which form a differential input pair. The input signal, V_{IN}, is defined as

$$V_{IN} = (V_{IN}+) - (V_{IN}-) \quad (4)$$

Figure 22 shows the expected input signal range. Note that the common mode input voltage, V_{CM}, should be 1.5V. Using V_{RM} (pin 45) for V_{CM} will ensure the proper input common mode level for the analog input signal. The peaks of the individual input signals should each never exceed 2.6V. Each analog input pin of the differential pair should have a peak-to-peak voltage equal to the reference voltage, V_{REF}, be 180° out of phase with each other and be centered around V_{CM}.The peak-to-peak voltage swing at each analog input pin should not exceed the value of the reference voltage or the output data will be clipped.

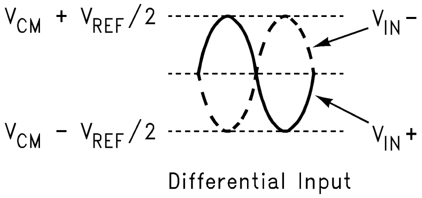


Figure 22. Expected Input Signal Range

For single frequency sine waves the full scale error in LSB can be described as approximately:

E_{FS} = 4096 (1 - sin (90° + dev))

where

- dev is the angular difference in degrees between the two signals having a 180° relative phase relationship to each other (see Figure 23) (5)

For single frequency inputs, angular errors result in a reduction of the effective full scale input. For complex waveforms, however, angular errors will result in distortion.

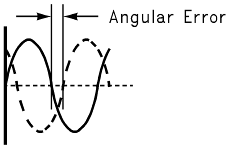


Figure 23. Angular Errors Between the Two Input Signals Will Reduce the Output Level or Cause Distortion

It is recommended to drive the analog inputs with a source impedance less than 100Ω. Matching the source impedance for the differential inputs will improve even ordered harmonic performance (particularly second harmonic).

Table 1 indicates the input to output relationship of the ADC12V170.

Table 1. Input to Output Relationship

V_{IN}^+	V_{IN}^-	Binary Output	2's Complement Output	
$V_{CM} - V_{REF}/2$	$V_{CM} + V_{REF}/2$	0000 0000 0000	1000 0000 0000	Negative Full-Scale
$V_{CM} - V_{REF}/4$	$V_{CM} + V_{REF}/4$	0100 0000 0000	1100 0000 0000	
V_{CM}	V_{CM}	1000 0000 0000	0000 0000 0000	Mid-Scale
$V_{CM} + V_{REF}/4$	$V_{CM} - V_{REF}/4$	1100 0000 0000	0100 0000 0000	
$V_{CM} + V_{REF}/2$	$V_{CM} - V_{REF}/2$	1111 1111 1111	0111 1111 1111	Positive Full-Scale

Driving the Analog Inputs

The $V_{IN}+$ and the $V_{IN}-$ inputs of the ADC12V170 have an internal sample-and-hold circuit which consists of an analog switch followed by a switched-capacitor amplifier. The analog inputs are connected to the sampling capacitors through NMOS switches, and each analog input has parasitic capacitances associated with it.

When the clock is high, the converter is in the sample phase. The analog inputs are connected to the sampling capacitor through the NMOS switches, which causes the capacitance at the analog input pins to appear as the pin capacitance plus the internal sample and hold circuit capacitance (approximately 9 pF). While the clock level remains high, the sampling capacitor will track the changing analog input voltage. When the clock transitions from high to low, the converter enters the hold phase, during which the analog inputs are disconnected from the sampling capacitor. The last voltage that appeared at the analog input before the clock transition will be held on the sampling capacitor and will be sent to the ADC core. The capacitance seen at the analog input during the hold phase appears as the sum of the pin capacitance and the parasitic capacitances associated with the sample and hold circuit of each analog input (approximately 6 pF). Once the clock signal transitions from low to high, the analog inputs will be reconnected to the sampling capacitor to capture the next sample. Usually, there will be a difference between the held voltage on the sampling capacitor and the new voltage at the analog input. This will cause a charging glitch that is proportional to the voltage difference between the two samples to appear at the analog input pin. The input circuitry must be fast enough to allow the sampling capacitor to settle before the clock signal goes low again, as incomplete settling can degrade the SFDR performance.

A single-ended to differential conversion circuit is shown in Figure 24. A transformer is preferred for high frequency input signals. Terminating the transformer on the secondary side provides two advantages. First, it presents a real broadband impedance to the ADC inputs and second, it provides a common path for the charging glitches from each side of the differential sample-and-hold circuit.

One short-coming of using a transformer to achieve the single-ended to differential conversion is that most RF transformers have poor low frequency performance. A differential amplifier can be used to drive the analog inputs for low frequency applications. The amplifier must be fast enough to settle from the charging glitches on the analog input resulting from the sample-and-hold operation before the clock goes high and the sample is passed to the ADC core.

The SFDR performance of the converter depends on the external signal conditioning circuity used, as this affects how quickly the sample-and-hold charging glitch will settle. An external resistor and capacitor network as shown in Figure 24 should be used to isolate the charging glitches at the ADC input from the external driving circuit and to filter the wideband noise at the converter input. These components should be placed close to the ADC inputs because the analog input of the ADC is the most sensitive part of the system, and this is the last opportunity to filter that input. For Nyquist applications the RC pole should be at the ADC sample rate. The ADC input capacitance in the sample mode should be considered when setting the RC pole. For wideband undersampling applications, the RC pole should be set at about 1.5 to 2 times the maximum input frequency to maintain a linear delay response.

Input Common Mode Voltage

The input common mode voltage, V_{CM}, should be in the range of 1.4V to 1.6V and be a value such that the peak excursions of the analog signal do not go more negative than ground or more positive than 2.6V. It is recommended to use V_{RM} (pin 45) as the input common mode voltage.

Reference Pins

The ADC12V170 is designed to operate with an internal 1.0V reference, or an external 1.0V reference, but performs well with external reference voltages in the range of 0.9V to 1.1V. The internal 1.0 Volt reference is the default condition when no external reference input is applied to the V_{REF} pin. If a voltage in the range of 0.9V to 1.1V is applied to the V_{REF} pin, then that voltage is used for the reference. The V_{REF} pin should always be bypassed to ground with a 0.1 µF capacitor close to the reference input pin. Lower reference voltages will decrease the signal-to-noise ratio (SNR) of the ADC12V170. Increasing the reference voltage (and the input signal swing) beyond 1.1V may degrade THD for a full-scale input, especially at higher input frequencies.

It is important that all grounds associated with the reference voltage and the analog input signal make connection to the ground plane at a single, quiet point to minimize the effects of noise currents in the ground path.

The Reference Bypass Pins (V_{RP}, V_{RM}, and V_{RN}) are made available for bypass purposes. All these pins should each be bypassed to ground with a 0.1 µF capacitor. A 0.1 µF and a 10 µF capacitor should be placed between the V_{RP} and V_{RN} pins, as shown in Figure 24. This configuration is necessary to avoid reference oscillation, which could result in reduced SFDR and/or SNR. V_{RM} may be loaded to 1mA for use as a temperature stable 1.5V reference. The remaining pins should not be loaded.

Smaller capacitor values than those specified will allow faster recovery from the power down and sleep modes, but may result in degraded noise performance. Loading any of these pins, other than V_{RM}, may result in performance degradation.

The nominal voltages for the reference bypass pins are as follows:

$V_{RM} = 1.5\ V$

$V_{RP} = V_{RM} + V_{REF} / 2$

$V_{RN} = V_{RM} - V_{REF} / 2$

Control Inputs

Power-Down & Sleep (PD/Sleep)

The power-down and sleep modes can be enabled through this three-state input pin. Table 2 shows how to utilize these options.

Table 2. Power Down/Sleep Selection Table

PD Input Voltage	Power State
V_A	Power-down
$V_A/2$	Sleep
AGND	On

The power-down and sleep modes allows the user to conserve power when the converter is not being used. In the power-down state all bias currents of the analog circuitry, excluding the reference are shut down which reduces the power consumption to 15 mW. In sleep mode some additional buffer circuitry is left on to allow an even faster wake time; power consumption in the sleep mode is 50 mW. In both of these modes the output data pins are undefined and the data in the pipeline is corrupted.

The Exit Cycle time for both the sleep and power-down mode is determined by the value of the capacitors on the V_{RP}, V_{RM} and V_{RN} reference bypass pins (pins 43, 44 and 45). These capacitors lose their charge when the ADC is not operating and must be recharged by on-chip circuitry before conversions can be accurate. For power-down mode the Exit Cycle time is about 3 ms with the recommended component values. The Exit Cycle time is faster for sleep mode. Smaller capacitor values allow slightly faster recovery from the power down and sleep mode, but can result in reduced performance.

Clock Mode Select/Data Format (CLK_SEL/DF)

Single-ended versus differential clock mode and output data format are selectable using this quad-state function pin. Table 3 shows how to select between the clock modes and the output data formats.

Table 3. Clock Mode and Data Format Selection Table

CLK_SEL/DF Input Voltage	Clock Mode	Output Data Format
V_A	Differential	2's Complement
$(2/3) * V_A$	Differential	Offset Binary
$(1/3) * V_A$	Single-Ended	2's Complement
AGND	Single-Ended	Offset Binary

CLOCK INPUTS

The CLK+ and CLK− signals control the timing of the sampling process. The CLK_SEL/DF pin (pin 8) allows the user to configure the ADC for either differential or single-ended clock mode (see Clock Mode Select/Data Format (CLK_SEL/DF)). In differential clock mode, the two clock signals should be exactly 180° out of phase from each other and of the same amplitude. In the single-ended clock mode, the clock signal should be routed to the CLK+ input and the CLK− input should be tied to AGND in combination with the correct setting from Table 3.

To achieve the optimum noise performance, the clock inputs should be driven with a stable, low jitter clock signal in the range indicated in the Electrical Table. The clock input signal should also have a short transition region. This can be achieved by passing a low-jitter sinusoidal clock source through a high speed buffer gate. This configuration is shown in Figure 24. The trace carrying the clock signal should be as short as possible and should not cross any other signal line, analog or digital, not even at 90°. Figure 24 shows the recommended clock input circuit.

The clock signal also drives an internal state machine. If the clock is interrupted, or its frequency is too low, the charge on the internal capacitors can dissipate to the point where the accuracy of the output data will degrade. This is what limits the minimum sample rate.

The clock line should be terminated at its source in the characteristic impedance of that line. Take care to maintain a constant clock line impedance throughout the length of the line. Refer to Application Note AN-905 (SNLA035) for information on setting characteristic impedance.

It is highly desirable that the the source driving the ADC clock pins only drive that pin. However, if that source is used to drive other devices, then each driven pin should be AC terminated with a series RC to ground, such that the resistor value is equal to the characteristic impedance of the clock line and the capacitor value is

$$C \geq \frac{4 \times t_{PD} \times L}{Z_o}$$

where

- t_{PD} is the signal propagation rate down the clock line
- "L" is the line length
- Z_O is the characteristic impedance of the clock line (6)

This termination should be as close as possible to the ADC clock pin but beyond it as seen from the clock source. Typical t_{PD} is about 150 ps/inch (60 ps/cm) on FR-4 board material. The units of "L" and t_{PD} should be the same (inches or centimeters).

The duty cycle of the clock signal can affect the performance of the A/D Converter. Because achieving a precise duty cycle is difficult, the ADC12V170 has a Duty Cycle Stabilizer. It is designed to maintain performance over a clock duty cycle range of 30% to 70%.

DIGITAL OUTPUTS

Digital outputs consist of the LVDS signals D0-D11, DL, DRDY and OVR.

The ADC12V170 has 16 LVDS compatible data output pins: 12 data output bits corresponding to the converted input value, 2 output pins that are always set to LVDS low, a data ready (DRDY) signal that should be used to capture the output data and an over-range indicator (OVR) which is set high when the sample amplitude exceeds the 12-Bit conversion range. Valid data is present at these outputs while the PD/Sleep pin is low.

The odd data bits should be captured with the falling edge of DRDY and the even data bits should be captured with the rising edge of DRDY.

Be very careful when driving a high capacitance bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through V_{DR} and DRGND. These large charging current spikes can cause on-chip ground noise and couple into the analog circuitry, degrading dynamic performance. Adequate bypassing, limiting output capacitance and careful attention to the ground plane will reduce this problem. Additionally, bus capacitance beyond the specified 5 pF/pin will cause t_{OD} to increase, reducing the setup and hold time of the ADC output data. The result could be an apparent reduction in dynamic performance.

To minimize noise due to output switching, the load currents at the digital outputs should be minimized. This can be achieved by keeping the PCB traces less than 2 inches long; longer traces are more susceptible to noise. Try to place the 100 ohm termination resistor as close to the receiving circuit as possible. See Figure 24.

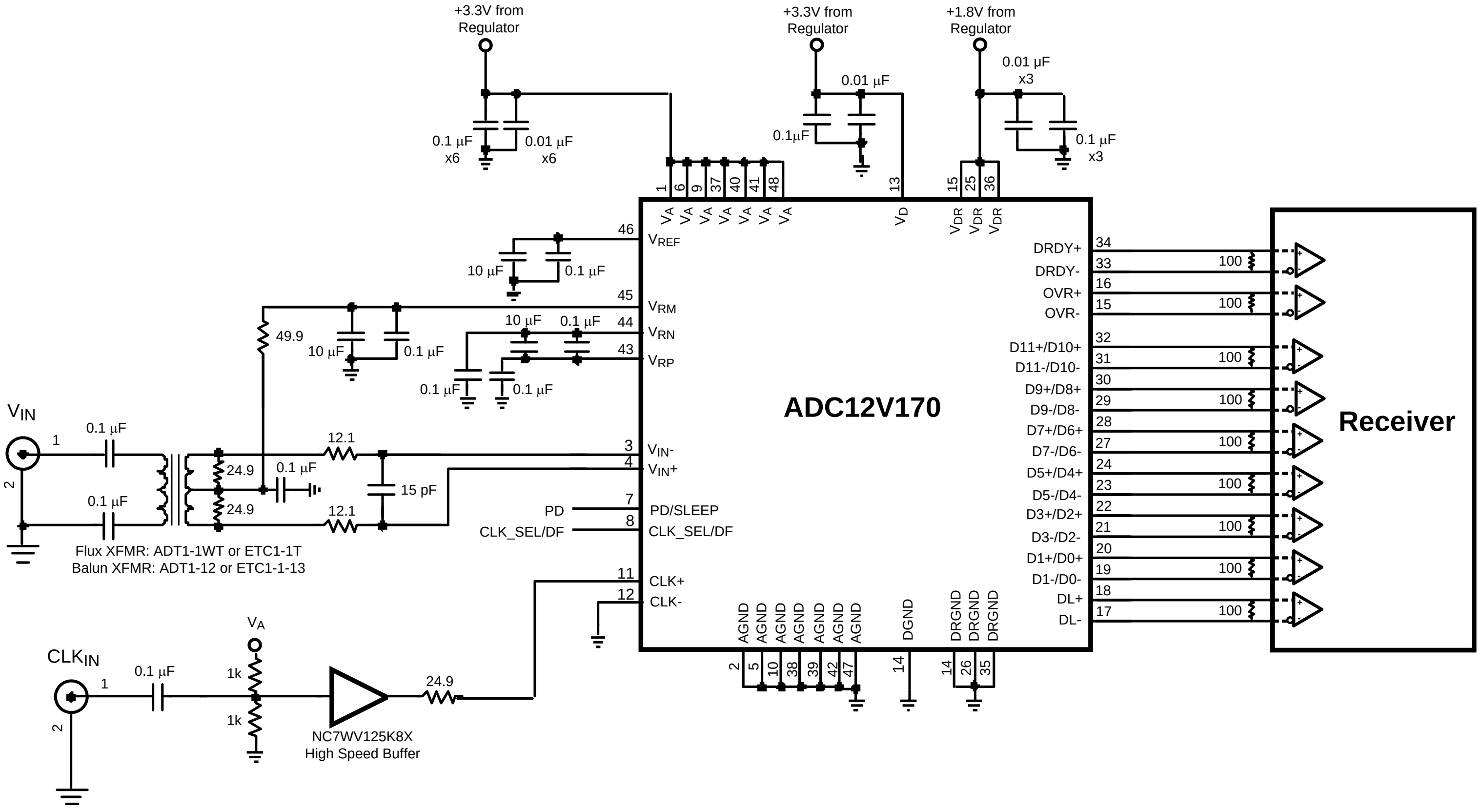


Figure 24. Application Circuit using Transformer Drive Circuit (If 14-bit compatibility is not required do not connect pin 17 and 18)

POWER SUPPLY CONSIDERATIONS

The power supply pins should be bypassed with a 0.1 µF capacitor and with a 0.01 µF ceramic chip capacitor close to each power pin. Leadless chip capacitors are preferred because they have low series inductance.

As is the case with all high-speed converters, the ADC12V170 is sensitive to power supply noise. Accordingly, the noise on the analog supply pin should be kept below 100 mV_{P-P}.

No pin should ever have a voltage on it that is in excess of the supply voltages, not even on a transient basis. Be especially careful of this during power turn on and turn off.

The V_{DR} pin provides power for the output drivers and may be operated from a supply in the range of 1.6V to 2.0V. This enables lower power operation, reduces the noise coupling effects from the digital outputs to the analog circuitry and simplifies interfacing to lower voltage devices and systems. Note, however, that t_{OD} increases with reduced V_{DR}.

LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. Maintaining separate analog and digital areas of the board, with the ADC12V170 between these areas, is required to achieve specified performance.

The ground return for the data outputs (DRGND) carries the ground current for the output drivers. The output current can exhibit high transients that could add noise to the conversion process. To prevent this from happening, the DRGND pins should NOT be connected to system ground in close proximity to any of the ADC12V170's other ground pins.

Capacitive coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry, and to keep the clock line as short as possible.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane area.

Generally, analog and digital lines should cross each other at 90° to avoid crosstalk. To maximize accuracy in high speed, high resolution systems, however, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. Even the generally accepted 90° crossing should be avoided with the clock line as even a little coupling can cause problems at high frequencies. This is because other lines can introduce jitter into the clock line, which can lead to degradation of SNR. Also, the high speed clock can introduce noise into the analog chain.

Best performance at high frequencies and at high resolution is obtained with a straight signal path. That is, the signal path through all components should form a straight line wherever possible.

Be especially careful with the layout of inductors and transformers. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors and transformers should *not* be placed side by side, even with just a small part of their bodies beside each other. For instance, place transformers for the analog input and the clock input at 90° to one another to avoid magnetic coupling.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the ground plane.

All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed in the analog area of the board. All digital circuitry and dynamic I/O lines should be placed in the digital area of the board. The ADC12V170 should be between these two areas. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground should be connected together with short traces and enter the ground plane at a single, quiet point. All ground connections should have a low inductance path to ground.

DYNAMIC PERFORMANCE

To achieve the best dynamic performance, the clock source driving the CLK input must have a sharp transition region and be free of jitter. Isolate the ADC clock from any digital circuitry with buffers, as with the clock tree shown in Figure 25. The gates used in the clock tree must be capable of operating at frequencies much higher than those used if added jitter is to be prevented. Best performance will be obtained with a single-ended drive input drive, compared with a differential clock.

As mentioned in Layout and Grounding, it is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce jitter into the clock signal, which can lead to reduced SNR performance, and the clock can introduce noise into other lines. Even lines with 90° crossings have capacitive coupling, so try to avoid even these 90° crossings of the clock line.

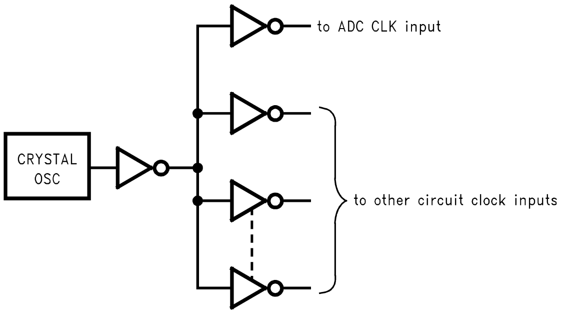


Figure 25. Isolating the ADC Clock from other Circuitry with a Clock Tree

REVISION HISTORY

Changes from Revision E (April 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	26

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC12V170CISQ/NOPB	ACTIVE	WQFN	RHS	48	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	ADC12V170	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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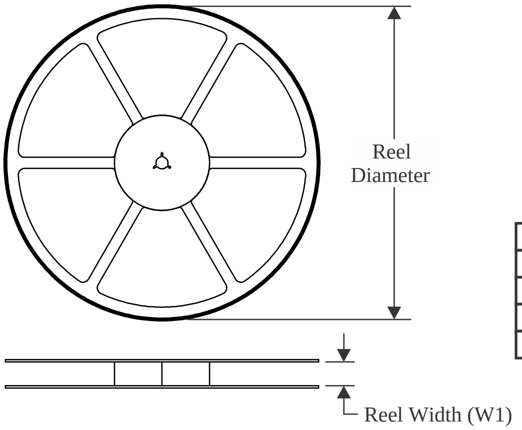
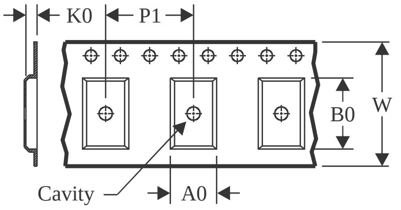
TAPE AND REEL INFORMATION

REEL DIMENSIONS

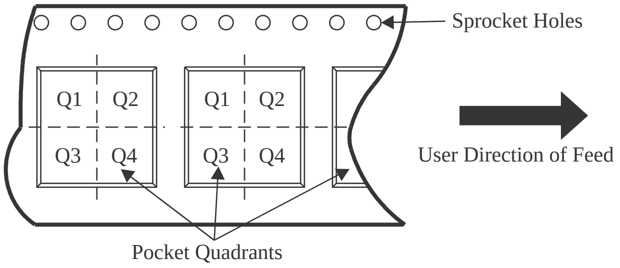


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

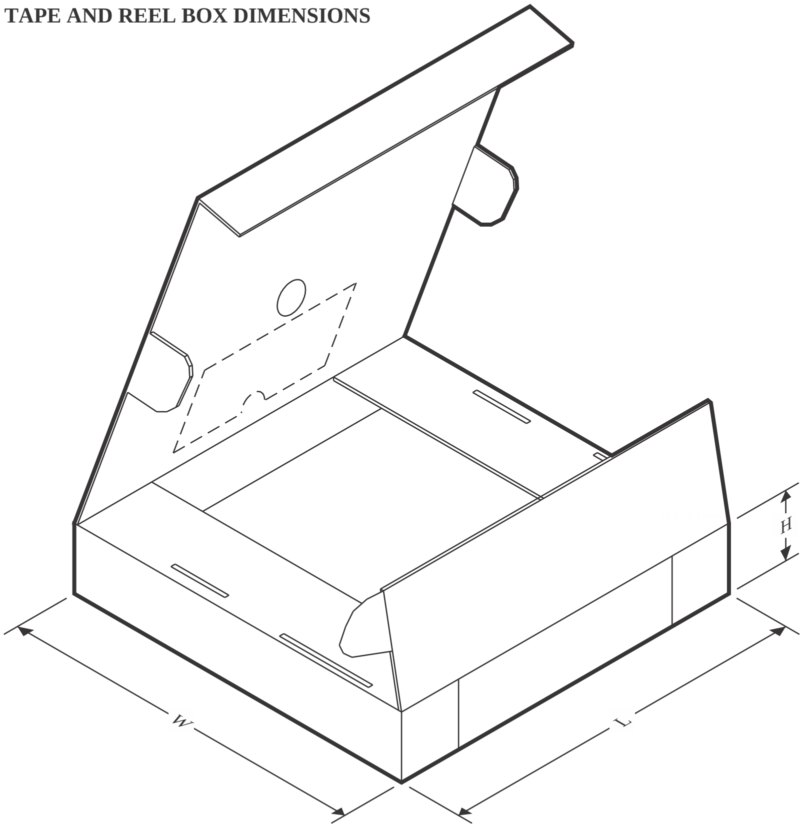
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

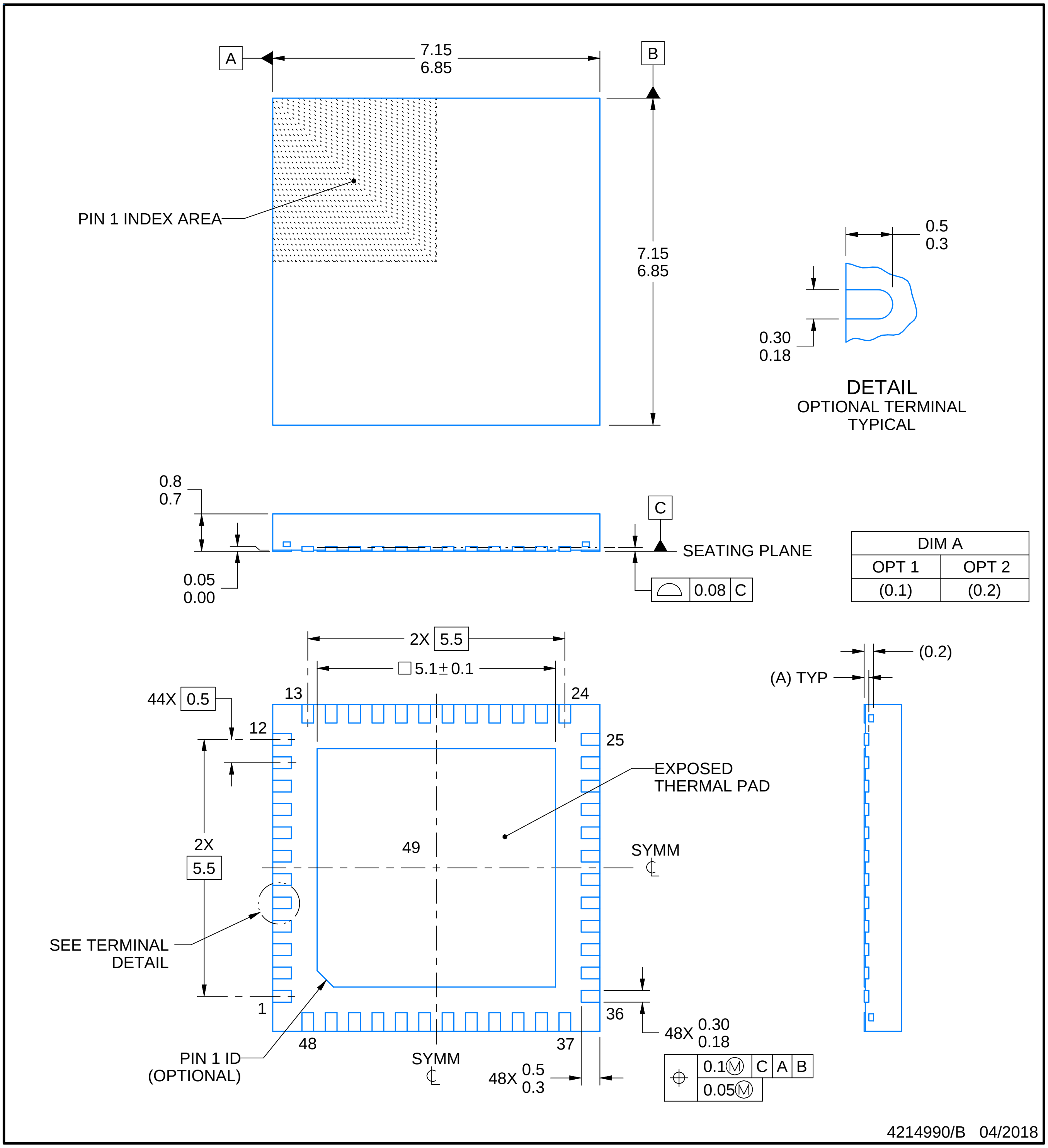
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC12V170CISQ/NOPB	WQFN	RHS	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC12V170CISQ/NOPB	WQFN	RHS	48	250	208.0	191.0	35.0

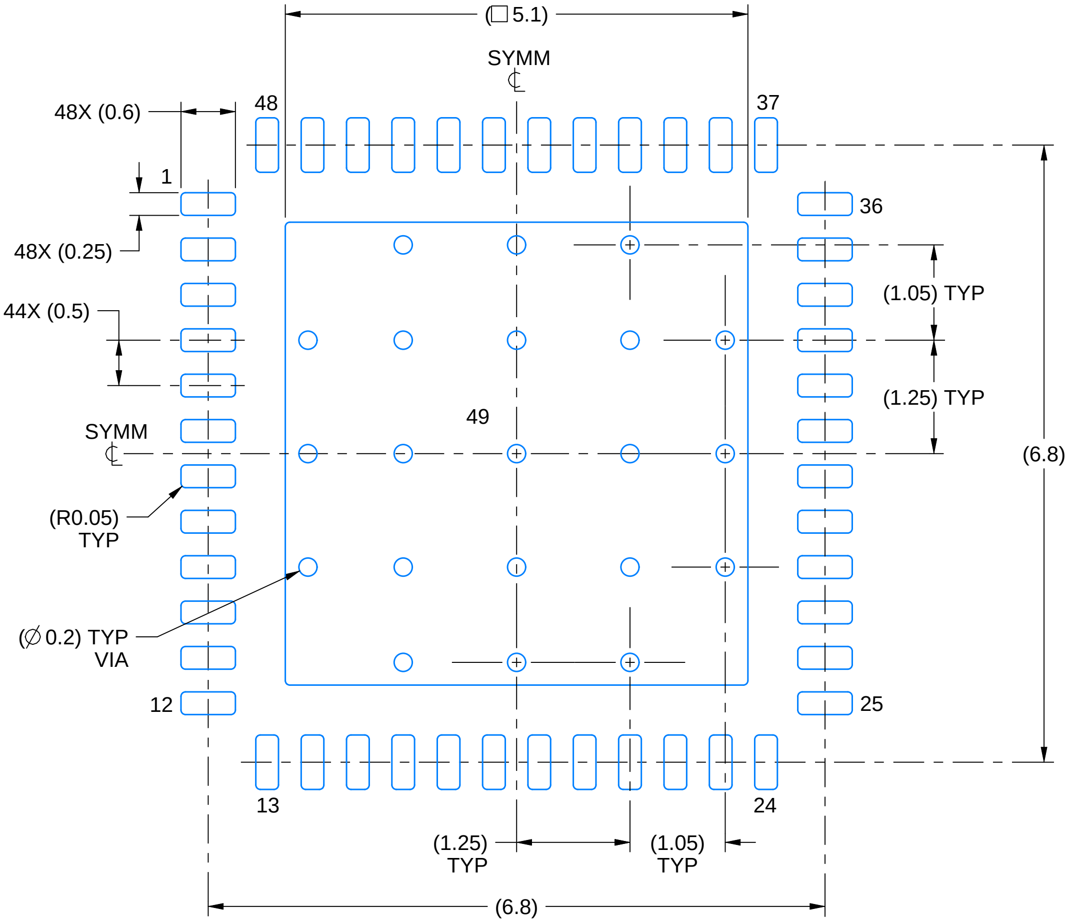


DIM A	
OPT 1	OPT 2
(0.1)	(0.2)

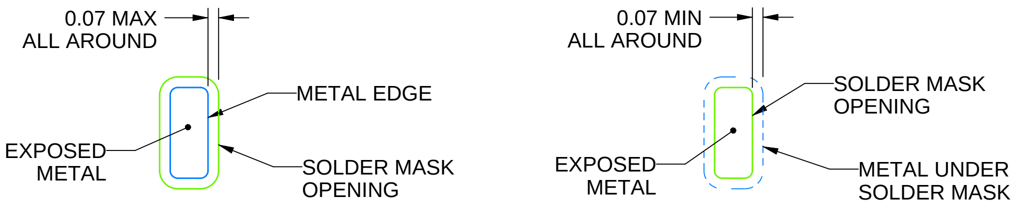
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



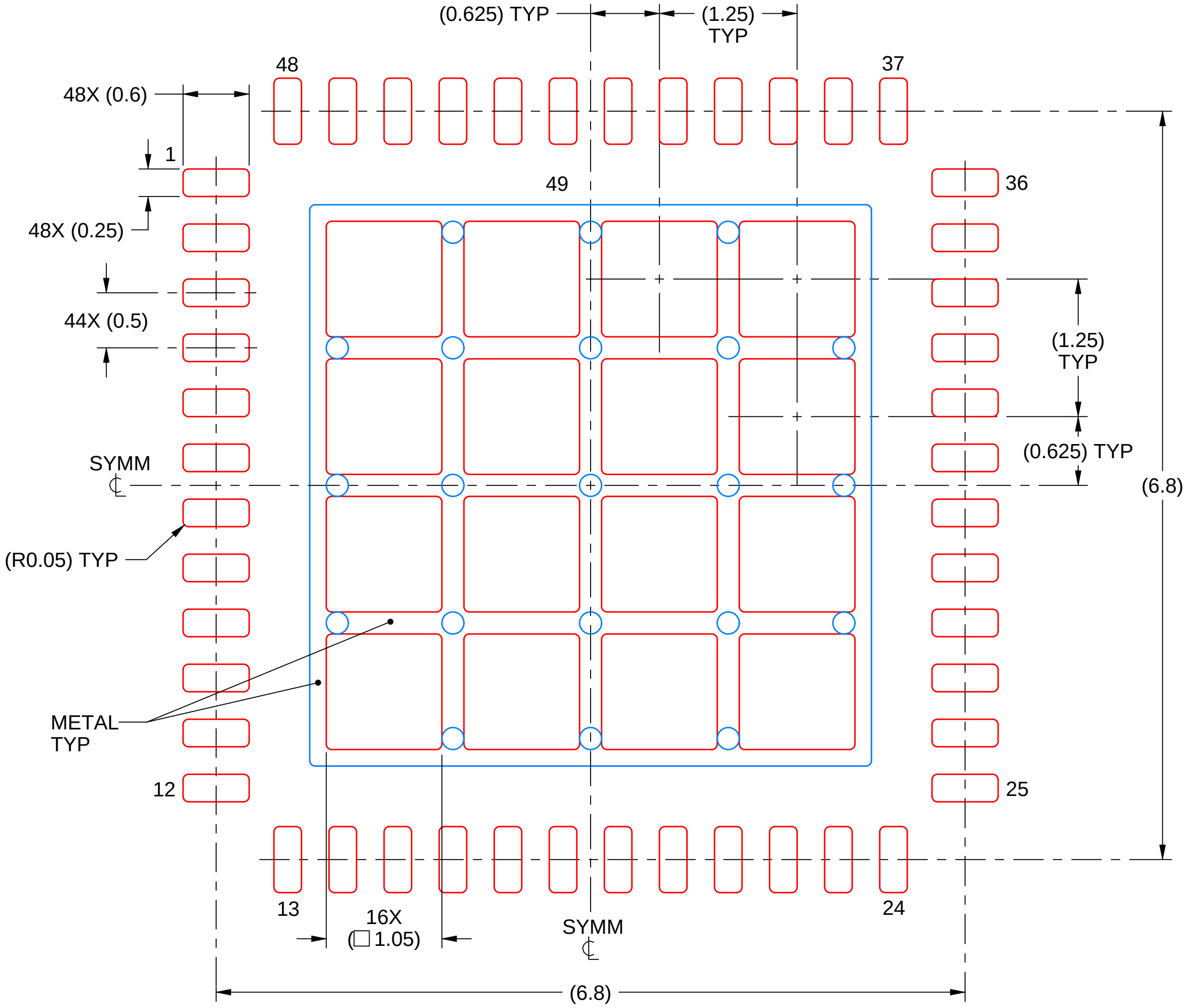
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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