SEMTECH
GENNUM PRODUCTS

GS3441

Extended Reach 3G/HD/SD Adaptive Cable Equalizer with Dual Outputs

Key Features

- SMPTE ST 424, SMPTE ST 292 and SMPTE ST 259 compliant
- Automatic cable equalization
- Multi-standard operation from 125Mb/s to 2.97Gb/s
- Performance optimized for 270Mb/s, 1.485Gb/s and 2.97Gb/s. Typical equalized length of Belden 1694A cable up to:
  - 210m at 2.97Gb/s
  - 300m at 1.485Gb/s
  - 550m at 270Mb/s
- Supports DVB-ASI at 270Mb/s
- Supports MADI at 125Mb/s
- Dual, independently-controlled outputs
- Manual bypass (useful for low data rates with slow rise/fall times)
- Programmable carrier detect with squelch threshold adjustment
- Cable Length Indicator (CLI) output; varies monotonically with input cable length
- Automatic power-down on loss of signal
  - Standby power <35 mW (typical)
- Differential outputs support DC coupling from 1.2V to 3.3V CML logic
- Option to compensate for 6dB flat attenuation prior to input of device
- Selectable output de-emphasis: 2dB, 4dB and 6dB
- Standard EIA/JEDEC logic control and status signal levels
- Single 3.3V power supply operation
- 180mW (one output enabled), 212mW (both outputs enabled) typical power consumption
- Wide operating temperature range of -40°C to +85°C
- Small footprint QFN package (4mm x 4mm)
- Pb-free and RoHS compliant

Applications

- SMPTE ST 424, SMPTE ST 292 and SMPTE ST 259 coaxial cable serial digital interfaces

Description

The GS3441 is a high-speed BiCMOS device designed to equalize and restore signals received over 75Ω coaxial cable.

The device is designed to support SMPTE ST 424, SMPTE ST 292 and SMPTE ST 259, and is optimized for performance at 270Mb/s, 1.485Gb/s and 2.97Gb/s.

The GS3441 features DC restoration to compensate for the DC content of SMPTE pathological signals.

The Carrier Detect output pin ($\overline{CD}$) indicates whether an input signal has been detected. It can be connected directly to the SLEEP pin to enable automatic power-down upon loss of carrier.

A voltage programmable threshold, set via the SQ_ADJ pin, forces $\overline{CD}$ high when the input signal amplitude falls below the threshold. This allows the GS3441 to distinguish between low-amplitude SDI signals and noise at the input of the device.

The equalizing and DC restore stages are disengaged and no equalization occurs when the BYPASS pin is HIGH. Setting the BYPASS pin HIGH is useful for signals launched at the signal source with low data rates and/or slow rise/fall times.

The GS3441 features a gain selection pin (GAIN_SEL) which can be used to compensate for 6dB flat attenuation prior to input of the device.

The differential outputs can be DC-coupled to Semtech's reclockers and cable drivers, as well as industry-standard 1.2V, 1.8V, 2.5V and 3.3V CML logic by changing the voltage applied to the VCC_O pin. In general, DC-coupling to any termination voltage between 1.2V and 3.3V is supported.

Description (Continued)

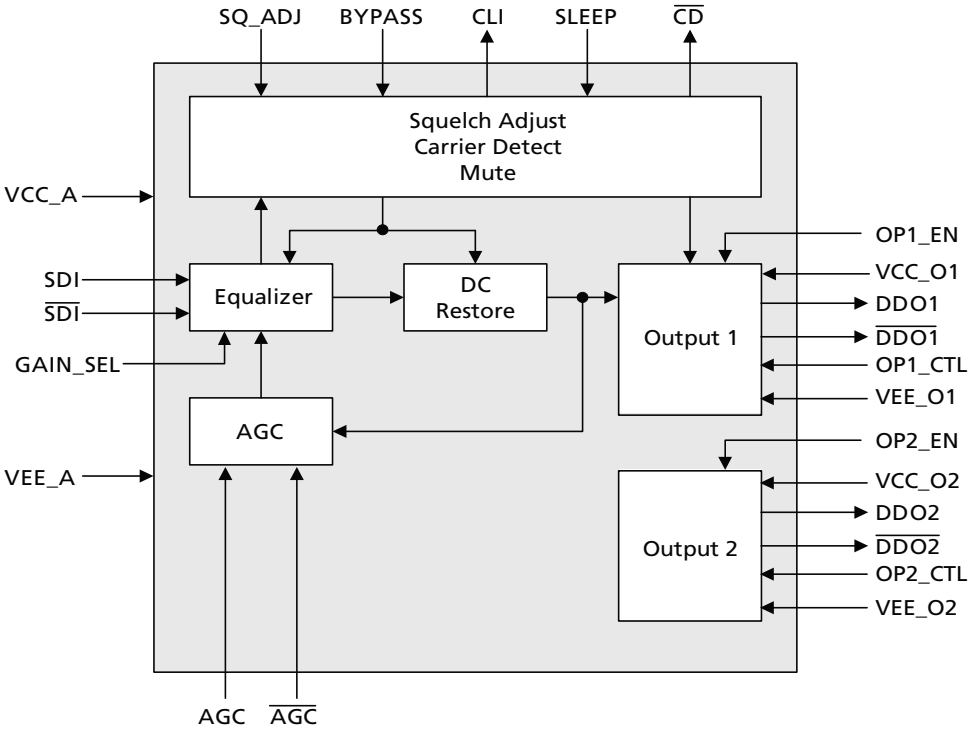
The GS3441 also features programmable output de-emphasis with three, user-selectable operating levels to support long PCB traces at the output of the device.

The device comes in a 24-pin, 4mm x 4mm QFN package and is footprint compatible with Semtech's GS2993 equalizer.

Power consumption of the GS3441 is typically 212mW when DC-coupled at 1.2V.

The GS3441 is Pb-free, and the encapsulation compound does not contain halogenated flame retardant.

This component and all homogeneous subcomponents are RoHS compliant.



GS3441 Functional Block Diagram

Contents

1. Pin Out

1.1 GS3441 Pin Assignment

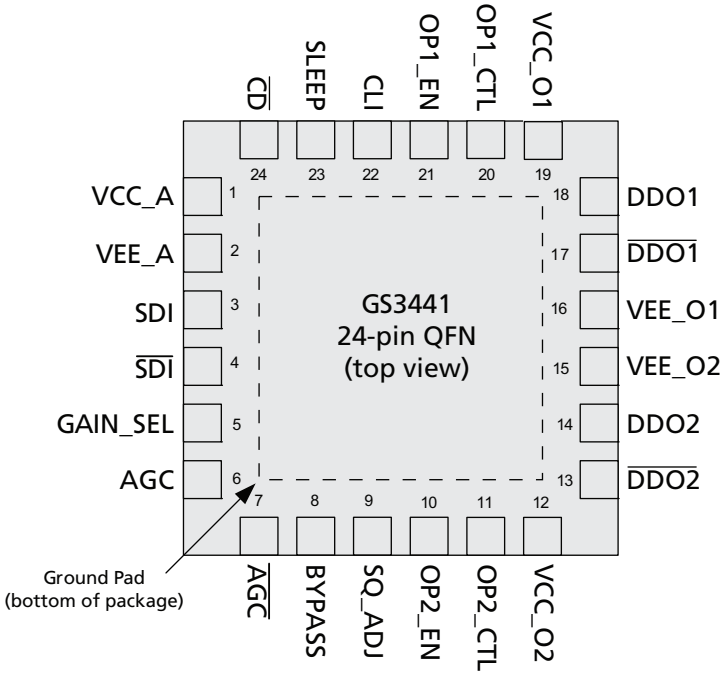


Figure 1-1: GS3441 Pin Out

1.2 GS3441 Pin Descriptions

Table 1-1: GS3441 Pin Descriptions

Pin Number	Name	Timing	Type	Description
1	VCC_A	Analog	Power	Most positive power supply connection for the input buffer, core and control circuits. Connect to +3.3V DC.
2	VEE_A	Analog	Power	Most negative power supply connection for the input buffer, core and control circuits Connect to GND.
3, 4	SDI, $\overline{\text{SDI}}$	Analog	Input	Serial digital differential input.
5	GAIN_SEL	Not Synchronous	Input	Input Sensitivity Control. Please refer to the input logic parameter in the DC Electrical Characteristics table for logic level threshold and compatibility. This pin is a 2.5V input that is tolerant to 3.3V levels. When HIGH, the device compensates for an additional 6dB of loss across the entire operating band. This pin has an internal pull-down resistor.

Table 1-1: GS3441 Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
6, 7	AGC, $\overline{\text{AGC}}$	Analog	—	External AGC capacitor connection.
8	BYPASS	Not Synchronous	Input	Core Bypass Control. Please refer to the input logic parameter in the DC Electrical Characteristics table for logic level threshold and compatibility. This pin is a 2.5V input that is tolerant to 3.3V levels. Forces the equalizer and DC-restore stages into Bypass mode when HIGH. No equalization occurs in this mode. This pin has an internal pull-down resistor.
9	SQ_ADJ	Analog	Input	Squelch Threshold Adjust. Adjusts the input signal amplitude threshold of the carrier detect function. The serial data output of the device can be muted when the serial data input signal amplitude is too low by connecting the $\overline{\text{CD}}$ and OPn_CTL pins via suitable resistor networks (see Figure 4-2 and Figure 4-3). This pin has an internal pull-down resistor. **Note:** The SQ_ADJ function is only available when the device is not in auto-sleep mode. Reference Section 4.5 for more detail.
10	OP2_EN	—	Input	Output 2 Enable. Please refer to the input logic parameter in the DC Electrical Characteristics table for logic level threshold and compatibility. When HIGH, Output 2 is operational. When LOW, Output 2 is powered-down and the outputs are both at VCC_O2. This pin has an internal pull-down resistor.
11	OP2_CTL	Not Synchronous	Input	Controls the Output Swing, De-emphasis and Mute features of the DDO/$\overline{\text{DDO}}$ outputs for Output 2. When this pin is connected to GND, the output swing is 850mV$_{ppd}$ with no de-emphasis. With this pin connected to a 2.5V, the output is muted. Intermediate voltages and functions are shown in Table 4-5. These voltages can be achieved as shown in Figure 4-2 and Figure 4-3. This pin has an internal pull-down resistor.
12	VCC_O2	Analog	Power	Most positive power supply connection for the output buffer for output 2. Connect to 1.2 - 3.3V DC.
13, 14	$\overline{\text{DDO2}}$, DDO2	Analog	Output	Serial digital differential output 2.
15	VEE_O2	Analog	Power	Most negative power supply connection for the output buffer for output 2. Connect to GND.
16	VEE_O1	Analog	Power	Most negative power supply connection for the output buffer for output 1. Connect to GND.
17, 18	$\overline{\text{DDO1}}$, DDO1	Analog	Output	Serial digital differential output 1.

Table 1-1: GS3441 Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
19	VCC_O1	Analog	Power	Most positive power supply connection for the output buffer for output 1. Connect to 1.2 - 3.3V DC.
20	OP1_CTL	Not Synchronous	Input	Controls the Output Swing, De-emphasis and Mute features of the DDO/$\overline{\text{DDO}}$ outputs for Output 1. When this pin is connected to GND, the output swing is 800mV$_{ppd}$ with no de-emphasis applied to the output signal. With this pin connected to the 2.5V, the output is MUTED. Intermediate voltages and functions are shown in Table 4-5. These voltages can be achieved as shown in Figure 4-2 and Figure 4-3. This pin has an internal pull-down resistor.
21	OP1_EN	—	Input	Output 1 Enable. Please refer to the input logic parameter in the DC Electrical Characteristics table for logic level threshold and compatibility. When HIGH, Output 1 is operational. When LOW, Output 1 is powered-down and the outputs are both at VCC_O1. This pin has an internal pull-up resistor.
22	CLI	—	Output	Cable Length Indicator
23	SLEEP	Not Synchronous	Input	SLEEP Control. Please refer to the input logic parameter in the DC Electrical Characteristics table for logic level threshold and compatibility. This pin is a 2.5V input that is tolerant to 3.3V levels. When HIGH the part is powered-down except for the Carrier Detect function. This pin may be connected directly to the $\overline{\text{CD}}$ pin to automatically put the device to sleep (low-power operation) on loss of carrier. This pin has an internal pull-down resistor. **Note:** When SLEEP is connected to $\overline{\text{CD}}$ for automatic power reduction on loss of carrier, the SQ_ADJ pin will not modify the $\overline{\text{CD}}$ threshold. The $\overline{\text{CD}}$ threshold will revert to the default value used when SQ_ADJ is pulled LOW.
24	$\overline{\text{CD}}$	Not Synchronous	Output	Carrier Detect Status Output. Please refer to the output logic parameter in the DC Electrical Characteristics table for logic level threshold and compatibility. This pin is a 2.5V output. Indicates presence of an input signal. When the $\overline{\text{CD}}$ pin is LOW, a signal has been detected at the input. When this pin is HIGH, it indicates loss of input signal.
—	Center Pad	—	Power	Internally bonded to VEE_A. Connect to GND with at least 5 VIAs.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
Supply Voltage - Core/Output Driver	-0.5V to +3.6V DC
Input ESD Voltage (HBM)	5kV
Storage Temperature Range	-50°C to 125°C
Input Voltage Range (any input)	-0.3 to (V_{CC_A} +0.3)V
Operating Temperature Range	-40°C to +85°C
Solder Reflow Temperature	260°C

Note: Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation outside of the ranges shown in Table 2-1 is not implied.

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

V_{CC} = +3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage - Core	V_{CC_A}	–	3.135	3.3	3.465	V	–
Supply Voltage - Output Driver	V_{CC_O}	–	1.14	1.2	1.26	V	1
		–	2.375	2.5	2.625	V	1
		–	3.135	3.3	3.465	V	1

Table 2-2: DC Electrical Characteristics (Continued)

V_{CC} = +3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Power Consumption	P_D	V_{CC_O1} = 1.2V, V_{CC_O2}= OFF, $\Delta V_{DDO1} = \Delta V_{DDO2}$ = 425mV$_{ppd}$	–	180	218	mW	2
		V_{CC_O1} = 1.2V, V_{CC_O2}= 1.2V, $\Delta V_{DDO1} = \Delta V_{DDO2}$ = 425mV$_{ppd}$	–	212	260	mW	2
		V_{CC_O1} = 1.2V, V_{CC_O2}= 1.2V, $\Delta V_{DDO1} = \Delta V_{DDO2}$ = 850mV$_{ppd}$	–	237	290	mW	2
		V_{CC_O1} = 2.5V, V_{CC_O2}= 2.5V, $\Delta V_{DDO1} = \Delta V_{DDO2}$ = 850mV$_{ppd}$	–	245	299	mW	2
		V_{CC_O1} = 3.3V, V_{CC_O2}= OFF, $\Delta V_{DDO1} = \Delta V_{DDO2}$ = 425mV$_{ppd}$	–	202	244	mW	2
		V_{CC_O1} = 3.3V, V_{CC_O2}= OFF, $\Delta V_{DDO1} = \Delta V_{DDO2}$ = 850mV$_{ppd}$	–	240	292	mW	2
		V_{CC_O1} = 3.3V, V_{CC_O2}= 3.3V, $\Delta V_{DDO1} = \Delta V_{DDO2}$ = 425mV$_{ppd}$	–	258	316	mW	2
		V_{CC_O1} = 3.3V, V_{CC_O2}= 3.3V, $\Delta V_{DDO1} = \Delta V_{DDO2}$ = 850mV$_{ppd}$	–	325	395	mW	2
Supply Current - Core	I_s	Both outputs on	–	53	59	mA	3
Supply Current - Output Driver (one output enabled)	$I_{Output\ Driver}$	V_{CC_O1} & V_{CC_O2} = 3.3V, $\Delta V_{DDO1} = \Delta V_{DDO2}$ = 425mV$_{ppd}$	–	10	14	mA	–
		V_{CC_O1} & V_{CC_O2} = 3.3V, $\Delta V_{DDO1} = \Delta V_{DDO2}$ = 850mV$_{ppd}$	–	19	24	mA	–
Input Common Mode Voltage	V_{CMIN}	–	1.62	1.71	1.80	V	–

Table 2-2: DC Electrical Characteristics (Continued)

V_{CC} = +3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
$\overline{CD}$ Output Voltage	$V_{\overline{CD}(OH)}$	Carrier not present	2.0	–	–	V	–
	$V_{\overline{CD}(OL)}$	Carrier present	–	–	0.4	V	–
Input Voltage - Digital pins	V_{GAIN_SEL} V_{BYPASS} V_{SLEEP} V_{OP1_EN} V_{OP2_EN}	Minimum to assert	1.7	–	–	V	4
		Maximum to de-assert	–	–	0.7	V	4

Notes:

1. V_{CC_O} operates from 1.2V through 3.3V (±5%).
2. De-emphasis off.
3. An additional 6mA when de-emphasis is enabled (dual-output mode).
4. Digital Input Pins are 2.5V but 3.3V tolerant.

2.3 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

V_{CC} = +3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial input data rate	DR_{SDO}	–	125	–	2970	Mb/s	1
Input Voltage Swing	ΔV_{SDI}	Differential, 270Mb/s and 1.485Gb/s	720	800	950	mV_{ppd}	2
		Differential, 2.97Gb/s	720	800	880	mV_{ppd}	2
Output Voltage Swing	ΔV_{DDO}	100Ω load, differential, OP_CTL set for high swing	700	850	1000	mV_{ppd}	–
		100Ω load, differential, OP_CTL set for low swing	350	425	500	mV_{ppd}	–
Output Jitter of Various Cable Lengths and Data Rates	–	2.97Gb/s Belden 1694A: 0-120m	–	–	0.25	UI	3, 4, 5
	–	2.97Gb/s Belden 1694A: 120-150m	–	–	0.3	UI	3, 4, 5
	–	2.97Gb/s Belden 1694A: 150-170m	–	–	0.45	UI	3, 4, 5
	–	2.97Gb/s Belden 1694A: 170-190m	–	–	0.55	UI	3, 4, 5
	–	2.97Gb/s Belden 1694A: 190-210m	–	0.55	–	UI	3, 4, 5
	–	1.485Gb/s Belden 1694A: 0-200m	–	–	0.2	UI	3, 4, 5
	–	1.485Gb/s Belden 1694A: 200-260m	–	–	0.3	UI	3, 4, 5
	–	1.485Gb/s Belden 1694A: 260-300m	–	0.3	–	UI	3, 4, 5
	–	270Mb/s Belden 1694A: 0-300m	–	0.1	0.15	UI	3, 4, 5
	–	270Mb/s Belden 1694A: 300-500m	–	–	0.25	UI	3, 4, 5
	–	270Mb/s Belden 1694A: 500-550m	–	0.25	–	UI	3, 4, 5
Output Rise/Fall time	–	2.97Gb/s & 1.485Gb/s 20% - 80%	–	75	–	ps	–
	–	270Mb/s (see Section 4.8) 20% - 80%	–	150	–	ps	–
Mismatch in rise/fall time	–	–	–	–	30	ps	–
Duty cycle distortion	–	SD/HD/3G	–	–	30	ps	–
Overshoot	–	–	–	–	10	%	–

Table 2-3: AC Electrical Characteristics (Continued)

V_{CC} = +3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Input Return Loss	–	5MHz - 1.485GHz	15	–	–	dB	–
	–	1.485GHz - 2.97GHz	10	–	–	dB	–
Input Resistance	–	single-ended	–	1.9	–	kΩ	–
Input Capacitance	–	single-ended	–	1.3	–	pF	–
Output Resistance	–	single-ended	–	50	–	Ω	–

Notes:

1. Device performance is optimized for standard data rates (SD = 270Mb/s, HD = 1.485Gb/s, 3G = 2.970Gb/s)
2. 0m cable length.
3. All parts are production tested. In order to guarantee jitter over the full range of specification (V_{CC_A} = 3.3V ±5%, T_A = -40°C to +85°C, and 720-880mV_{pp} launch swing from the SDI cable driver) the recommended applications circuit must be used.
4. Based on validation data using the recommended applications circuit, at V_{CC_A} = 3.3V, T_A = -40°C to +85°C and 800mV_{pp} launch swing from the SDI cable driver.
5. GAIN_SEL = 0

3. Input/Output Circuits

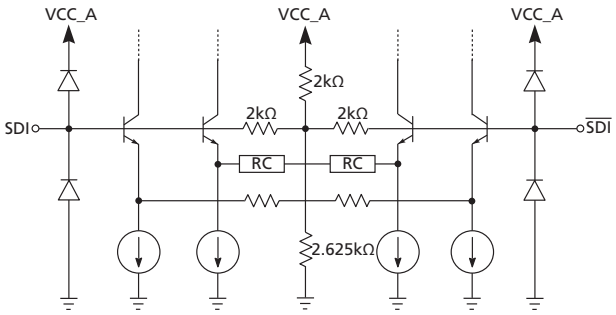


Figure 3-1: Input Equivalent Circuit

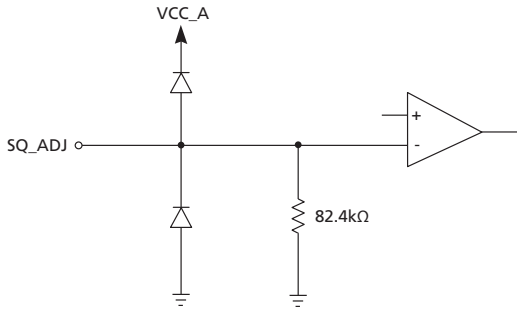


Figure 3-2: SQ_ADJ Equivalent Circuit

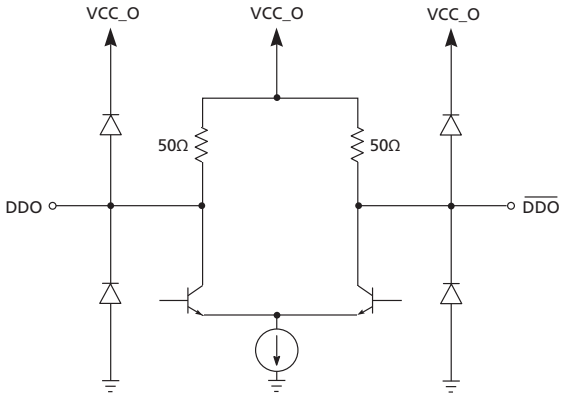


Figure 3-3: Output Circuit

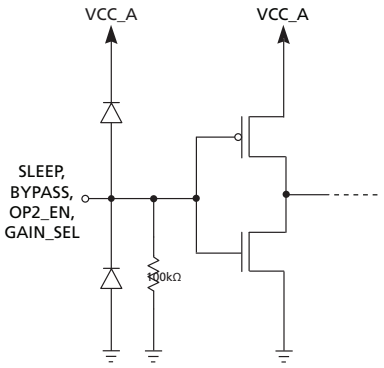


Figure 3-4: SLEEP, BYPASS, OP2_EN and GAIN_SEL Circuits

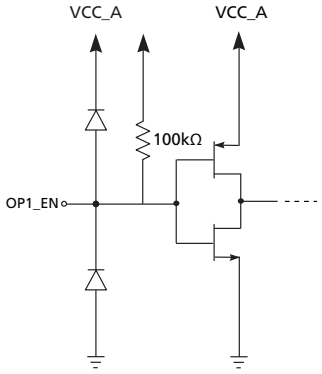


Figure 3-5: OP1_EN Circuit

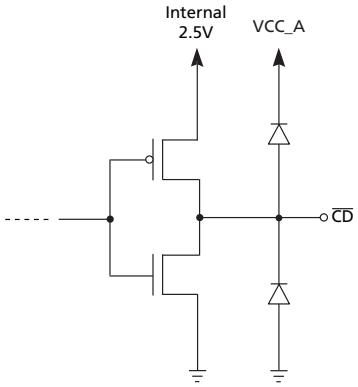


Figure 3-6: $\overline{CD}$ Circuit

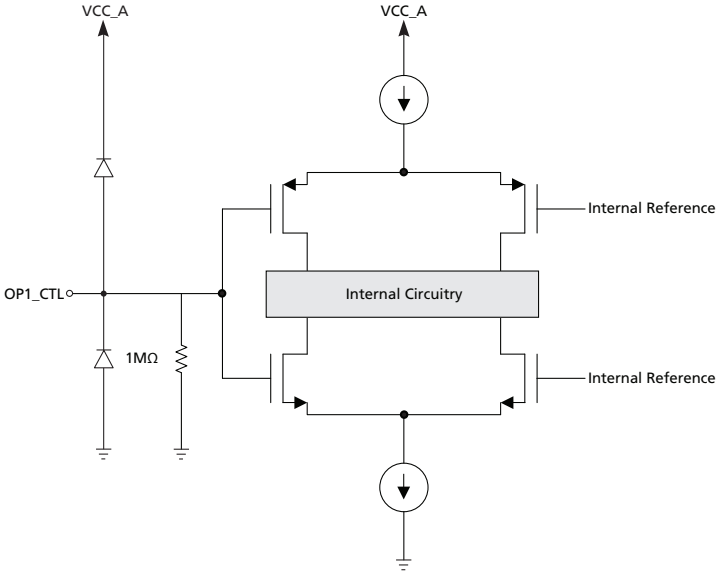


Figure 3-7: OP1_CTL Circuit

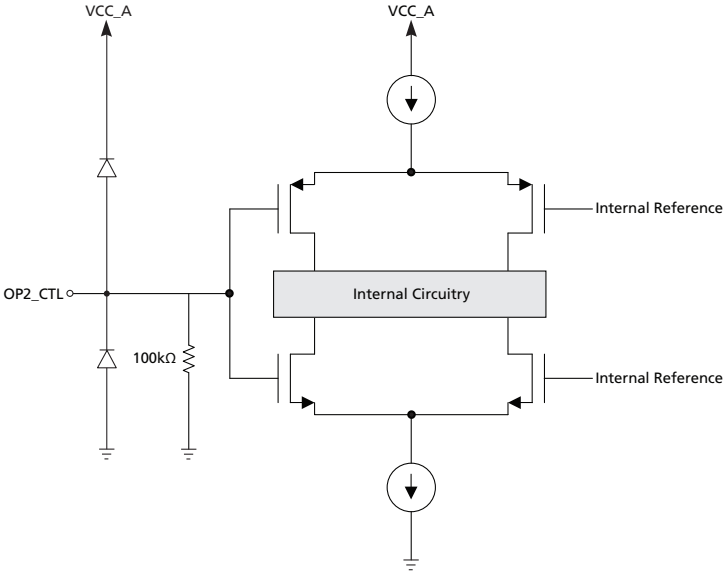


Figure 3-8: OP2_CTL Circuit

4. Detailed Description

The GS3441 is a high-speed BiCMOS IC designed to equalize serial digital signals.

The GS3441 can equalize 3Gb/s, HD and SD serial digital signals, and will typically equalize 210m of Belden 1694A cable at 2.97Gb/s, 300m at 1.485Gb/s and 550m at 270Mb/s. When DC coupling the output of a device to a 1.2V CML load, the GS3441 typically consumes approximately 180mW (one output enabled), 212mW (both outputs enabled). The GS3441 features dual, independently-controlled outputs, and can be operated from a single +3.3V DC power supply.

4.1 Serial Digital Inputs

The received serial data signal is connected to the input pins (SDI/$\overline{\text{SDI}}$) in either a differential or single-ended configuration. AC-coupling of the inputs is recommended, because the SDI and $\overline{\text{SDI}}$ inputs are internally biased to approximately 1.87V.

4.2 Automatic (Adaptive) Cable Equalization

The input signal passes through a variable gain equalizing stage, whose frequency response closely matches the inverse of the cable (Belden 1694A) loss characteristic. In addition, the variation of the frequency response with control voltage imitates the variation of the inverse cable loss characteristic with cable length ensuring that the correct amount of gain is automatically applied to the input signal for any cable length within the supported ranges.

The equalized signal is DC-restored, effectively restoring the logic threshold of the equalized signal to its correct level independent of shifts due to AC-coupling.

4.3 Differential Digital Data Outputs

The digital data output signals have a nominal output voltage swing of either 850mV$_{ppd}$ or 425mV$_{ppd}$, as set by the OP1_CTL pin for DDO1 and the OP2_CTL pin for DDO2.

Table 4-1 shows the typical output common mode voltage levels related to the two output swing options and the chosen coupling (DC vs. AC).

Table 4-1: Typical Common Mode Output Voltage Levels

Supply Voltage (VCC_O)	425mV$_{ppd}$ Swing (DC-coupled Output)	425mV$_{ppd}$ Swing (AC-coupled Output)	850mV$_{ppd}$ Swing (DC-coupled Output)	850mV$_{ppd}$ Swing (AC-coupled Output)
3.3V	3.2V	3.1V	3.1V	2.9V
2.5V	2.4V	2.3V	2.3V	2.1V
1.8V	1.7V	1.6V	1.6V	1.4V
1.2V	1.1V	1.0V	1.0V	0.8V

4.4 Programmable Squelch Adjust (SQ_ADJ)

The GS3441 features a programmable Squelch Adjust (SQ_ADJ) threshold.

This feature can be useful in applications where there are multiple input channels using the GS3441 and the maximum gain can be limited to avoid crosstalk.

The SQ_ADJ pin acts to change the threshold of the Carrier Detect ($\overline{CD}$) pin, through voltage level variances. When the input signal drops below a certain threshold set by SQ_ADJ, the $\overline{CD}$ pin will be driven HIGH, indicating that there is not a valid input signal. In applications where programmable squelch adjust is not required, the SQ_ADJ pin can be left unconnected.

This feature has been designed for use in applications such as routers, where signal crosstalk and circuit noise cause the equalizer to output erroneous data when no input signal is present. The use of a Carrier Detect function with a fixed internal reference does not solve this problem, since the signal-to-noise ratio on the circuit board could be significantly less than the default signal detection level set by the on-chip reference.

Note: When using SQ_ADJ to limit the maximum gain of the GS3441, $\overline{CD}$ should not be connected to SLEEP.

4.5 Carrier Detect, Sleep, and Auto-Sleep

The Carrier Detect output pin ($\overline{CD}$) indicates the presence of a valid signal at the input of the GS3441. When $\overline{CD}$ is LOW, the device has detected a valid input on SDI and $\overline{SDI}$. When $\overline{CD}$ is HIGH, the device has not detected a valid input.

The GS3441 includes a SLEEP input pin, which can be used to put the device into a low-power sleep mode, consuming less than 35mW. In this mode, the outputs are high impedance and will be pulled high by the on-chip termination. Set the SLEEP pin HIGH to place the chip in this low-power state. In this mode, the Carrier Detect output will still function to facilitate the detection of a valid serial input data signal.

Auto-Sleep is enabled by connecting $\overline{CD}$ to SLEEP. When connected, the GS3441 will automatically go into low-power sleep mode when there is a loss of Serial Digital Input signal.

Note 1: $\overline{CD}$ will only detect loss of carrier for data rates greater than 19Mb/s.

Note 2: If SQ_ADJ is being used to limit the maximum gain of the device, and the maximum cable length is exceeded when BYPASS pin is set LOW, the $\overline{CD}$ pin will be set HIGH even if a carrier is present.

Note 3: If the $\overline{CD}$ pin is connected to the SLEEP pin, SQ_ADJ must be either left open, or connected to ground.

Table 4-2: SLEEP Input Table

SLEEP	Function
0	The GS3441 operates normally
1	The GS3441 enters low-power sleep mode. $\overline{CD}$ output remains valid

Table 4-3: $\overline{CD}$ Output Table

$\overline{CD}$	Input Status
0	Valid input on SDI, $\overline{SDI}$ pins
1	Input is not valid

4.6 GAIN_SEL

The GS3441 has an option of compensating for 6dB of flat attenuation prior to the equalizer.

Table 4-4: GAIN_SEL Input Table

GAIN_SEL	Function
0	No flat band gain is applied
1	6dB of flat attenuation will be compensated by the device

4.7 Adjustable Output Swing, De-Emphasis and Mute

The OP1_CTL input pin determines the output swing and de-emphasis settings for the first output (DDO1/$\overline{DDO1}$), and OP2_CTL input pin determines the output swing and de-emphasis settings for the second output (DDO2/$\overline{DDO2}$).

The OP1_CTL and OP2_CTL pins are both analog inputs, allowing different combinations of output swing, de-emphasis and mute. The possible values are listed in Table 4-5 below:

Table 4-5: OP1_CTL and OP2_CTL Functions and Levels

Level	Swing (mV_{ppd})	De-emphasis	Mute	Voltage (V)
0	$850mV_{ppd}$	Off	N	0.000 - 0.083
1	$850mV_{ppd}$	2dB	N	0.234 - 0.394
2	$850mV_{ppd}$	4dB	N	0.545 - 0.704
3	$850mV_{ppd}$	6dB	N	0.856 - 1.015
4	$425mV_{ppd}$	Off	N	1.166 - 1.333
5	$425mV_{ppd}$	2dB	N	1.484 - 1.644
6	$425mV_{ppd}$	4dB	N	1.795 - 1.954
7	$425mV_{ppd}$	6dB	N	2.106 - 2.265
8	$425mV_{ppd}$	N/A	Y	2.416 - 2.500

When muted, the output swing is set to $425mV_{ppd}$ and the outputs are latched.

Automatic muting of the output can be enabled by connecting the $\overline{CD}$ pin to the OP1_CTL and OP2_CTL pins.

If the connection is made directly, as shown in Figure 4-1, the output would be in its default mode (850mV$_{ppd}$ swing with no de-emphasis) when there is signal present.

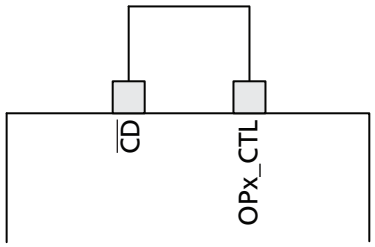


Figure 4-1: Direct Loopback

To enable automatic muting while the output is configured for other settings, a resistor network should be used between $\overline{CD}$ and VCC_A. The intermediate voltages of this resistor ladder can set the output to any one of the nine different settings as shown in Figure 4-2 and Figure 4-3.

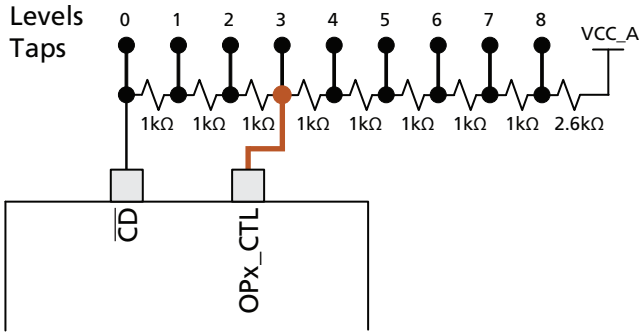


Figure 4-2: Resistor Divider Loopback Example #1 (Function Level 3 from Table 4-5)

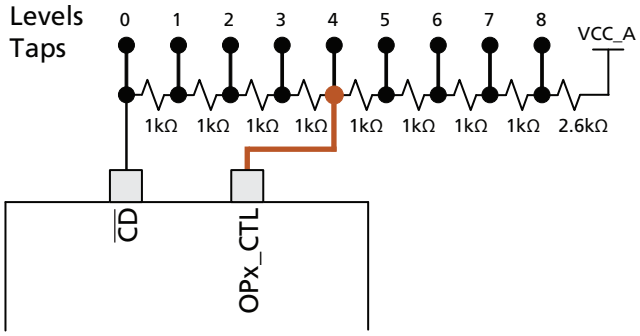


Figure 4-3: Resistor Divider Loopback Example #2 (Function Level 4 from Table 4-5)

In Figure 4-2, automatic muting of the output is established by connecting node 3 to the OPx_CTL pin. In this scenario, the output would be 850mV$_{ppd}$ with 6dB of de-emphasis when there is a signal present.

In Figure 4-3, the OPx_CTL pin is connected to node 4. In this scenario, the output would be 425mV$_{ppd}$ with no de-emphasis when there is a signal present.

In both cases, the output would be muted when no carrier is detected.

Note: When the device is in SLEEP mode, automatic muting and SQ_ADJ do not function. Asserting the SLEEP pin manually overrides all other functionality.

4.8 Cable Length Indicator (CLI)

The GS3441 has a Cable Length Indicator output. This is an analog voltage in the range of 0V to 3.3V, varying monotonically with the input cable length. See Figure 4-4 and Table 4-6 below.

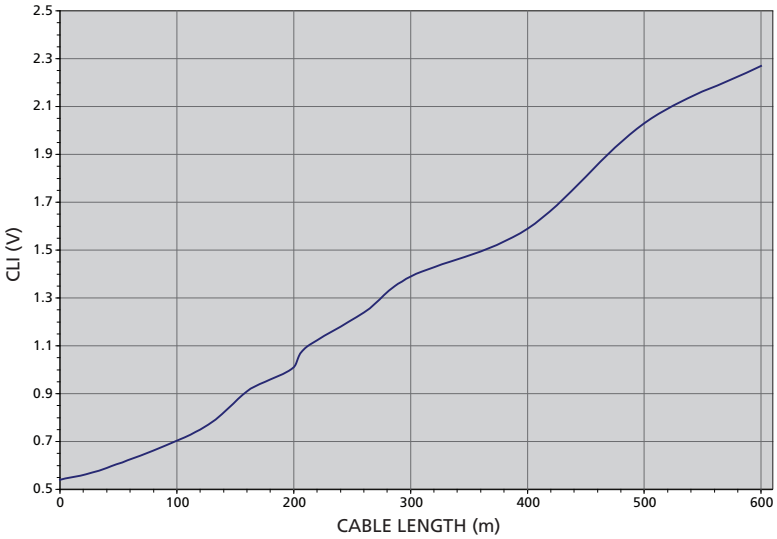


Figure 4-4: Cable Length Indicator Output

Table 4-6: Cable Length Indicator Output

Cable Length (m)	0	40	120	160	180	200	210	260	300	400	500	600
CLI (V)	0.54	0.59	0.75	0.91	0.96	1.01	1.09	1.24	1.39	1.59	2.03	2.27

Note: The CLI output voltage is referenced to VCC_A.

5. Application Information

5.1 High Gain Adaptive Cable Equalizers

The GS3441 is a multi-rate adaptive cable equalizer. In order to continue to extend the cable length that the device can support, it is necessary to have high-gain in the equalizer.

A video cable equalizer must provide wide band gain over a range of frequencies in order to accommodate the range of data rates and signal patterns that are present in a SMPTE compliant serial video stream.

Small levels of signal or noise present at the input pins of the equalizer may cause chatter at the output. In order to prevent this from happening, particular attention must be paid to board layout.

5.2 PCB Layout

Special attention must be paid to component layout when designing Serial Digital Interfaces for HDTV. A FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

- PCB trace width for 3Gb/s rate signals is closely matched to SMT component width to minimize reflections due to change in trace impedance.
- High-speed traces are curved to minimize impedance changes.
- Cutouts in the inner layers should be used under the GS3441 input and output components to minimize parasitic capacitance. For more detail on this and other layout recommendations, please refer to A Guide For Designing With Gennum's 3G-SDI Equalizers.

5.3 Typical Application Circuit

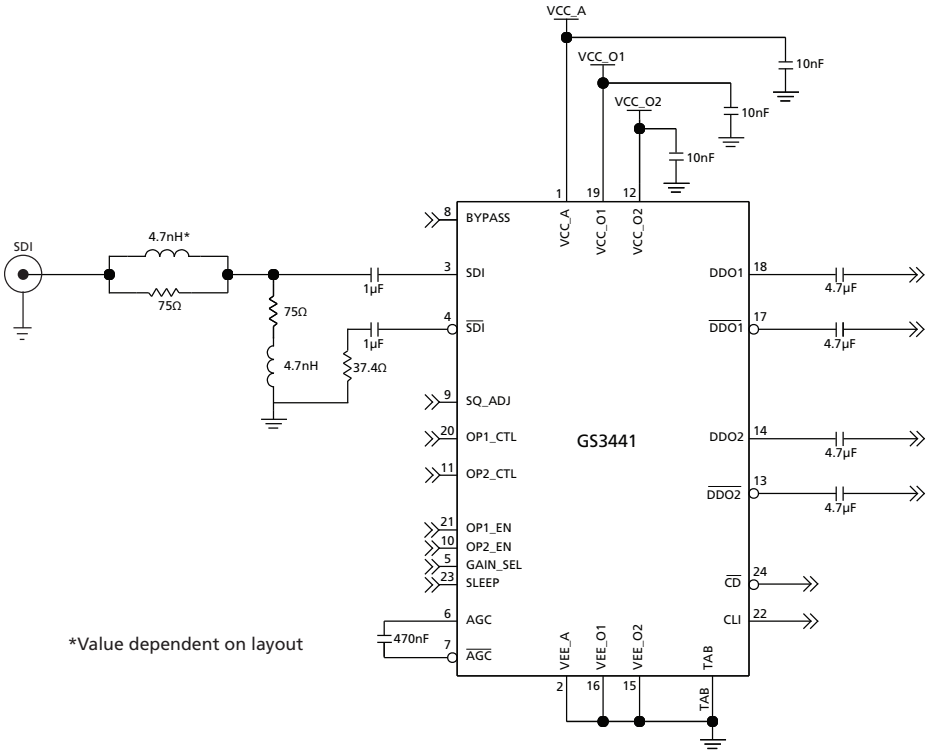


Figure 5-1: GS3441 Typical Application Circuit

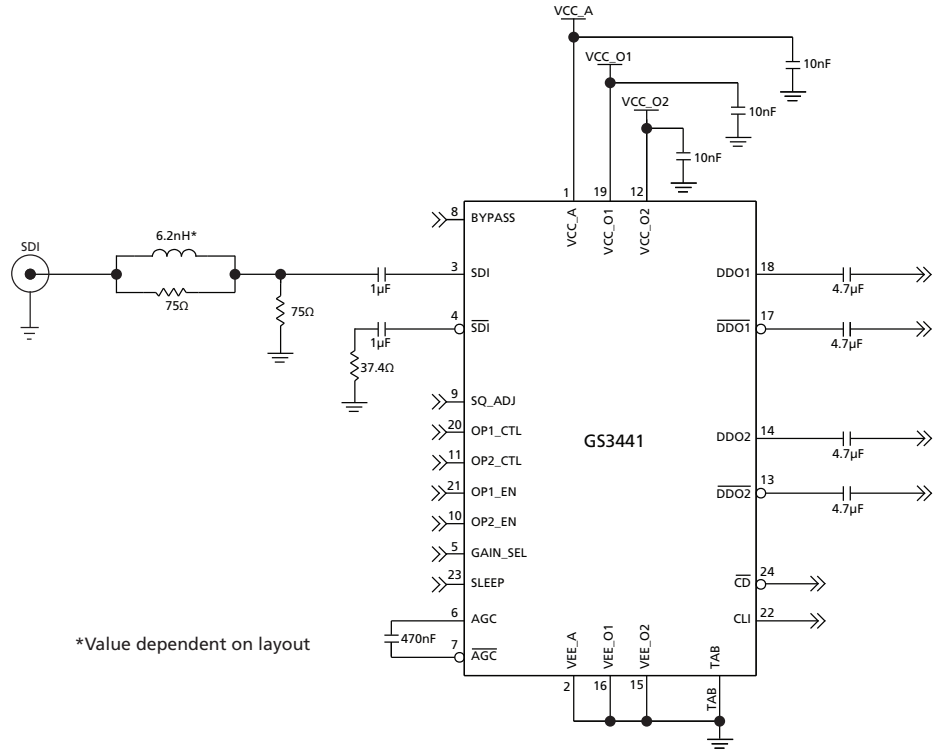
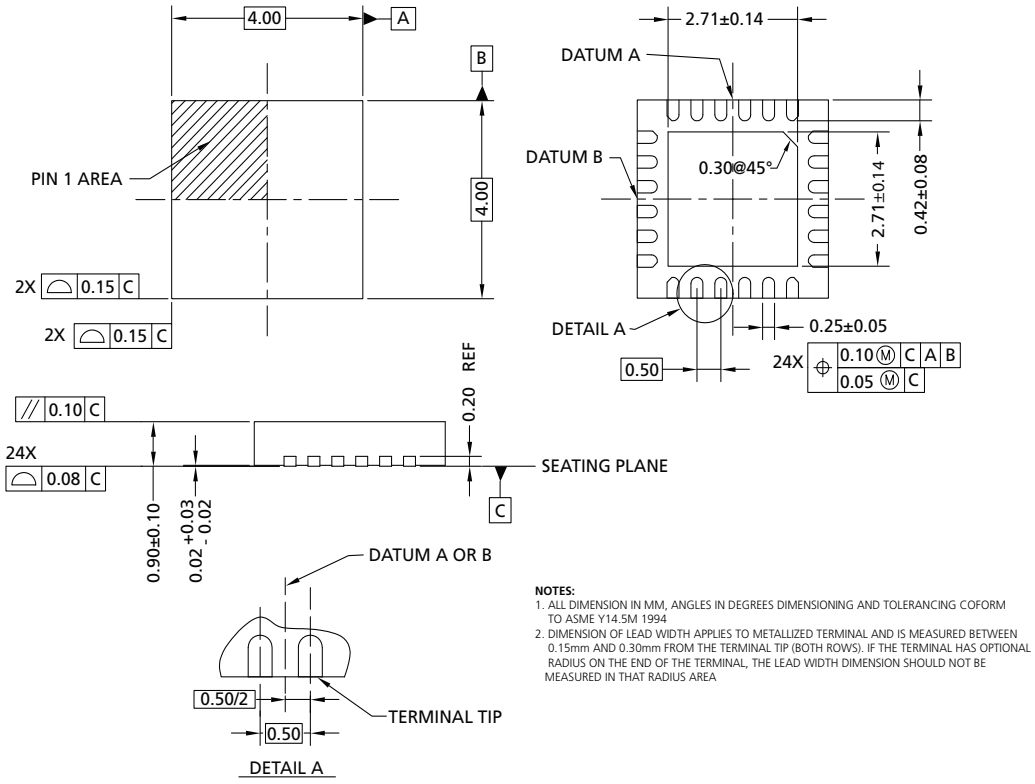


Figure 5-2: GS3441 Alternate Application Circuit Recommended for Drop in Replacement Applications

6. Package & Ordering Information

6.1 Package Dimensions

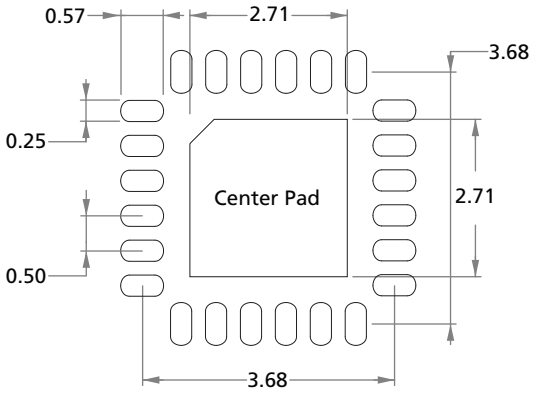


NOTES:
1. ALL DIMENSION IN MM, ANGLES IN DEGREES DIMENSIONING AND TOLERANCING COFORM TO ASME Y14.5M 1994
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

6.2 Packaging Data

Parameter	Value
Package Type	4mm x 4mm 24-pin QFN
Package Drawing Reference	JEDEC M0220
Moisture Sensitivity Level	1
Junction to Case Thermal Resistance, θ_{j-c}	31.0°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	43.8°C/W
Psi, ψ	11.0°C/W
Pb-free and RoHS compliant	Yes

6.3 Recommended PCB Footprint

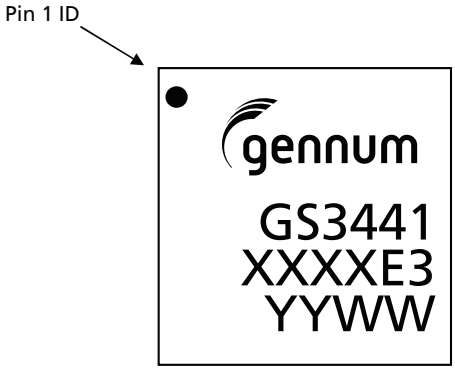


Note: All dimensions in mm

The Center Pad should be connected to the most negative power supply plane for analog circuitry in the device (VEE_A) by a minimum of 5 vias.

Note: Suggested dimensions only. Final dimensions should conform to customer design rules and process optimizations. Ideally, the solder mask and paste mask are slightly smaller than the center pad.

6.4 Marking Diagram



XXXX - Last 4 digits (excluding decimal) of SAP Batch Assembly (FIN) as listed on Packing Slip.
E3 - Pb-free & Green indicator
YYWW - Date Code

6.5 Solder Reflow Profiles

The GS3441 is available in a Pb-free package. It is recommended that the Pb-free package be soldered with Pb-free paste using the reflow profile shown in Figure 6-1.

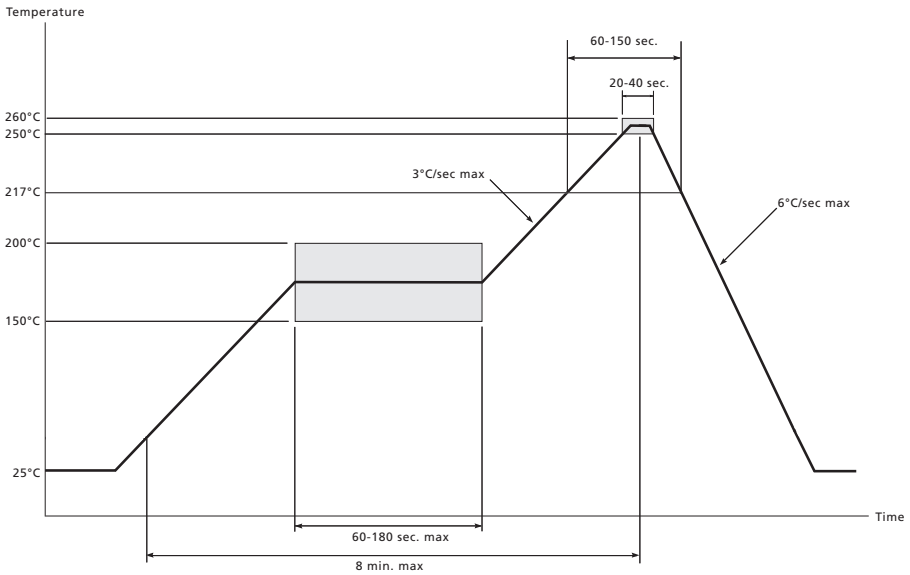


Figure 6-1: Maximum Pb-free Solder Reflow Profile

6.6 Ordering Information

	Part Number	Package	Temperature Range
GS3441	GS3441-INE3	24-pin QFN	-40°C to 85°C
GS3441	GS3441-INTE3	24-pin QFN Tape & Reel (250pcs)	-40°C to 85°C
GS3441	GS3441-INTE3Z	24-pin QFN Tape & Reel (2500pcs)	-40°C to 85°C

Appendix - Relevant Documentation

Document Name	Document Identification
A Guide For Designing With Gennum's 3G-SDI Equalizers	55280

Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
1	012810	–	May 2013	Updates throughout the document, and converted document to Final Data Sheet.
0	158445	–	September 2012	Updated document to the new Semtech format. Removed TBDs from the Typical Application Circuit in Figure 5-1. Updates throughout the document. Converted document to Preliminary Data Sheet.
F	157289	–	November 2011	Removed the Typical Usages section.
E	157162	–	November 2011	Updated the descriptions for the SQ_ADJ and GAIN_SEL pins in Table 1-1 to indicate that they have internal pull-down resistors.
D	156906	–	September 2011	Corrected Package Dimensions and Ordering Information (24-pin QFN package).
C	156829	–	August 2011	Updated power and cable reach numbers in Key Features, Description, DC Electrical Characteristics, AC Electrical Characteristics and Detailed Description.
B	156166	–	May 2011	Updated the cable reach lengths in Key Features and added more detail to section 4.7 Adjustable Output Swing, De-Emphasis and Mute.
A	155974	–	April 2011	New document.

SEMTECH

DOCUMENT IDENTIFICATION
FINAL DATA SHEET
Information relating to this product and the application or design described herein is believed to be reliable, however such information is provided as a guide only and Semtech assumes no liability for any errors in this document, or for the application or design described herein. Semtech reserves the right to make changes to the product or this document at any time without notice.

CAUTION
ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION

Contact Information

Semtech Corporation
Gennum Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com