I3C Master IP Core - Lattice Radiant Software

User Guide

FPGA-IPUG-02082-1.2

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
FPGA	Field Programmable Gate Array
IP	Intellectual Property
LUT	Lookup-Table
I^2C	Inter-Integrated Circuit
LMMI	Lattice Memory Mapped Interface
SDA	Serial Data
SCL	Serial Clock
DA	Dynamic Address
SA	Static Address
DAA	Dynamic Address Assignment
NVM	Non Volatile Memory

1. Introduction

I3C is a two-wire bi-directional serial bus, optimized for multiple sensor Slave devices and controlled by only one I3C Master device at a time. I3C is backward compatible with many legacy I^2C devices, but I3C devices also support significantly higher speeds, new communication modes, and new device roles, including an ability to change device roles over time. For example, the initial Master can cooperatively pass the mastership to another I3C device on the bus, if the requesting I3C device supports a Secondary Master feature.

The Lattice Semiconductor I3C IP improves upon the features of the I^2C interface, preserving backward compatibility.

Implementing the I3C specification greatly increases implementation flexibility for an ever-expanding sensor subsystem as efficiently as possible and at a low cost. Implementation follows the MIPI I3C specification to provide a single scalable, cost effective, power efficient protocol to solve issues with high protocol overhead, increased power consumption, nonstandard protocol, separate lines for interrupt, and the rest requirement. The MIPI I3C interface is developed to ease sensor system design architectures in mobile wireless products by providing a fast, low cost, low power, two-wire digital interface for sensors.

Two main concerns are paramount for the I3C IP Core:

- the use of as little energy as possible in transporting data and control, and
- reducing the number of physical pins used by the interface.

The I3C interface provides major efficiencies in bus power while providing greater than 10x speed improvements over I^2C.

This design is implemented in Verilog. The Lattice Radiant® software Place and Route tool, integrated with Synplify Pro® synthesis tool, is used for design implementation. The design can be targeted to all CrossLink™-NX and Certus™-NX family devices. When used on a different device, density, speed or grade, performance and utilization may vary.

1.1. Quick Facts

Table 1.1 presents a summary of the I3C Master IP Core.

Table 1.1. Quick Facts

IP Requirements	Supported FPGA Family	CrossLink-NX, Certus-NX
Resource Utilization	Targeted Devices	LIFCL-40, LIFCL-17, LFD2NX-40
	Supported User Interfaces	LMMI (Lattice Memory Mapped Interface), APB, AHB
Design Tool Support	Lattice Implementation	IP Core v1.0.x – Lattice Radiant Software 2.1
	Synthesis	Lattice Synthesis Engine (LSE)
		Synopsys® Synplify Pro for Lattice
	Simulation	For the list of supported simulators, see the Lattice Radiant Software 2.1 User Guide.

1.2. Features

An I3C bus requires exactly one I3C device at a time functioning as an I3C Master device. In I3C terms, this I3C Master device is the current master at that time. In typical applications, the current master is the I3C device on the bus that sends the majority of the I3C commands, addressing either all Slaves (Broadcast CCCs) or specific individual Slaves (Directed CCCs). The Current Master is also the only device on the I3C bus allowed to send I^2C Messages.

The MIPI I3C Master Controller supports the following features:

- Two wire serial interface up to 12.5 MHz using Push-Pull
- Legacy I^2C device coexist on the same bus (with some limitations)
- Dynamic Addressing while supporting Static Addressing for legacy I^2C devices
- I^2C -like SDR messaging
- HDR-DDR messaging
- Multi-Master capability
- In-Band Interrupt support
- Hot-Join support
- Synchronous Timing Support (not available in current release) and Asynchronous Time Stamping

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal names that end with:

- _*n* are active low (asserted when value is logic 0)
- _*i* are input signals
- _*o* are output signals

2. Functional Description

2.1. Overview

I3C IP Core supports several communication formats, all sharing a two-wire interface: SDA bidirectional data pin, and SCL bidirectional for the Masters.

The I3C communication protocol supports the following modes:

- SDR mode
- HDR-DDR mode

The I3C bus is always initialized and configured in SDR Mode. Current implementation supports SDR and HDR-DDR modes.

SDR Mode is the default Mode of the I3C bus and is primarily used for private messaging from the Current Master device to Slave devices. SDR Mode is also used to enter other modes and for built-in features, such as Common Commands (CCCs), In-Band Interrupts, and transition from I^2C to I3C by assignment of a Dynamic Address. I3C SDR Mode is significantly similar to the I^2C protocol in terms of procedures and conditions, as a result, I3C devices and many legacy I^2C Slave devices (but not I^2C Master devices) can coexist on the same I3C bus.

Like SDR Mode, HDR-DDR Mode uses SCL as a clock; but unlike SDR, Data and Commands change SDA on both SCL edges, effectively doubling the data rate. By contrast, in SDR Mode SDA is changed only when SCL is Low.

HDR-DDR moves data by Words. A Word generally contains 16 payload bits, as two bytes in a byte stream, and two parity bits.

Four HDR-DDR Word Types are defined:

- Command Word
- User Data
- CRC Word
- Reserved Word

The HDR-DDR Protocol precedes each 18-bit Word with a 2-bit Preamble, for a total of 20 bits per Word. The Preamble:

- Indicates the type of data that follows: either Command, Data, or CRC
- Allows the Master to terminate a Read and to determine whether the Slave is willing to respond to a Read. This is controlled such that the first bit is Parked High and the other side can choose either to drive Low or to leave High

The I3C Master Controller accepts commands from a LMMI interface. These commands are decoded into I3C Slave Device Read/Write transactions. Furthermore, the I3C Master Controller can operate in interrupt or polling mode. This means that the LMMI interface can choose to poll the I3C Master for a change in status at periodic intervals or wait to be interrupted by the I3C Master Controller when data needs to be read or written.

I3C Master IP Core functional diagram is shown in Figure 2.1.

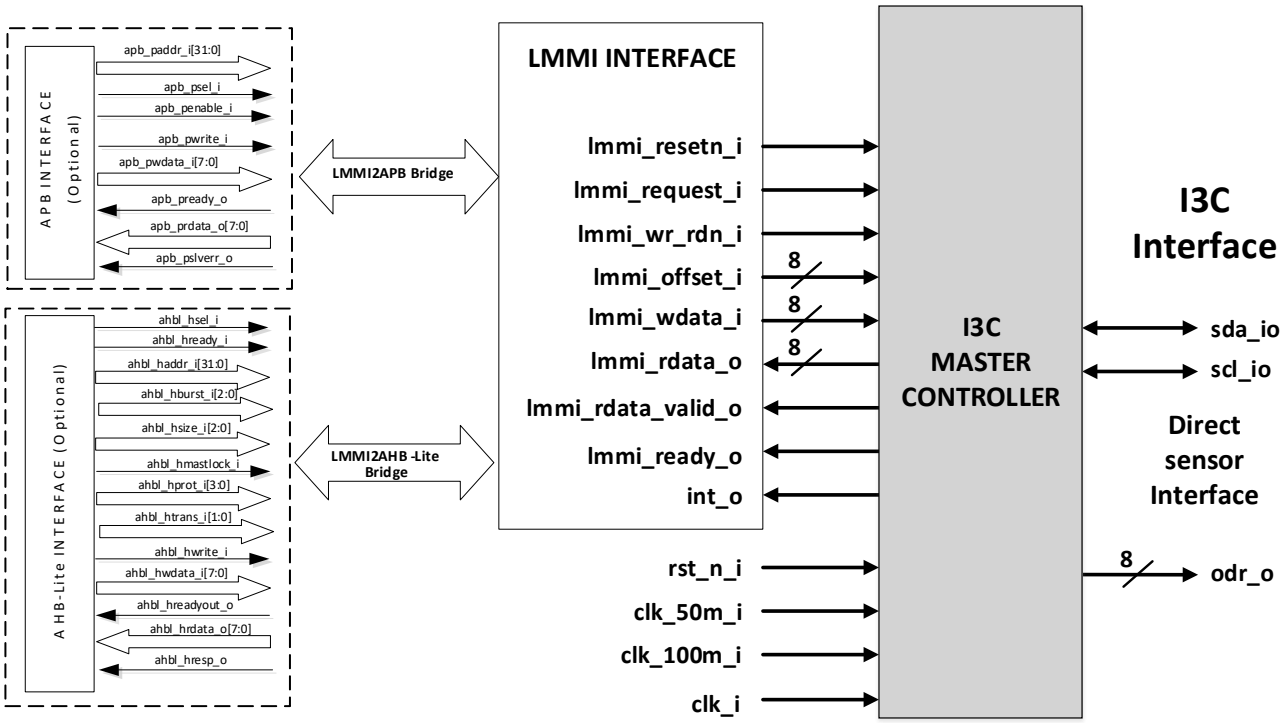

Figure 2.1. I3C Master IP Core Functional Diagram

The I3C Master Controller design module contains the following functional blocks:

- LMMI interface
- I3C Master Controller Top
  - Bus Management Block
    - Configuration Registers
    - Dynamic Address and Priority Levels Allocation
    - In-Band Interrupt and Hot-Join Management, Master level
    - Data Packet Generator HDR-DDR and/or I^2C
  - PHY Layer
    - ACTIVE DRIVER and PUR SDA
    - ACTIVE DRIVER and PUR SCL
    - IO PAD SDA
    - IO PAD SCL

A top-level block diagram of the I3C Master Controller is shown in Figure 2.2.

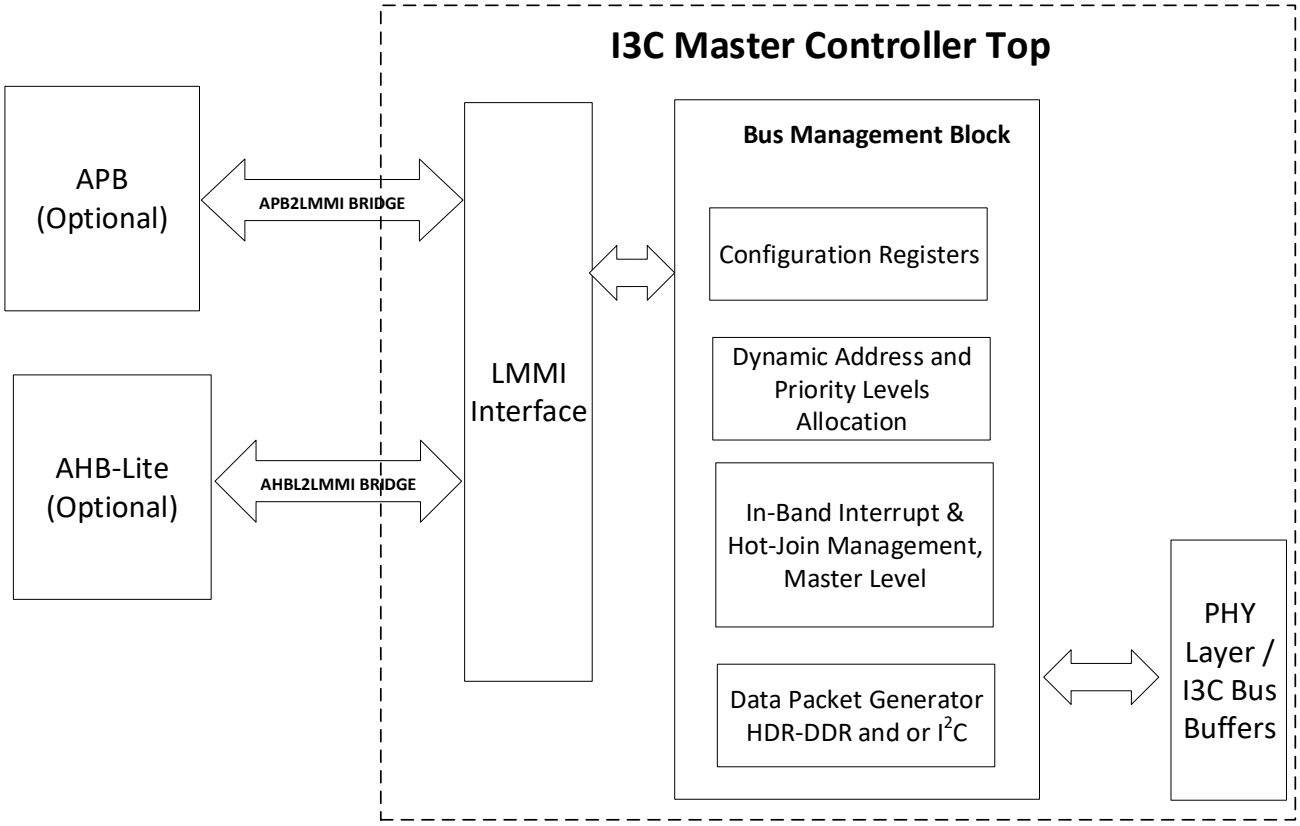

Figure 2.2. Top Level Block Diagram

2.1.1. I3C Master Controller Top Logic

This is the top-level HDL block of the I3C Master Controller design module. This block is created to instantiate all modules of the design and control of tristate drivers of the SDA and SCL signals. I3C Master Controller has two Main Master device roles and may also support one of the two Secondary Master device roles.

Two Main Master device roles are listed below.

- Main Master: The I3C Master device on the I3C bus that initially configures the I3C bus and serves as the first Current Master. Only one I3C device on a given I3C bus can take the Main Master role, that is, the role cannot be passed on to any other I3C device on the I3C bus. It supports both SDR Mode and HDR-DDR Mode.
- SDR-Only Main Master: A Main Master that only supports I3C's SDR Mode; does not support any of the HDR-DDR Mode.

There are two Secondary Master device roles, listed below.

- I3C Secondary Master: Any I3C device on the I3C bus, other than the Current Master, with I3C Master Capability. There can be multiple Secondary Masters on an I3C bus at the same time. By definition, a Secondary Master functions as an I3C Slave device until and unless it eventually becomes Current Master. It supports both SDR Mode and HDR-DDR Mode.
- SDR-Only Secondary Master: A Secondary Master that only supports I3C's SDR Mode; does not support any of the HDR-DDR Mode.

2.1.2. LMMI Interface

The LMMI device module implements memory mapped registers. This interface is suited for IP blocks which use dynamically programmable configuration/control bits and read/write transactions. LMMI is a memory-mapped address/data interface which supports both single and burst transactions with a maximum throughput of one transaction per clock cycle.

The LMMI Interface module is a fully synchronous module that runs off the LMMI clock. A number of registers are initialized via the LMMI interface to ensure that the I3C Master IP Core functions as intended. LMMI defines a standard set of interface signals for register/memory access. The basic requirement is that any additional interface signals must not duplicate functionality described in this spec, that is, there should be only one interface (LMMI) for register/memory access.

For this particular IP, this block has two main functions:

- Accepts write data from the microprocessor and latches the data into the appropriate registers and read/write buffers.
- Controls data being sent to the microprocessor from the I3C Master Controller.

This block also generates an interrupt signal when either Transmit Buffer Empty flag or Receive Buffer Full flag are set.

The LINTR (Lattice Interrupt Interface) Interface consists of an interrupt signal and a set of interrupt registers which are accessed through LMMI. These interrupt registers follow a standard functional definition, allowing you to implement common hardware/software to handle interrupts from a variety of Hard IP blocks.

For more information on LMMI, see the Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039).

2.1.3. AHB-Lite/APB to LMMI Bridge

When AHBL Mode is selected, AHBL2LMMI Bridge is instantiated inside the I3C Master IP and the native LMMI interface is translated to AHB-Lite interface.

When APB Mode is selected, APB2LMMI is instantiated inside the I3C Master IP and the native LMMI interface is translated to APB interface.

These optional bridges are implemented to easily interface the I3C Master IP in APB and AHB-Lite systems while preserving the native LMMI interface for writing and reading to internal registers and FIFO.

2.1.4. Bus Management Block

The I3C bus is configured as the link among several clients, in a flexible and efficient manner. At the system architecture level, eight roles are defined for I3C compatible devices. An example block diagram of I3C interconnections is shown in Figure 2.3. In this diagram there is a device with Main Master role, devices with I3C Slave role and devices with I^2C Slave role. Note that I3C Secondary Master devices are gradient shaded, illustrating their ability to function in both Master and Slave roles (at different times). I3C Master IP Core implements I3C Main Master and Secondary Master roles.

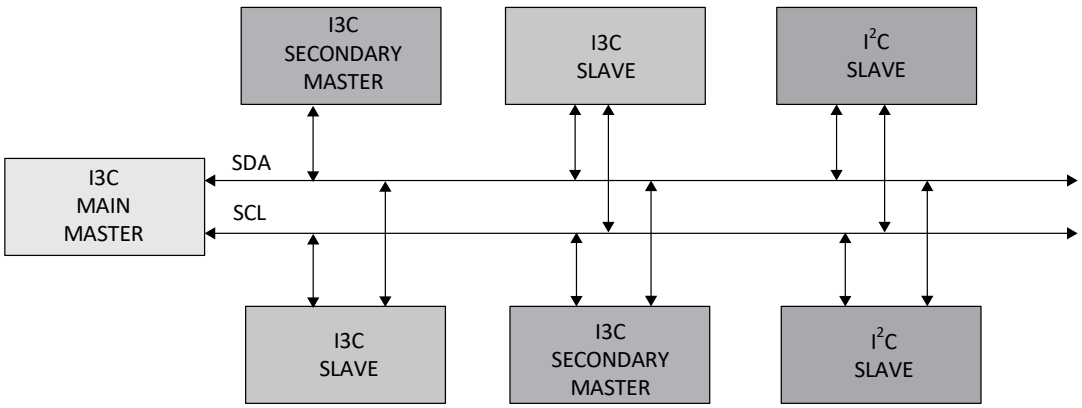

Figure 2.3. Bus Interconnect

2.1.4.1. I3C Configuration Registers

I3C Characteristics Registers describe and define an I3C compatible device's capabilities and functions on the I3C bus, as the device services a given system. devices without I3C Characteristics Registers should not be connected to a common I3C bus.

There are three Characteristics Register types:

- Bus Characteristics Register (BCR)
- Device Characteristics Register (DCR)
- Legacy Virtual Register (LVR)

Every I3C compatible device has associated Characteristics Registers, depending on the device types described below:

- Every I3C compliant device has one bus Characteristics Register, and one device Characteristics Register.
- Every legacy I^2C device to be connected to an I3C bus has one associated Legacy Virtual Register. Since these are legacy devices, it is understood that this register exists virtually, for example as part of the device's driver.

2.1.4.2. Dynamic Address and Priority Levels Allocation

The Main Master is responsible for performing a Dynamic Address Assignment procedure, to provide a unique Dynamic Address to each device connected to the I3C bus.

The Main Master provides Dynamic Address to a device:

- Upon any initialization of the I3C bus, and
- When the device is connected to an already configured I3C bus.

Once a device receives a Dynamic Address, that Dynamic Address is used in all of that device's subsequent transactions on the I3C bus, until and unless the Master changes the device's Dynamic Address. The only way for the Master to change the device's Dynamic Address is by using either the RSTDA CCC command or the SETNEWDA CCC command. The Master might choose to change the device's Dynamic Address due to re-prioritization. The Main Master controls the Dynamic Address Assignment process. This process includes an Address Arbitration procedure similar to I^2C's. The I3C Arbitration procedure differs from I^2C by using the values of the 48-bit Provisional ID and the device's I3C Characteristic Registers (that is, BCR and DCR), concatenated. The device on the I3C bus with the lowest concatenated value wins each Arbitration round in turn, and the Main Master assigns a unique Dynamic Address to each winning device.

2.1.4.3. In-Band Interrupt and Hot-Join Management block

In I3C, Priority Level controls the order in which Slaves' In-Band Interrupt requests and Master requests are processed. The Priority Level of each Slave in an I3C bus instantiation is encoded in its Slave Address, with lower addresses having higher Priority. That is, Slaves with lower value Addresses and higher Priority Levels have their In-Band Interrupts and Master requests processed sooner than Slaves with higher value Addresses and lower Priority Levels.

During each Dynamic Address Assignment operation, the I3C Master Controller assigns lower Addresses to Slaves for higher Priority In-Band Interrupt requests.

The In-Band Interrupt block does one of the following three things:

- Accept the IBI by providing the ACK bit. The actions available to the Current Master depend upon the value of the Slave's BCR [2] bit (in the Slave's BCR register)
- Refuse the IBI without disabling interrupts. To do this, the Current Master simply passively NACKs to deny the IBI. (The Current Master knows that the Slave should try to interrupt again on the next START, which causes the Current Master to issue a Repeated START.)
- Refuse the IBI and disable interrupts. To do this, the Current Master NACKs to deny the IBI, then sends a Repeated START, and finally sets the DISINT bit in the Command Code Disable Slave Events Command (DISEC) to the interrupting Slave. (The Current Master can set the ENINT bit in the Command Code Enable Slave Events Command (DISEC) in a later time.)

Hot-Join block implements a method that allows the system designer to prevent the I3C Master Controller from attempting to Hot-Join when the device is not being used as a Hot-Join device.

The Hot-Join block may power-up at the same time as the Main Master (e.g. may be connected to the I3C bus when power is applied to the system). In that case, the Main Master might pull SDA Low even before the I3C bus has been started, assuming that SCL and SDA are being pulled up. If a Main Master needs 1ms or more to start acting on the I3C bus, then that Main Master is able to accommodate the situation of SDA being held Low when it is ready to initialize the I3C bus, or it may instead delay pulling SDA High, and/or pulling SCL High, until it is ready.

2.1.4.4. Data Packet Generator HDR-DDR

This block generates an I3C HDR-DDR mode data signals. The HDR-DDR Protocol uses the same signaling as SDR, but operates with SDA changing after each SCL edge. Each Command Word and each Data Word is 20 bits in length (20 clock edges) including a two-bit Preamble. HDR-DDR Command Words indicate the direction of data movement: either Write (Master to Slave), or Read (Slave to Master). After the Command Word, zero or more Data Words are sent by the Master or by the Slave (unless NACK-ed) until done, followed by the CRC Word (unless NACK-ed).

In HDR-DDR Mode, just as in SDR Mode, only the I3C bus Master drives the SCL line. For Commands, the SDA line is driven by the Master. For Data, the SDA line is driven either by the Slave or by the Master, depending on the Command direction (Bus Turnaround).

There are three points of Bus Turnaround (between Master and Slave) with HDR-DDR Mode:

- After a Read Command from the Master, the Slave drives SDA to indicate that the Slave plans to return Data.
- After the end of Data from the Slave for a Read Command, the Master drives SDA again.
- There is an optional Bus Turnaround before Data Words are returned by the Slave, allowing the Master to prematurely terminate a Read.

2.1.5. Bus Characteristics Register (BCR)

Each I3C device that is connected to the I3C bus has an associated read-only Bus Characteristics Register (BCR). This read-only register describes the I3C compliant device's role and capabilities for use in Dynamic Address assignment and Common Command Codes.

Table 2.1. Bus Characteristics Register

Bit	Name	Description
7	Device Role [1]	2'b00 – I3C Slave 2'b01 – I3C Master 2'b10 – Reserved for future definition 2'b11 – Reserved for future definition
6	Device Role [0]	
5	SDR Only / SDR and HDR-DDR Capable	0 – SDR only 1 – HDR-DDR Capable
4	Bridge Identifier	0 – Not a Bridge device 1 – Is a Bridge device
3	Offline Capable	0 – Device always responds to I3C bus commands 1 – Device not always responds to I3C bus commands
2	IBI Payload	0 – No data byte follows the accepted IBI 1 – Mandatory one or more data bytes follow the accepted IBI. Data byte continuation is indicated by T-Bit
1	IBI Request Capable	0 – Not Capable 1 – Capable
0	Max Data Speed Limitation	0 – No Limitation 1 – Limitation

2.1.6. Device Characteristics Register (DCR)

Each I3C device that is connected to the I3C bus has an associated read-only Device Characteristics Register (DCR). This read-only register describes the I3C compliant device type (e.g. accelerometer, gyroscope, etc.) for use in Dynamic Address assignment and Common Command Codes.

Table 2.2. Device Characteristics Register

Bit	Name	Description
7	Device ID [7]	255 available codes for describing the type of sensor, or device. Examples: Accelerometer, gyroscope, composite devices. Default value is 8'b0: Generic device
6	Device ID [6]	
5	Device ID [5]	
4	Device ID [4]	
3	Device ID [3]	
2	Device ID [2]	
1	Device ID [1]	
0	Device ID [0]	

2.1.7. Legacy Virtual Register (LVR)

Each legacy I^2C device that can be connected to the I3C bus has an associated read-only Legacy Virtual Register (LVR) describing the device's significant features. Since these are legacy I^2C devices, it is understood that this register exists virtually, for example as part of the device's driver. When legacy I^2C devices are present on an I3C bus, LVR data determines allowed Modes and maximum SCL clock frequency. All LVRs are established by the higher-level entity controlling the I3C bus and transferred to the I3C bus Main Master prior to bus configuration. The LVR content for all I^2C devices is always known by the Main Master.

Table 2.3. Legacy Virtual Register

Bit	Name	Description
7	Legacy I^2C only [2]	3'b000 – Index 0 3'b001 – Index 1 3'b010 – Index 2 3'b011 – Index 3 (Reserved) 3'b100 – Index 4 (Reserved) 3'b101 – Index 5 (Reserved) 3'b110 – Index 6 (Reserved) 3'b111 – Index 7 (Reserved)
6	Legacy I^2C only [1]	
5	Legacy I^2C only [0]	
4	I^2C Mode Indicator	0 – I^2C Fm+ 1 – I^2C Fm
3	Reserved	15 available codes for describing the device capabilities and function on the sensors' system.
2	Reserved	
1	Reserved	
0	Reserved	

2.2. Signal Description

Table 2.4 lists the input and output signals for I3C Master IP Core along with their descriptions.

Table 2.4. Ports Description

Name	Direction	Description
System Clock and Reset		
clk_i	Input	System Clock
rst_n_i	Input	Master core reset
Master Clock		
clk_50m_i	Input	Master core clock
clk_100m_i	Input	Incorporated Slave core clock
I3C Interface		
scl_io	In/Out	SCL input for listening, SCL output for driving
sda_io	In/Out	SDA input to the master from the slave, SDA output from the master to the slave
LMMI Interface[1]		
lmmi_resetn_i	Input	Reset (active low) Resets the LMM interface and sets registers to their default values. Does not reset the internals of the Hard IP block.
lmmi_request_i	Input	Start transaction
lmmi_wr_rdn_i	Input	Write = HIGH, Read = LOW
lmmi_offset_i[n:0]	Input	Offset (0-31 bits) – register offset within the slave, starting at offset 0. Bit width is hard IP dependent.
lmmi_wdata_i[n:0]	Input	Write data (0-16 bits) Bit width is hard IP dependent.
lmmi_rdata_o[n:0]	Output	Read data (0-16 bits) Bit width is hard IP dependent.
lmmi_rdata_valid_o	Output	Read transaction is complete and lmmi_rdata[] contains valid data.
lmmi_ready_o	Output	Slave is ready to start a new transaction. Slave can insert wait states by holding this signal low. This signal is optional in hardware and mandatory in RTL soft wrappers. Hardware slaves may omit this signal if they do not need wait states. For zero-wait-state slaves, the soft wrapper ties this signal high.
LINTR Interface		
int_o	Output	Interrupt. Hard IP block has an interrupt, which needs to be serviced. Active high, level sensitive. Stays high while as any enabled interrupt is pending.
AHB-Lite Interface[2]		
ahbl_hsel_i	Input	AHB-Lite Select signal
ahbl_hready_i	Input	AHB-Lite Ready Input signal
ahbl_haddr_i[31:0]	Input	AHB-Lite Address signal (9 LSB used)
ahbl_hburst_i[2:0]	Input	AHB-Lite Burst Type signal
ahbl_hsize_i[2:0]	Input	AHB-Lite Transfer Size signal
ahbl_hmastlock_i	Input	AHB-Lite Lock signal
ahbl_hprot_i[3:0]	Input	AHB-Lite Protection Control signal
ahbl_htrans_i[1:0]	Input	AHB-Lite Transfer Type signal
ahbl_hwrite_i	Input	AHB-Lite Direction signal. Write = High, Read = Low
ahbl_hwdata_i[31:0]	Input	AHB-Lite Write Data signal (8 LSB used)
ahbl_hreadyout_o	Output	AHB-Lite Ready Output signal
ahbl_hrdata_o[31:0]	Output	AHB-Lite Read Data signal (8 LSB used)
ahbl_hresp_o	Output	AHB-Lite Transfer Response signal

Name	Direction	Description
APB Interface[3]		
apb_paddr_i[31:0]	Input	APB Address signal. (9 LSB used)
apb_psel_i	Input	APB Select signal
apb_penable_i	Input	APB Enable signal
apb_pwrite_i	Input	APB Direction signal
apb_pwdata_i[31:0]	Input	APB Write Data signal (8 LSB used)
apb_pready_o	Output	APB Ready signal
apb_prdata_o[31:0]	Output	APB Read Data signal (8 LSB used)
apb_pslverr_o	Output	APB Slave Error signal
Direct Sensor Interface		
sdr_o	Output	8-bit ODR data in KSPS

Notes:

1. LMMI Interface is only available when selected from the user interface.
2. AHB-Lite Interface is only available when selected from the user interface. Refer to AMBA 3 AHB-Lite Protocol Specification for details of the protocol.
3. APB Interface is only available when selected from the user interface. Refer to AMBA 3 APB Protocol v1.0 Specification for details of the protocol.

2.3. Attributes Summary

Table 2.5 provides the list of user-selectable and compile time configurable parameters for the I3C Master IP Core. Attributes are described in Table 2.6. The parameter settings are specified using I3C Master IP Core Configuration user interface in Lattice Radiant.

Table 2.5. Attributes Table

Attribute	Selectable Values	Default	Dependency on Other Attributes
General			
CPU Interface			
Interface	LMMI, APB, AHBL	LMMI	—
Bus Characteristics			
Device Role	Main Master, Secondary Master	Main Master	—
Bus Type	HDR-capable only	HDR-capable	—
HDR Type	DDR	DDR	Bus Type = HDR capable
Offline Capable	Not Checked	Not Checked	—
IBI Capable	Checked, Not Checked	Checked	Device Role = Secondary Master
IBI: Number of bytes in a single sample [0–128]	0–128	2	IBI Capable = True, Receive Buffer Address Width
Hot-Join Capable	Checked, Not Checked	Checked	Device Role = Secondary Master
Stall Support	Checked, Not Checked	Checked	—
Max Data Speed Limitation	Checked	Checked	Device Role = Secondary master
Number of Dynamic Address Devices on Bus [0–8]	0–8	1	—
Number of Static Address I3C Devices on Bus [0–8]	0–8	0	—

Attribute	Selectable Values	Default	Dependency on Other Attributes
Settings			
I3C Dynamic Address Table			
I3C Device 1 DA (hex) [4–7]	4–7D	35	Grayed out when Number of Dynamic Address Devices on Bus is less than 1
I3C Device 2 DA (hex) [4–7]	4–7D	4A	Grayed out when Number of Dynamic Address Devices on Bus is less than 2
I3C Device 3 DA (hex) [4–7]	4–7D	4C	Grayed out when Number of Dynamic Address Devices on Bus is less than 3
I3C Device 4 DA (hex) [4–7]	4–7D	5C	Grayed out when Number of Dynamic Address Devices on Bus is less than 4
I3C Device 5 DA (hex) [4–7]	4–7D	5D	Grayed out when Number of Dynamic Address Devices on Bus is less than 5
I3C Device 6 DA (hex) [4–7]	4–7D	68	Grayed out when Number of Dynamic Address Devices on Bus is less than 6
I3C Device 7 DA (hex) [4–7]	4–7D	6A	Grayed out when Number of Dynamic Address Devices on Bus is less than 7
I3C Device 8 DA (hex) [4–7]	4–7D	6C	Grayed out when Number of Dynamic Address Devices on Bus is less than 8
I3C Static Address Table			
I3C Device 1 SA (hex) [4–7D]	4–7D	9	Grayed out when Number of Static Address I3C Devices on Bus is less than 1
I3C Device 2 SA (hex) [4–7D]	4–7D	A	Grayed out when Number of Static Address I3C Devices on Bus is less than 2
I3C Device 3 SA (hex) [4–7D]	4–7D	B	Grayed out when Number of Static Address I3C Devices on Bus is less than 3
I3C Device 4 SA (hex) [4–7D]	4–7D	C	Grayed out when Number of Static Address I3C Devices on Bus is less than 4
I3C Device 5 SA (hex) [4–7D]	4–7D	D	Grayed out when Number of Static Address I3C Devices on Bus is less than 5
I3C Device 6 SA (hex) [4–7D]	4–7D	E	Grayed out when Number of Static Address I3C Devices on Bus is less than 6
I3C Device 7 SA (hex) [4–7D]	4–7D	F	Grayed out when Number of Static Address I3C Devices on Bus is less than 7
I3C Device 8 SA (hex) [4–7D]	4–7D	10	Grayed out when Number of Static Address I3C Devices on Bus is less than 8
Device Characteristics: Run-Time Configurable			
DCR Value (hex) [0–FF]	0 - FF	0	Device Role = Secondary Master
Static Address Enable	Checked, Unchecked	Checked	Device Role = Secondary Master
Static Address (hex) [4–7D]`	4–7D	28	Static Address Enable = True and device Role = Secondary Master
Dynamic Address of Main Master (hex) [4–7D]	4–7D	8	Device Role = Main Master
Manufacturer ID [0–32767]	0–32767	414	Device Role = Secondary Master
Part ID [0–65535]	0–65535	1	Device Role = Secondary Master
Instance ID [0–15]	0–15	1	Device Role = Secondary Master
Additional ID [0–4095]	0–4095	0	Device Role = Secondary Master
Clocks			
System Clock Frequency (MHz) [80–125]	80 - 125	100	-
I3C Core Clock Frequency (MHz)	N/A	50	Greyed out

Attribute	Selectable Values	Default	Dependency on Other Attributes
Slave Mode Timing Characteristics			
Max Write Data Speed	Max, 8MHz, 6MHz, 4MHz, 2MHz	Max	Device Role = Secondary Master
Max Read Data Speed	Max, 8MHz, 6MHz, 4MHz, 2MHz	Max	Device Role = Secondary Master
Max Clock to Data Turnaround Time	8ns, 9ns, 10ns, 11ns, 12ns	>12 ns	Greyed out, Device Role = Secondary Master
Storage Characteristics			
Max Write Address Depth [8–256]	8 - 256	256	Device Role = Secondary Master
Max Read Address Depth [16–256]	16 - 256	256	Device Role = Secondary Master

Table 2.6. Attributes Descriptions

Attribute	Description
General	
CPU Interface	
Interface	Selects memory-mapped interface from the list for register access by the host Available values: LMMI (default), APB, AHBL
Bus Characteristics	
Device Role	Selects the role of device according to the I3C Specification v1.0.
Bus Type	HDR capability. Always capable (common state machine for all modes). Grayed out.
HDR Type	HDR supported modes. Only DDR is supported. Grayed out
Offline Capable	Offline capability support. Currently grayed out, not supported, since the related data must be stored in NVM.
IBI Capable	IBI capability selector for Secondary Master. For the Main Master IBI is always supported.
IBI: Number of bytes in a single sample	IBI payload size. Must be less or equal to 2**(Receive Buffer Address Width). I.e. Main Master's maximum IBI payload size acceptance depends on Master's Receive Buffer Address Width. After IBI request processing first location in FIFO is the DA of the Slave, which requested the interrupt.
Hot-Join Capable	HJ capability for Secondary Master. Main Master always supports HJ.
Stall Support	If checked, extends T-bit by two core clock cycles. Recommended for robust I3C bus operation.
Max Data Speed Limitation	Secondary master feature. Checked for not supported TSL/TSP modes. Grayed out.
Number of Dynamic Address Devices on Bus	Activates "I3C Dynamic Address Table" fields for editing. Aggregate number of DA capable and SA capable devices must be from 1 to 8.
Number of Static Address I3C Devices on Bus	Activates "I3C Static Address Table" fields for editing. Aggregate number of DA capable and SA capable devices must be from 1 to 8.
Settings	
I3C Dynamic Address Table	
I3C Device 1 DA	I3C DA address to be assigned to the Slave device during address assignment procedure. Device 1 default is 0x35. Allowable address range is 0x04-0x7D. User must choose the addresses based on recommendations given in I3C Specification v1.0.
I3C Device 2 DA	Device 2 default is 0x4A.
I3C Device 3 DA	Device 3 default is 0x4C.
I3C Device 4 DA	Device 4 default is 0x5C.
I3C Device 5 DA	Device 5 default is 0x5D.

Attribute	Description
I3C Device 6 DA	Device 6 default is 0x68.
I3C Device 7 DA	Device 7 default is 0x6A.
I3C Device 8 DA	Device 8 default is 0x6C.
I3C Static Address Table	
I3C Device 1 SA	I3C SA address of the Slave device, if known. Device 1 default is 0x09. Allowable address range is 0x04-0x7D. Currently these values are stored in the Master registers for being accessible from the host side and not used in any other way.
I3C Device 2 SA	Device 2 default is 0x0A.
I3C Device 3 SA	Device 3 default is 0x0B.
I3C Device 4 SA	Device 4 default is 0x0C.
I3C Device 5 SA	Device 5 default is 0x0D.
I3C Device 6 SA	Device 6 default is 0x0E.
I3C Device 7 SA	Device 7 default is 0x0F.
I3C Device 8 SA	Device 8 default is 0x10.
Device Characteristics: Run-Time Configurable	
DCR Value (hex)	Device Characteristics Register. It is recommended to assign a value to this register according to the list of the devices, which can be found at : https://www.mipi.org/MIPI_I3C_device_characteristics_register.
Static Address Enable	If Secondary Master, a SA may be assigned to device, which is accessible to the host. Main Master may assign DA to this device using the SA bypassing the DAA procedure, if knows its SA (designer must pass the SA to the Main Master host application).
Static Address (hex)	If Secondary Master and “Static Address Enable” is checked, defines device’s SA.
Dynamic Address of Main Master (hex)	DA of the Main Master used in DEFSLVS transaction CCC.
Manufacturer ID	If Secondary Master, defines Provisional ID[47:33] bits.
Part ID	If Secondary Master, defines Provisional ID[31:16] bits.
Instance ID	If Secondary Master, defines Provisional ID[15:12] bits
Additional ID	If Secondary Master, defines Provisional ID[11:0] bits
Clocks	
System Clock Frequency (MHz)	Interface clock frequency. Recommended value is 100MHz.
I3C Core Clock Frequency (MHz)	Must be 50 MHz for correct I3C bus timing.
Slave Mode Timing Characteristics	
Max Write Data Speed	Maximum I3C bus data write speed for device. Required by I3C Specification but actually capable of maximum speed, since it is a master more. Can be set, if a third party Main Master differentiates the speed. Current implementation of the Master does not support low speeds.
Max Read Data Speed	Maximum I3C bus data read speed for device. Required by I3C Specification but actually capable of maximum speed, since it is a master more. Can be set, if a third party Main Master differentiates the speed. Current implementation of the Master does not support low speeds.
Max Clock to Data Turnaround Time	The time duration between reception of an SCL edge and the start of driving an SDA change. Set to maximum for safety.
Slave Mode Storage Characteristics	
Max Write Address Depth	Secondary Master’s maximum write depth.
Max Read Address Depth	Secondary Master’s maximum read depth.

2.4. Register Description

The I3C Master Controller is projected to work in close cooperation with the host application. It translates the commands latched in the control registers into the I3C bus activity according to I3C bus protocol. It has built-in LMMI interface. Since the Master device must support secondary master requests and if the request is granted, it must act as a slave before requesting the mastership back.

I3C Master Controller configuration registers are located at the addresses shown in Table 2.7 detailed description of the register bits is in the

Registers Bits Description section. To distinguish between the Master and Slave functionality registers LMMI interface has 9-bit addressing. Bit [8] of the LMMI offset, if set, addresses the Slave functional registers. If bit [8] is equal to zero, it addresses the Master related registers.

Table 2.7 the addresses belonging to the Secondary master functionality (0x1XX) are shaded.

Table 2.7. Register Address Map

LMMI offset HEX	APB/AHB Offset HEX	RW	Register (RTL name)	Used bits	Description
000	0000	R	addr_reg0	[7:0]	Revision, current revision is AB
001	0004	RW	addr_reg1	[0]	Command start strobe
002	0008	RW	addr_reg2	[7:0]	Command register
003	000C	RW	addr_reg3	[7:0]	Dynamic/Static address register
004	0010	RW	addr_reg4	[7:0]	Transaction length in bytes
005	0014	RW	addr_reg5	[7:0]	Write buffer
006	0018	RW	addr_reg6	[7:0]	Read buffer
007	001C	R	addr_reg7	[7:0]	Command execution status
008	0020	RW	addr_reg8	[0]	Combined command control
009	0024	RW	addr_reg9	[0]	Secondary master request
00A	0028	RC	addr_rega	[0]	Read Clear register. Read data from sensor over flag
00B	002C	RW	addr_regb	[4], [0]	ssp_control_init
00C	0030	R	addr_regc	[5:0]	Management state machine state
00E	0038	R	addr_rege	[7], [4:0]	Command done, Processed command status
00F	003C	RW	addr_regf	[7:0]	Test register
010	0040	R	addr_reg10	[7:0]	i3c_number (NOT implemented, 0)
011	0044	R	addr_reg11	[7:0]	pid_byte5
012	0048	R	addr_reg12	[7:0]	Got pid_byte4
013	004C	R	addr_reg13	[7:0]	Got pid_byte3
014	0050	R	addr_reg14	[7:0]	Got pid_byte2
015	0054	R	addr_reg15	[7:0]	Got pid_byte1
016	0058	R	addr_reg16	[7:0]	Got pid_byte0
017	005C	R	addr_reg17	[7:0]	Got bcr
018	0060	R	addr_reg18	[7:0]	Got dcr
019	0064	R	addr_reg19	[7:0]	Got mwl_msb
01A	0068	R	addr_reg1a	[7:0]	Got mwl_lsb
01B	006C	R	addr_reg1b	[7:0]	Got mrl_msb
01C	0070	R	addr_reg1c	[7:0]	Got mrl_lsb
01D	0074	R	addr_reg1d	[7:0]	Got mrl_ibi_size
01E	0078	R	addr_reg1e	[7:0]	Got dynamic
01F	007C	R	addr_reg1f	[7:0]	Got status_msb
020	0080	R	addr_reg20	[7:0]	Got status_lsb
021	0084	R	addr_reg21	[7:0]	maxwr

LMMI offset HEX	APB/AHB Offset HEX	RW	Register (RTL name)	Used bits	Description
022	0088	R	addr_reg22	[7:0]	maxrd
023	008C	R	addr_reg23	[7:0]	maxrdturn
024	0090	RC	addr_reg24	[0]	IBI_request
025	0094	RC	addr_reg25	[0]	HJ_request
026	0098	R	addr_reg26	[7:0]	IBI_byte
027	009C	R	addr_reg27	[7:0]	Number of slaves detected on the I3C bus
028	00A0	R	addr_reg28	[7:0]	Got ibi_slave_addr
029	00A4	RW	addr_reg29	[7:0]	{6'd0, ssp_contorl_clear[0], cmd_done}
02A	00A8	RO	addr_reg2A	[0]	Slave's HDR Capability
02B	00AC	RO	addr_reg2B	[7:0]	Timing Control Supported Modes
02C	00B0	RO	addr_reg2C	[7:0]	Timing Control State Byte
02D	00B4	RO	addr_reg2D	[7:0]	Timing Control Frequency Byte
02E	00B8	RO	addr_reg2E	[7:0]	Timing Control Inaccuracy Byte
030	00C0	RW	addr_reg30	[7:0]	ENEC data byte to send
031	00C4	RW	addr_reg31	[7:0]	DISEC data byte to send
032	00C8	RW	addr_reg32	[7:0]	setmwl_msb
033	00CC	RW	addr_reg33	[7:0]	setmwl_lsb
034	00D0	RW	addr_reg34	[7:0]	setmrl_msb
035	00D4	RW	addr_reg35	[7:0]	setmrl_lsb
036	00D8	RW	addr_reg36	[7:0]	setmrl_ibi_size
037	00DC	RW	addr_reg37	[7:0]	Test mode byte
038	00E0	RW	addr_reg38	[7:0]	DA for SETDASA and SETNEWDA commands
040	0100	RW	intr_sta	[7:0]	LMMI interrupt status, if current master
041	0104	RW	intr_ena	[7:0]	LMMI interrupt enable, if current master
042	0108	W	intr_set	[7:0]	LMMI interrupt set, if current master
050-057	0140-015C	RW	DA_mem_N	[6:0]	Dynamic Addresses of the slaves on the bus
060	0180	RW	setxtime_db_o	[7:0]	Defining byte of SETXTIME
061	0184	RW	setxtime_data_o	[7:0]	Additional byte of SETXTIME
070-0FF	01C0-03FC	R	ssp_slave_info	[7:0]	List of slaves present on the bus
100	0400	RW	BCR	[7:0]	Write is for debugging only. Parameter BCR
101	0404	RW	DCR	[7:0]	Write is for debugging only. Parameter DCR
102	0408	RW	DA	[6:0]	Dynamic Address assigned by Master
103	040C	RW	HjMrIbi	[5:0]	LMMI / I3C bus controllable HJ and IBI enables
104	0410	RO	is_M	[0]	Device is current Master
107	041C	RO	mwl_msb	[7:0]	mwl[15:8]. Max value is 1024 (EBR)
108	0420	RO	mwl_lsb	[7:0]	mwl[7:0]
109	0424	RO	mrl_msb	[7:0]	mrl[15:8]. Max value is 1024 (EBR)
10A	0428	RO	mrl_lsb	[7:0]	mrl[7:0]
10B	042C	RW	mxds2_msb	[7:0]	two bytes of max data speed (GETMXDS). Write is for debugging only
10C	0430	RW	mxds2_lsb	[7:0]	parameter MAX_D_SPEED
10D	0434	RW	mtrt0	[7:0]	max turnaround time byte 0
10E	0438	RW	mtrt1	[7:0]	max turnaround time byte 1
10F	043C	RW	mtrt2	[7:0]	max turnaround time byte 2

LMMI offset HEX	APB/AHB Offset HEX	RW	Register (RTL name)	Used bits	Description
110	0440	RW	pid5	[7:0]	PID_MANUF[14:7].
111	0444	RW	pid4	[7:0]	{PID_MANUF[6:0], 1'b0}
112	0448	RW	pid3	[7:0]	PID_PART[15:8]
113	044C	RW	pid2	[7:0]	PID_PART[7:0]
114	0450	RW	pid1	[7:0]	{PID_INST, PID_ADD[11:8]}
115	0454	RW	pid0	[7:0]	PID_ADD[7:0]
116	0458	RW	SA	[6:0]	Static Address (hardwired in core but may be modified by LMMI) parameter STAT_ADDR
117	045C	RW	inaccuracy	[7:0]	Internal frequency oscillator inaccuracy in 0.1% increments
118	0460	R	odr_o	[7:0]	ODR value of the sensor received from I3C bus
119	0464	R	max_ibi_pl_o	[7:0]	Max IBI payload size received from I3C bus
120	0480	LMMI-R I3C-W	Read FIFO	[7:0]	I3C bus write to device. In HDR mode first LMMI read returns MSB, next - LSB
121	0484	RO	num_slvs_o	[3:0]	Number of slaves got from the latest DEFSLVS
122	0488	LMMI-W I3C-R	Write FIFO	[7:0]	Device read by I3C bus. In HDR mode first LMMI write is for MSB, next - LSB
124	0490	RW	hdr_wrcmd_code	[7:0]	HDR Write Command Code
125	0494	RW	hdr_rdcmd_code	[7:0]	HDR Read Command Code
126	0498	LMMI-RO	block_ibi	[0]	P2P SETDASA Configuration Indication
138	04E0	LMMI-RO	i3c_sts_sdr_msb	[7:0]	I3C status SDR [15:8]
139	04E4	LMMI-RO	i3c_sts_sdr_lsb	[7:0]	I3C status SDR [7:0]
13A	04E8	LMMI-RO	i3c_sts_hdr_msb	[7:0]	I3C status HDR [15:8]
13B	04EC	LMMI-RO	i3c_sts_hdr_lsb	[7:0]	I3C status HDR [7:0]
13C	04F0	LMMI-WO	rst_errors	NA	SDR/HDR status reset
13D	04F4	LMMI-WO	rst_ibiack	NA	IBI ACK flag reset
13E	04F8	LMMI-WO	rst_mrack	NA	Master Request ACK flag reset
1F0	07C0	RW	intr_status	[7:0]	Interrupt status register, if not current master
1F1	07C4	RW	intr_enable	[7:0]	Interrupt enable register, if not current master
1F2	07C8	W	intr_set	[7:0]	Interrupt set register, if not current master
1F3	07CC	R	FIFO status	[3:0]	FIFO Current State if not Current Master

2.4.1. Registers Bits Description

Each table below represents a register bit from the Table 2.7.

Table 2.8. Current Revision

Bits	Mode	Description
[7:0]	R	FW revision

Table 2.9. Start Command Strobe

Bits	Mode	Description
[0]	W	Write 1 to start the requested command. Write the necessary registers before. This register is cleared automatically on command execution done pule (0x029)

Table 2.10. CCC or Direct Command

Bits	Mode	Description
[7:0]	RW	I3C CCC or Direct command code to execute

Table 2.11. Slave Address

Bits	Mode	Description
[6:0]	RW	DA or SA (if DA is not assigned or the device is I^2C) address of the slave

Table 2.12. Transaction Length in Bytes

Bits	Mode	Description
[7:0]	RW	Transaction length in bytes. 0…255

Table 2.13. Write Buffer (FIFO)

Bits	Mode	Description
[7:0]	RW	Host to I3C FIFO (write FIFO)

Note: HDR-DDR command code (read or write) must be written into first location of Write FIFO before starting the HDR command.

Table 2.14. Read Buffer (FIFO)

Bits	Mode	Description
[7:0]	RW	I3C to Host FIFO (read FIFO)

Note: After IBI request processing first location in FIFO is the DA of the Slave, which requested the interrupt. The rest is the IBI payload.

Table 2.15. Command Execution Status

Bits	Mode	Description
[7]	R	If set indicates command execution completion.
[6:5]	R	RESERVED
[4:0]	R	0 - normal completion (numbers are decimal) 1 - slave NACK 2 - IBI event (slave initial start condition) 3 - address arbitration failed, IBI 4 - HJ event 5 - send data error 6 - Rx CCC message error 7 - Tx data error 8 - broadcast 7E NACK 9 - DDR slave NACK 10 - Rx DDR CRC error

Bits	Mode	Description
		11 - Rx DDR parity error 12 - Rx DDR data not enough 13 - address arbitration failed, SMR 14 - SMR event

Table 2.16. Combined Commands Mode

Bits	Mode	Description
[0]	RW	Combined commands mode. Set this bit if several commands must be executed without introducing a Stop

Table 2.17. Secondary Master Request Received

Bits	Mode	Description
[0]	RW	This bit is set if secondary master request has been received. Write 0 to clear this bit.

Table 2.18. Read Is Over

Bits	Mode	Description
[0]	RC	This bit is set if the ordered number of bytes has been received (read). Self- clearing on read

Table 2.19. Initial Start of Procedure

Bits	Mode	Description
[7:5]	RW	RESERVED
[4]	W	Enter idle direct. Force the management SM to go to IDLE state.
[3]	R	Must be written to 0
[2]	W	Issue DEFSLVS command
[1]	W	Reset DA assignment
[0]	W	Initiate start. Master issues ENTDAA.

Note: One-time executable after the reset. The SM is in INITIAL state at reset not IDLE. This register provides a choice to force one of the following procedures. If bit [0] is set, Master executes ENTDAA. If bit [4] is set, SM goes to IDLE state. Normally only bit [0] is used. After execution of the choice, the SM is in the IDLE state. Another scenario is to force IDLE state and issue ENTDAA ordered by CCC or any desired command, if applicable to not initialized I3C bus.

Table 2.20. Management State

Bits	Mode	Description
[7:5]	R	RESERVED
[4:0]	R	Binary coded management SM state (for debugging). In reality the SM is one-hot

Table 2.21. Coded subset of the command execution status

Bits	Mode	Description
[7:0]	RC	Coded subset of the command execution status (hex) 81 - normal completion 82 - slave NACK 83 - IBI event (slave initial start condition) 84 - address arbitration failed, IBI 85 - HJ event 86 - send data error (HJ) 87 - illegal CCC detected 88 - Tx data error 89 - broadcast 7E NACK 8A - DDR slave NACK 8B - Rx DDR CRC error 8C - Rx DDR parity error 8D - Rx DDR data not enough 8E - address arbitration failed, SMR 8F - SMR event

Table 2.22. Test Register

Bits	Mode	Description
[7:0]	RW	For neutral RW checking

Table 2.23. PID Byte 5 … PID Byte 0

Bits	Mode	Description
[7:0]	R	PID byte 5 (4, 3, 2, 1, 0) of the accessed slave device

Table 2.24. BCR of the accessed slave device

Bits	Mode	Description
[7:0]	R	BCR of the accessed slave device

Table 2.25. DCR of the accessed slave device

Bits	Mode	Description
[7:0]	R	DCR of the accessed slave device

Table 2.26. Maximum Write Length MSB

Bits	Mode	Description
[7:0]	R	MWL MSB of the accessed slave device

Table 2.27. Maximum Write Length LSB

Bits	Mode	Description
[7:0]	R	MWL LSB of the accessed slave device

Table 2.28. Maximum Read Length MSB

Bits	Mode	Description
[7:0]	R	MRL MSB of the accessed slave device

Table 2.29. Maximum Read Length LSB

Bits	Mode	Description
[7:0]	R	MRL LSB of the accessed slave device

Table 2.30. IBI Size Received with Maximum Read Length

Bits	Mode	Description
[7:0]	R	MRL third byte – IBI size, if IBI payload is supported

Table 2.31. Slave Dynamic Address

Bits	Mode	Description
[7:0]	R	Dynamic address of the slave, if transaction assumes receiving of the DA from the slave

Table 2.32. Slave Status MSB

Bits	Mode	Description
[7:0]	R	Slave status word, MSB

Table 2.33. Slave Status LSB

Bits	Mode	Description
[7:0]	R	Slave status word, LSB

Since maxwr/maxread/maxrdturn are not supported, the following three registers are for information only.

Table 2.34. Max Write Speed

Bits	Mode	Description
[7:0]	R	Max write speed got from the target slave (informative)

Table 2.35. Max Read Speed

Bits	Mode	Description
[7:0]	R	Max read speed got from the target slave (informative)

Table 2.36. Max Turnaround Time

Bits	Mode	Description
[7:0]	R	Max Turnaround time got from the target slave (informative)

Table 2.37. IBI Request Detected

Bits	Mode	Description
[7:1]	R	RESERVED
[0]	R	IBI request has been detected and processed (must be enabled by ENEC and from the slave's Host side)

Table 2.38. HJ Request Detected

Bits	Mode	Description
[7:1]	R	RESERVED
[0]	R	HJ request has been detected and processed (must be enabled by ENEC and from the slave's Host side)

Table 2.39. Received IBI Byte

Bits	Mode	Description
[7:0]	R	Received IBI mandatory byte

Table 2.40. Number of Detected Slaves

Bits	Mode	Description
[7:0]	R	Number of slaves detected on the bus

Table 2.41. IBI Slave Address

Bits	Mode	Description
[7:0]	R	DA of the winning slave during IBI address arbitration

Table 2.42. Command Done Flag

Bits	Mode	Description
[7:2]	R	RESERVED
[1]	R	Management response pulse
[0]	R	Management response extended by one clock cycle

Note: Debug information; internal status readback.

Table 2.43. Slave's HDR Capability

Bits	Mode	Description
[7:1]	R	RESERVED
0	R	Selected Slave's HDR capability

Table 2.44. Timing Control Supported Modes

Bits	Mode	Description
[7:5]	R	RESERVED
4	R	Async Mode 3
3	R	Async Mode 2
2	R	Async Mode 1
1	R	Async Mode 0
0	R	Sync Mode

Note: Master and Secondary Master support only Async Mode 0.

Table 2.45. Timing Control State Byte

Bits	Mode	Description
7	R	Overflow
[6:5]	R	RESERVED
4	R	Async Mode 3 enabled
3	R	Async Mode 2 enabled
2	R	Async Mode 1 enabled
1	R	Async Mode 0 enabled
0	R	Sync Mode enabled

Table 2.46. Timing Control Frequency Byte

Bits	Mode	Description
[7:0]	R	Frequency Byte: This byte represents the Slave's internal oscillator frequency in increments of 0.5 megahertz (500 KHz), up to 127.5 MHz

Table 2.47. Timing Control Inaccuracy Byte

Bits	Mode	Description
[7:0]	R	This byte represents the maximum variation of the Slave's internal oscillator in 1/10th percent (0.1%) increments, up to 25.5%

Table 2.48. ENEC Event Data Byte to Send

Bits	Mode	Description
[7:4]	R	RESERVED
[3]	RW	ENHJ - enable HJ
[2]	R	RESERVED
[1]	RW	ENMR - enable master request
[0]	RW	ENINT - enable IBI

Table 2.49. DISEC Event Data Byte to Send

Bits	Mode	Description
[7:4]	R	RESERVED
[3]	RW	DISHJ - disable HJ
[2]	R	RESERVED
[1]	RW	DISMR - disable master request
[0]	RW	DISINT - disable IBI

Table 2.50. SETMWL MSB

Bits	Mode	Description
[7:0]	RW	Data MSB of SETMWL command

Table 2.51. SETMWL LSB

Bits	Mode	Description
[7:0]	RW	Data LSB of SETMWL command

Table 2.52. SETMRL MSB

Bits	Mode	Description
[7:0]	RW	Data MSB of SETMRL command

Table 2.53. SETMRL LSB

Bits	Mode	Description
[7:0]	RW	Data LSB of SETMRL command

Table 2.54. SETMRL IBI Size

Bits	Mode	Description
[7:0]	RW	IBI size of SETMRL command, if payload is supported by Slave

Table 2.55. ENTTM Mode byte

Bits	Mode	Description
[7:0]	RW	Mode byte for ENTTM command. *ENTTM is not supported in current release of the I3C Slave IP*

Table 2.56. DA for SETDASA and SETNEWDA commands

Bits	Mode	Description
[7:0]	RW	DA for SETDASA and SETNEWDA commands

The three registers below serve the LMMI interrupt functionality. Interrupts are event edge triggered.

If 1 is written into the corresponding bit of Status register, bit is cleared.

Interrupt Set register is self-clearing, that is, 1 written to a bit is cleared at the next clock cycle. This register allows host to set the desired interrupt.

Table 2.57. LMMI Interrupt Status if Current Master

Bits	Mode	Description
[7]	RW	Latched command completion flag
[6]	RW	Latched HJ request (Master got HJ interrupt)
[5]	RW	Latched SM request (Master got SMR interrupt)
[4]	RW	Latched IBI request (Master got IBI)
[3:0]	RW	RESERVED

Table 2.58. LMMI Interrupt Enable if Current Master

Bits	Mode	Description
[7]	RW	Enable command completion interrupt
[6]	RW	Enable HJ event interrupt
[5]	RW	Enable SMR event interrupt
[4]	RW	Enable IBI to the Host event interrupt
[3:0]	RW	RESERVED

Table 2.59. LMMI Interrupt Set if Current Master

Bits	Mode	Description
[7]	W	Set command completion interrupt
[6]	W	Set HJ interrupt
[5]	W	Set SMR interrupt
[4]	W	Set IBI
[3:0]	W	RESERVED

Table 2.60. SETXTIME Supported Defining Bytes

Bits	Mode	Description
[7:0]	RW	DF - Set Async 0 mode (only this mode is supported) Each DF command toggles the Async 0 mode ON and OFF for debugging, regardless of directed or broadcast transaction type
[7:0]	RW	8F – ODR. ODR value must be written into 0x61 below

Table 2.61. SETXTIME Additional Data Byte

Bits	Mode	Description
[7:0]	RW	If Defining Byte is ODR (0x8F), represents the ODR value in KSPS

GETXTIME returns the data in the read FIFO (0x006) in the following order:

- Supported modes (only 0x02)
- Current State
- Internal frequency in 0.5MHz increments
- Frequency inaccuracy in 0.1% increments

Table 2.62. List of Slaves.

Addr	Description
070	PID 5
071	PID 4
072	PID 3
073	PID 2
074	PID 1
075	PID 0
076	BCR
077	DCR
078	DA
079	RESERVED
07A	RESERVED

Note: 11 Bytes per Slave (from 0x070 to 0x0FF).

2.4.2. Secondary Master Related Registers

Table 2.63. ODR Value

Bits	Mode	Description
[7:0]	R	ODR value of the sensor received from I3C bus

Table 2.64. Max IBI Payload Size

Bits	Mode	Description
[7:0]	R	Max IBI payload size. Limitation received from I3C bus

Table 2.65. Number of Slaves captured from DEFSLVS

Bits	Mode	Description
[7:4]	R	RESERVED
[3:0]	R	Number of slave devices on I3C bus returned by latest DEFSLVS command

Table 2.66. Regaining Bus Ownership Request

Bits	Mode	Description
[7:1]	R	RESERVED
[0]	R/W	Regaining Bus Ownership Request

Table 2.67. HDR Write Command Code

Bits	Mode	Description
[7:0]	R/W	HDR Write Command Code of the Secondary Master in Slave mode. Defaults to 0x20

Table 2.68. HDR Read Command Code

Bits	Mode	Description
[7:0]	R/W	HDR Read Command Code of the Secondary Master in Slave mode. Defaults to 0xA0

Table 2.69. P2P SETDASA Configuration Indication

Bits	Mode	Description
[7:1]	R	RESERVED
[0]	R/W	Indicates IBI Blocking

Note: Peer-to-Peer configuration for DA == 0x01.

Table 2.70. Error Status for SDR when Master is Not Current Master

{0x138, 0x139}

Bits	Description
0x0001	T-bit error
0x0002	DA parity error
0x0004	abnormal command termination with stop
0x0008	IBI read data master abort
0x0010	early data devastation (IBI)
0x0020	directed read master abort

Table 2.71. Error Status for HDR when Master is Not Current Master

Bits	Description
0x0001	wrong preamble in cmd phase
0x0002	unsupported cmd
0x0004	cmd+DA parity error
0x0008	preamble bit1 is not 1
0x0010	master abort HDR during read
0x0020	data transfer limit is hit
0x0040	first write preamble error (must be 10)
0x0080	wrong preamble during write (00 or 10)
0x0100	write FIFO is full
0x0200	CRC_W error

Note: {0x13A, 0x13B}

Three registers below serve the LMMI interrupt functionality. Interrupts are event edge triggered.

If 1 is written into the corresponding bit of Status register, bit is cleared.

Interrupt Set register is self-clearing, that is, 1 written to a bit is cleared at the next clock cycle. This register allows host to set the desired interrupt.

Table 2.72. LMMI Interrupt Status if not Current Master

Bits	Mode	Description
[7]	RW	Latched HJ event request (Slave, if Secondary Master is not current master, has generated HJ request)
[6]	RW	Latched SMR event request
[5]	RW	Latched IBI event request
[4]	RW	Latched HJ acknowledge
[3]	RW	Latched SMR acknowledge
[2]	RW	Latched IBI acknowledge
[1]	RW	Latched Read FIFO is not empty event (I3C to host)
[0]	RW	Latched Write FIFO is full event

Table 2.73. LMMI Interrupt Enable if not Current Master

Bits	Mode	Description
[7]	RW	Enable HJ event interrupt
[6]	RW	Enable SMR event interrupt
[5]	RW	Enable IBI to the Host event interrupt
[4]	RW	Enable HJ acknowledge interrupt
[3]	RW	Enable SMR acknowledge interrupt
[2]	RW	Enable IBI acknowledge interrupt
[1]	RW	Enable Read FIFO is not empty interrupt
[0]	RW	Enable Write FIFO is full interrupt

Table 2.74. LMMI Interrupt Set if not Current Master

Bits	Mode	Description
[7]	W	Set HJ event interrupt
[6]	W	Set SMR event interrupt
[5]	W	Set IBI event interrupt
[4]	W	Set HJ acknowledge interrupt
[3]	W	Set SMR acknowledge interrupt
[2]	W	Set IBI acknowledge interrupt
[1]	W	Set Read FIFO is not empty interrupt
[0]	W	Set Write FIFO is full interrupt

Table 2.75. FIFO Current State if not Current Master

Bits	Mode	Description
[7:4]	R	RESERVED
[3]	R	Read FIFO is almost empty
[2]	R	Read FIFO is empty
[1]	R	Write FIFO is almost full
[0]	R	Write FIFO is full

2.5. Programming Flow

Figure 2.4 illustrates I3C Master key transmission modes.

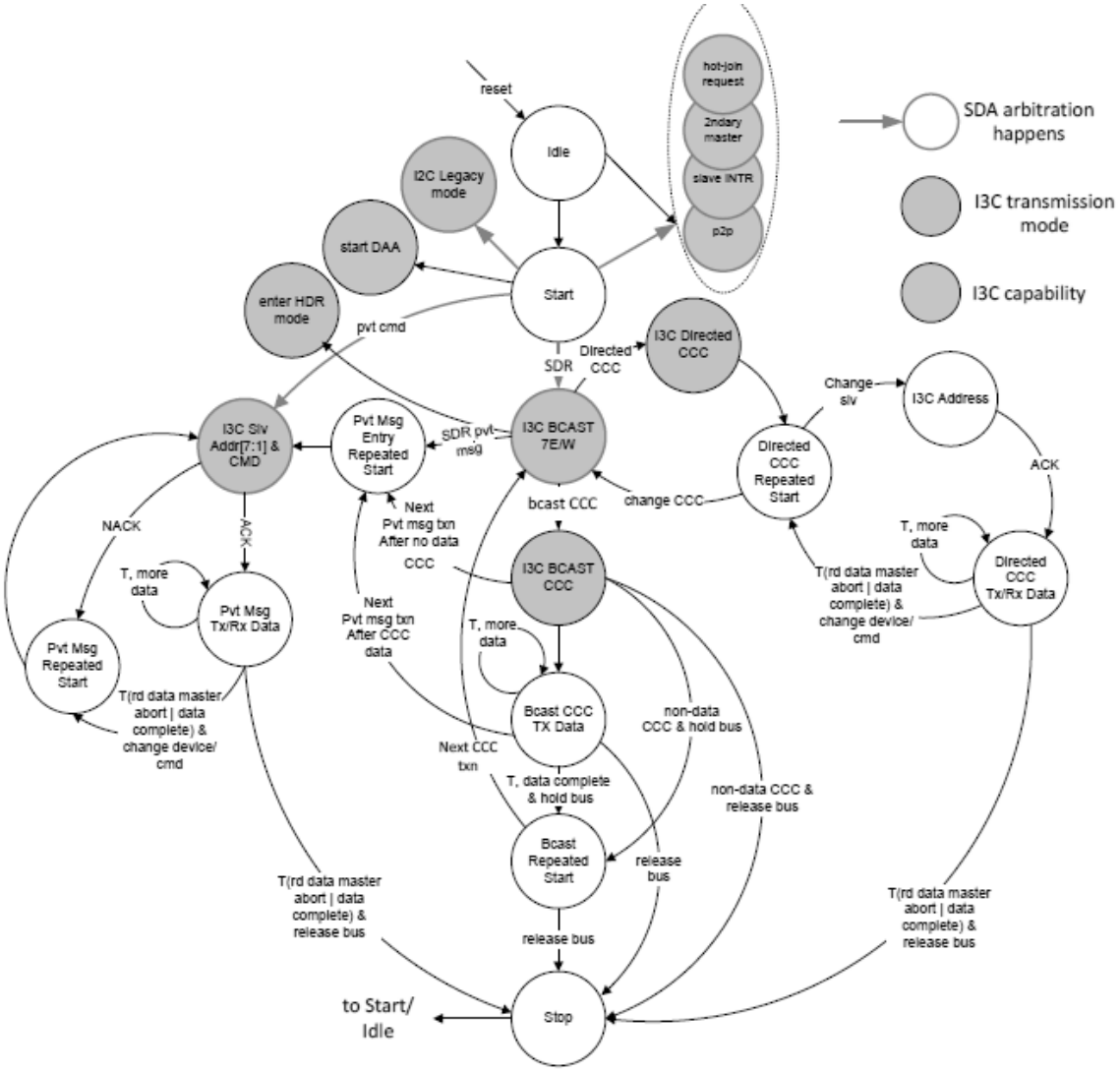

Figure 2.4. I3C Main Master Key Transmission Modes

Table 2.76. State Control and Special Commands

mgmt_cmd_reg Value	Command name	Description
E0	FORCE_STOP	Force STOP condition
E1	FORCE_HDREXIT_STOP	Force HDR-Exit pattern generation
E2	I2C_WR	I^2C write with static address
E3	I2C_RD	I^2C read with static address
E4	I2C_7EWR	I^2C write with 7E and static address
E5	I2C_7ERD	I^2C read with 7E and static address
E6	PRVT_WR	Private write with dynamic address
E7	PRVT_RD	Private read with dynamic address
E8	PRVT_7EWR	Private write with 7E and dynamic address
E9	PRVT_7ERD	Private read with 7E and dynamic address

2.6. Transaction Control

The I3C command code written in *mgmt_cmd_reg* register (0x002), the slave address written in *slv_address* register (0x003) and the transaction length in bytes written in *trans_length* register (0x004) are translated into I3C bus sequence after writing 1 into *exec_strobe[0]* - command strobe register (0x001). The transaction result (status) must be read from the *mngmt_cmd_stat* register (0x00E) before issuing any other command. Table 2.77 describes all possible statuses.

Table 2.77. Transaction Control Status

Status [7:0]	Description
0x14	SMR flag w addr arbitration
0x13	SMR flag on bus free
0x12	RX DDR data not enough
0x11	RX DDR parity error
0x10	RX DDR CRC error
0x09	DDR Slave NACK
0x08	7E NACK error flag
0x07	TX data error flag
0x06	RX CCC error flag
0x05	HJ flag
0x03	IBI flag w addr arbitration
0x02	IBI flag on bus free
0x01	All other NACKs
0x00	No errors

Bit [7] of mngmt_cmd_stat register, if set, shows the command completion. Writing new strobe or reading this register clears it. Alternatively, the LMMI interrupt enable bit[7] allows the interrupt on command completion to the Host to be generated. It must be cleared by writing 0 to the bit [7] before issuing the next command.

In case of HDR-DDR transaction, the 0x20 CCC is written into the mgmt_cmd_reg register and the HDR command is written into the wr_buffer address (transmit FIFO – 0x005). If the command is a write command the bytes of data must be written into the same buffer just after the HDR command.

All statuses generated by the Slave component of I3C Master are presented in Table 2.70 and Table 2.71.

2.7. Combined Transactions

Transaction is supposed to end with STOP condition. If more than one transaction is necessary to send before issuing the STOP, the *combined[0]* bit must be set (0x008). This allows you to write a new set of the control registers before completion of the sequence with STOP. Each command in the combined sequence must be issued (strobe register is written) after previous command completion, which may be checked:

(a) by reading back the command execution status register *mngmt_cmd_stat*,

(b) waiting for calculated I3C bus transaction time for the current command, or

(c) enabling the LMMI interrupt [7] (0x041). During waiting for the next command in the sequence the master stalls the SCL (parks low).

Combined HDR commands are ended with HDR-Restart pattern after SCL going active, to allow back to back transactions. The last command in the sequence ends with HDR-Exit pattern. Before issuing the last strobe *combined[0]* bit must be cleared to allow HDR-Exit pattern generation.

Since any new command clears the receive buffer pointers, the content of read buffer must be read before issuing new command (the host has ordered the number of bytes to read – 0x004).

2.8. Transaction Termination

To terminate the command execution the following means are implemented (see Table 2.76).

- Force TX Stop (FORCE_STOP) - forces a stop condition on the bus, terminating any TX transaction.
- Force TXHDR-Exit pattern generation (FORCE_HDREXIT_STOP).

2.9. ENEC, DISEC, SETMWL, SETMRL Commands

These commands are executed using the following scheme. Before executing the command, the value to be set is written into the *enec_event*, *disec_event*, *mwl_msb_val*, *mwl_lsb_val*, *mrl_msb_val*, *mrl_lsb_val*, or *mrl_ibi_size* registers. The data format is described in *mipi_I3C_specification_v1-0.pdf*. The corresponding command code must be written into *mgmt_cmd_reg* register, the slave address - into the *slv_address* register and the transaction length in bytes - into the *trans_length* register. Writing 1 into *exec_strobe[0]* - command strobe register starts the transaction.

2.10. IBI and Hot Join Request Results

When IBI or HJ event is enabled by ENEC command (*enec_event*) and the Master has detected the event, the following registers are filled in with the IBI/HJ relevant data.

ibi_req (0x024) – Bit [0] is set, if the IBI event has been detected. After the interrupt processing, if enabled, the host must write 0 to this register to arm the next interrupt detection, if any.

ibi_byte (0x026) – Assuming a single byte IBI payload is captured in this register, if the IBI event has been detected.

If the IBI payload is more than zero, the rest of the bytes except of the mandatory byte, which is stored in *ibi_byte*, are in the receive FIFO.

ht_req (0x025) – Bit [0] is set, if the Hot Join event has been detected. After the interrupt processing, if enabled, the host must write 0 to this register to arm the next request detection, if any.

ibi_slave_addr (0x028) – Bits [7:1] contain the slave address, which has generated the interrupt/request.

If the corresponding LMMI interrupt is enabled, the host is informed of the IBI or HJ request.

2.10.1. Macro Commands

The rest of the commands described in Table 2.76 are designed to facilitate the I^2C access and Private access involving the static or dynamic address of the target device or devices in case of the broadcast writes.

The Static or dynamic address must be written into *slv_address* register before starting the transaction.

Before issuing the Write commands make sure the necessary number of bytes are written into the transmit buffer.

Since any new command clears the receive buffer pointers, the content of read buffer must be read before issuing new command.

2.10.2. List of Slaves Found on the I3C Bus

The list of slaves with the corresponding parameters obtained during the ENTDAA execution is available starting from the 0x070 offset. The border line of the memory is 0x0FF, that is, only 8 slave support.

3. IP Generation and Evaluation

This section provides information on how to generate the I3C Master IP Core using the Lattice Radiant software and how to run simulation and synthesis. For more details on the Lattice Radiant software, refer to the Lattice Radiant Software 2.1 User Guide.

3.1. Licensing the IP

An IP core-specific license string is required enable full use of the I3C Master IP Core in a complete, top-level design. When the IP Core is used in LIFCL or LFD2NX devices, you can fully evaluate the IP core through functional simulation and implementation (synthesis, map, place and route) without an IP license string. This IP core supports Lattice's IP hardware evaluation capability, which makes it possible to create versions of the IP core, which operate in hardware for a limited time (approximately four hours) without requiring an IP license string. See Hardware Evaluation section for further details. However, a license string is required to enable timing simulation and to generate bitstream file that does not include the hardware evaluation timeout limitation.

3.2. Generation and Synthesis

Lattice Radiant software allows you to generate and customize modules and IPs and integrate them into the device architecture.

To generate the I3C Master IP Core:

1. In the **Module/IP Block Wizard** create a new Lattice Radiant software project for I3C Master module.
2. In the dialog box, configure the I3C Master module according to custom specifications, using drop-down menus and check boxes. As a sample configuration, see Figure 3.1. For configuration options, see Table 2.5

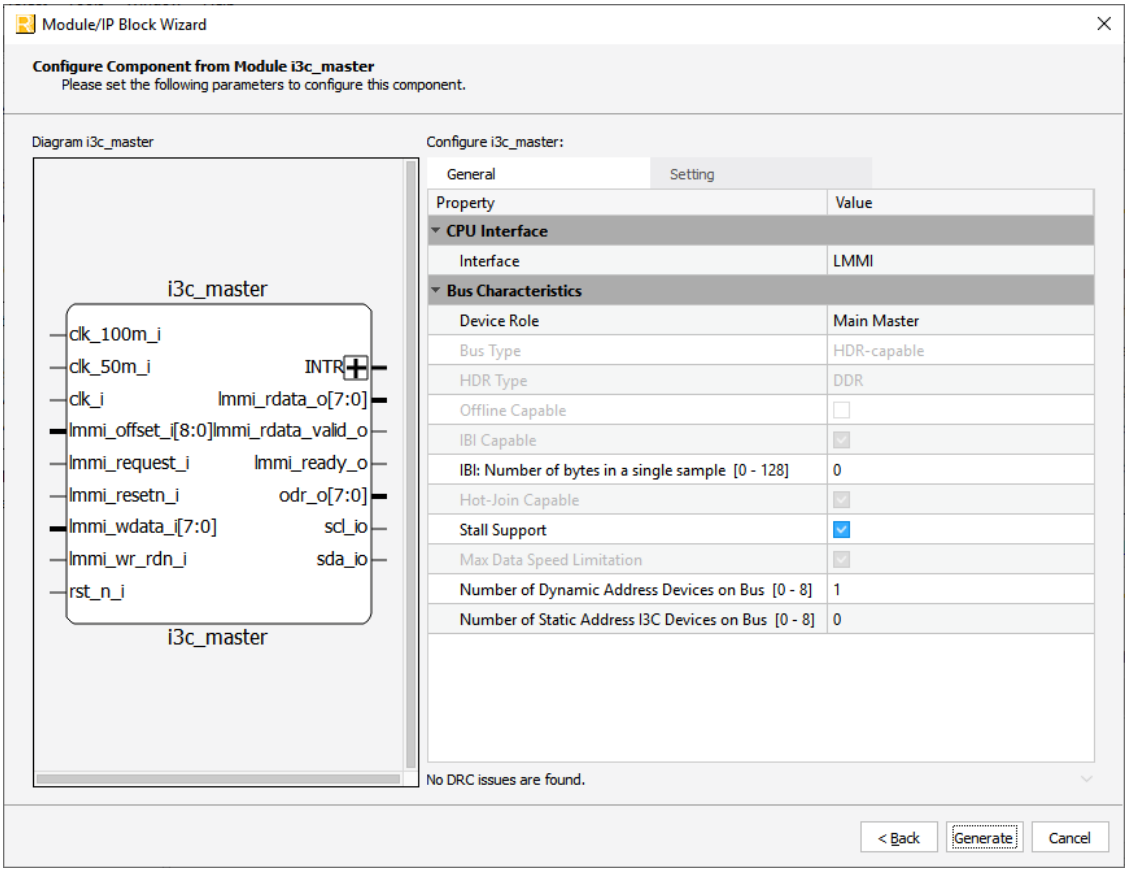

Figure 3.1. Configure Block of I3C Master Module

3. Click **Generate**. The **Check Generating Result** dialog box opens, showing design block messages and results, as shown in Figure 3.2.

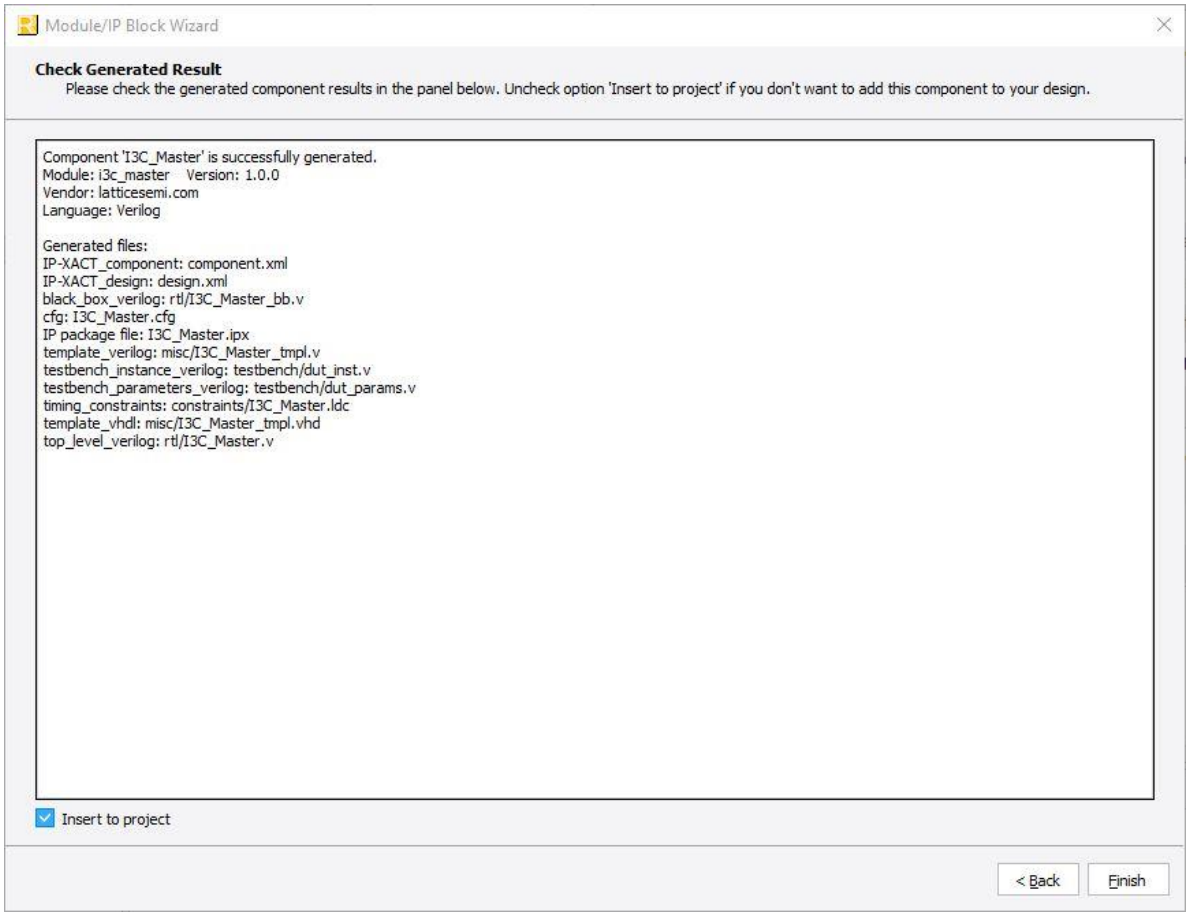

Figure 3.2. Check Generating Results Window

4. Click the **Finish** button to generate the Verilog file.

The generated I3C Master IP Core package includes the black box (<Instance Name>_bb.v) and instance templates (<Instance Name>_tmpl.v/vhd) that can be used to instantiate the core in a top-level design. An example RTL top-level reference source file (<Instance Name>.v) that can be used as an instantiation template for the IP core is also provided. You may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in Table 3.1.

Table 3.1. Generated File List

Attribute	Description
<Instance Name>.ipx	This file contains the information on the files associated to the generated IP.
<Instance Name>.cfg	This file contains the parameter values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Instance Name>.v	This file provides an example RTL top file that instantiates the IP core.
rtl/<Instance Name>_bb.v	This file provides the synthesis black box.
misc/<Instance Name>_tmpl.v misc /<Instance Name>_tmpl.vhd	These files provide instance templates for the IP core.

5. Upon generating desired design, you can synthesize it by clicking **Synthesize Design** located in the top left corner of the screen, as shown in Figure 3.3.

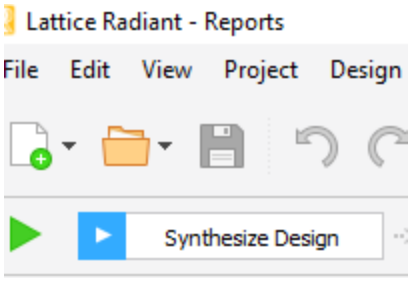

Figure 3.3. Synthesizing Design

3.3. Running Functional Simulation

To run Verilog simulation:

1. Click the  button located on the **Toolbar** to initiate the **Simulation Wizard** shown in Figure 3.4.

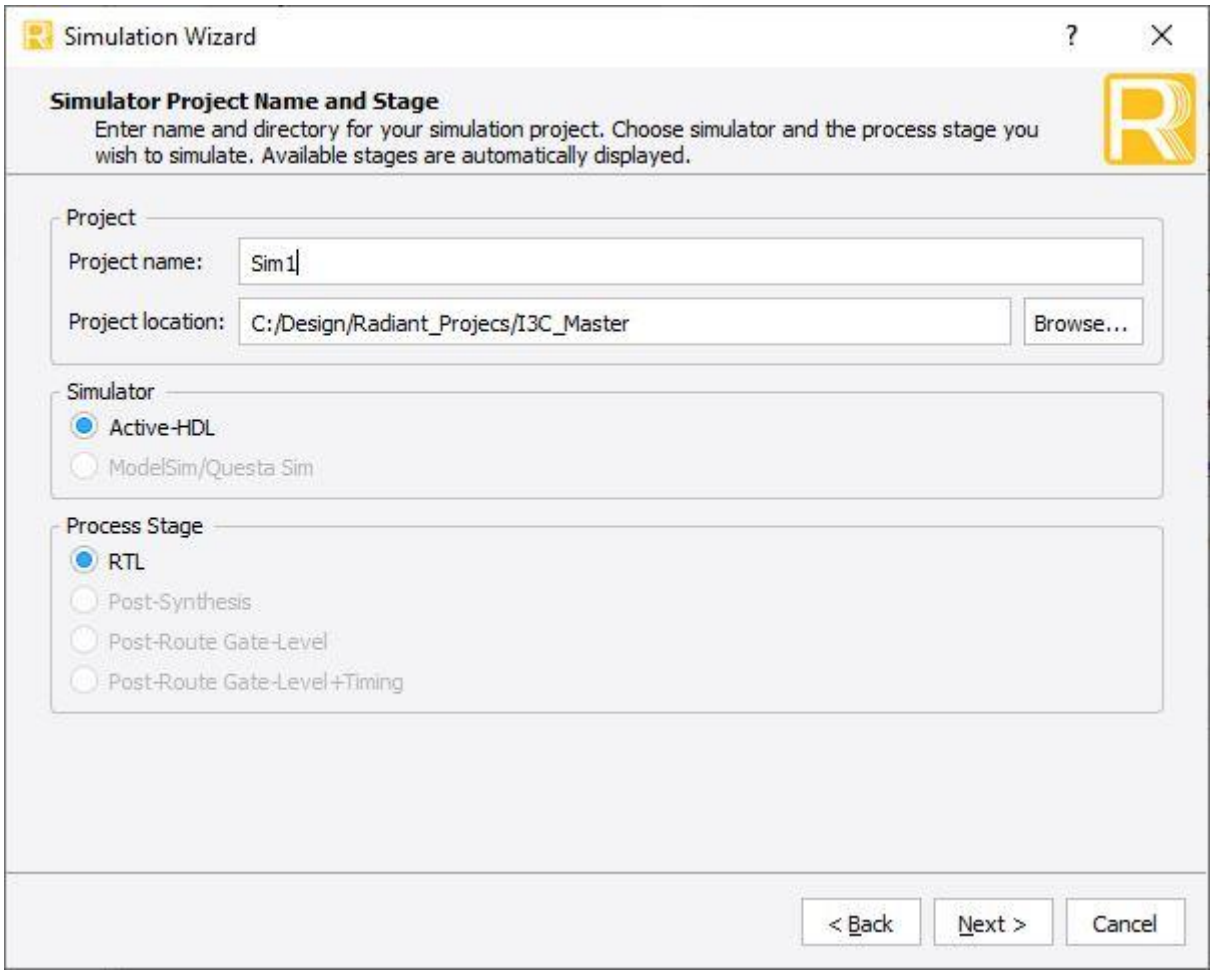

Figure 3.4. Simulation Wizard

2. Click **Next** twice to open the **Add and Reorder Source** window as shown Figure 3.5.

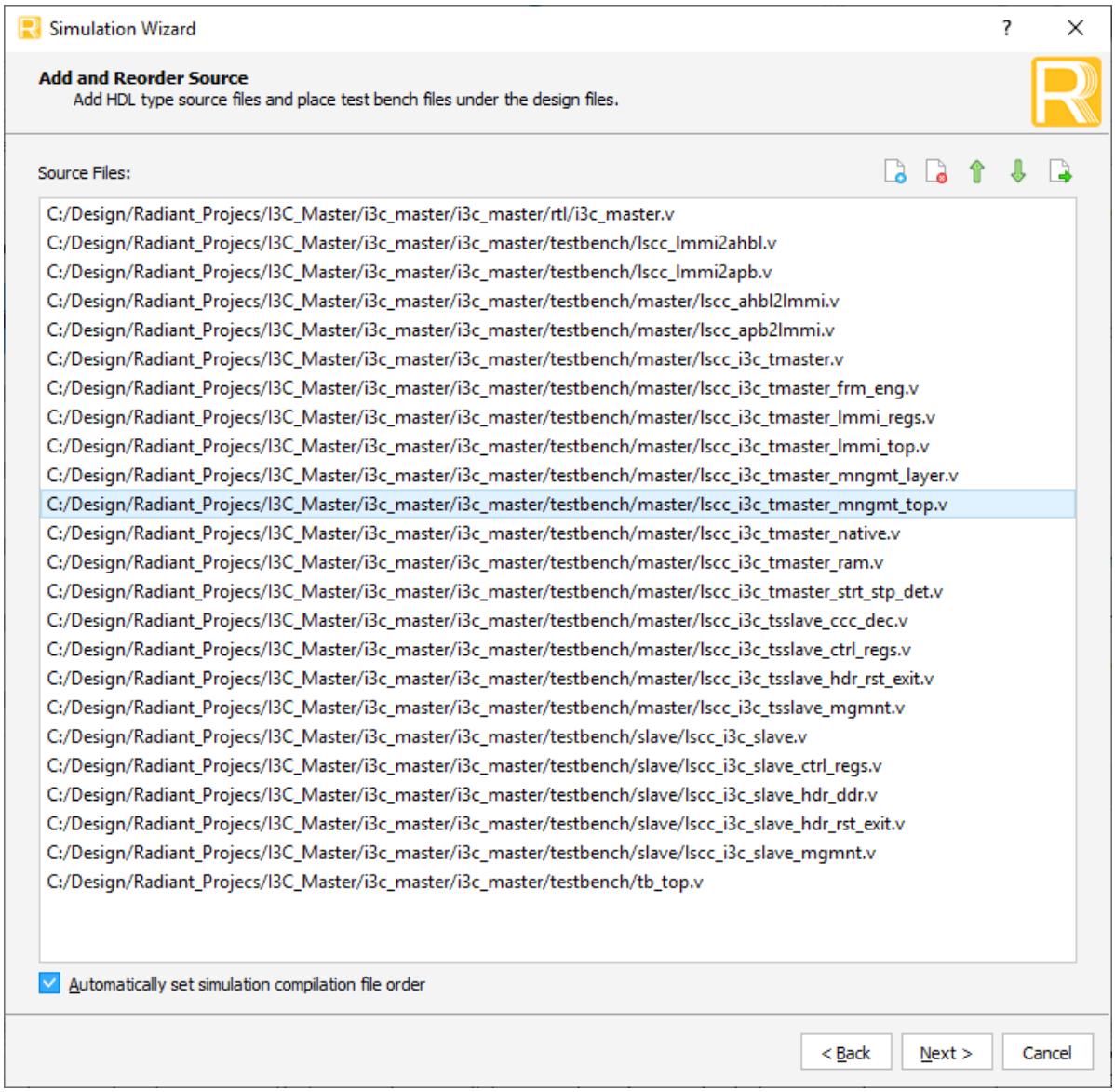

Figure 3.5. Adding and Reordering Source

3. Delete all files except tb_top.v and generated core file (i3c_master.v in our example.)
4. Click **Next** and **Finish** to run simulation.

Figure 3.6, Figure 3.7, and Figure 3.8 show the sample simulation diagrams.

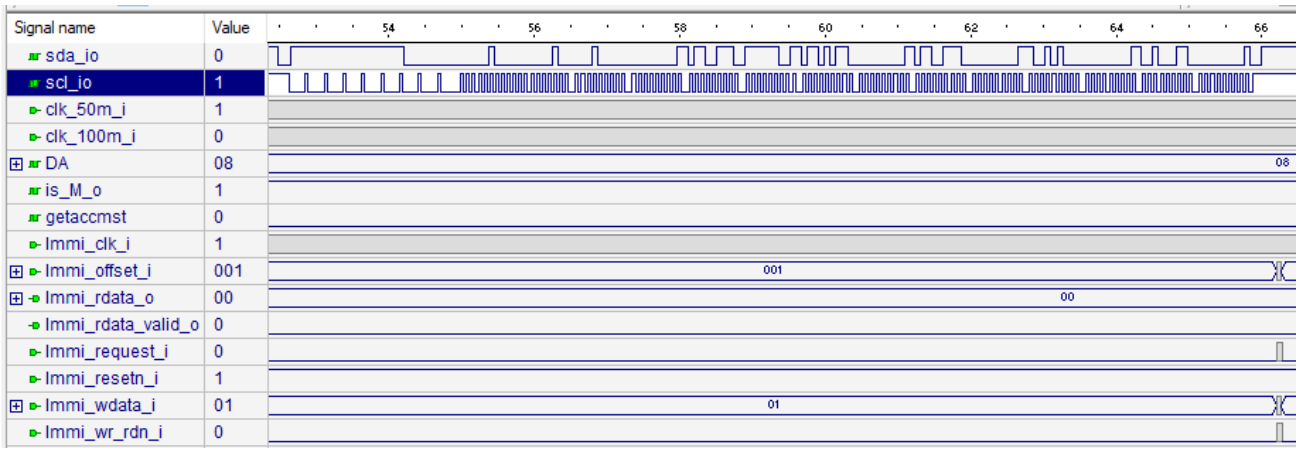

Figure 3.6. Dynamic Address Assignment

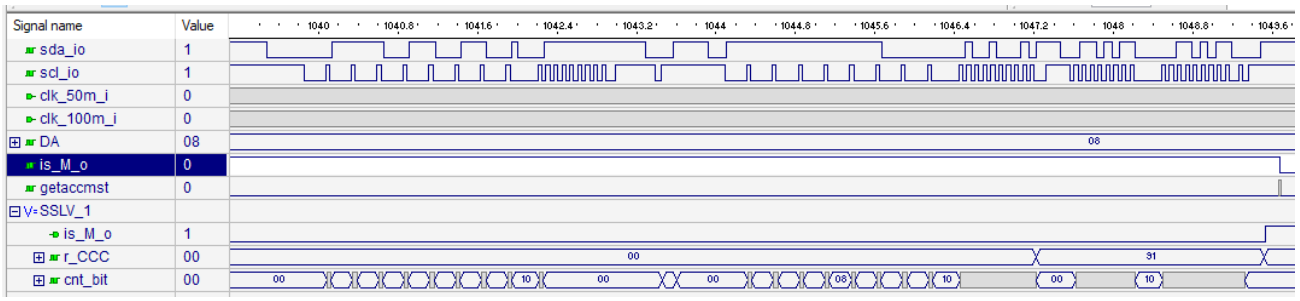

Figure 3.7. Master Request from Secondary Master

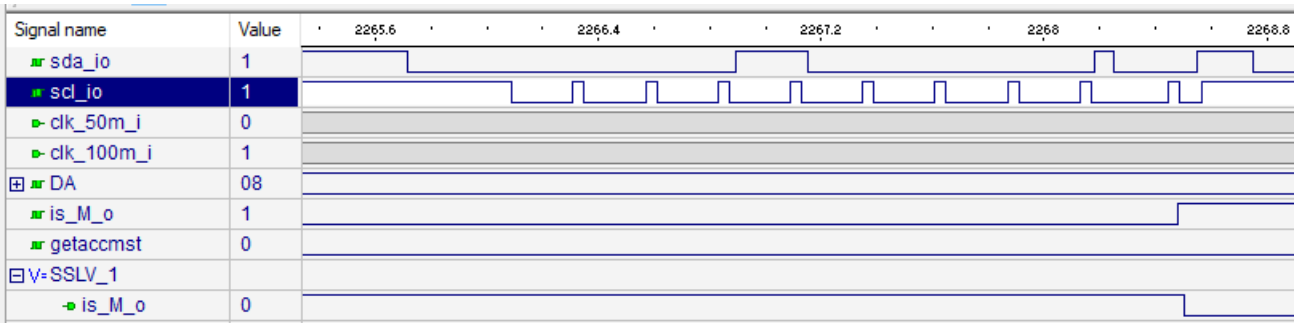

Figure 3.8. Main Master Regains Mastership

3.4. Hardware Evaluation

The I3C Master IP Core supports Lattice's IP hardware evaluation capability when used with LIFCL and LFD2NX devices. This makes it possible to create versions of the IP core that operate in hardware for a limited period of time (approximately four hours) without requiring the purchase of an IP license. It may also be used to evaluate the core in hardware in user-defined designs. The hardware evaluation capability may be enabled/disabled in the Strategy dialog box. It is enabled by default. To change this setting, go to Project > Active Strategy > LSE/Synplify Pro Settings.

4. Ordering Part Number

The Ordering Part Number (OPN) for I3C Master IP Core targeting CrossLink-NX FPGA devices are the following:

- I3C-M-CNX-U – I3C Master for CrossLink-NX – Single Design License
- I3C-M-CNX-UT – I3C Master for CrossLink-NX – Site License
- I3C-M-CTNX-U – I3C Master for Certus-NX – Single Design License
- I3C-M-CTNX-UT – I3C Master for Certus-NX – Site License

Appendix A. Resource Utilization

Table A.1 show configuration and resource utilization for LIFCL-40-9BG400I using Synplify Pro of Lattice Radiant Software 2.1.

Table A.1. Resource Utilization

Configuration	Clk Fmax (MHz)*	Slice Registers	LUTs	EBRs
Default	200	2251	7233	6
Interface = APB, Device Role = Secondary Master, Others = Default	172.891	2233	7745	6
Interface = AHBL, IBI:Number of bytes in a single sample [0-128] = 128, Number of Dynamic Address Devices on Bus [0 – 8] = 4, Others = Default	185.494	2290	7669	6

***Note:** Fmax is generated when the FPGA design only contains I^3C Slave IP Core and the target Frequency is 100 MHz. These values may be reduced when user logic is added to the FPGA design.

References

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow and Tasks, as well as on the Simulation Flow, see the Lattice Radiant Software 2.1 User Guide.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.2, June 2020

Section	Change Summary
Introduction	Updated Table 1.1 to add Certus-NX as supported FPGA family and LFD2NX-40 as targeted device.
Functional Description	Updated Table 2.5.
IP Core Generation, Simulation, and Validation	Updated section content.
Ordering Part Number	Updated this section.
Appendix A. Resource Utilization	Added this section.
References	Updated this section.

Revision 1.1, February 2020

Section	Change Summary
Introduction	Updated Table 1.1 to add LIFCL-17 as targeted device.

Revision 1.0, December 2019

Section	Change Summary
All	Initial release

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