19-1755; Rev 1; 3/01

EVALUATION KIT AVAILABLE

Wide Brightness Range CCFL Backlight Controllers

General Description

The MAX1739/MAX1839 fully integrated controllers are optimized to drive cold-cathode fluorescent lamps (CCFLs) using the industry-proven Royer oscillator inverter architecture. The Royer architecture provides near sinusoidal drive waveforms over the entire input range to maximize the life of CCFLs. The MAX1739/MAX1839 optimize this architecture to work over a wide input voltage range, achieve high efficiency, and maximize the dimming range.

The MAX1739/MAX1839 monitor and limit the transformer center-tap voltage when required. This ensures minimal voltage stress on the transformer, which increases the operating life of the transformer and eases its design requirements. These controllers also provide protection against many other fault conditions, including lamp-out and buck short faults.

These controllers achieve 50:1 dimming range by simultaneously adjusting lamp current and "chopping" the CCFL on and off using a digitally adjusted pulse-width modulated (DPWM) method. CCFL brightness is controlled by an analog voltage or is set with an SMBus™-compatible two-wire interface (MAX1739).

The MAX1739/MAX1839 drive an external high-side N-channel power MOSFET and two low-side N-channel power MOSFETs, all synchronized to the Royer oscillator. An internal 5.3V linear regulator powers the MOSFET drivers and most of the internal circuitry. The MAX1739/MAX1839 are available in space-saving 20-pin QSOP packages and operate over the -40°C to +85°C temperature range.

Applications

Notebook/Laptop Computers

Car Navigation Displays

LCD Monitors

Point-of-Sale Terminals

Portable Display Electronics

SMBus is a trademark of Intel Corp.

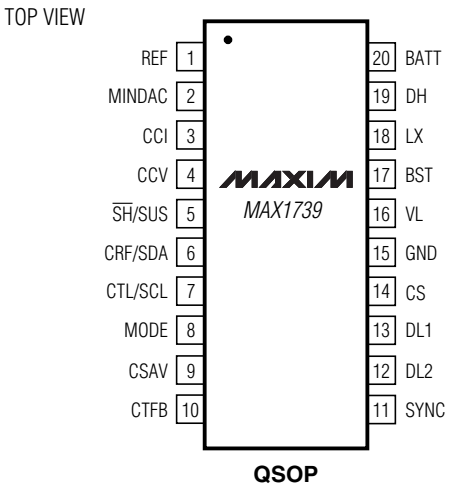
Features

- ♦ **Fast Response to Input Change**
- ♦ **Wide Input Voltage Range (4.6V to 28V)**
- ♦ **High Power-to-Light Efficiency**
- ♦ **Minimizes Transformer Voltage Stress**
- ♦ **Lamp-Out Protection with 2s Timeout**
- ♦ **Buck Switch Short and Other Single-Point Fault Protection**
- ♦ **Integrated Royer MOSFET Drivers Reduce Transformer Pin Count**
- ♦ **Buck Operation Synchronized to Royer Oscillator**
- ♦ **Synchronizable DPWM Frequency**
- ♦ **Pin-Selectable Brightness Control Interface**
- ♦ **SMBus Serial Interface (MAX1739)**
- ♦ **Analog Interface (MAX1739/MAX1839)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1739EEP	-40°C to +85°C	20 QSOP
MAX1839EEP	-40°C to +85°C	20 QSOP

Pin Configuration



QSOP

Pin Configurations continued at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Wide Brightness Range CCFL Backlight Controllers

ABSOLUTE MAXIMUM RATINGS

V_{BATT} to GND .....-0.3V to 30V
V_{BST}, V_{SYNC} to GND.....-0.3V to 34V
V_{BST} to V_{LX} .....-0.3V to 6V
V_{DH} to V_{LX}.....-0.3V to (V_{BST} + 0.3V)
V_{LX} to GND.....-6V to (V_{BST} + 0.3V)
VL to GND.....-0.3V to 6V
V_{CCV}, V_{CCI}, V_{REF}, V_{DL1}, V_{DL2} to GND .....-0.3V to (VL + 0.3V)
V_{MINDAC}, V_{CTFB}, V_{CSAV} to GND .....-0.3V to 6V
V_{CS} to GND.....-0.6V to (VL + 0.3V)
V_{MODE} to GND.....-6V to 12V
$V_{CRF/SDA}$, V_{CRF}, $V_{CTL/SCL}$, V_{CTL}, $V_{\overline{SH}/SUS}$,
$V_{\overline{SH}}$ to GND .....-0.3V to 6V
Continuous Power Dissipation (T_A = +70°C)
20-Pin QSOP (derate 9.1mW/°C above +70°C).....727mW
Operating Temperature .....-40°C to +85°C
Storage Temperature.....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 8.2V, $V_{\overline{SH}/SUS}$ = $V_{\overline{SH}}$ = 5.5V, MINDAC = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY AND REFERENCE						
V_{BATT} Input Voltage Range	V_L = V_{BATT}		4.6		5.5	V
	V_L = open		6		28	
V_{BATT} Quiescent Current, Operation with Full Duty Cycle on DH	DH = DL1 = DL2 = open	V_{BATT} = 28V		3.2	6	mA
		V_{BATT} = V_L = 5V		3.2	6	
V_{BATT} Quiescent Current, Shutdown	$\overline{SH}/SUS$ = $\overline{SH}$ = GND			6	20	µA
VL Output Voltage, Normal Operation	6V < V_{BATT} < 28V, 0 < I_{LOAD} < 15mA		5.0	5.35	5.5	V
VL Output Voltage, Shutdown	$\overline{SH}/SUS$ = $\overline{SH}$ = GND, no load		3.5	4.5	5.5	V
VL Undervoltage Lockout Threshold	VL rising (leaving lockout)				4.6	
	VL falling (entering lockout)		4.0			V
VL Undervoltage Lockout Hysteresis				300		mV
REF Output Voltage, Normal Operation	4.5V < VL < 5.5V, I_{REF} = 40µA		1.96	2.00	2.04	V
V_L POR Threshold			0.9		2.7	V
SWITCHING REGULATOR						
DH Driver On-Resistance					18	Ω
DL1, DL2 Driver On-Resistance					18	Ω
Minimum DH Switching Frequency	$1/t_{DH}$, SYNC = CS or GND, not synchronized		49	56	64	kHz
DH Minimum Off-Time			250	375	500	ns
DH Maximum Duty Cycle				98		%
SYNC Synchronization Range	Detect falling edges on SYNC		64		200	kHz
SYNC Input Current	0 < V_{SYNC} < 30V		-2		2	µA
SYNC Input Threshold	SYNC falling, referred to CS		400	500	600	mV
SYNC Input Hysteresis	Referred to the SYNC input threshold		50	100	150	mV
SYNC Threshold Crossing to DL1, DL2 Toggle Delay	V_{SYNC} = 0 to 5V, C_{DL_1} and C_{DL_2} < 100pF, 50% point on SYNC to 50% point on DL1 or DL2				120	ns
CS Overcurrent Threshold			408	450	492	mV

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 8.2V, $V_{\overline{SH}}$/SUS = $V_{\overline{SH}}$ = 5.5V, MINDAC = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DAC AND ERROR AMPLIFIER						
DAC Resolution	Guaranteed monotonic		5			Bits
MINDAC Input Voltage Range			0		2	V
MINDAC Input Bias Current	0 < V_{MINDAC} < 2V		-1		1	µA
MINDAC Digital PWM Disable Threshold	MINDAC = VL		2.4	2.9	4	V
CSAV Input Voltage Range			0		0.8	V
CSAV Regulation Point	V_{MINDAC} = 0, DAC code = 11111 binary		188	194	200	mV
	V_{MINDAC} = 0, DAC code = 00001 binary		2	6.25	16	
	V_{MINDAC} = 1V, DAC code = 00000 binary		93	100	110	
CSAV Input Bias Current			-1		1	µA
CSAV to CCI Transconductance	1V < V_{CCI} < 2.7V			100		µmho
CTFB Input Voltage Range			0		2	V
CTFB Input Bias Current			-1		1	µA
CTFB Regulation Point			570	600	630	mV
CTFB to CCV Transconductance	1V < V_{CCV} < 2.7V		30	40	50	µmho
TIMERS AND FAULT DETECTION						
Chopping Oscillator Frequency	No AC signal on MODE, not synchronized		24	28	32	kHz
Digital PWM Chop-Mode Frequency	No AC signal on MODE		205	220	235	Hz
	32kHz AC signal on MODE			250		
	100kHz AC signal on MODE			781		
MODE to DPWM Sync Ratio	F_{MODE} / F_{DPWM}			128		
Lamp-Out Detection Timeout Timer (Center-Tap Voltage Stuck at Maximum) (Note 1)	V_{CSAV} < CSAV lamp-out threshold	No AC signal on MODE	2.06	2.33	2.73	s
		32kHz AC signal on MODE		2.05		
		100kHz AC signal on MODE		0.66		
CSAV Lamp-Out Threshold			50	75	100	mV
Fault-Detection Threshold on CCV	(Note 2)		0.4		1	V
Shorted Buck-Switch Detection Timeout Timer (UL1950 Protection) (Note 3)	V_{CCV} < fault-detection threshold on CCV	No AC signal on MODE	332	291	259	ms
		32kHz AC signal on MODE		256		
		100kHz AC signal on MODE		82		
Lamp Turn-On Delay	After $\overline{SH}$/SUS or SH forces device on or $\overline{SH}$ rises			4		ms
MODE Operating Voltage Range			-5.5		11	V
MODE = GND Threshold (min Brightness = 0)	To sync DPWM oscillator, not in shutdown (Note 4)				0.6	V
MODE = REF Threshold (max Brightness = 0)	To sync DPWM oscillator, not in shutdown (Note 4)		1.4		2.6	V
MODE = V_L Threshold (MAX1739 SMB Interface Mode)	To sync DPWM oscillator, not in shutdown (Note 4)		VL - 0.6			V
MODE AC Signal Amplitude	Peak to peak (Note 5)		2			V
MODE AC Signal Synchronization Range	Chopping oscillator synchronized to MODE AC signal		32		100	kHz

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 8.2V, $V_{\overline{SH}}$/SUS = $V_{\overline{SH}}$ = 5.5V, MINDAC = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INTERFACE BRIGHTNESS CONTROL (MODE connected to REF or GND)					
CRF/SDA, CRF Input Range		2.7		5.5	V
CRF/SDA, CRF Input Current	$V_{CRF/SDA}$ = V_{CRF} = 5.5V			20	µA
	$V_{CRF/SDA}$ = V_{CRF} = 5.5V, $\overline{SH}$/SUS = $\overline{SH}$ = 0	-1		1	µA
CTL/SCL, Input Range	MAX1739	0		CRF/ SDA	V
CTL Input Range	MAX1839	0		CRF	V
CTL/SCL, CTL Input Current	MODE = REF or GND	-1		1	µA
ADC Resolution	Guaranteed monotonic		5		Bits
ADC Hysteresis			1		LSB
$\overline{SH}$ Input Low Voltage				0.8	V
$\overline{SH}$ Input High Voltage		2.1			V
$\overline{SH}$/SUS Input Hysteresis when Transitioning In and Out of Shutdown			150		mV
$\overline{SH}$ Input Bias Current		-1		1	µA
SYSTEM MANAGEMENT BUS BRIGHTNESS CONTROL (MAX1739, MODE connected to V_L, see Figures 12 and 13)					
CRF/SDA, CTL/SCL, $\overline{SH}$/SUS Input				0.8	V
CRF/SDA, CTL/SCL, $\overline{SH}$/SUS Input		2.1			V
CRFSDA, CTLSCL Input Hysteresis			300		mV
CRF/SDA, CTL/SCL, $\overline{SH}$/SUS Input		-1		1	µA
CRF/SDA Output Low Sink Current	$V_{CRF/SDA}$ = 0.4V	4			mA
CTL/SCL Serial Clock High Period	t_{HIGH}	4			µs
CTL/SCL Serial Clock Low Period	t_{LOW}	4.7			µs
Start Condition Setup Time	$t_{SU:STA}$	4.7			µs
Start Condition Hold Time	$t_{HD:STA}$	4			µs
CRF/SDA Valid to CTL/SCL Rising Edge Setup Time, Slave Clocking in Data	$t_{SU:DAT}$	250			ns
CTL/SCL Falling Edge to CRF/SDA Transition	$t_{HD:DAT}$	0			ns
CTL/SCL Falling Edge to CRF/SDA Valid, Reading Out Data	t_{DV}			1	µs

ELECTRICAL CHARACTERISTICS

(V+ = 8.2V, $V_{\overline{SH}}$/SUS = $V_{\overline{SH}}$ = 5.5V, MINDAC = GND, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 6)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY AND REFERENCE					
V_{BATT} Input Voltage Range	VL = V_{BATT}	4.6		5.5	V
	VL = open	6		28	
V_{BATT} Quiescent Current, Shutdown	$\overline{SH}$/SUS = $\overline{SH}$ = GND			20	µA
VL Output Voltage, Normal Operation	6V < V_{BATT} < 28V, 0 < I_{LOAD} < 15mA	5.0		5.6	V
VL Undervoltage Lockout Threshold	VL rising (leaving lockout)			4.6	V
	VL falling (entering lockout)	4.0			
REF Output Voltage, Normal Operation	4.5V < VL < 5.5V, I_{REF} = 40µA	1.95		2.05	V
VL POR Threshold		0.9		2.7	V
SWITCHING REGULATOR					
DH Driver On-Resistance				18	Ω
DL1, DL2 Driver On-Resistance				18	Ω
SYNC Synchronization Range	Detect falling edges on SYNC	64		200	kHz
CS Overcurrent Threshold		408		492	mV
DAC AND ERROR AMPLIFIER					
CSAV Regulation Point	V_{MINDAC} = 0, DAC code = 11111 binary	186		202	mV
CTFB Regulation Point		560		640	mV
CTFB to CCV Transconductance	1V < V_{CCV} < 2.7V	30		50	µmho
ANALOG INTERFACE BRIGHTNESS CONTROL (MODE connected to REF or MODE connected to GND)					
$\overline{SH}$ Input Low Voltage				0.8	V
$\overline{SH}$ Input High Voltage		2.1			V
SYSTEM MANAGEMENT BUS BRIGHTNESS CONTROL (MODE connected to VL)					
CRF/SDA, CTL/SCL, $\overline{SH}$/SUS Input Low Voltage				0.8	V
CRF/SDA, CTL/SCL, $\overline{SH}$/SUS Input High Voltage		2.1			V
CRF/SDA Output Low Sink Current	$V_{CRF/SDA}$ = 0.4V	4			mA

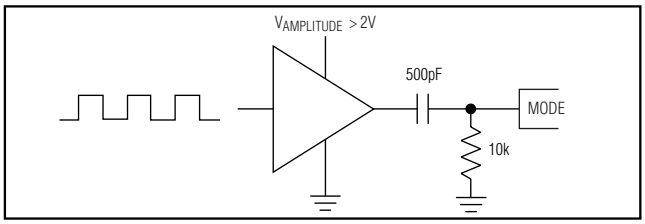
Note 1: Corresponds to 512 DPWM cycles or 65536 MODE cycles.

Note 2: When the buck switch is shorted, V_{CTFB} goes high causing V_{CCV} to go below the fault detection threshold.

Note 3: Corresponds to 64 DPWM cycles or 8192 MODE cycles.

Note 4: The MODE pin thresholds are only valid while the part is operating. In shutdown, V_{REF} = 0 and the part only differentiates between SMB mode and ADC mode. In shutdown with ADC mode selected, the CRF/SDA and CTL/SCL pins are at high impedance and will not cause extra supply current when their voltages are not at GND or VL.

Note 5: The amplitude is measured with the following circuit:



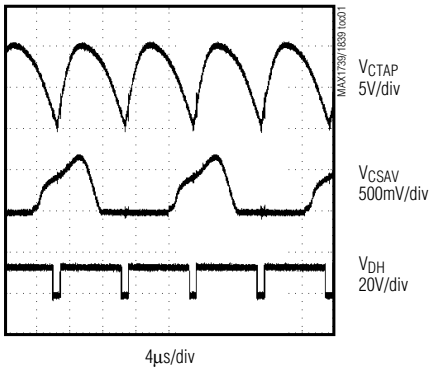
Note 6: Specifications from -40°C to +85°C are guaranteed by design, not production tested.

Wide Brightness Range CCFL Backlight Controllers

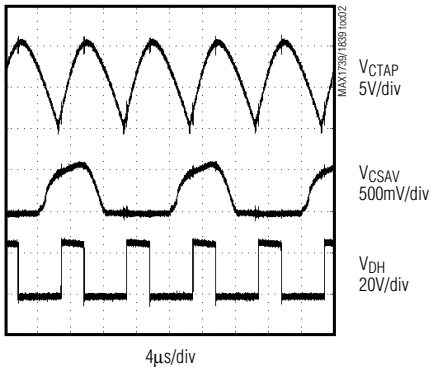
Typical Operating Characteristics

(V_{IN} = 12V, V_{CTL} = V_{CRF}, V_{MINDAC} = 1V, MODE = GND, Circuit of Figure 8.)

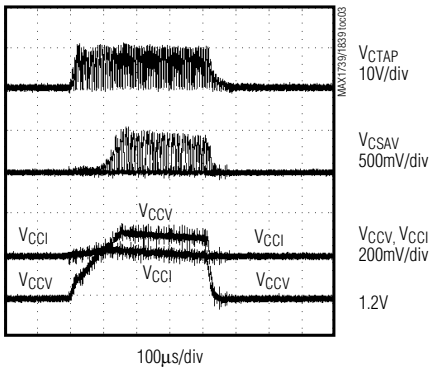
WIDE INPUT RANGE (V_{BATT} = 8V)



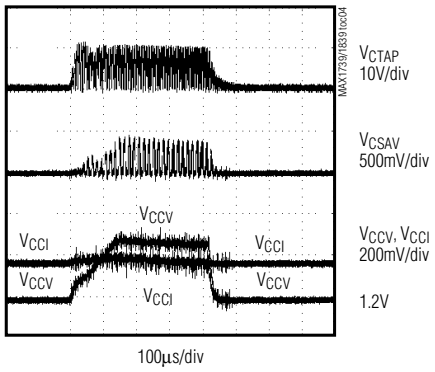
WIDE INPUT RANGE (V_{BATT} = 20V)



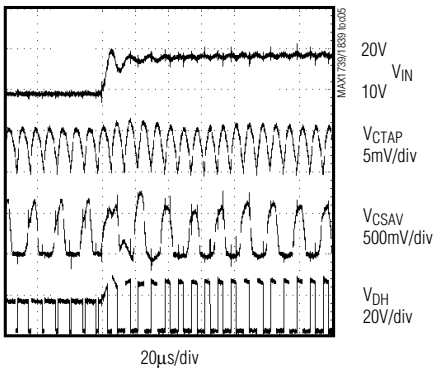
WIDE INPUT RANGE (V_{BATT} = 8V, DPWM = 9%, V_{CTL} = 0)



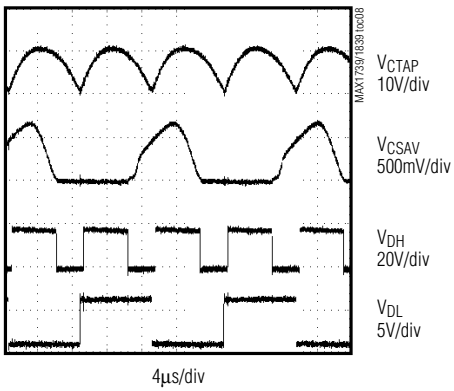
WIDE INPUT RANGE (V_{BATT} = 20V, DPWM = 9%, V_{CTL} = 0)



FEED-FORWARD COMPENSATION



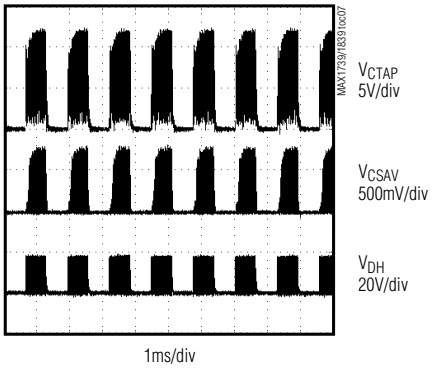
SWITCHING WAVEFORMS



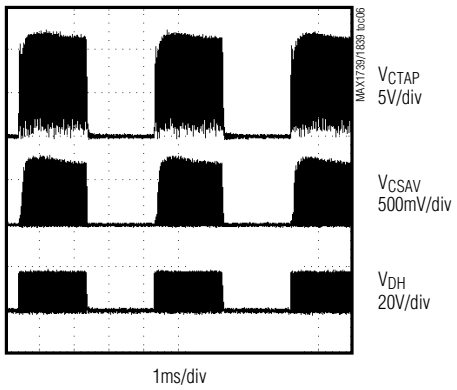
Typical Operating Characteristics (continued)

(V_{IN} = 12V, V_{CTL} = V_{CRF}, V_{MINDAC} = 1V, MODE = GND, Circuit of Figure 8.)

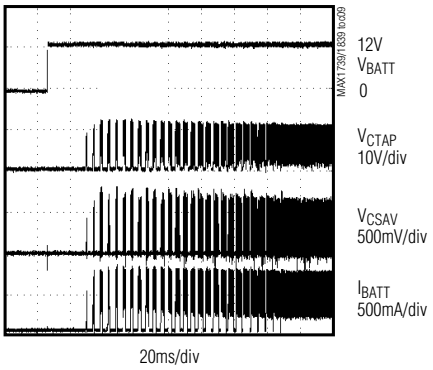
SYNCHRONIZED DPWM
(f_{MODE} = 100kHz, V_{CTL} = V_{CRF}/2)



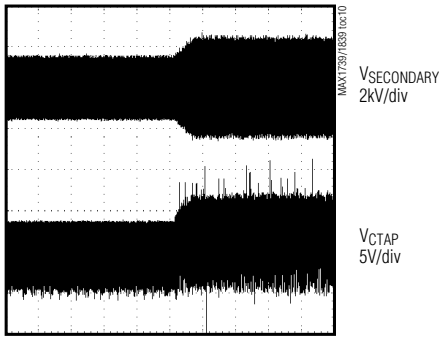
SYNCHRONIZED DPWM
(f_{MODE} = 32kHz, V_{CTL} = V_{CRF}/2)



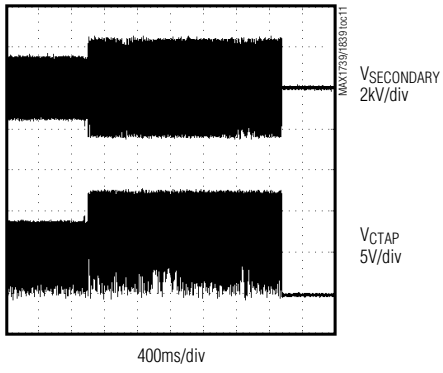
STARTUP
(ADC SOFT-START, MODE = GND)



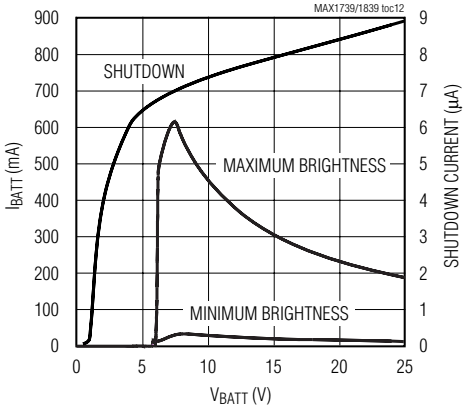
LAMP-OUT VOLTAGE LIMITING



LAMP-OUT VOLTAGE LIMITING



INPUT CURRENT vs. INPUT VOLTAGE

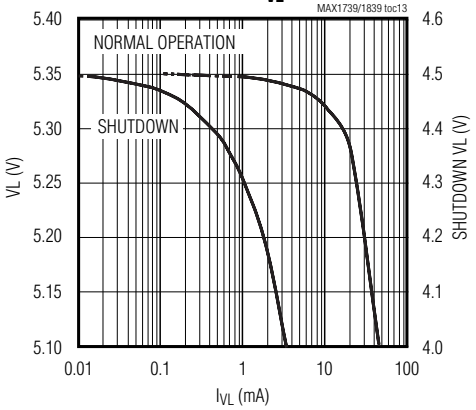


Wide Brightness Range CCFL Backlight Controllers

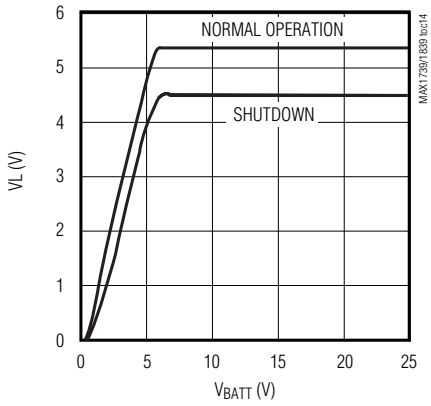
Typical Operating Characteristics (continued)

(V_{IN} = 12V, V_{CTL} = V_{CRF}, V_{MINDAC} = 1V, MODE = GND, Circuit of Figure 8.)

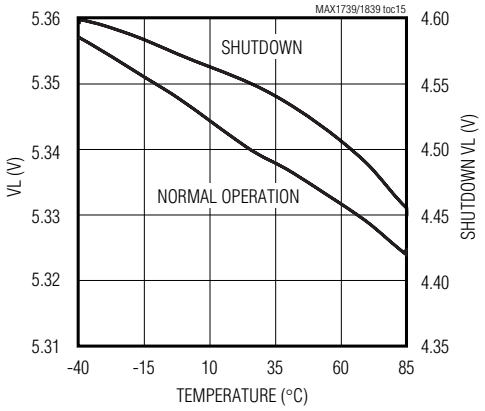
VL vs. I_{VL}



VL vs. BATT VOLTAGE



VL vs. TEMPERATURE



Pin Description

PIN	NAME		FUNCTION
	MAX1739	MAX1839	
1	REF	REF	2V Reference Output. Bypass to GND with 0.1µF. Forced low during shutdown.
2	MINDAC	MINDAC	DAC Zero-Scale Input. V_{MINDAC} sets the DAC's minimum scale output voltage. Disable DPWM by connecting MINDAC to VL.
3	CCI	CCI	GMI Output. Output of the current loop GMI amplifier that regulates the CCFL current. Typically bypass to GND with 0.1µF.
4	CCV	CCV	GMV Output. Output of the voltage loop GMV amplifier that regulates the maximum average primary transformer voltage. Typically bypass to GND with 3300pF.
5	$\overline{SH}$/SUS	$\overline{SH}$	Logic Low Shutdown Input in Analog Interface Mode. SMBus suspends input in SMBus interface mode (MAX1739 only).
6	CRF/SDA	CRF	5-Bit ADC Reference Input in Analog Interface Mode. Bypass to GND with 0.1µF. SMBus serial data input/open-drain output (MAX1739 only) in SMBus interface mode.
7	CTL/SCL	CTL	CCFL Brightness Control Input in Analog Interface Mode. SMBus serial clock input (MAX1739 only) in SMBus interface mode.
8	MODE	MODE	Interface Selection Input and Sync Input for DPWM Chopping (see *Synchronizing the DPWM Frequency*). The average voltage on the MODE pin selects one of three CCFL brightness control interfaces: 1) MODE = VL, enables SMBus serial interface (MAX1739 only). 2) MODE = GND, enables the analog interface (positive scale analog interface mode); $V_{CTL/SCL}$ = 0 means minimum brightness. 3) MODE = REF, enables the analog interface (negative scale analog interface mode); $V_{CTL/SCL}$ = 0 means maximum brightness.
9	CSAV	CSAV	Current-Sense Input. Input to the GMI error amplifier that drives CCI.
10	CTFB	CTFB	Center-Tap Voltage Feedback Input. The average V_{CTFB} is limited to 0.6V.
11	SYNC	SYNC	Royer Synchronization Input. Falling edges on SYNC force DH on and toggle the DL1 and DL2 drivers. Connect directly to the Royer center tap.
12	DL2	DL2	Low-Side N-Channel MOSFET 2 Gate Drive. Drives the Royer oscillator switch. DL1 and DL2 have make-before-break switching, where at least one is always on. Falling edges on SYNC toggle DL1 and DL2 and turn DH on.
13	DL1	DL1	Low-Side N-Channel MOSFET 1 Gate Drive
14	CS	CS	Current-Sense Input (Current Limit). The current-mode regulator terminates the switch cycle when V_{CS} exceeds (V_{REF} - V_{CCI}).
15	GND	GND	System Ground
16	VL	VL	5.3V Linear Regulator Output. Supply voltage for most of the internal circuits. Bypass with 1µF capacitor to GND. Can be connected to V_{BATT} if V_{BATT} < 5.5V.
17	BST	BST	High-Side Driver Bootstrap Input. Connect through a diode to VL and bypass with 0.1µF capacitor to LX.
18	LX	LX	High-Side Driver Ground Input
19	DH	DH	High-Side Gate Driver Output. Falling edges on SYNC turn on DH.
20	BATT	BATT	Supply Input. Input to the internal 5.3V linear regulator that powers the chip.

Wide Brightness Range CCFL Backlight Controllers

Detailed Description

The MAX1739/MAX1839 regulate the brightness of a CCFL in three ways:

1) Linearly controlling the lamp current.

2) Digitally pulse-width modulating (or chopping) the lamp current (DPWM).

3) Using both methods simultaneously for widest dimming range.

DPWM is implemented by pulse-width modulating the lamp current at a rate faster than the human eye can detect. Figure 1 shows the current and voltage waveforms for the three operating modes with the brightness control set to 50% of full scale.

The MAX1739/MAX1839 include a 5.3V linear regulator to power most of the internal circuitry, drivers for the buck and Royer switches, and the synchronizable DPWM oscillator. The MAX1739/MAX1839 are very flexible and include a variety of operating modes, an analog interface, an SMBus interface (MAX1739 only), a shutdown mode, lamp-out detection, and buck-switch short detection.

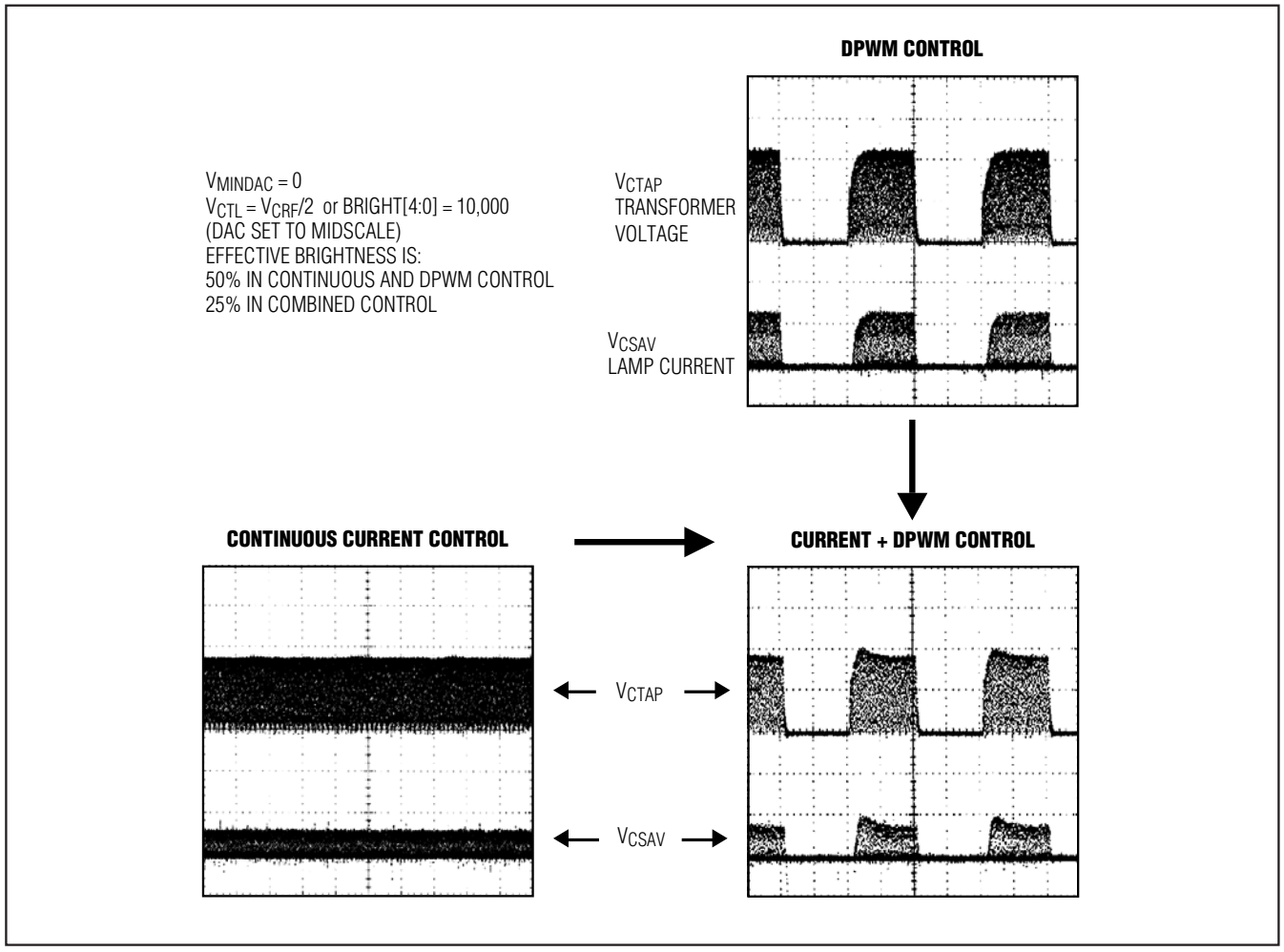


Figure 1. Brightness Control Methods

Voltage and Current Control Loops

The MAX1739/MAX1839 use two control loops. The current control loop regulates the average lamp current. The voltage control loop limits the maximum average primary-side transformer voltage. The voltage control loop is active during the beginning of DPWM on-cycles and in some fault conditions. Limiting the transformer primary voltage allows for a lower transformer secondary voltage rating that can increase reliability and decrease cost of the transformer. The voltage control loop acts to limit the transformer voltage any time the current control loop attempts to steer the transformer voltage above its limit as set by V_{CTFB} (see *Sense Resistors*).

The voltage control loop uses a transconductance amplifier to create an error current based on the voltage between CTFB and the internal reference level (600mV typ) (Figure 2). The error current is then used to charge and discharge C_{CCV} to create an error voltage V_{CCV}. The current control loop produces a similar signal based on the voltage between CSAV and its internal reference level (see the *Dimming Range* section). This error voltage is called V_{CCI}. The lower of V_{CCV} and V_{CCI} is used with the buck regulator's PWM ramp generator to set the buck regulator's duty cycle.

During DPWM, the two control loops work together to limit the transformer voltage and to allow wide dimming range with good line rejection. During the DPWM off-cycle, V_{CCV} is set to 1.2V and CCI is set to high impedance. V_{CCV} is set to 1.2V to create soft-start at the beginning of each DPWM on-cycle in order to avoid overshoot on the transformer primary. V_{CCI} is set to high impedance to keep V_{CCI} from changing during the off-cycles. This allows the current control loop to regulate the average lamp current only during DPWM on-cycles and not the overall average lamp current.

Upon power-up, V_{CCI} slowly rises, increasing the duty cycle, which provides soft-start. During this time, V_{CCV}, which is the faster control loop, is limited to 150mV above V_{CCI} by the CCV-CLAMP. Once the secondary voltage reaches the strike voltage, the lamp current begins to increase. When the lamp current reaches the regulation point, V_{CCI} reaches steady state. With MINDAC = VL (DPWM disabled), the current control loop remains in control and regulates the lamp current.

With MINDAC between REF and GND, DPWM is enabled and the MAX1739/MAX1839 begin pulsing the lamp current. During the on-cycle, V_{CCV} is at 150mV above V_{CCI}. After the on-cycle, V_{CCV} is forced down to 1.2V to provide soft-start at the beginning of the next on-cycle. Also, V_{CCI} retains its value until the beginning of the next on-cycle. When V_{CCV} increases, it causes the buck regulator duty cycle to increase and provides soft-start. When V_{CCV} crosses over V_{CCI}, the current control loop regains control and regulates the lamp current. V_{CCV} is limited to 150mV above V_{CCI} for the remainder of the on-cycle.

In a lamp-out condition, V_{CCI} increases the primary voltage in an attempt to maintain lamp current regulation. As V_{CCI} rises, V_{CCV} rises with it until the primary voltage reaches its set limit point. At this point, V_{CCV} stops rising and limits the primary voltage by limiting the duty cycle. Because V_{CCV} is limited to 150mV above V_{CCI}, the voltage control loop is quickly able to limit the primary voltage. Without this clamping feature, the transformer voltage would overshoot to dangerous levels because V_{CCV} would take more time to slew down from its supply rail. Once the MAX1739/MAX1839 sense less than 1/6 the full-scale current through the lamp for 2 seconds, it shuts down the Royer oscillator (see *Lamp-Out Detection*).

See the *Sense Resistors* section for information about setting the voltage and current control loop thresholds.

Feed-Forward Control

Both control loops are influenced by the input voltage feed-forward (V_{BATT}) control circuitry of the MAX1739/MAX1839. Feed-forward control instantly adjusts the buck regulator's duty cycle when it detects a change in input voltage. This provides immunity to changes in input voltage at all brightness levels. This feature makes compensation over wide input ranges easier, makes startup transients less dependent on input voltage, and improves line regulation for short DPWM on-times.

The MAX1739/MAX1839 feed-forward control is implemented by varying the amplitude of the buck-switch's PWM ramp amplitude. This has the effect of varying the duty cycle as a function of input voltage while maintaining the same V_{CCI} and V_{CCV}. In other words, V_{BATT} feed forward has the effect of not requiring changes in error-signal voltage (V_{CCI} and V_{CCV}) to respond to changes in V_{BATT}. Since the capacitors only need to change their voltage minimally to respond to changes in V_{BATT}, the controller's response is essentially instantaneous.

Transient Overvoltage Protection from Dropout

The MAX1739/MAX1839 are designed to maintain tight control of the transformer primary under all transient conditions. This includes transients from dropout, where V_{BATT} is so low that the controller loses regulation and reaches maximum duty cycle. Backlight designs will want to choose circuit component values to minimize the transformer turns ratio in order to minimize primary-side currents and I^2R losses. To achieve this,

Wide Brightness Range CCFL Backlight Controllers

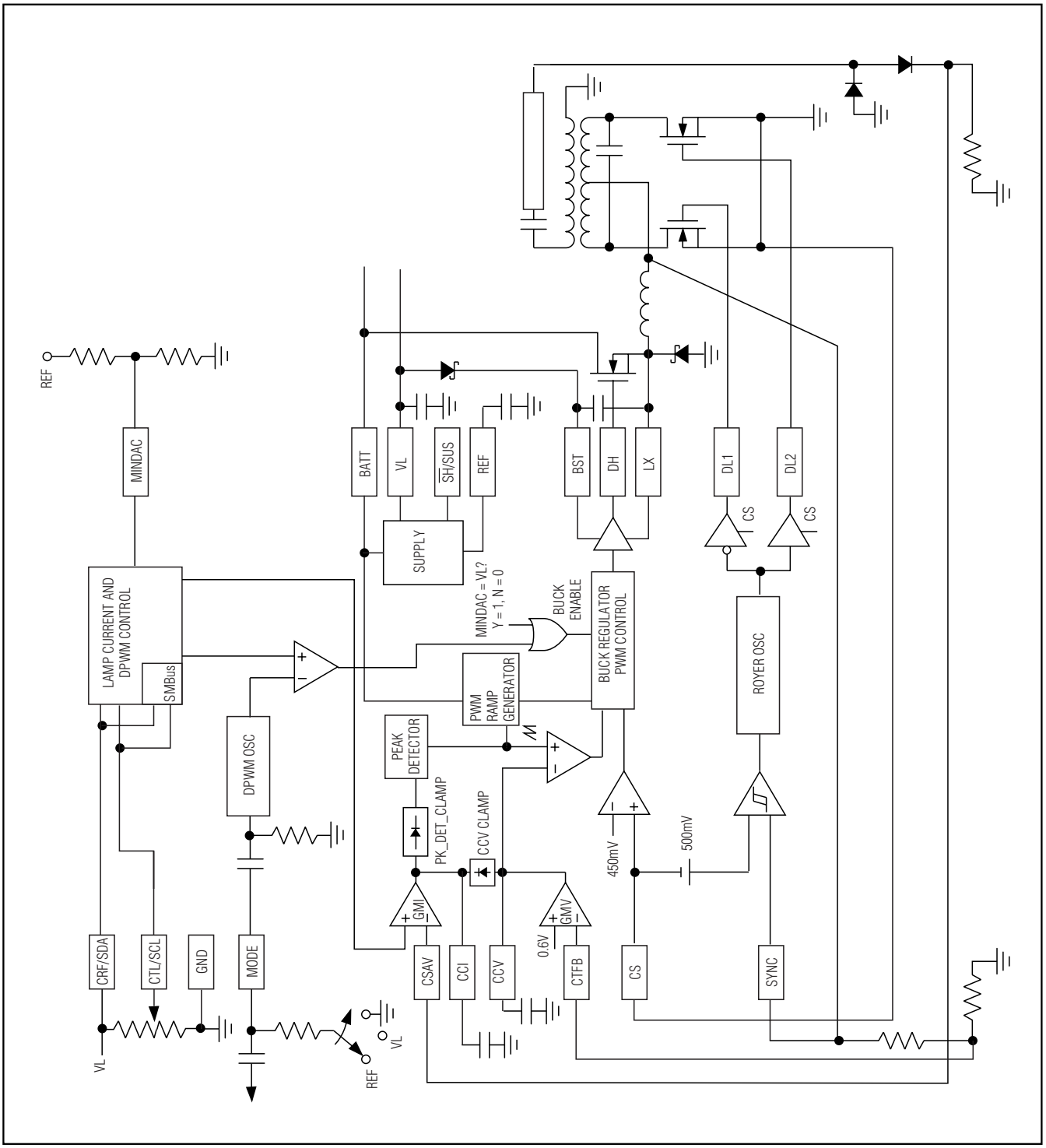


Figure 2. Functional Diagram

allow the circuit to operate in dropout at extremely low battery voltages where the backlight's performance is secondary. All backlight circuit designs can undergo a transient overvoltage condition when the laptop is plugged into the AC adapter and V_{BATT} suddenly increases. The MAX1739/MAX1839 contain a unique clamp circuit on V_{CCI}. Along with the feed-forward circuitry, it ensures that there is not a transient transformer overvoltage when leaving dropout.

The PK_DET_CLAMP circuit limits V_{CCI} to the peaks of the buck-regulator's PWM ramp generator. As the circuit reaches dropout, V_{CCI} approaches the peaks of the PWM ramp generator in order to reach maximum duty cycle. If V_{BATT} decreases further, the control loop loses regulation and V_{CCI} tries to reach its positive supply rail. The clamp circuit on V_{CCI} keeps this from happening, and V_{CCI} rides just above the peaks of the PWM ramp. As V_{BATT} decreases further, the feed-forward PWM ramp generator loses amplitude and the clamp drags V_{CCI} down with it to a voltage below where V_{CCI} would have been if the circuit was not in dropout. When VBATT is suddenly increased out of dropout, V_{CCI} is still low and maintains the drive on the transformer at the old dropout level. The circuit then slowly corrects and increases V_{CCI} to bring the circuit back into regulation.

Buck Regulator

The buck regulator uses the signals from the PWM comparator, the current-limit detection on CS, and DPWM signals to control the high-side MOSFET duty cycle. The regulator uses voltage-mode PWM control and is synchronized to the Royer oscillator. A falling edge on SYNC turns on the high-side MOSFET after a 375ns minimum off-time delay. The PWM comparator or the CS current limit ends the on-cycle.

Interface Selection

Table 1 lists the functionality of $\overline{SH}$/SUS, CRF/SDA, and CTL/SCL in each of the three interface modes of the MAX1739/MAX1839. The MAX1739 features both an SMBus digital interface and an analog interface, while the MAX1839 features only the analog interface. Note that MODE can also synchronize the DPWM frequency (see *Synchronizing the DPWM Frequency*).

Dimming Range

Brightness is controlled by either the analog interface (see *Analog Interface*) or the SMBus interface (see *SMBus Interface*). CCFL brightness is adjusted in three ways:

1) Lamp current control, where the magnitude of the average lamp current is adjusted.

2) DPWM control, where the average lamp current is pulsed to the lamp with a variable duty cycle.

3) A combination of the first two methods.

In each of the three methods, a 5-bit brightness code is generated from the selected interface and is used to set the lamp current and/or DPWM duty cycle.

The 5-bit brightness code defines the lamp current level with ob00000 representing minimum lamp current and ob11111 representing maximum lamp current. The average lamp current is measured across an external sense resistor (see *Sense Resistors*). The voltage on the sense resistor is measured at CSAV. The brightness code adjusts the regulation voltage at CSAV (V_{CSAV}). The minimum average V_{CSAV} is V_{MINDAC}/10, and the maximum average is set by the following formula:

$$V_{CSAV} = V_{REF} \times 31 / 320 + V_{MINDAC} / 320$$

which is between 193.75mV and 200mV.

Note that if V_{CSAV} does not exceed 100mV peak (which is about 32mV average) for over 2 seconds, the MAX1739/MAX1839 will assume a lamp-out condition and shut down (see *Lamp-Out Detection*).

The equation relating brightness code to C_{SAV} regulation voltage is:

$$V_{CSAV} = V_{REF} \times n / 320 + V_{MINDAC} \times (32 - n) / 320$$

where n is the brightness code.

To always use maximum average lamp current when using DPWM control, set V_{MINDAC} to V_{REF}.

DPWM control works similar to lamp current control in that it also responds to the 5-bit brightness code. A

Table 1. Interface Modes

PIN	DIGITAL INTERFACE	ANALOG INTERFACE	
	MODE = VL (MAX1739 only)	MODE = REF, V_{CTL}/SCL = 0 = maximum brightness	MODE = GND, V_{CTL}/SCL = 0 = minimum brightness
$\overline{SH}$/SUS	SMBus suspend	Logic-level shutdown control input	
CRF/SDA	SMBus data I/O	Reference input for minimum brightness	Reference input for maximum brightness
CTL/SCL	SMBus clock input	Analog control input to set brightness (range from 0 to CRF/SDA)	

brightness code of ob00000 corresponds to a 9.375% DPWM duty cycle, and a brightness code of ob11111 corresponds to a 100% DPWM duty cycle. The duty cycle changes by 3.125% per step, except codes ob00000 to ob00011 all produce 9.375% (Figure 3).

To disable DPWM and always use 100% duty cycle, set V_{MINDAC} to VL. Note that with DPWM disabled, the equations above should assume V_{MINDAC} = 0 instead of V_{MINDAC} = VL. Table 2 lists MINDAC's functionality, and Table 3 shows some typical settings for the brightness adjustment.

In normal operation, V_{MINDAC} is set between 0 and V_{REF}, and the MAX1739/MAX1839 use both lamp current control and DPWM control to vary the lamp brightness (Figure 4). In this mode, lamp current control regulates the average lamp current during a DPWM on-cycle and not the overall average lamp current.

Analog Interface and Brightness Code

The MAX1739/MAX1839 analog interface uses an internal ADC with 1-bit hysteresis to generate the brightness code used to dim the lamp (see *Dimming Range*). CTL/SDA is the ADC's input, and CRF/SCL is its reference voltage. The ADC can operate in either positive-scale ADC mode or negative-scale ADC mode. In positive-scale ADC mode, the brightness code increases from 0 to 31 as V_{CTL} increases from 0 to V_{CRF}. In negative-scale mode, the brightness scale decreases from 31 to 0 as V_{CTL} increases from 0 to V_{CRF} (Figure 5).

The analog interface's internal ADC uses 1-bit hysteresis to keep the lamp from flickering between two codes. VCTL's positive threshold ($V_{CTL(TH)}$) is the voltage required to transition the brightness code as V_{CTL} increases and can be calculated as follows:

$$V_{CTL(TH)} = (n + 2) / 33\ V_{CRF}$$
(positive-scale ADC mode, MODE = GND)

$$V_{CTL(TH)} = (33 - n) / 33\ V_{CRF}$$
(negative-scale ADC mode, MODE = REF)

where n is the current selected brightness code. VCTL's negative threshold is the voltage required to transition the brightness code as V_{CTL} decreases and can be calculated as follows:

$$V_{CTL(TH)} = n / 33\ V_{CRF}$$
(positive-scale ADC mode, MODE = GND)

$$V_{CTL(TH)} = (31 - n) / 33\ V_{CRF}$$
(negative-scale ADC mode, MODE = REF)

Figure 5 shows a graphic representation of the thresholds. CRF/SDA's and CTL/SCL's input voltage range is 2.7V to 5.5V.

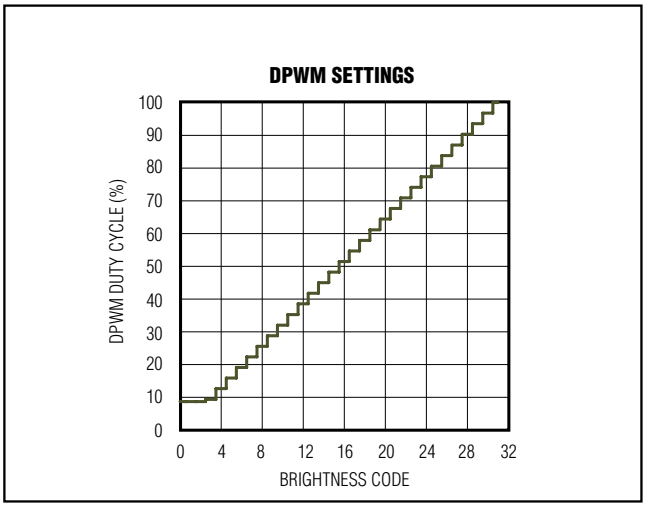


Figure 3. DPWM Settings

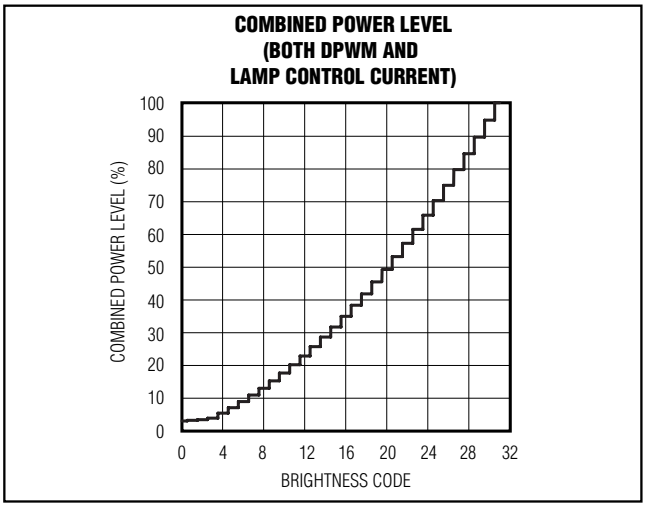


Figure 4. Combined Power Level

Table 2. MINDAC Functionality

MINDAC = VL	DPWM disabled (always on 100% duty cycle). Operates in lamp current control only. (Use V_{MINDAC} = 0 in the equations.)
MINDAC = REF	DPWM control enabled, duty cycle ranges from 9% to 100%. Lamp current control is disabled (always maximum current).
0 ≤ V_{MINDAC} < V_{REF}	The device uses both lamp current control and DPWM.