ISL54217

USB 2.0 High-Speed x 2 Channels/Stereo Audio Dual SP3T (Dual 3-to-1 Multiplexer)

FN6817
Rev.5.00
Dec 12, 2018

The ISL54217 is a single supply dual SP3T analog switch that operates from a single supply in the range of 2.7V to 4.6V. It was designed to multiplex between audio stereo signals and two different USB 2.0 high speed differential data signals. The audio channels allow signal swings below ground, allowing the multiplexing of voice and data signals through a common headphone connector in Personal Media Players and other portable battery powered devices.

The audio switch cells can pass ±1V ground referenced audio signals with very low distortion (<0.03% THD+N when driving 5mW into 32Ω loads). The USB switch cells have very low ON-capacitance (8pF) and high bandwidth to pass USB high speed signals (480Mbps) with minimal edge and phase distortion.

The ISL54217 is available in a tiny 12 Ld 2.2mmx1.4mm ultra thin QFN and a 12 Ld 3mmx3mm TQFN package. It operates over a temperature range of -40°C to +85°C.

Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)

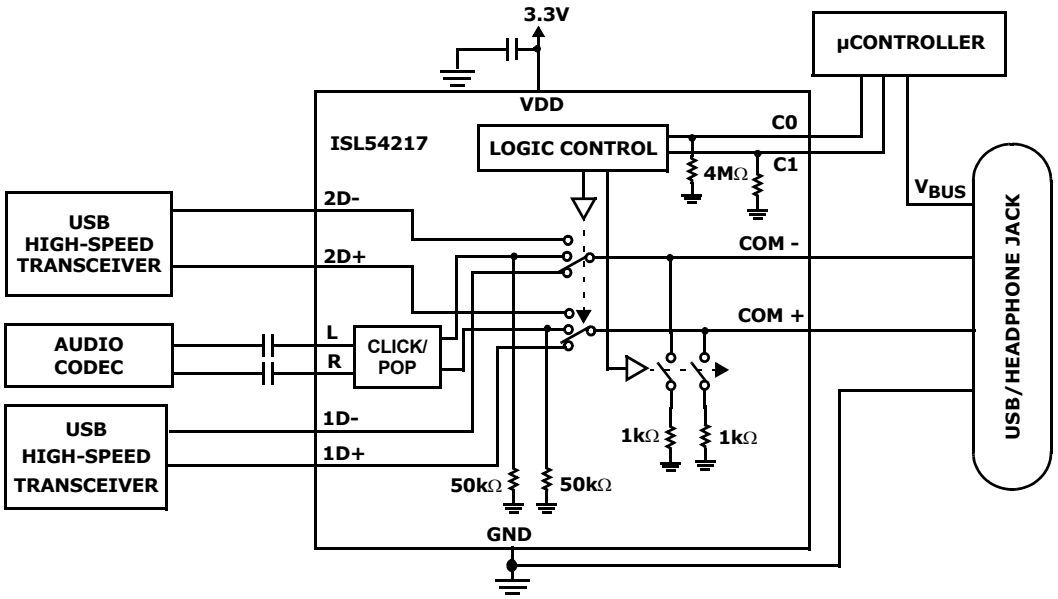
Features

- High Speed (480Mbps) and Full Speed (12Mbps) Signaling Capability per USB 2.0
- Low Distortion Negative Signal Capability Audio Switches
- Clickless/Popless Audio Switches
- Power OFF Protection
- COM Pins Overvoltage Tolerant to 5.5V
- Low Distortion Headphone Audio Signals
  - THD+N at 5mW into 32Ω Load . . . . . <0.03%
- Crosstalk (100kHz) . . . . . -98dB
- OFF-Isolation (100kHz) 95.5dB
- Single Supply Operation (V_{DD}) . . . . . 2.7V to 4.6V
- -3dB Bandwidth USB Switches 700MHz
- Available in Tiny 12 Ld µTQFN and TQFN Packages
- Compliant with USB 2.0 Short Circuit Requirements Without Additional External Components
- Pb-Free (RoHS Compliant)

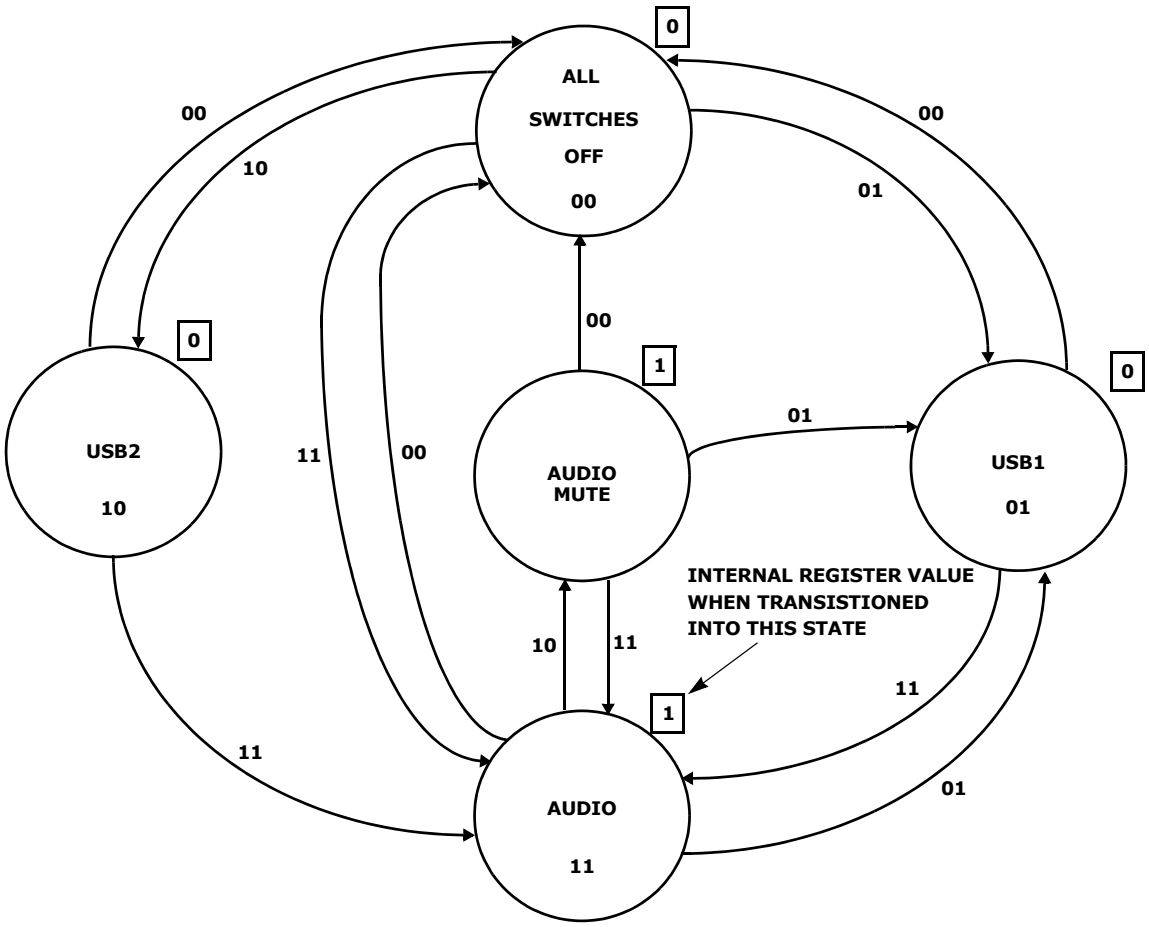
Applications

- MP3 and other Personal Media Players
- Cellular/Mobile Phone

Application Block Diagram

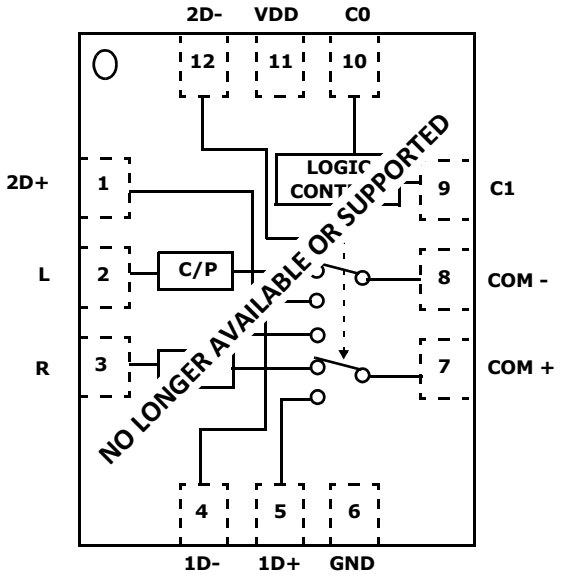


State Diagram

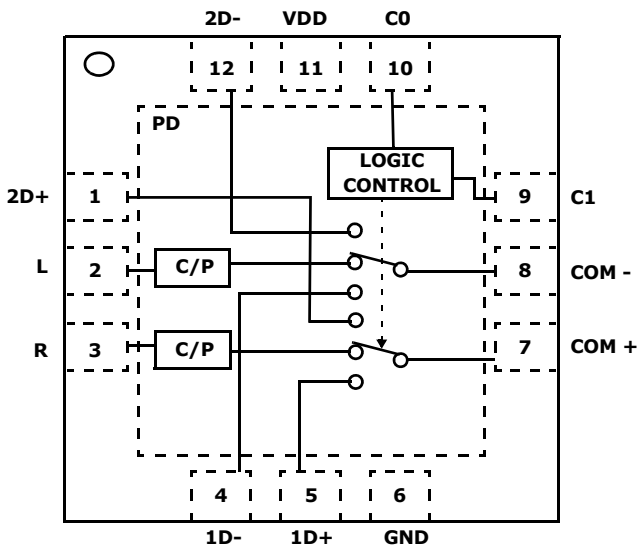


Pin Configurations

ISL54217
(12 LD 2.2X1.4 µTQFN)
TOP VIEW



ISL54217
(12 LD 3X3 TQFN)
TOP VIEW



NOTE:

1. ISL54217 Switches Shown for C1 = Logic "1" and C0 = Logic "1". The R and L 50kΩ pull-down resistors, C1 and CO 4MΩ pull-down resistors and COM- and COM+ 1kΩ Shunts are not shown.

Pin Descriptions

µTQFN	TQFN	NAME	FUNCTION
1	1	2D+	USB2 Differential Input
2	2	L	Audio Left Input
3	3	R	Audio Right Input
4	4	1D-	USB1 Differential Input
5	5	1D+	USB1 Differential Input
6	6	GND	Ground Connection
7	7	COM+	Voice and Data Common Pin
8	8	COM-	Voice and Data Common Pin
9	9	C1	Digital Control Input
10	10	C0	Digital Control Input
11	11	V_{DD}	Power Supply
12	12	2D-	USB2 Differential Input
-	PD	PD	Thermal Pad. Tie to Ground or Float

Truth Table

CURRENT CODE		LAST CODE			SHUNT SWITCHES		
C1	C0	C1	C0	MODE	CLICK/POP AUDIO SHUNTS	1kΩ COM SHUNTS	INTERNAL REGISTER
0	0	X	X	All Switches Off	ON	OFF	0
0	1	X	X	USB1	ON	OFF	0
1	0	0	0	USB2	ON	OFF	0
1	0	0	1	USB2	ON	OFF	0
1	0	1	0	USB2	ON	OFF	0
1	1	X	X	AUDIO	OFF	OFF	1
1	0	1	0	MUTE	OFF	ON	1
1	0	1	1	MUTE	OFF	ON	1

NOTE: C0, C1: Logic "0" when ≤ 0.5V, Logic "1" when ≥ 1.4V with V_{DD} in the range of 2.7V to 3.6V.

Ordering Information

PART NUMBER (Note 5)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL54217IRUZ-T (Notes 2, 3) **(No longer available or supported)**	GP	-40 to +85	12 Ld 2.2mmx1.4mm µTQFN (Tape and Reel)	L12.2.2x1.4A
ISL54217IRTZ (Note 4)	4217	-40 to +85	12 Ld 3mmx3mm TQFN	L12.3x3A
ISL54217IRTZ-T (Notes 2, 4)	4217	-40 to +85	12 Ld 3mmx3mm TQFN (Tape and Reel)	L12.3x3A
ISL54217EVAL1Z	Evaluation Board			

NOTES:

2. Please refer to TB347 for details on reel specifications.
3. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
5. For Moisture Sensitivity Level (MSL), please see device information page for ISL54217. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

V_{DD} to GND . . . . . -0.3V to 5.5V
Input Voltages
1D+, 1D-, L, R, 2D+, 2D- . . . . . -2V to 5.5V
C0, C1 (Note 6) . . . . . -0.3V to 5.5V
Output Voltages
COM-, COM+ . . . . . -2V to 5.5V
Continuous Current (L, R) . . . . . ±60mA
Peak Current (L, R)
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±120mA
Continuous Current (1D-, 1D+, 2D-, 2D+) . . . . . ±40mA
Peak Current (1D-, 1D+, 2D-, 2D+)
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±100mA
ESD Rating:
Human Body Model . . . . . >5kV
Machine Model . . . . . >500V
Charged Device Model . . . . . >2kV
Latch-up Tested per JEDEC; Class II Level A . . . . . at 85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
12 Ld µTQFN Package (Note 7, 10).	155	90
12 Ld TQFN Package (Notes 8, 9). .	58	1.0

Maximum Junction Temperature (Plastic Package). . +150°C
Maximum Storage Temperature Range. . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Operating Conditions

Temperature Range . . . . . -40°C to +85°C
Supply Voltage Range . . . . . 2.7V to 4.6V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. Signals on C1 and C0 exceeding GND by specified amount are clamped. Limit current to maximum current ratings.
7. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
8. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
9. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
10. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications - 2.7V to 3.6V Supply Test Conditions: V_{DD} = +3.0V, GND = 0V, V_{C0H}, V_{C1H} = 1.4V, V_{C0L}, V_{C1L}= 0.5V, (Note 11), Unless Otherwise Specified. Boldface limits apply over the operating temperature range, -40°C to +85°C.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 12, 13)	TYP	MAX (Notes 12, 13)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Audio Switches (L, R)						
Analog Signal Range, V_{ANALOG}	V_{DD} = 3.0V to 3.6V, Audio Mode (C0 = V_{DD}, C1 = V_{DD})	Full	**-1.5**	-	**1.5**	V
ON-Resistance, r_{ON}	V_{DD} = 3.0V, Audio Mode (C0 = 1.4V, C1 = 1.4V), I_{COMx} = 60mA, V_L or V_R = -0.85V to 0.85V, (see Figure 3, Note 15)	+25	-	2.3	2.8	Ω
		Full	-	-	**3.4**	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V_{DD} = 3.0V, Audio Mode (C0 = 1.4V, C1 = 1.4V), I_{COMx} = 60mA, V_L or V_R = Voltage at max r_{ON} over signal range of -0.85V to 0.85V, (Notes 15, 16)	+25	-	0.04	0.25	Ω
		Full	-	-	**0.26**	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V_{DD} = 3.0V, Audio Mode (C0 = 1.4V, C1 = 1.4V), I_{COMx} = 60mA, V_L or V_R = -0.85V to 0.85V, (Notes 14, 15)	+25	-	0.03	0.05	Ω
		Full	-	-	**0.07**	Ω
Click/Pop Shunt Resistance, R_L, R_R	V_{DD} = 3.6V, ALL OFF Mode (C0 = 0.5V, C1 = 0.5V), V_{COM-} or V_{COM+} = -0.85V, 0.85V, V_L or V_R = -0.85V, 0.85V, Measure current into L or R pin and calculate resistance value.	+25	-	28	-	Ω
USB/DATA Switches (1D+, 1D-, 2D+, 2D-)						
Analog Signal Range, V_{ANALOG}	V_{DD} = 2.7V to 4.6V, USB1 mode (C0 = 0V, C1 = V_{DD}) or USB2 Mode (C0 = V_{DD}, C1 = 0V)	Full	**-1**	-	**VDD**	V

Electrical Specifications - 2.7V to 3.6V Supply Test Conditions: V_{DD} = +3.0V, GND = 0V, V_{C0H}, V_{C1H} = 1.4V, V_{C0L}, V_{C1L}= 0.5V, (Note 11), Unless Otherwise Specified. Boldface limits apply over the operating temperature range, -40°C to +85°C.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 12, 13)	TYP	MAX (Notes 12, 13)	UNITS
ON-Resistance, r_{ON}	V_{DD} = 2.7V, USB1 mode (C0 = 0.5V, C1 = 1.4V) or USB2 Mode (C0 = 1.4V, C1 = 0.5V), I_{COMx} = 40mA, V_{D+} or V_D = 0V to 400mV (see Figure 4, Note 15)	25	-	6.2	8	Ω
		Full	-	-	**10**	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V_{DD} = 2.7V, USB1 mode (C0 = 0.5V, C1 = 1.4V) or USB2 Mode (C0 = 1.4V, C1 = 0.5V), I_{COMx} = 40mA, V_{D+} or V_{D-}= Voltage at max r_{ON}, (Notes 15, 16)	25	-	0.08	0.5	Ω
		Full	-	-	**0.55**	Ω
r_{ON} Flatness, $R_{FLAT(ON)}$	V_{DD} = 2.7V, USB1 mode (C0 = 0.5V, C1 = 1.4V) or USB2 Mode (C0 = 1.4V, C1 = 0.5V), I_{COMx} = 40mA, V_{D+} or V_{D-}= 0V to 400mV, (Notes 14, 15)	25	-	0.26	1	Ω
		Full	-	-	**1.2**	Ω
ON-Resistance, r_{ON}	V_{DD} = 3.3V, USB1 mode (C0 = 0.5V, C1 = 1.4V) or USB2 Mode (C0 = 1.4V, C1 = 0.5V), I_{COMx} = 40mA, V_{D+} or V_{D-} = 3.3V (see Figure 4, Note 15)	+25	-	9.8	20	Ω
		Full	-	-	**25**	Ω
OFF Leakage Current, $I_{D+(OFF)}$ or $I_{D-(OFF)}$	V_{DD} = 3.6V, All OFF Mode (C0 = 0.5V, C1 = 0.5V), V_{COM-} or V_{COM+} = 0.5V, 0V, V_{D+} or V_{D-} = 0V, 0.5V, L = R = float	25	-15	0.11	15	nA
		Full	**-20**	-	**20**	nA
ON Leakage Current, I_{DX}	V_{DD} = 3.3V, USB1 mode (C0 = 0.5V, C1 = 1.4V) or USB2 Mode (C0 = 1.4V, C1 = 0.5V), V_{D+} or V_{D-} = 2.7V, COM- = COM+ = Float, L and R = float	25	-20	2.4	20	nA
		Full	**-25**	-	**25**	nA
DPDT DYNAMIC CHARACTERISTICS						
ALL OFF to USB or USB to All OFF Address Transition Time, t_{TRANS}	V_{DD} = 2.7V, R_L = 50Ω, C_L = 10pF, (see Figure 1)	25	-	175	-	ns
Audio to USB1 Address Transition Time, t_{TRANS}	V_{DD} = 2.7V, R_L = 50Ω, C_L = 10pF, (see Figure 1)	25	-	12	-	µs
Break-Before-Make Time Delay, t_D	V_{DD} = 3.6V, R_L = 50Ω, C_L = 10pF, (see Figure 2)	25	-	52	-	ns
Skew, ($t_{SKEWOUT}$ - t_{SKEWIN})	V_{DD} = 3.0V, USB1 mode (C0 = 0V, C1 = V_{DD}) or USB2 Mode (C0 = V_{DD}, C1 = 0V), R_L = 45Ω, C_L = 10pF, t_R = t_F = 500ps at 480Mbps, (Duty Cycle = 50%) (see Figure 7)	25	-	75	-	ps
Total Jitter, t_J	V_{DD} =3.0V, USB1 mode (C0 = 0V, C1 = V_{DD}) or USB2 Mode (C0 = V_{DD}, C1 = 0V), R_L = 45Ω, C_L = 10pF, t_R = t_F = 500ps at 480Mbps	25	-	210	-	ps
Rise/Fall Degradation (Propagation Delay), t_{PD}	V_{DD} = 3.0V, USB1 mode (C0 = 0V, C1 = V_{DD}) or USB2 Mode (C0 = V_{DD}, C1 = 0V), R_L = 45Ω, C_L = 10pF, (see Figure 7)	25	-	250	-	ps
Audio Crosstalk R to COM-, L to COM+	V_{DD} = 3.0V, Audio Mode (C0 = V_{DD}, C1 = V_{DD}), R_L = 32Ω, f = 20Hz to 20kHz, V_R or V_L = 0.707V_{RMS}, (see Figure 6)	25	-	-88	-	dB
Crosstalk (Audio to USB, USB to Audio)	V_{DD} = 3.0V, R_L = 50Ω, f = 100kHz	25	-	-98	-	dB
OFF-Isolation	V_{DD} = 3.0V, R_L = 50Ω, f = 100kHz	25	-	95.5	-	dB
Audio OFF-Isolation (All OFF Mode)	V_{DD} = 3.0V, C0 = 0V, C1 = 0V, R_L = 32Ω, f = 20Hz to 20kHz	25	-	115	-	dB
Audio OFF-Isolation (Mute Mode)	V_{DD} = 3.0V, C1 = V_{DD} , C0 = 0V, R_L = 32Ω, f = 20Hz to 20kHz	25	-	105	-	dB
Audio OFF-Isolation (Mute Mode)	V_{DD} = 3.0V, C1 = V_{DD} , C0 = 0V, R_L = 20kΩ, f = 20Hz to 20kHz	25	-	77	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{DD} = 3.0V, C0 = V_{DD}, C1 = V_{DD}, L or R = 0.707V_{RMS} ($2V_{P-P}$), R_L = 32Ω	25	-	0.045	-	%

Electrical Specifications - 2.7V to 3.6V Supply Test Conditions: V_{DD} = +3.0V, GND = 0V, V_{C0H}, V_{C1H} = 1.4V, V_{C0L}, V_{C1L}= 0.5V, (Note 11), Unless Otherwise Specified. Boldface limits apply over the operating temperature range, -40°C to +85°C.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 12, 13)	TYP	MAX (Notes 12, 13)	UNITS
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{DD} = 3.0V, C0 = V_{DD}, C1 = V_{DD}, 5mW into R_L = 32Ω	25	-	0.025	-	%
Click and Pop	V_{DD} = 3.3V, Audio Mute (C0 = 0V, C1 = 0V), R_L =1kΩ, L or R = 0 to 1.25V DC step or 1.25V to 0V DC step, (see Figure 8)	25	-	75	-	µVp
Click and Pop	V_{DD} = 3.3V, C0, C1 = 0.5Hz Square Wave, R_L = 1kΩ, L or R = AC coupled to ground, (see Figure 9)	25	-	520	-	µVp
USB Switch -3dB Bandwidth	Signal = 0dBm, 0.2VDC offset, R_L = 50Ω, C_L = 5pF	25	-	700	-	MHz
Audio Switch -3dB Bandwidth	Signal = 0dBm, R_L = 50Ω, C_L = 5pF	25	-	330	-	MHz
1D+/1D- OFF Capacitance, C_{1D+OFF}, C_{1D-OFF}	f = 1MHz, V_{DD} = 3.0V, C0 = V_{DD}, C1 = V_{DD}, V_{D-} or V_{D+} = V_{COMx} = 0V (see Figure 5)	25	-	3	-	pF
L/R OFF Capacitance, C_{LOFF}, C_{ROFF}	f = 1MHz, V_{DD} = 3.0V, C0 = 0V, C1 = V_{DD}, L or R = COMx = 0V (see Figure 5)	25	-	5	-	pF
2D+/2D- OFF Capacitance, C_{2D+OFF}, C_{2D-OFF}	f = 1MHz, V_{DD} = 3.3V, C0 = V_{DD}, C1 = V_{DD}, Tx or Rx = COMx = 0V (see Figure 5)	25	-	3	-	pF
COM ON Capacitance, $C_{COM-(ON)}$, $C_{COM+(ON)}$	f = 1MHz, V_{DD} = 3.0V, USB1 mode (C0 = 0V, C1 = V_{DD}) or USB2 Mode (C0 = V_{DD}, C1 = 0V) (see Figure 5)	25	-	8	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range, V_{DD}		Full	**2.7**		**4.6**	V
Positive Supply Current, I_{DD} (ALL OFF Mode)	V_{DD} = 3.6V, C1 = GND, C0 = GND	25	-	6.2	10	µA
		Full	-	-	**15**	µA
Positive Supply Current, I_{DD} (USB1 Mode)	V_{DD} = 3.6V, C1 = GND, C0 = V_{DD}	25	-	6.5	10	µA
		Full	-	-	**15**	µA
Positive Supply Current, I_{DD} (USB2 Mode)	V_{DD} = 3.6V, C1 = V_{DD}, C0 = GND	25	-	6.2	10	µA
		Full	-	-	**15**	µA
Positive Supply Current, I_{DD} (Audio Mode)	V_{DD} = 3.6V, C0 = C1 = V_{DD})	25	-	9	14	µA
		Full	-	-	**20**	µA
Positive Supply Current, I_{DD} (MUTE Mode)	V_{DD} = 3.6V, C1 = V_{DD}, C0 = GND	25	-	6.6	10	µA
		Full	-	-	**15**	µA
Power OFF COMx Current, I_{COMx}	V_{DD} = 0V, C0 = C1 = Float, COMx = 5.25V	25	-	-	4	µA
Power OFF Logic Current, I_{C0}, I_{C1}	V_{DD} = 0V, C0 = C1 = 5.25V	25	-	11	-	µA
Power OFF D+/D- Current, I_{XD+}, I_{XD-}	V_{DD} = 0V, C0 = C1 = Float, XD- = XD+ = 5.25V	25	-	5	-	µA
DIGITAL INPUT CHARACTERISTICS						
C0, C1 Voltage Low, V_{C0L}, V_{C1L}	V_{DD} = 2.7V to 3.6V	Full	-	-	**0.5**	V
C0, C1 Voltage High, V_{C0H}, V_{C1H}	V_{DD} = 2.7V to 3.6V	Full	**1.4**	-	**5.25**	V
C0, C1 Input Current, I_{C0L}, I_{C1L}	V_{DD} = 3.6V, C0 = C1= 0V or Float	Full	**-50**	6.2	**50**	nA
C0, C1 Input Current, I_{C0H}, I_{C1H}	V_{DD} = 3.6V, C0 = C1= 3.6V	Full	**-2**	1.6	**2**	µA
C0, C1 Pull-Down Resistor, R_{Cx}	V_{DD} = 3.6V, C0 = C1= 3.6V, Measure current into C0 or C1 pin and calculate resistance value.	Full	-	4	-	MΩ

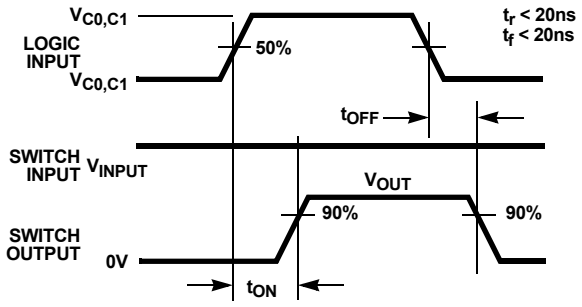
Electrical Specifications - 2.7V to 3.6V Supply Test Conditions: V_{DD} = +3.0V, GND = 0V, V_{C0H}, V_{C1H} = 1.4V, V_{C0L}, V_{C1L}= 0.5V, (Note 11), Unless Otherwise Specified. Boldface limits apply over the operating temperature range, -40°C to +85°C.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 12, 13)	TYP	MAX (Notes 12, 13)	UNITS

NOTES:

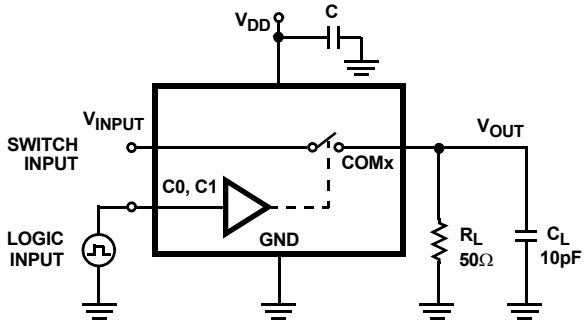
11. V_{LOGIC} = Input voltage to perform proper function.
12. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
13. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
14. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.
15. Limits established by characterization and are not production tested.
16. r_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max r_{ON} value, between L and R or between 1D+ and 1D- or between 2D+ and 2D-.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. ADDRESS t_{TRANS} MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(INPUT)} \frac{R_L}{R_L + r_{ON}}$$

FIGURE 1B. ADDRESS t_{TRANS} TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

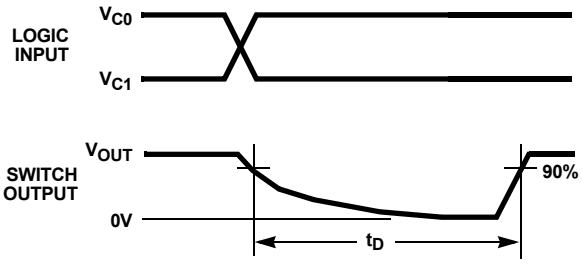
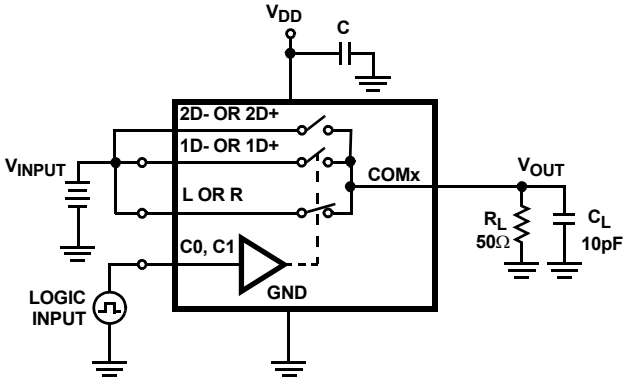


FIGURE 2A. MEASUREMENT POINTS

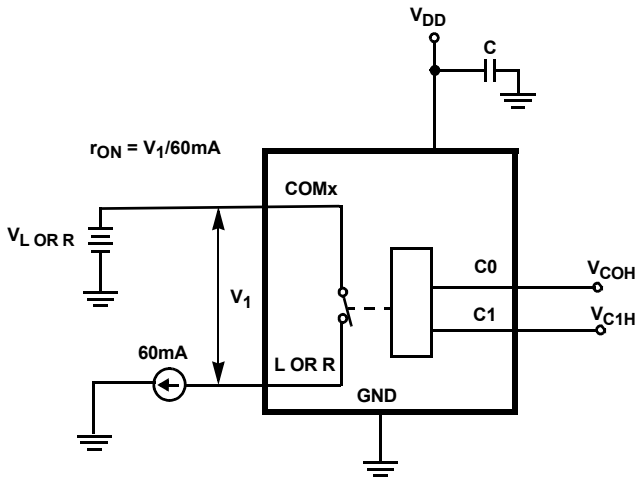


Repeat test for all switches. C_L includes fixture and stray capacitance.

FIGURE 2B. TEST CIRCUIT

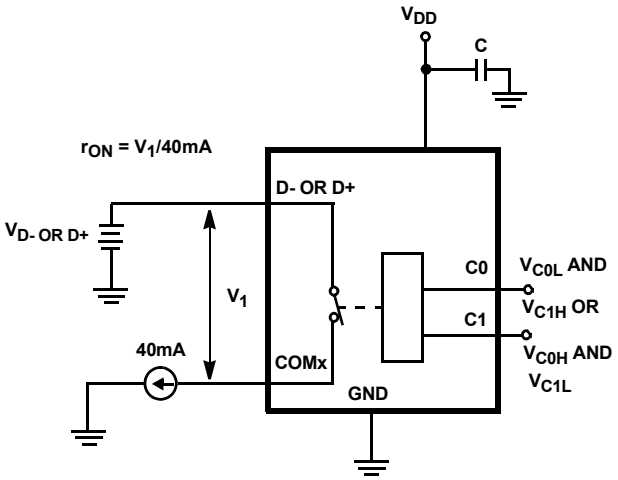
FIGURE 2. BREAK-BEFORE-MAKE TIME

Test Circuits and Waveforms (Continued)



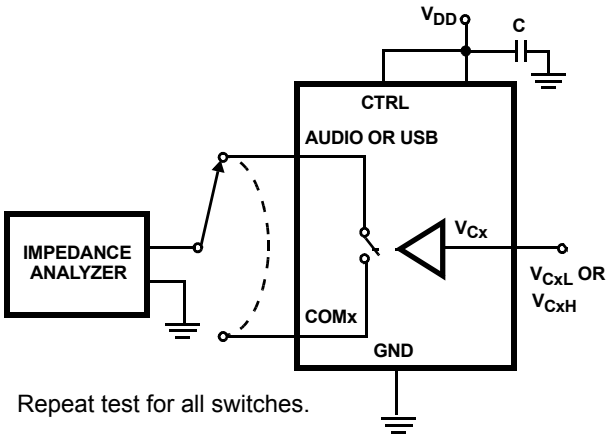
Repeat test for all switches.

FIGURE 3. AUDIO r_{ON} TEST CIRCUIT



Repeat test for all switches.

FIGURE 4. USB r_{ON} TEST CIRCUIT



Repeat test for all switches.

FIGURE 5. CAPACITANCE TEST CIRCUIT

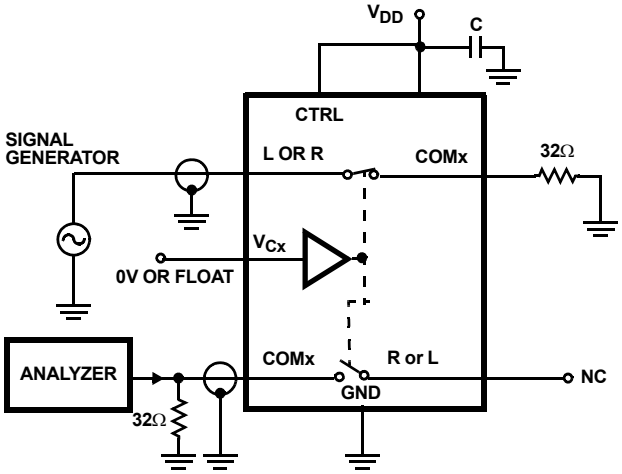


FIGURE 6. AUDIO CROSSTALK TEST CIRCUIT

Test Circuits and Waveforms (Continued)

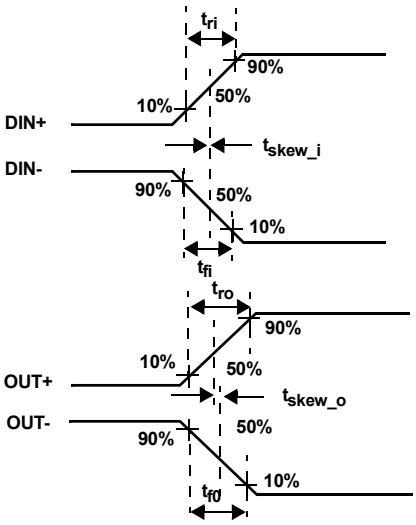
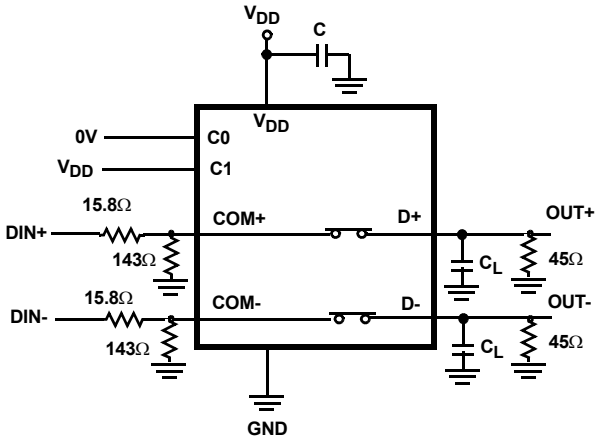


FIGURE 7A. MEASUREMENT POINTS



|tro - tri| Delay Due to Switch for Rising Input and Rising Output Signals.

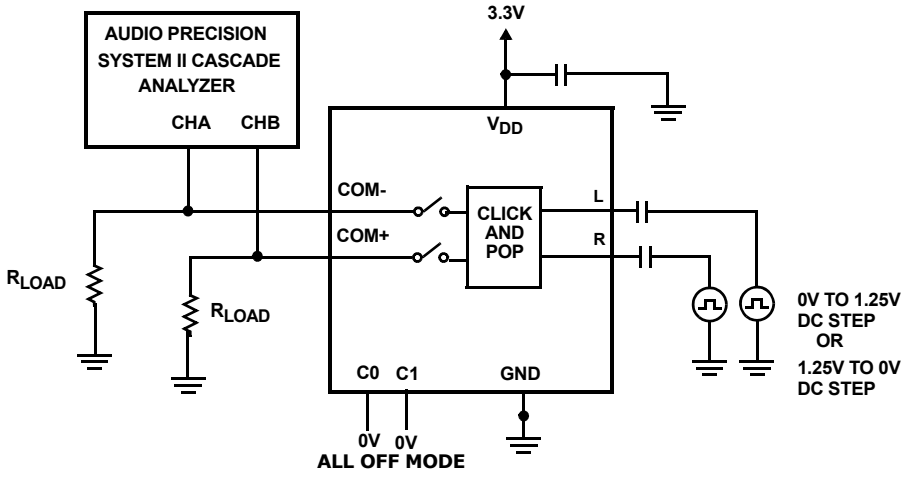
|tfo - tfi| Delay Due to Switch for Falling Input and Falling Output Signals.

|tskew_0| Change in Skew through the Switch for Output Signals.

|tskew_i| Change in Skew through the Switch for Input Signals.

FIGURE 7B. TEST CIRCUIT

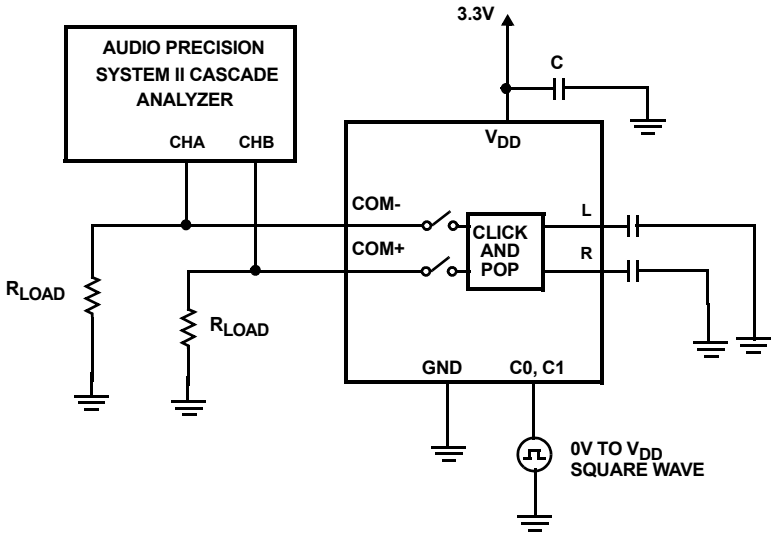
FIGURE 7. SKEW TEST



Set Audio Analyzer for Peak Detection, 32 Samples/Sec, Aweighted Filter, Manual Range 1X/Y, Units to dBV

FIGURE 8. CLICK AND POP TEST CIRCUIT

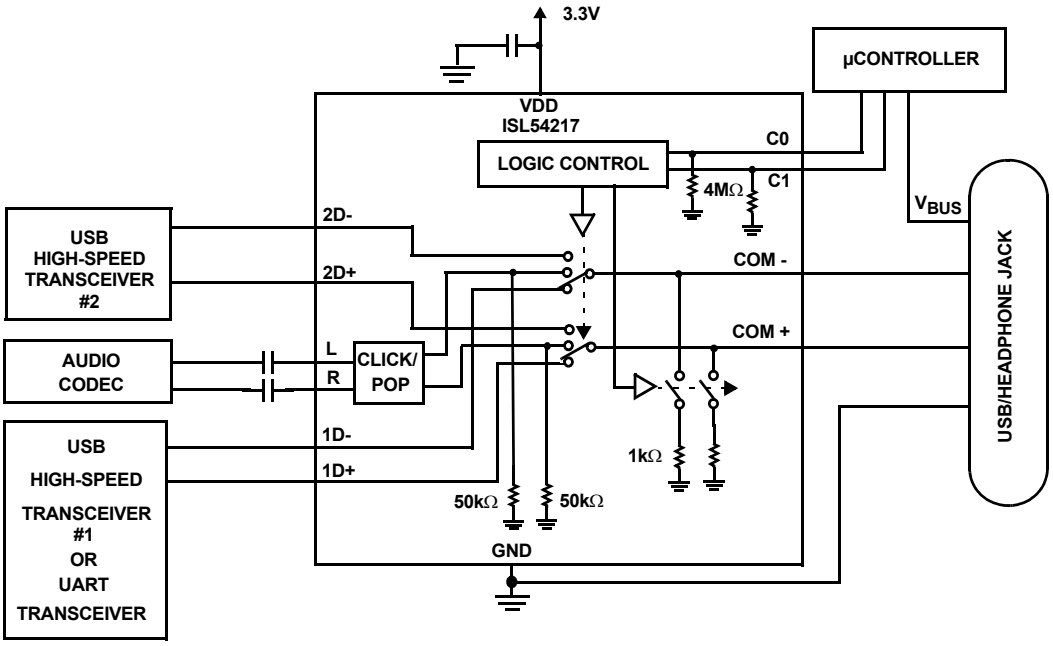
Test Circuits and Waveforms (Continued)



Set Audio Analyzer for Peak Detection, 32 Samples/Sec, Aweighted Filter, Manual Range 1X/Y, Units to dBV

FIGURE 9. CLICK AND POP TEST CIRCUIT

Block Diagram



Detailed Description

The ISL54217 device consists of dual SP3T (single pole/triple throw) analog switches. It operates from a single DC power supply in the range of 2.7V to 4.6V. It was designed to function as differential 3-to-1 multiplexer to select between two different USB differential data signals and audio L and R stereo signals. It comes in a tiny µTQFN and TQFN packages for use in MP3 players, PDAs, cell phones, and other personal media players.

A device consists of two 2.3Ω audio switches and four 6.2Ω USB switches. The audio switches can accept signals that swing below ground. They were designed to pass audio left and right stereo signals, that are ground referenced, with minimal distortion. The USB switches were designed to pass high-speed USB differential data signals with minimal edge and phase distortion.

The ISL54217 was specifically designed for MP3 players, personal media players and cellphone applications that need to combine the stereo audio and USB data channels into a single shared connector, thereby saving space and component cost. The "Block Diagram" of this functionality is shown on page 11.

The ISL54217 contains two logic control pins (C1 and C0) that determine the state of the device. The part has the following five states or modes of operation: All SWITCHES OFF; USB1; USB2; Audio; and Audio Mute. These states are discussed in detail in "Logic Control" on page 12.

A detailed description of the various types of switches are provided in "Audio Switches" beginning on page 12.

Audio Switches

The two audio switches (L, R) are 2.3Ω switches that can pass signals that swing below ground.

Over a signal range of ±1V ($0.707V_{RMS}$) with VDD > 2.7V, these switches have an extremely low r_{ON} resistance variation. They can pass ground referenced audio signals with very low distortion (<0.05% THD+N) when delivering 15.6mW into a 32Ω headphone speaker load. See Figures 20, 21, 22, 23 and 24 THD+N performance curves.

Crosstalk between the L and R audio switches over the frequency range of 20Hz to 20kHz when driving a 32Ω load is <-88dB. These switches have excellent off-isolation >105dB over the audio band when connected to 32Ω loads and 77dB when connected to 20kΩ loads (In Audio Mute mode). See Figures 25 and 26 in "Typical Performance Curves" section beginning on page 14.

The audio drivers should be connected at the L and R side of the switch (pins 2 and 3) and the speaker loads should be connected at the COM side of the switch (pins 7 and 8).

The switches have click and pop circuitry on the L and R side that is activated when the part comes out of Audio mode by taking the C1 and C0 logic pins low (All OFF mode). The ISL54217 should be put in this mode before powering down or powering up of the audio CODEC drivers. In this mode the audio, USB1, USB2 switches will be OPEN (OFF) and the audio click and pop circuitry will be ON. The high off-isolation of the audio switches along with the click and pop circuitry will isolate the transients generated during power-up and power down of the audio CODECs from getting through to the headphones thus eliminating click and pop noise in the headphones. See the "AC COUPLED CLICK AND POP OPERATION" on page 14.

The audio switches are active (turned ON) whenever the C1 and C0 logic pins are logic "1" (High).

USB Switches

The four USB switches (1D+, 1D-, 2D+, 2D-) are 6.2Ω bidirectional switches that were specifically designed to pass high-speed USB differential data signals in the range of 0V to 400mV. The switches have low capacitance and high bandwidth to pass USB high-speed signals (480Mbps) with minimum edge and phase distortion to meet USB 2.0 signal quality specifications. See Figures 27 and 28 for High-speed Eye Pattern taken with switch in the signal path.

These switches can also swing rail to rail and pass USB full-speed signals (12Mbps) with minimal distortion. See Figure 29 for Full-speed Eye Pattern taken with switch in the signal path.

The maximum normal operating signal range for the USB switches is from -1V to V_{DD}. The signal voltage at D- and D+ should not be allow to exceed the V_{DD} voltage rail or go below ground by more than -1V for normal operation.

However, in the event that the USB 5.25V V_{BUS} voltage were shorted to one or both of the COM pins, the ISL54217 has fault protection circuitry to prevent damage to the ISL54217 part. The fault circuitry allows the signal pins (COM-, COM+, 1D-, 1D+, 2D-, 2D+, L and R) to be driven up to 5.25V while the V_{DD} supply voltage is in the range of 0V to 4.6V. This fault condition causes no stress to the IC. In addition, when V_{DD} is at 0V (ground) all switches are OFF and the fault voltage is isolated from the other side of the switch. When V_{DD} is in the range of 2.7V to 4.6V the fault voltage will pass through to the output of an active switch channel. Note: During the fault condition normal operation is not guaranteed until the fault condition is removed.

The USB (1D+ and 1D-) switches are active (turned ON) whenever the C1 is logic "0" (Low) and C0 is logic "1" (High). The USB (2D+ and 2D-) switches are active (turned ON) whenever the C1 is logic "1" (High) and C0 is logic "0" (Low) provided the last state was not the Audio or Audio Mute state.

ISL54217 Operation

The discussion that follows will discuss using the ISL54217 in the "Block Diagram" on page 11.

LOGIC CONTROL

The state of the ISL54217 device is determined by the voltage at the C1 pin (pin 9) and the C0 pin (pin 10). The part has five states or modes of operation. The All SWITCHES OFF mode, USB1 mode, USB2 mode, Audio mode and Audio Mute mode. Refer to "Truth Table" on page 3 and "State Diagram" on page 2 of data sheet.

The C1 pin and C0 pin are internally pulled low through 4MΩ resistors to ground and can be tri-stated or left floating.

The C1 pin and C0 pin can be driven with a voltage that is higher than the V_{DD} supply voltage. They can be driven up to 5.25V with the V_{DD} supply in the range of 2.7V to 4.6V. Driving the logic higher than the supply rail will cause the logic current to increase. With V_{DD} = 2.7V and V_{LOGIC} = 5.25V, I_{LOGIC} current is approximately 5.5µA.

Logic Control Voltage Levels

With VDD in the range of 2.7V to 3.6V the logic levels are:
C1, C0 = Logic "0" (Low) when ≤ 0.5V or Floating.
C1, C0 = Logic "1" (High) when ≥ 1.4V.

ALL SWITCHES OFF Mode

If the C1 pin = Logic "0" and C0 pin = Logic "0" the part will be in the ALL SWITCHES OFF mode. In this mode the 2D- and 2D+ USB switches, the L and R audio switches and the 1D- and 1D+ USB switches will be OFF (high impedance).

The audio click and pop shunt circuitry will be activated (ON) and the 1kΩ COM shunt resistors will be disconnected (OFF).

Before powering down or powering up of the audio CODECs drivers the ISL54217 should be put in the ALL SWITCHES OFF mode. In this mode transients present at the L and R signal pins due to the changing DC voltage of the audio drivers will not pass to the headphones, preventing clicks and pops in the headphones. See the "AC COUPLED CLICK AND POP OPERATION" on page 14.

It is recommended that when transitioning from USB1 to USB2 or from USB2 to USB1 that you always pass through the All Switches OFF state.

Audio Mode

If the C1 pin = Logic "1" and C0 pin = Logic "1" the part will be in the Audio mode. In Audio mode the L (left) and R (right) 2.3Ω audio switches are ON. The 1D- and 1D+ 6.2Ω USB switches and 2D- and 2D+ 6.2Ω USB switches will be OFF (high impedance).

The audio click and pop circuitry is de-activated. The 1kΩ shunts on the COM side of the switch will be disconnected (OFF).

When a headphone is plugged into the common connector, the µcontroller will drive the C1 and C0 logic pins "High" putting the part in the audio mode. In the audio mode, the audio drivers of the player can drive the headphones and play music.

USB1 Mode

If the C1 pin = Logic "0" and C0 pin = Logic "1" the part will go into USB1 mode. In USB1 mode the 1D- and 1D+ 6.2Ω switches are ON. The L and R 2.3Ω audio switches and 2D- and 2D+ 6.2Ω USB switches will be OFF (high impedance).

The audio L and R click and pop shunt circuitry will be activated and the 1kΩ COM shunt resistors will be disconnected (OFF).

When a USB cable from a computer or USB hub is connected at the common connector, the µcontroller will route the incoming USB signal to USB transceiver section #1 by taking the C1 pin "Low" and the C0 pin "High" putting the ISL54217 part into the USB1 mode. In USB1 mode the computer or USB hub transceiver and the MP3 player or cellphone USB transceiver #1 are connected and digital data will be able to be transmit back and forth.

USB2 Mode

If the C1 pin = Logic "1" and C0 pin = Logic "0" the part will be in the USB2 mode provided that the last state was not the Audio or Audio Mute state. In the USB2 mode the 2D- and 2D+ 6.2Ω USB switches will be ON and audio switches and the 1D- and 1D+ USB switches will be OFF (high impedance).

The audio L and R click and pop shunt circuitry will be activated and the 1kΩ COM shunt resistors will be disconnected (OFF).

When a USB cable from a computer or USB hub is connected at the common connector, the µcontroller will route the incoming USB signal to USB transceiver section #2 by taking the C1 pin "High" and the C0 pin "Low" putting the ISL54217 part into the USB2 mode. In USB2 mode the computer or USB hub transceiver and the MP3 player or cellphone USB transceiver #2 are connected and digital data will be able to be transmit back and forth.

Audio MUTE Mode

If the C1 pin = Logic "1" and C0 pin = Logic "0" the part will be in the Audio MUTE mode provided that the last state was the Audio state. In the audio MUTE mode the 2D- and 2D+ USB switches, the L and R audio switches and the 1D- and 1D+ USB switches will be OFF (high impedance).

The audio click and pop shunt circuitry will be de-activated and the 1kΩ COM shunt resistors will be connected (ON). Note: 1kΩ COM shunt resistors are only ON when in Audio MUTE mode.

The 1kΩ shunts provide 77dB of off-isolation when driving 10kΩ to 20kΩ amplifier inputs.

Logic Control Timing Between C1 and C0

The ISL54217 has a unique logic control architecture. The part has five different logic states but only two external logic control pins, C1 and C0. Refer to "State Diagram" on page 2 and "Truth Table" on page 3.

The following state transitions require both C1 and C0 logic control bits to change their logic levels in unison:
All OFF(C1 = 0, C0 = 0) -----> Audio (C1 = 1, C0 =1)
Audio (C1 = 1, C0 = 1) -----> All OFF (C1 = 0, C0 = 0)
Audio Mute (C1 = 1, C0 = 0) ---> USB1 (C1 = 0, C0 = 1)

The delay time between transition of these bits must be <100ns to ensure that you directly move between these states without momentarily transitioning to one of the other states.

For example, if you are going from the "All OFF" state to the "Audio" state and C0 does not go high until 100ns after C1 went high you will momentarily transition to the "USB2" state. Any signals connected at the USB2 signal lines will momentarily get passed through to the COM outputs.

Delay time between C1 and C0 must be <100ns and should be controlled by logic control drivers with well behaved monotonic transitions from High to Low and Low to High and with typical logic family rise and fall times of 1ns to 6ns.

POWER

The power supply connected at VDD (pin 11) provides power to the ISL54217 part. Its voltage should be kept in the range of 2.7V to 4.6V. In a typical application, V_{DD} will be in the range of 2.7V to 4.3V and will be connected to the battery or LDO of the MP3 player or cellphone.

A 0.01µF or 0.1µF decoupling capacitor should be connected from the VDD pin to ground to filter out any power supply noise from entering the part. The capacitor should be located as close to the VDD pin as possible.

Before power-up and power-down of the ISL54217 part, the C1 and C0 control pins should be driven to ground or tri-stated. This will put the switch in the ALL SWITCHES OFF state, which turns all switches OFF and activate the click and pop circuitry. This will minimize transients at the speaker loads during power-up and power-down of the ISL54217 device. See Figure 32 in the "Typical Performance Curves" section.

AC COUPLED CLICK AND POP OPERATION

Single supply audio drivers have their signal biased at a DC offset voltage, usually at 1/2 the DC supply voltage of the driver. As this DC bias voltage comes up or goes down during power-up or power-down of the driver, a transient can be coupled into the speaker load through the DC blocking capacitor (see the "Block Diagram" on page 11).

When a driver is OFF and suddenly turned ON the rapidly changing DC bias voltage at the output of the driver will cause an equal voltage at the input side of the switch due to the fact that the voltage across the blocking capacitor cannot change instantly. If the switch is in the Audio mode or there is no low impedance path to discharge the blocking capacitor voltage, before turning the audio switch ON, a transient discharge will occur in the speaker, generating a click/pop noise.

Proper elimination of a click/pop transient at the speaker loads while powering up or down of the audio drivers requires that the ISL54217 have its click/pop circuitry activated by putting the part in the ALL SWITCHES OFF mode. This allows the transients generated by the audio drivers to be discharged through the click and pop shunt circuitry.

Once the driver DC bias has reached VDD/2 and the transient on the switch side of the DC blocking capacitor has been discharged to ground through the click/pop shunt circuitry, the audio switches can be turned ON and connected through to the speaker loads without generating any undesirable click/pop noise in the speakers.

With a typical DC blocking capacitor of 220µF and the click/pop shunt circuitry designed to have a resistance of 20Ω to 70Ω, allowing a 100ms wait time to discharge the transient before placing the switch in the Audio mode will prevent the transient from getting through to the speaker load. See Figures 30 and 31 in the "Typical Performance Curves" section.

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified

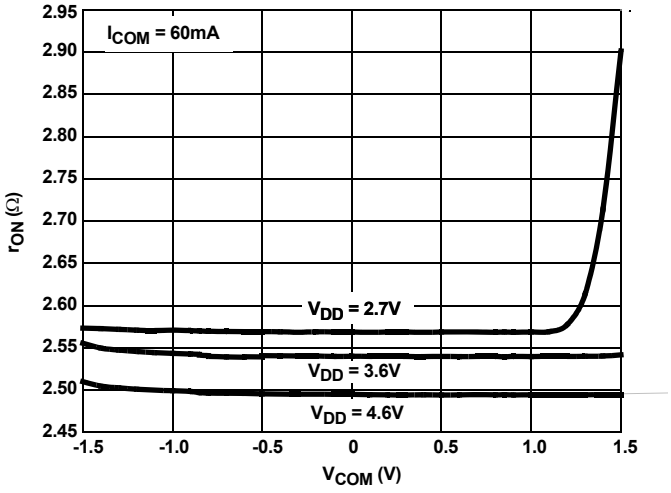


FIGURE 10. AUDIO ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

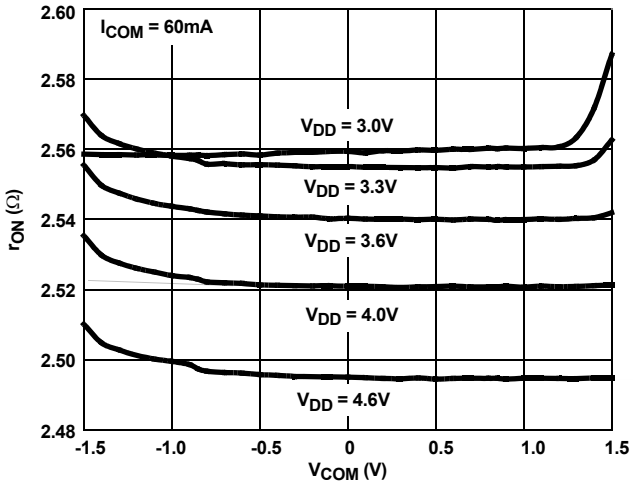


FIGURE 11. AUDIO ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

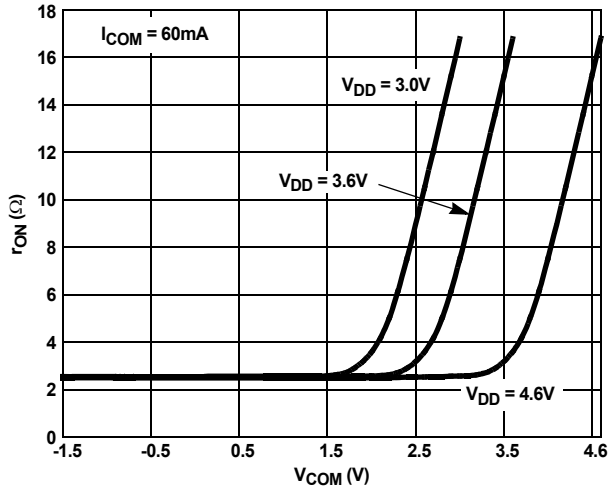


FIGURE 12. AUDIO ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

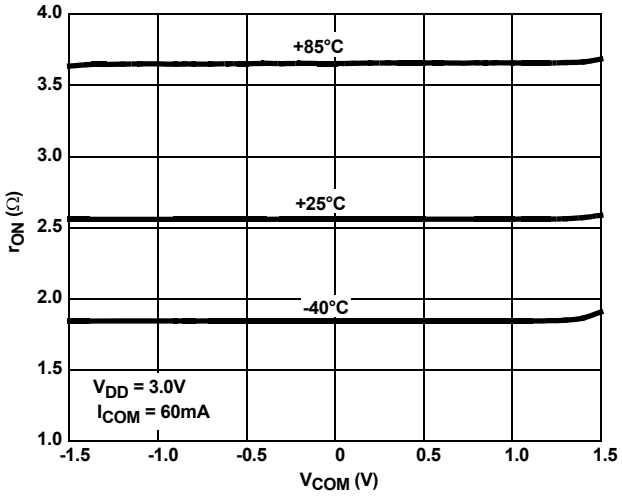


FIGURE 13. AUDIO ON-RESISTANCE vs SWITCH VOLTAGE vs TEMPERATURE

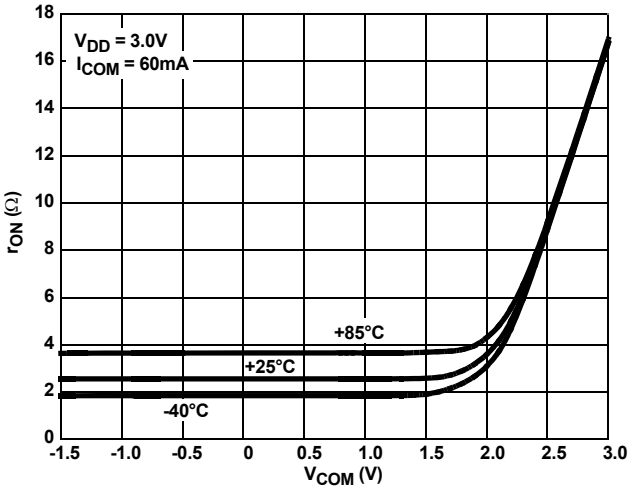


FIGURE 14. AUDIO ON-RESISTANCE vs SWITCH VOLTAGE vs TEMPERATURE

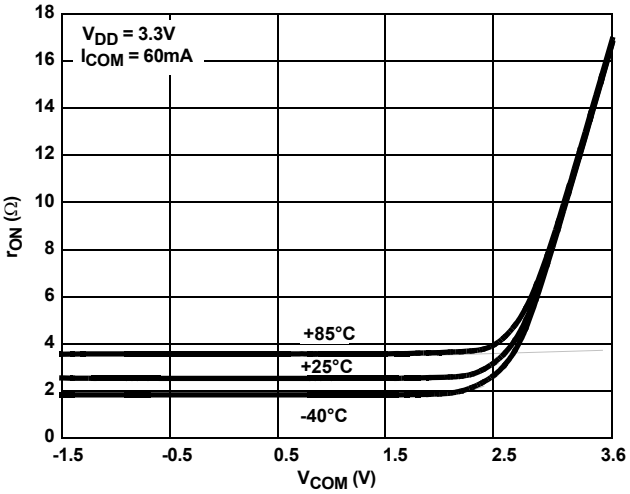


FIGURE 15. AUDIO ON-RESISTANCE vs SWITCH VOLTAGE vs TEMPERATURE

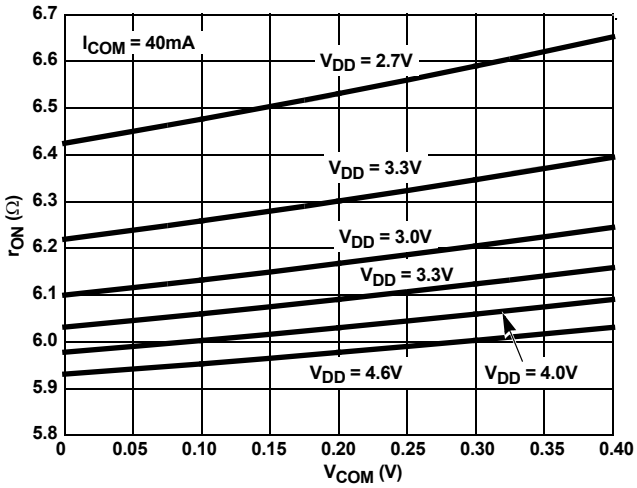


FIGURE 16. USB ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

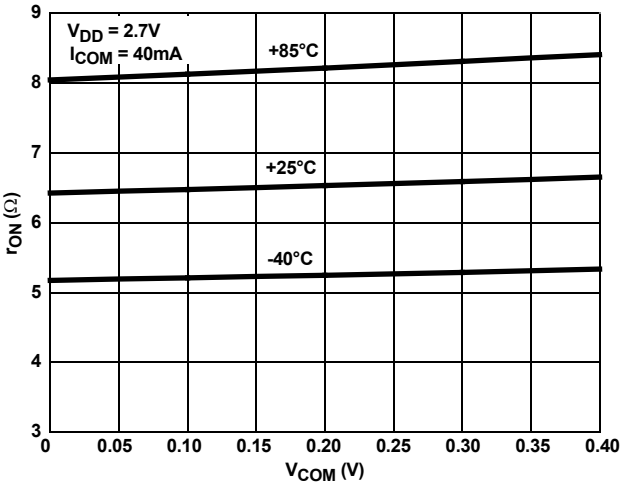


FIGURE 17. USB ON-RESISTANCE vs SWITCH VOLTAGE vs TEMPERATURE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

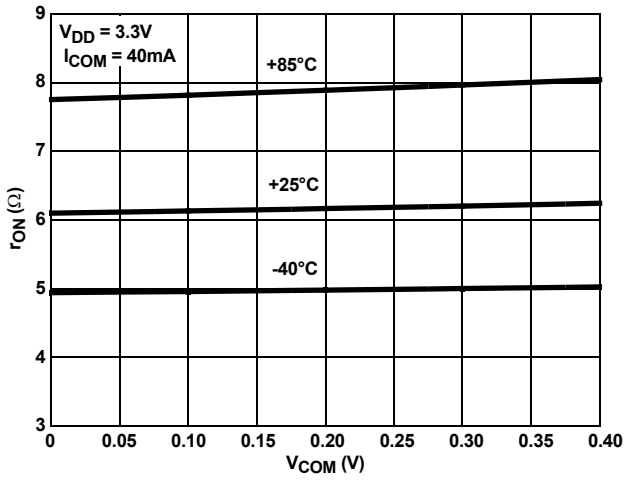


FIGURE 18. USB ON-RESISTANCE vs SWITCH VOLTAGE vs TEMPERATURE

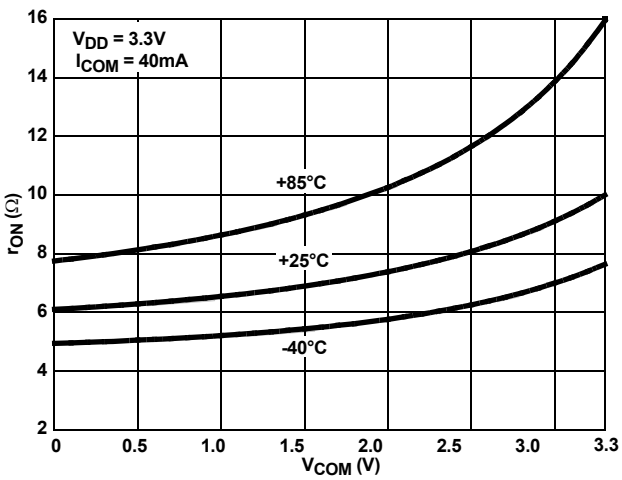


FIGURE 19. USB ON-RESISTANCE vs SWITCH VOLTAGE vs TEMPERATURE

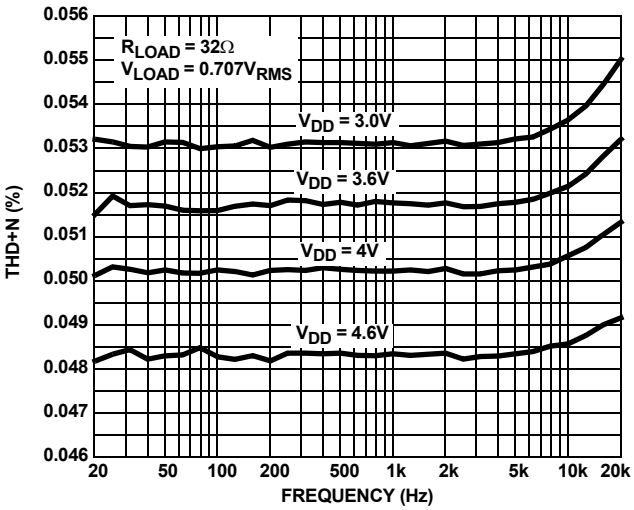


FIGURE 20. THD+N vs SUPPLY VOLTAGE vs FREQUENCY

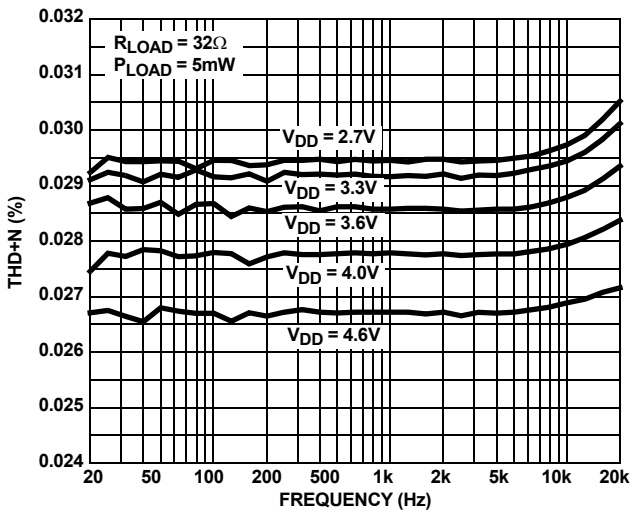


FIGURE 21. THD+N vs SUPPLY VOLTAGE vs FREQUENCY

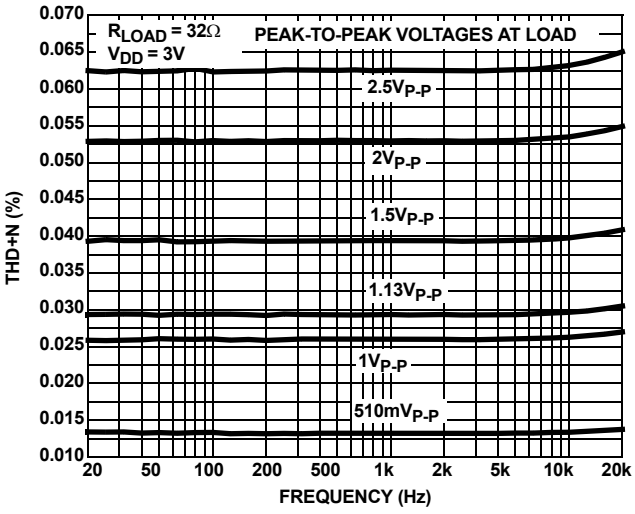


FIGURE 22. THD+N vs SIGNAL LEVELS vs FREQUENCY

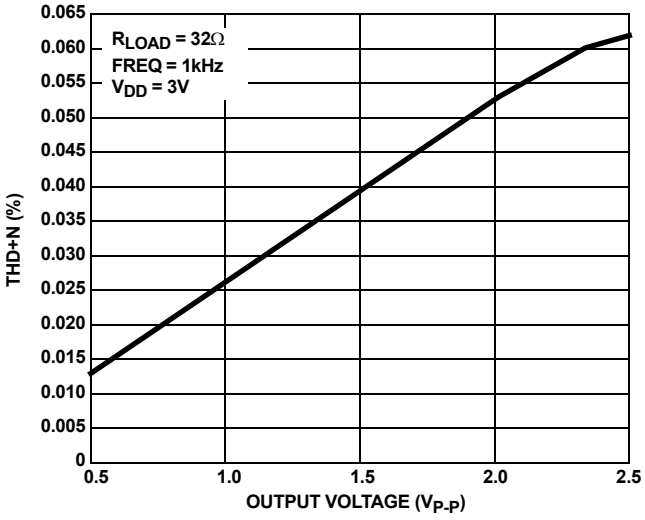


FIGURE 23. THD+N vs OUTPUT VOLTAGE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

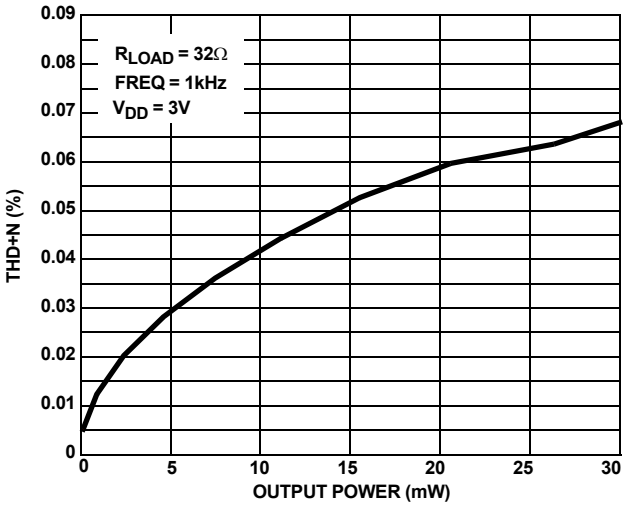


FIGURE 24. THD+N vs OUTPUT POWER

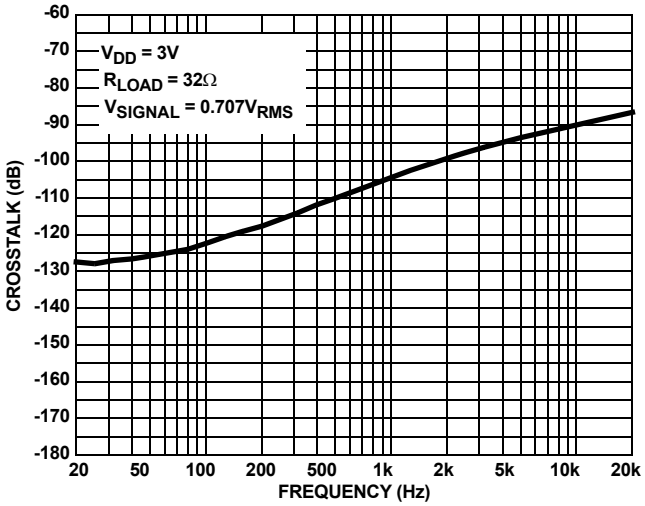


FIGURE 25. AUDIO CHANNEL-TO-CHANNEL CROSSTALK

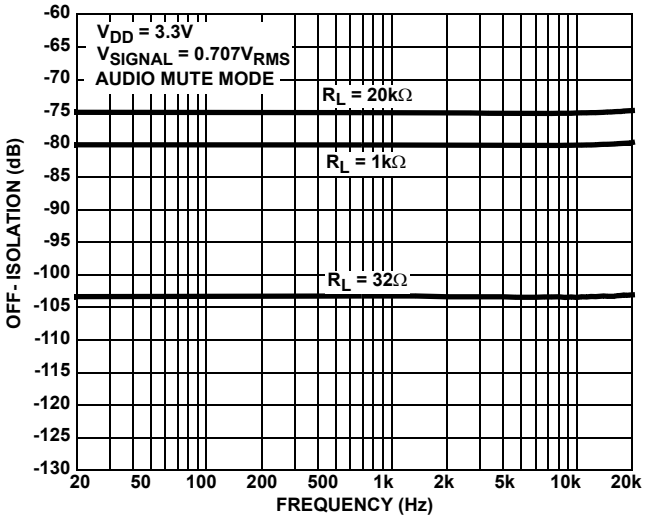


FIGURE 26. OFF-ISOLATION AUDIO SWITCH vs LOADING vs FREQUENCY

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

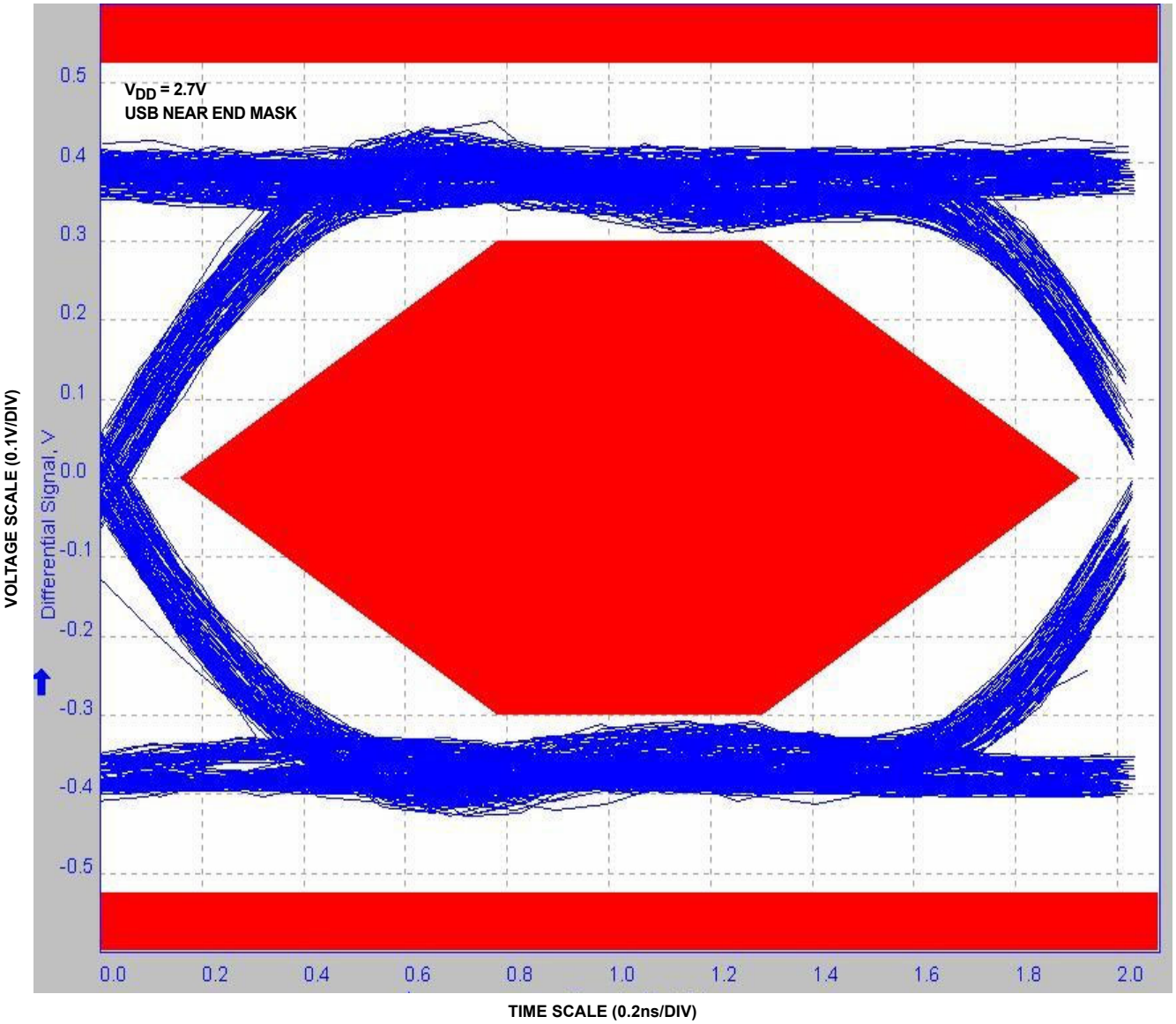


FIGURE 27. EYE PATTERN: 480Mbps WITH USB SWITCHES IN THE SIGNAL PATH

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

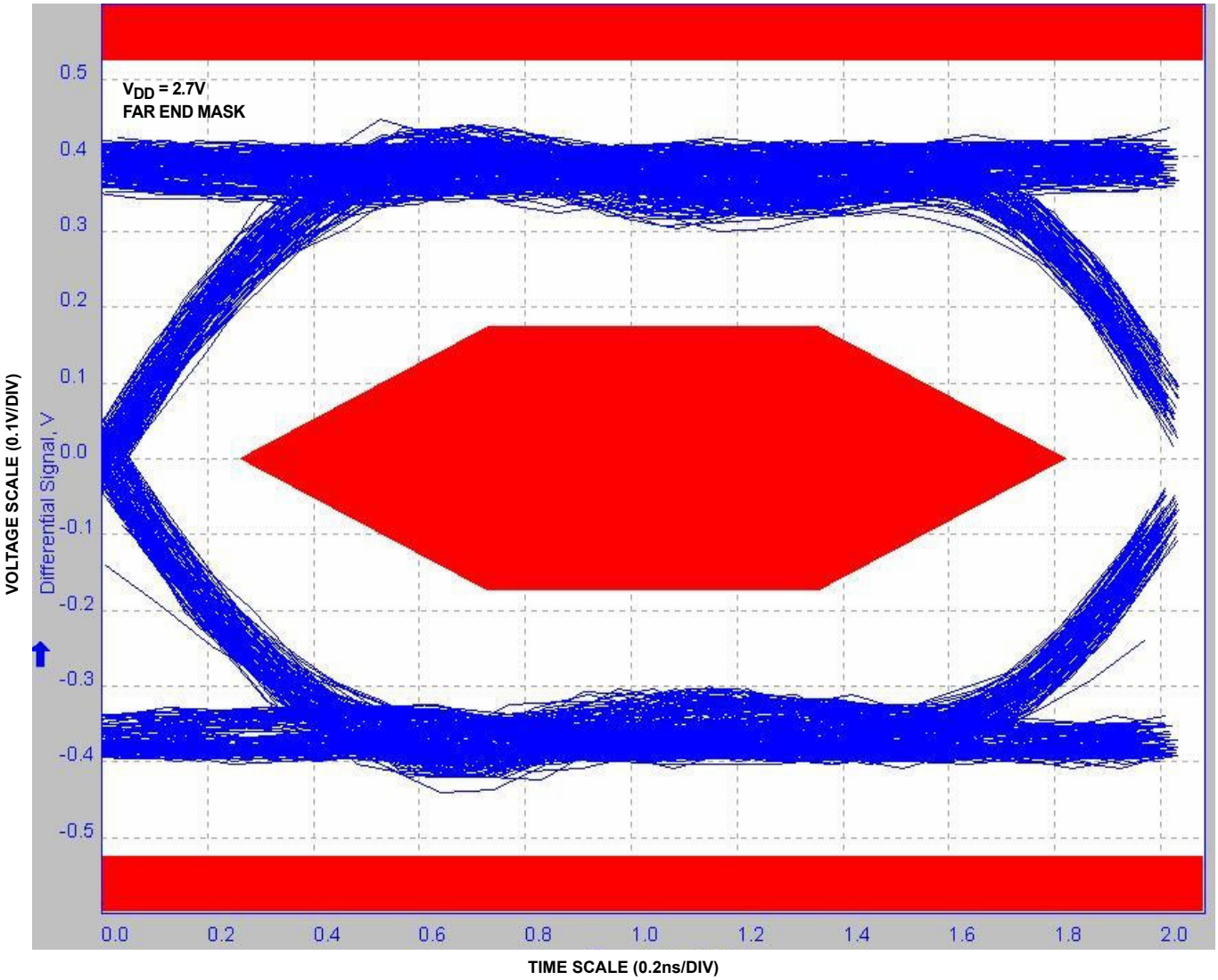


FIGURE 28. EYE PATTERN: 480Mbps WITH USB SWITCHES IN THE SIGNAL PATH

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

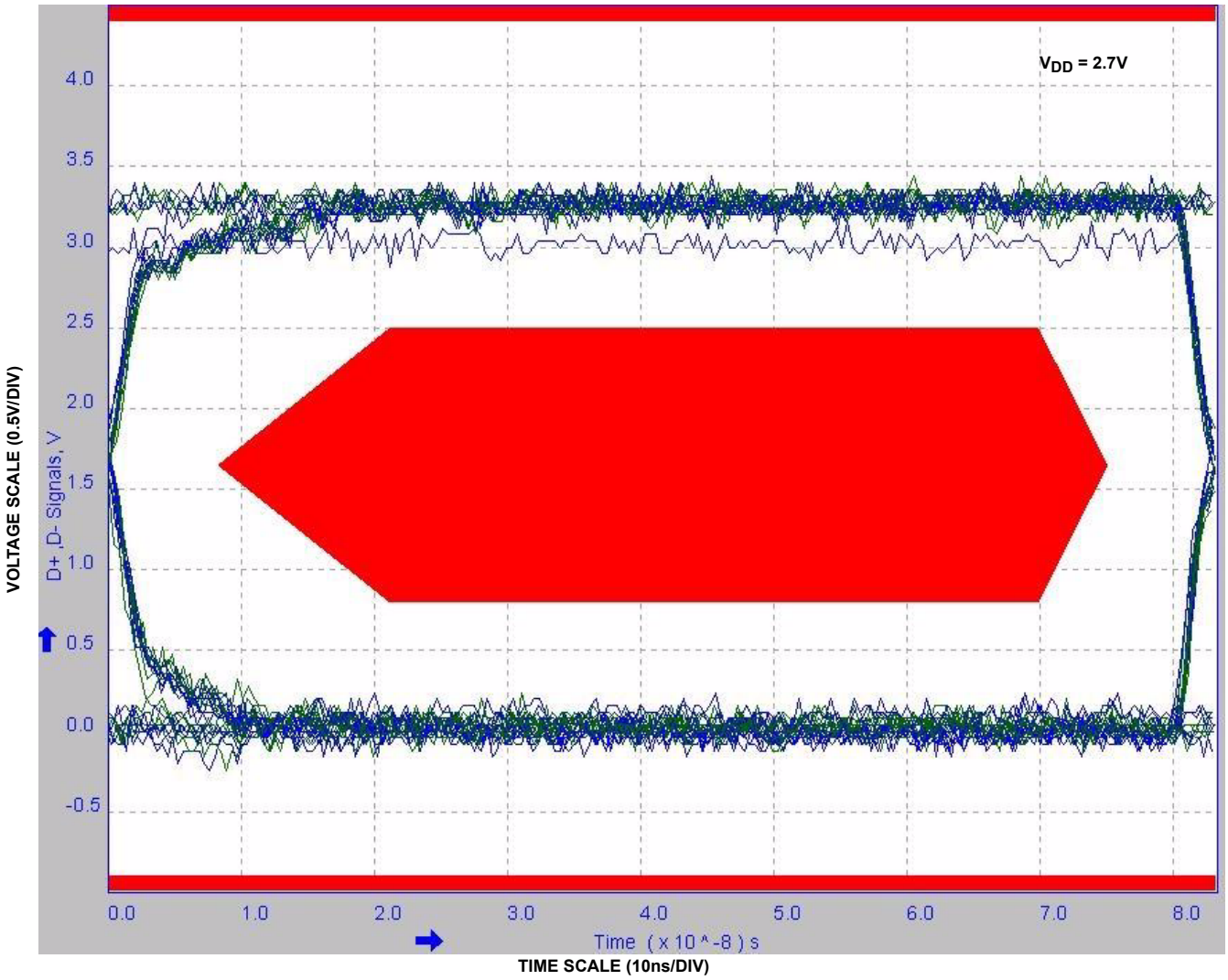


FIGURE 29. EYE PATTERN: 12Mbps USB SIGNAL WITH USB SWITCHES IN THE SIGNAL PATH

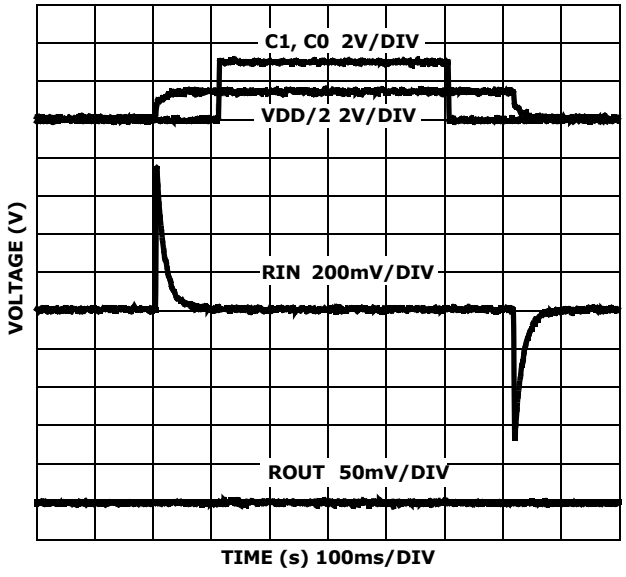


FIGURE 30. 32Ω AC COUPLED CLICK/POP REDUCTION

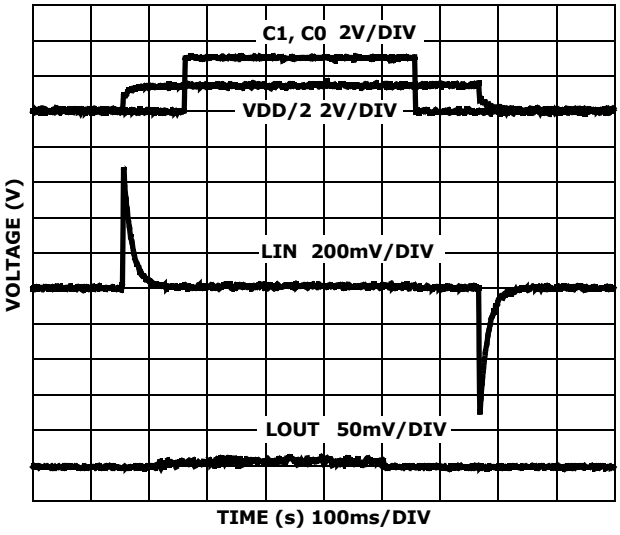


FIGURE 31. 1kΩ AC COUPLED CLICK/POP REDUCTION

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

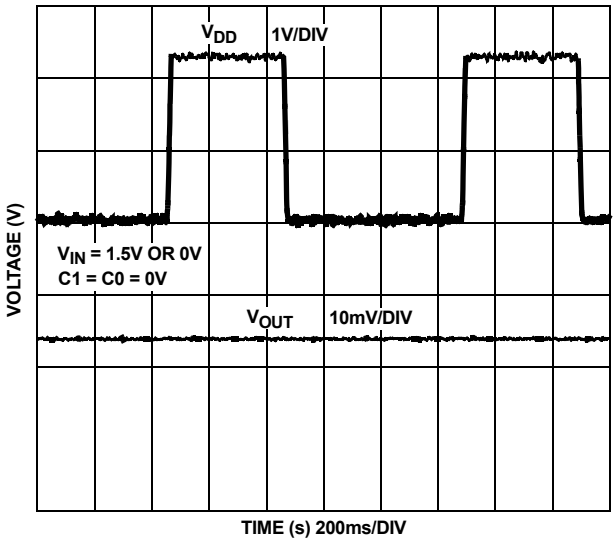


FIGURE 32. POWER-UP/POWER-DOWN CLICK AND POP TRANSIENT

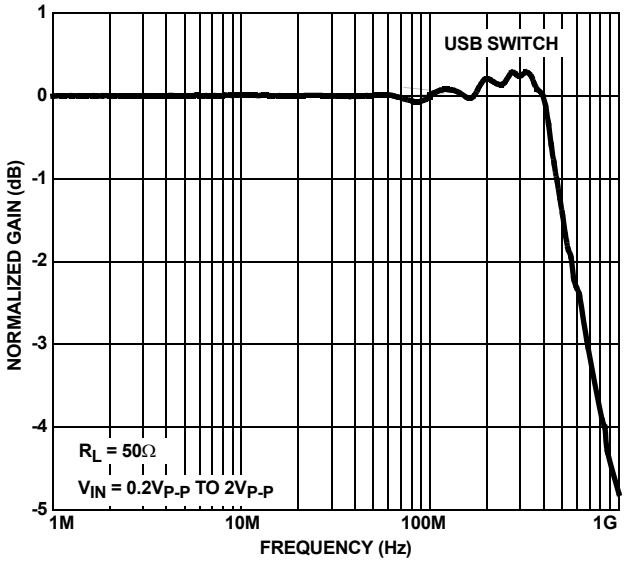


FIGURE 33. FREQUENCY RESPONSE

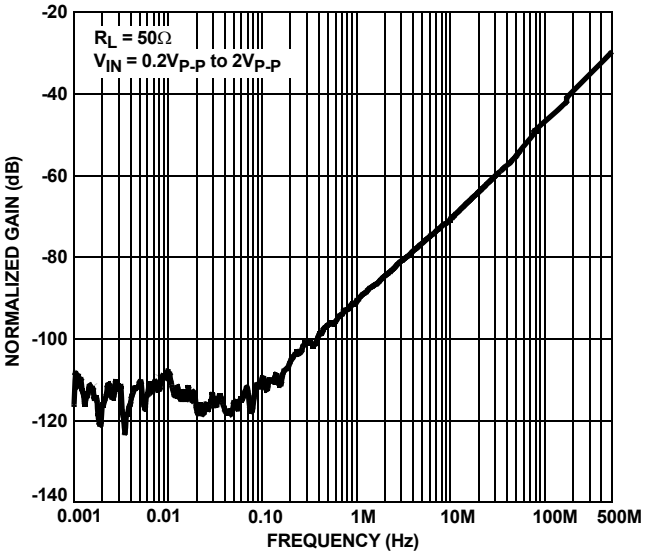


FIGURE 34. OFF-ISOLATION USB SWITCHES

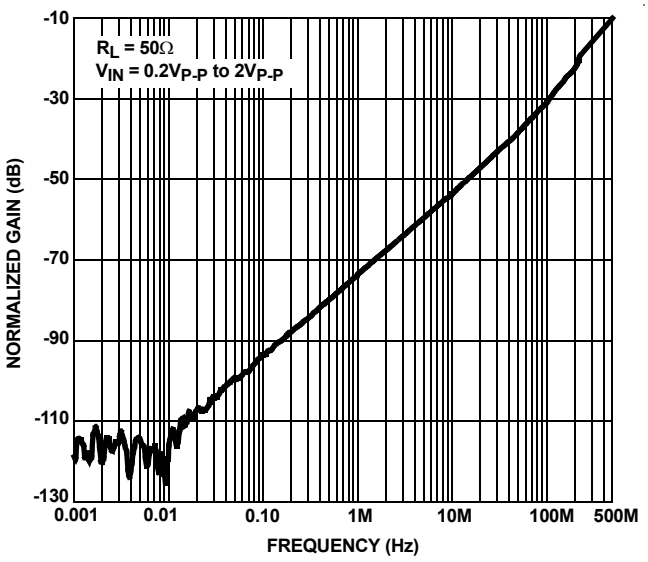


FIGURE 35. OFF-ISOLATION AUDIO SWITCHES

Die Characteristics

SUBSTRATE AND TQFN THERMAL PAD POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT

837

PROCESS

Submicron CMOS

Revision History

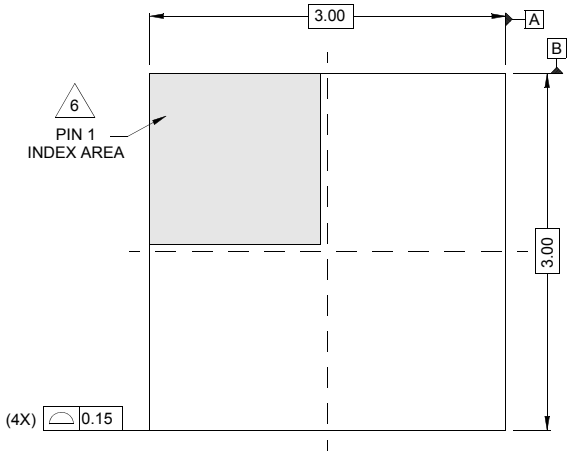
DATE	REVISION	CHANGE
Dec 12, 2018	FN6817.5	Updated ordering information table. Removed Products section. Updated disclaimer.
Apr 28, 2010	FN6817.4	On page 2 , added separate pin configuration diagrams for the µTQFN and TQFN parts. On page 7, changed “Positive Supply Current, IDD” MAX for “(ALL OFF Mode)”,“(USB1 Mode)”, “(USB2 Mode)”, and “(MUTE Mode)” for 25°C from:8µA, to 10µA. On page 7, changed “Power OFF COMx Current, ICOMx” current limit for 25°C from:1µA, to:4µA. Converted to new Intersil template. Changes include: Added Note 5 to “Ordering Information” on page 4. On page 3 in “Pin Descriptions”, updated to show the thermal pad. “Absolute Maximum Ratings” on page 5, added latch-up level. Added “Products” section. Added “Revision History”.
May 4, 2009	FN6817.3	On page 7, under Parameter “Power OFF D+/D- Current, IXD+, IXD-”, changed units from "nA" to "µA"
Apr 1, 2009	FN6817.2	“Absolute Maximum Ratings” on page 5, changed C0,C1... From "-0.3 to (VDD) + 0.3V" to "-0.3V to 5.5V" “Power OFF COMx Current, ICOMx” on page 7 max limit changed from "100nA" to "1µA" “Power OFF Logic Current, IC0, IC1” on page 7 added typ "11µa", deleted max limit of "550nA" “Power OFF D+/D- Current, IXD+, IXD-” on page 7, added typ "5µa", deleted max limit of "500nA" Under - “DIGITAL INPUT CHARACTERISTICS” on page 7 For “C0, C1 Voltage High, VC0H, VC1H” Parameter with test conditions of VDD = 2.7V to 3.6V, Full temp range; added a MAX spec of 5.25V Added “Logic Control” on page 12.
Feb 27, 2009	FN6817.1	Removed Off_isolation Left Audio Switch vs Loading curve (was Figure 26)
Dec 11, 2008	FN6817.0	Initial release

Package Outline Drawings

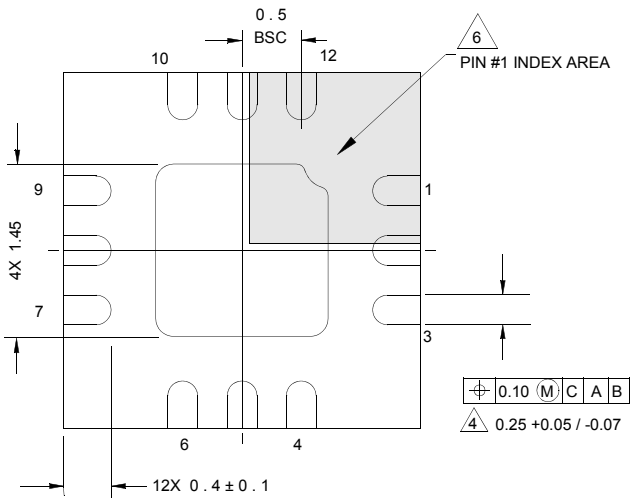
For the most recent package outline drawing, see L12.3x3A.

L12.3x3A

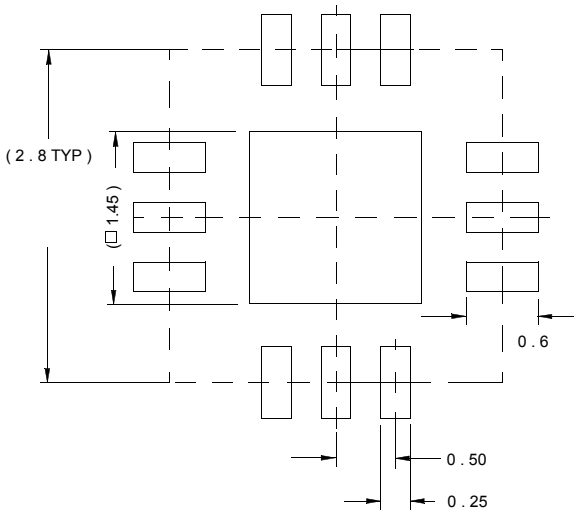
12 LEAD THIN QUAD FLAT NO LEAD PLASTIC PACKAGE
Rev 0, 09/07



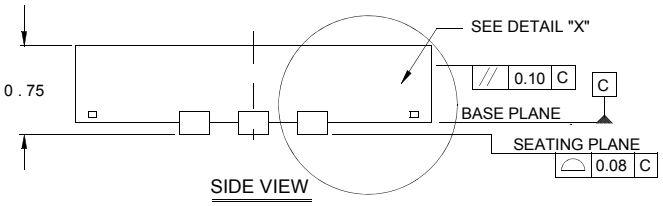
TOP VIEW



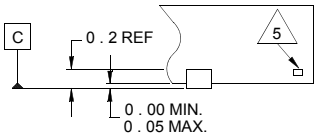
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

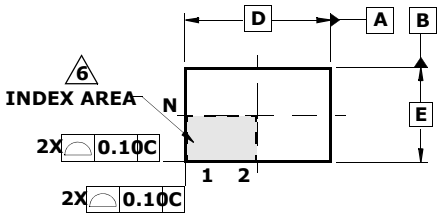
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

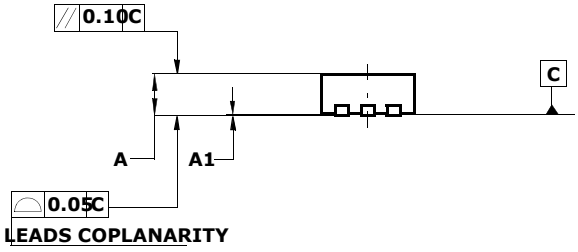
For the most recent package outline drawing, see L12.2.2x1.4A.

L12.2.2x1.4A

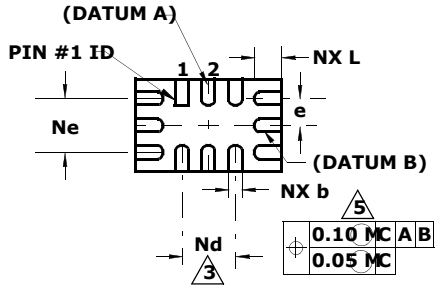
12 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE (UTQFN)



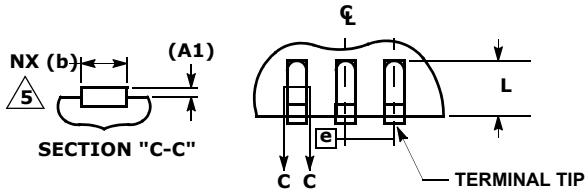
TOP VIEW



SIDE VIEW



BOTTOM VIEW



SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3		0.127 REF		-
b	0.15	0.20	0.25	5
D	2.15	2.20	2.25	-
E	1.35	1.40	1.45	-
e		0.40 BSC		-
k	0.20	-	-	-
L	0.35	0.40	0.45	-
N		12		2
Nd		3		3
Ne		3		3
θ	0	-	12	4

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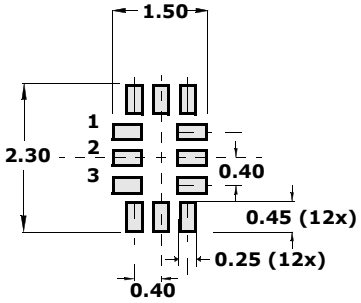
NOTES:

17. Dimensioning and tolerancing conform to ASME Y14.5-1994.
18. N is the number of terminals.
19. Nd and Ne refer to the number of terminals on D and E side, respectively.
20. All dimensions are in millimeters. Angles are in degrees.
21. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
22. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
23. Maximum package warpage is 0.05mm.
24. Maximum allowable burrs is 0.076mm in all directions.
25. Same as JEDEC MO-255UABD except:
    No lead-pull-back, "A" MIN dimension = 0.45 not 0.50mm
    "L" MAX dimension = 0.45 not 0.42mm.
26. For additional information, to assist with the PCB Land Pattern Design effort, see TB389.



TYPICAL RECOMMENDED LAND PATTERN 10

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