ADS8472EVM

This user guide describes the characteristics, operation, and use of the ADS8472 16-bit, 1MHz parallel interface analog-to-digital converter evaluation board. A complete circuit description as well as schematic diagram and bill of materials is included.

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1.1 Features

- Full-featured Evaluation Board for the high-speed ADS8472 16-bit, 1MSPS single channel, parallel interface SAR type Analog to Digital Converters.
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- Input and Output Digital Buffers
- On board decoding for stacking multiple EVMs.

1.2 Related Documentation from Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. When ordering, identify this booklet by its title and literature number. Updated documents can also be obtained through our website at www.ti.com.

Data Sheets:	Literature Number:
ADS8472	SLAS514
REF3240	SBVS058
REF3225	SBVS058
SN74AHC138	SCLS258
SN74AHC245	SCLS230
SN74AHC1G04	SCLS318
THS4031	SLOS224
THS4032	SLOS224

2 Introduction

The ADS8472 is 16-bit, 1-MSPS analog to digital converter (ADC) with an internal 4.096V reference and a pseudo-bipolar, fully differential input. The device is a capacitor based successive approximation register (SAR) converter with an inherent sample and hold. The ADS8472 has a 16-bit and 8-bit parallel interface bus options, allowing a variety of processors to interface easily with it.

The ADS8472EVM is an evaluation and demonstration platform for the ADS8472 ADC. The board is a flexible design that allows the user to choose among many different analog signal conditioning, reference and interface modes. The standardized I/O headers not only allow the user to quickly interface to FPGAs, but also to the full line of microprocessors and digital signal processors from Texas Instruments.

3 Analog Interface

The analog-to-digital converter accepts a pseudo-bipolar differential input. A pseudo-bipolar differential signal is a fully differential signal that has a common-mode voltage such that the voltage on each input is always equal to or above zero volts. The common mode voltage should typically be half the reference voltage. The peak-to-peak amplitude on each input leg can be as large as the reference voltage.

The positive leg of the input signal can be applied at connector P1 pin 2 (shown in Table 1) or via center pin of SMA connector J1. Likewise the negative input signal can be applied at P1 pin1 or via center pin of SMA connector J2.

Table 1. Analog Input Connector

Description	Signal Name	Connector.Pin#		Signal Name	Description
Inverting Input Channel	—	P1.1	P1.2	+	Non-inverting Input Channel
Reserved	N/A	P1.3	P1.4	N/A	Reserved
Reserved	N/A	P1.5	P1.6	N/A	Reserved
Reserved	N/A	P1.7	P1.8	N/A	Reserved
Reserved	N/A	P1.9	P1.10	N/A	Reserved
Pin tied to Ground	AGND	P1.11	P1.12	N/A	Reserved
Pin tied to Ground	AGND	P1.13	P1.14	N/A	Reserved
N/A	Reserved	P1.15	P1.16	N/A	Reserved
Pin tied to Ground	AGND	P1.17	P1.18	N/A	Reserved
Pin tied to Ground	AGND	P1.19	P1.20	REF+	External Reference Input

3.1 Input Signal Conditioning

The analog input circuitry, consisting of the THS4031 and THS4032 operational amplifiers, allow the user to install passive components to configure it for positive or negative gains, as well as input range scaling, filtering and leveling translation (e.g., adding a DC offset). The operational amplifiers are housed in an industry standard SOIC footprint. This enables the user to replace the THS4031 with a plethora of dual and single supply amplifiers housed in an SOIC package.

When choosing the driver amplifier the user should consider the following requirements. The driving amplifier must be able to settle the input to 16-bit level within the sample time of the converter. It should have Total Harmonic Distortion(THD) characteristics comparable to or better than the ADS8472. Lastly, the noise generated by the amplifier needs to be as low as possible, so as not to degrade the SNR performance of the ADS8472.

The noise coming through the driver amplifiers are filtered by a single-pole filter using R = 10.2Ω and C= 2.2nF with a corner frequency of 7MHz. The 5.1-Ωseries resistor works with the capacitor to filter the input signal, but also isolates the amplifier from the capacitive load. The 2200-pF capacitor to ground at the input of the ADC works with the series resistor to filter the input signal, behaves like a charge reservoir, and provides a path to ground for high-frequency noise and the low small input current transient which occurs when the device switches from hold to sample mode. This external filter capacitor works with the amplifier to charge the internal sampling capacitor during sampling mode.

The supplies to the input amplifier are selectable with solder jumper pad SJP3, and SJP4. Shorting across pads 1 and 2 will ground the negative rail. Shorting across pads 2 and 3 will tie the negative supply of the amplifiers to the voltage applied at node –VCC.

When deciding on supply rails, a good rule of thumb is to add at least 2V of head room on either side to achieve optimal performance. For example, if the signal applied to the amplifier is 0–4V, then the amplifier rails should be at least –2V and +6V. At the 16-bit performance node, the amplifier introduced distortion can become significant. Be aware when reading amplifiers data sheets that they may not be specified with large amplitudes. Therefore, it may not be possible to surmise from a cursory glance how well the amplifier will behave in system.

Single-ended signal sources are readily available, but rarely allow the user to evaluate the full performance of 16-bit converters. Although the ADS8472EVM can be configured for this input configuration, the factory set configuration of the input circuitry is for a bipolar fully differential input signal. The necessary DC component to offset the signal at U7 is generated by U4. U4 is the low noise THS4032 amplifier. It can be configured to further filter the reference voltage IC, U2, and provide positive or negative gains. The ADS8472EVM leaves the factory with potentiometer, R24, set to 2.048V and set as shown in Figure 1. Table 1 indicates how the solder pad jumpers should be set to select from the various supply and input options for the analog driver circuitry. The copy of the schematic for the ADS8472EVM is attached at the end of this document.

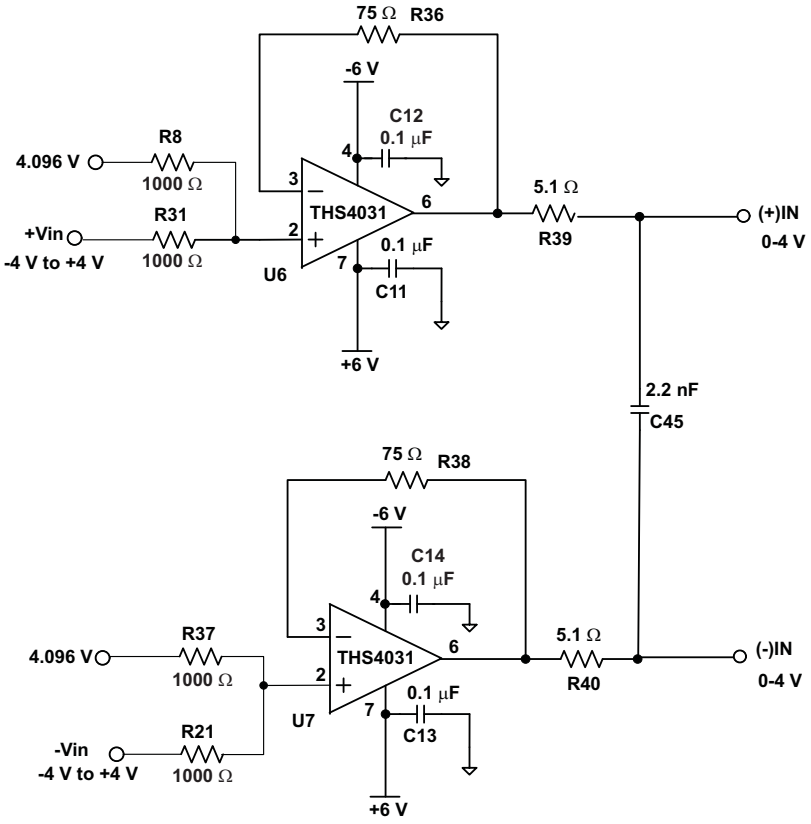


Figure 1. Input Buffer, Bipolar Fully Differential Input

Table 2. Analog Circuitry Jumper Configurations

Reference Designator	1-2	2-3	Description
SJP1	Installed†(1)	Not Installed	Select onboard reference (REF3230).
	Not Installed	Installed	Select user-supplied reference at P1 pin 20.
SJP2	Installed†(1)	Not Installed	Set REFIN pin of ADS8472 to on-chip (internal) reference voltage.
	Not Installed	Installed	Set REFIN pin of ADS8472 to reference selected by SJP1.
SJP3	Installed	Not Installed	Set U6 operational amplifier minus rail supply to ground.
	Not Installed	Installed†(1)	Set U6 operational amplifier minus rail supply to –VCC.
SJP4	Installed	Not Installed	Set U7 operational amplifier minus rail supply to ground.
	Not Installed	Installed†(1)	Set U7 operational amplifier minus rail supply to –VCC.
SJP5	Not Installed	N/A	Short voltage node –DC to U6 pin 2 via R35.
SJP6	Not Installed	N/A	Short –IN pin of U5 to ground at C45.

(1) † Indicates factory installed option.

3.2 Reference

The ADS8472 can operate with an external reference voltage in the range of 3.0V up to 4.2V. It generates an on-chip 4.096V reference voltage. The ADS8472EVM allows the user to select the external reference voltage from three sources. The first option is to use the internally generated 4.096V from the ADC. The other two options are to select from the on board reference (U1) or a user supplied voltage applied at pin 20 of P1. Refer to Table 1 for solder jumper options for selecting from the various reference sources.

The reference voltage provides the scale factor for the conversion result. The input voltage is measured against the reference voltage. It is imperative the reference voltage be clean, low noise and well decoupled.

The default configuration is to use the internal on-chip reference.

4 Digital Interface

The ADS8472EVM is designed for easy interfacing to multiple platforms. The digital interface input and output signals of the converter are on connectors P2, P3, J6 and J7. These are 0.1" on-centers, plug and socket connectors, allowing the user to plug the ADS8472EVM onto the various motherboard interface cards from Texas Instruments, or ribbon cable onto the user development board. The following tables list the connector pin outs.

Table 3. Pinout for Parallel Control Connector P3

Description	Signal Name	Connector.Pin#		Signal Name	Description
Not connected	$\overline{\text{DC\_CS}}$	P3.1	P3.2	+	Non-inverting Input Channel
Reserved	N/A	P3.3	P3.4	GND	Ground
Reserved	N/A	P3.5	P3.6	GND	Ground
Address line 0	A0	P3.7	P3.8	GND	Ground
Address line 1	A1	P3.9	P3.10	GND	Ground
Address line 2	A2	P3.11	P3.12	GND	Ground
Reserved	N/A	P3.13	P3.14	GND	Ground
Reserved	N/A	P3.15	P3.16	GND	Ground
Convert Start	$\overline{\text{DC\_CONVST}}$	P3.17	P3.18	GND	Ground
Interrupt pin	INTC	P3.19	P3.20	GND	Ground

Conversions are initiated on the falling edge of the convert start signal. It is therefore critical when measuring large amplitude and/or high frequency input signals, the user provide a clean low jitter convert start pulse.

The convert start signal can be applied to the ADS8472 from the decoder outputs or from connector P3 pin 17. Address decoder SN74ACH138 is used to generate the read ($\overline{\text{RD}}$) and conversion start ($\overline{\text{CONVST}}$) signals to the converter. Jumpers W3 and W4 allow the user to assign these two signals to different addresses in memory. This allows for the stacking of up to two ADS8472EVMs into processor memory. See Table 3 for jumper settings. If the user applies a convert start signal directly on P3 pin 17, then be sure to short W6 pins 1-2. This will bypass the decoder output selected by position of W4.

Note, the evaluation module does not allow chip select ($\overline{\text{CS}}$) line of the converter to be assigned to different memory locations. It is therefore suggested the $\overline{\text{CS}}$ line be grounded or wired to an appropriate signal of the processor.

Table 4. Jumper Settings

Reference Designator	Description	1-2	2-3
W1	Set digital buffer supply voltage to +5V	Installed	Not installed
	Set digital buffer supply voltage to +3.3V	Not installed	Installed †(1)
W2	Apply inverted BUSY to INTC signal	Installed †(1)	Not installed
	Apply BUSY signal to INTC signal	Not installed	Installed
W3	Set $\overline{\text{RD}}$ signal to add[0x3]	Installed	Not installed
	Set $\overline{\text{RD}}$ signal to add[0x4]	Not installed	Installed
W4	Set $\overline{\text{CONVST}}$ signal to add[0x1]	Installed	Not installed
	Set $\overline{\text{CONVST}}$ signal to add[0x2]	Not installed	Installed

(1) † Indicates factory installed option.

Table 4. Jumper Settings (continued)

Reference Designator	Description	1-2	2-3
W5	Set $\overline{\text{DC\_CS}}$ to $\overline{\text{CS}}$ of ADS8472	Installed	N/A
W6	Set $\overline{\text{DC\_CONVST}}$ to $\overline{\text{CONVST}}$ of ADS8472	Installed	Installed
	Set decoder output to $\overline{\text{CONVST}}$ of ADS8472	Not installed	Installed

The data bus is available at connector P2, see Table 4 for pin out information.

Table 5. Data Bus Connector P2

Description	Signal Name	Connector.Pin#		Signal Name	Description
Reserved	N/A	P2.1	P2.2	GND	Ground
Reserved	N/A	P2.3	P2.4	GND	Ground
Data Bit 0	DB0	P2.5	P2.6	GND	Ground
Data Bit 1	DB1	P2.7	P2.8	GND	Ground
Data Bit 2	DB2	P2.9	P2.10	GND	Ground
Data Bit 3	DB3	P2.11	P2.12	GND	Ground
Data Bit 4	DB4	P2.13	P2.14	GND	Ground
Data Bit 5	DB5	P2.15	P2.16	GND	Ground
Data Bit 6	DB6	P2.17	P2.18	GND	Ground
Data Bit 7	DB7	P2.19	P2.20	GND	Ground
Data Bit 8	DB8	P2.21	P2.22	GND	Ground
Data Bit 9	DB9	P2.23	P2.24	GND	Ground
Data Bit 10	DB10	P2.25	P2.26	GND	Ground
Data Bit 11	DB11	P2.27	P2.28	GND	Ground
Data Bit 12	DB12	P2.29	P2.30	GND	Ground
Data Bit 13	DB13	P2.31	P2.32	GND	Ground
Data Bit 14	DB14	P2.33	P2.34	GND	Ground
Data Bit 15	DB15	P2.35	P2.36	GND	Ground

In addition to interfacing to the various micro controller and digital signal processors from Texas Instruments, this board also plugs into the TSW1100 card. The TSW1100 is a PC-based data capture card. J7 connector is installed to allow the user to plug the ADS8472EVM directly and collect data for analysis.

Table 6. TSW1100 Connector

Description	Signal Name	Connector.Pin#		Signal Name	Description
Ground	Ground	J7.1	J7.2	N/C	Not Connected
Ground	Ground	J7.3	J7.4	N/C	Not Connected
Ground	Ground	J7.5	J7.6	D0	Data Bit 0 (LSB)
Ground	Ground	J7.7	J7.8	D1	Data Bit 1
Ground	Ground	J7.9	J7.10	D2	Data Bit 2
Ground	Ground	J7.11	J7.12	D3	Data Bit 3
Ground	Ground	J7.13	J7.14	D4	Data Bit 4
Ground	Ground	J7.15	J7.16	D5	Data Bit 5
Ground	Ground	J7.17	J7.18	D6	Data Bit 6
Ground	Ground	J7.19	J7.20	D7	Data Bit 7
Ground	Ground	J7.21	J7.22	D8	Data Bit 8
Ground	Ground	J7.23	J7.24	D9	Data Bit 9
Ground	Ground	J7.25	J7.26	D10	Data Bit 10

Table 6. TSW1100 Connector (continued)

Description	Signal Name	Connector.Pin#		Signal Name	Description
Ground	Ground	J7.27	J7.28	D11	Data Bit 11
Ground	Ground	J7.29	J7.30	D12	Data Bit 12
Ground	Ground	J7.31	J7.32	D13	Data Bit 13
Ground	Ground	J7.33	J7.34	D14	Data Bit 14
Ground	Ground	J7.35	J7.36	D15	Data Bit 15
Ground	Ground	J7.37	J7.38	N/C	Not Connected
Ground	Ground	J7.39	J7.40	INTc	**Trigger Clock**

This evaluation module provides direct access to all the analog-to-digital converter input control and output signals via connector J6, see Table 6.

Table 7. Pin out for Converter Control Connector, J6

Description	Signal Name	Connector.Pin#		Signal Name	Description
Chip Select Signal	$\overline{CS}$	J6.1	J6.2	GND	Ground
Read Signal	$\overline{RD}$	J6.3	J6.4	GND	Ground
Convert Start Signal	$\overline{CONVST}$	J6.5	J6.6	GND	Ground
Byte Signal	BYTE	J6.7	J6.8	GND	Ground
RESERVED	RESERVED	J6.9	J6.10	GND	Ground
Busy Signal	BUSY	J6.11	J6.12	GND	Ground

5 Power Supplies

The EVM accepts four power supplies.

- A dual ±VA DC supply for the dual supply op-amps. Recommend ±6VDC supply.
- A single +5.0 V DC supply for analog section of the board (A/D + Reference).
- A single +5.0V or +3.3V DC supply for digital section of the board (A/D + address decoder + buffers).

There are two ways to provide these voltages.

1. Wire in the voltages at test points on the EVM. See Table 8.

Table 8. Power Supply Test Points

Test Point	Signal	Description
TP6	+BVDD	Apply +3.3VDC or +5.0VDC. See ADC datasheet for full range.
TP3	+AVCC	Apply +5.0VDC.
TP4	+VA	Apply +6.0VDC. Positive supply for amplifier.
TP5	–VA	Apply -6.0VDC. Negative supply for amplifier.

2. Use the power connector J5, and derive the voltages elsewhere. The pinout for this connector is shown in Table 9. If using this connector, then set W1 jumper to connect +3.3VD or +5VD from connector to +BVDD. Short between pins 1-2 to select +5VD, or short between pins 2-3 to select +3.3VD as the source for the digital buffer voltage supply (+BVDD).

Table 9. Power Connector, J5, Pin Out

Signal	Power Connector – J5		Signal
+VA(+6V)	1	2	–VA (-6V)
+5VA	3	4	N/C
DGND	5	6	AGND
N/C	7	8	N/C
+3.3VD	9	10	+5VD

6 Using the ADS8472EVM

The ADS8472EVM serves the functions of being a reference design, a prototyping board, and finally as an software test platform.

6.1 As a Reference Board

As a reference design, the ADS8472EVM contains the essential circuitry to showcase the analog-to-digital converter. This essential circuitry includes the input amplifier, reference circuit, and buffers. The ADS8472EVM analog input circuit is optimized for a wide bandwidth signal; therefore, the user may need to adjust the input buffer circuitry to better suit your needs. In AC-type applications where signal distortion is a concern, the user should use high quality capacitors such as Mica, polypropylene or COGs type capacitors in the signal path. In applications where the input is multiplexed, the A/D input resistor and capacitor may need to be adjusted further.

6.2 As a Prototype Board

As a prototype board, the ADS8472EVM features amplifiers in a standard 8-pin SOIC package and many resistor pads scattered around allowing the user to experiment with a host of circuits, as needed. The ADS8472EVM can be used to evaluate both dual- and single-supply amplifiers in both inverting and non-inverting configurations. The ADS8472EVM comes installed with a dual-supply amplifier which allows the user to take advantage of the full input voltage range of the converter. For applications that require signal supply operation and smaller input voltage range, the THS4031 can be replaced with the single-supply amplifier like the OPA300 or OPA350. Pad jumper SJP3 should be shorted between pads 1 and 2. This shorts the minus supply pin of the amplifier to ground. Positive supply voltage can be applied at test point TP4 or at connector J5 pin 1.

6.2.1 Evaluation Board

There are two common methods to evaluate the ADS8472EVM's performance.

1. EVM used as a stand-alone system. The user is responsible for capturing and analyzing the data, typically via a logic analyzer and analysis software (LABView, MATLAB, etc)
2. EVM used in conjunction with TI's TSW1100 data capture card, http://focus.ti.com/docs/toolsw/folders/print/tsw1100.html

The following section discusses method two.

6.2.2 EVM and TSW1100 Capture Card

The User's Guide for the data capture card is available at http://focus.ti.com/lit/ug/slau155a/slau155a.pdf. Refer to this guide for detailed information and set-up instructions.

The ADS8472EVM mates with the TSW1100 card via J7. There are two data ports available on the capture card, the reference designators are J1 and J2. The ADS8472EVM can be plugged into either port.

The TSW1100 is a data capture card and provides no control signals to the ADS8472. The ADS8472 requires a $\overline{\text{CONVST}}$ pulse to begin digitizing the signal. Therefore, the user must provide a $\overline{\text{CONVST}}$ to the ADS8472 at P3 pin 17 or at J6 pin 5 on the ADS8472EVM. In this case, it is recommended the ADS8472 be operated in the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ tied low mode, as this requires only $\overline{\text{CONVST}}$ to toggle. To short this signals to ground, simply short across pins 1 and 2, and 3 and 4 of J6, respectively. The digitized data is available on the data bus at the end of every busy cycle. In this operating scheme, the inverted BUSY signal is used to trigger the TSW1100 card to read the data bus. To avoid line contention remove jumpers from W3, W4, W5, and W6 on the ADS8472EVM.

The ADS8472 EVM is supported with the TSW1100 capture card firmware release 1.x. Please use the ADS1610EVM entry as a template for acquiring data from the ADS8374EVM. Due to hardware limitations on the TSW1100 platform, data capture from the ADS8472EVM is restricted to 1MSPS minimum.

6.3 As a Software Test Platform

As a software test platform, connectors P1, P2, and P3 plug into the parallel interface connectors of the 5-6K interface board. The 5-6K interface board sits on the C5000 and C6000 digital signal processor starter kits (DSK). The ADS8472EVM is mapped then into the processor's memory space. The 5-6k interface board also provides an area for signal conditioning. This area can be used to install application circuit(s) for digitization by the ADS8472 analog-to-digital converter. For more information, see the 5-6K Interface Board user's guide (SLAU104) .

For the software engineer, the ADS8472EVM provides a simple platform for interfacing to the converter. The EVM provides standard 0.1-inch headers and sockets to wire into prototype boards. The user need only provide three address lines (A2, A1, and A0) and address valid line ($\overline{DC\_CS}$) to connector P3. To select which address combinations generate $\overline{RD}$ and $\overline{CONVST}$, set jumpers as shown in Table 3. Recall that the Chip Select ($\overline{CS}$) signal is not memory-mapped; therefore, it must be controlled by a general-purpose pin or shorted to ground at J6 pin 1. If address decoding is not required, the EVM provides direct access to converter data bus by P3 and control by J6.

7 ADS8472EVM BoM

The following table contains a complete Bill of Materials for the ADS8472EVM. The schematic diagram is also provided for reference. Contact the Product Information Center or e-mail dataconvapps@list.ti.com for questions regarding this EVM.

Table 10. Bill of Materials

QTY	Value	REF DES	Footprint	MFG	MFG Part No.	Description
3	0	R16 R17 R33	603	Panasonic – ECG or Alternate	ERJ-3GEY0R00V	RES 0Ω 1/16W 5% 0603 SMD
2	0	R19 R22	805	Panasonic – ECG or Alternate	ERJ-6GEY0R00V	RES 0.0 Ω 1/10W 5% 0805 SMD
2	5.1	R39 R40	805	Panasonic – ECG or Alternate	ERJ-6GEYJ5R1V	Resistor 5.1Ω 1/8W 5% 0805
3	33	R5 R25 R26	603	Yageo America or Alternate	9C06031A33R0FKHFT	RES 33.0Ω 1/10W 1% 0603 SMD
3	49.9	R1–R3	603	Panasonic - ECG or Alternate	ERJ-3EKF49R9V	RES 49.9 Ω 1/10W 1% 0603 SMD
2	75	R36 R38	805	Yageo America or Alternate	9C08052A75R0FKHFT	RES 75.0 Ω 1/8W 1% 0805 SMD
3	300	R4 R27 R29	603	Yageo America or Alternate	RC0603FR-07300RL	RES 300 Ω 1/10W 1% 0603 SMD
4	1k	R8 R21 R31 R37	805	Yageo America or Alternate	9C08052A1001JLHFT	RES 1.0kΩ 1/8W 5% 0805 SMD
5	10k	R41–R45	603	Panasonic - ECG or Alternate	ERJ-3EKF1002V	RES 10.0kΩ 1/10W 1% 0603 SMD
1	10k	R46	805	Panasonic - ECG or Alternate	ERJ-6GEYJ103V	RES 10kΩ 1/8W 5% 0805 SMD
2	NI	R6 R28	603	Not Installed	Not Installed	
11	NI	R7 R9–R13 R18 R20 R32 R34 R35	805	Not Installed	Not Installed	
2	47	RP1 RP2	CTS_742	CTS Corporation	742C163470JTR	RES ARRAY 47Ω 16TERM 8RES SMD
1	1K	RP3	CTS_742	CTS Corporation	742C163102JTR	RES ARRAY 1kΩ 16TERM 8RES SMD
1	51	RP4	CTS_742_4RES	CTS Corporation	742C083510JTR	RES ARRAY 51Ω 8TERM 4RES SMD
1	10K	R24	BOURNS_3296Y	Bourns Inc.	3296Y-1-103	POT 10kΩ 3/8" SQ CERM SL MT
4	MMZ2012 R601A	L1–L4	805	TDK Corporation	MMZ2012R601A	FERRITE CHIP 600Ω 500MA 0805
13	1000pF	C28–C36 C62–C65	603	TDK Corporation or Alternate	C1608X7R1H102K	CAP CER 1000pF 50V XR7 10% 0603
1	2200pF	C45	603	TDK Corporation or Alternate	C1608C0G1H222J	CAP CER 2200pF 50V C0G 5% 0603
6	0.1µF	C66–C71	603	TDK Corporation or Alternate	C1608X7R1E104K	CAP CER 0.10µF 25V X7R 10% 0603
6	0.1µF	C9–C14	805	TDK Corporation or Alternate	C2012X7R1H104K	CAP CER 0.10µF 50V X7R 10% 0805
2	0.47µF	C1 C2	603	TDK Corporation or Alternate	C1608X5R1A474K	CAP CER 0.47µF 10V X5R 10% 0603
2	1µF	C5 C7	603	TDK Corporation or Alternate	C1608X5R1A105KT	CAP CER 1.0µF 10V X5R 10% 0603

Table 10. Bill of Materials (continued)

QTY	Value	REF DES	Footprint	MFG	MFG Part No.	Description
2	1µF	C41 C42	805	TDK Corporation or Alternate	C2012X7R1E105K	CAP CER 1.0µF 25V X7R 0805 T/R
8	2.2µF	C20–C27	603	TDK Corporation or Alternate	C1608X5R1A225MT	CAP CER 2.2µF 6.3V X5R 20% 0603
1	10µF	C40	805	TDK Corporation or Alternate	C2012X5R0J106M	CAP CER 10µF 6.3V X5R 20% 0805
8	10µF	C48–C55	1206	TDK Corporation or Alternate	C3216X5R1C106M	CAP CER 10µF 16V X5R 20% 1206
1	22µF	C6	805	TDK Corporation or Alternate	C2012X5R0J226M	CAP CER 22µF 6.3V X5R 20% 0805
1	47µF	C37	1206	TDK Corporation or Alternate	C3216X5R0J476M	CAP CER 47µF 6.3V X5R 20% 1206
15	NI	C3 C4 C8 C15 C16 C18 C19 C46 C47 C56–C61	603	Not Installed	Not Installed	Multilayer Ceramic
4	NI	C38 C39 C43 C44	805	Not Installed	Not Installed	1/10W 0805 Chip Resistor
1	REF3230	U1	6-SOT(DBV)	Texas Instruments	REF3230AIDBVR	3.0V 4ppm/°C, 100µA SOT23-6 Series (Bandgap) Voltage Reference
1	REF3240	U2	6-SOT(DBV)	Texas Instruments	REF3240AIDBVR	4.096V 4ppm/°C, 100µA SOT23-6 Series (Bandgap) Voltage Reference
1	NI	U3	8-SOP(D)	Not Installed	Not Installed	SOIC reference alternate
1	THS4032	U4	8-SOP(D)	Texas Instruments	THS4032CD	100-MHz Low Noise Voltage-Feedback Amplifier, Dual
1	ADS8472	U5	48-QFN(RGZ)	Texas Instruments	ADS8472IBRGZR	ADS8472 16-bit 1MSPS A/D
2	THS4031	U6 U7	8-SOP(D)	Texas Instruments	THS4031IDR	100-MHz Low-noise high-speed amplifier
4	SN74AHC245PWR	U8–U11	20-TSSOP(PW)	Texas Instruments	SN74AHC245PWR	Octal Bus Transceiver, 3-State
1	SN74AHC1G04DBV	U12	5-SOT(DBV)	Texas Instruments	SN74AHC1G04DBVR	Single Inverter Gate
1	SN74AHC138PWR	U13	16-TSSOP(PW)	Texas Instruments	SN74AHC138PWR	3-Line to 8-Line Decoder / Demultiplexer
2	SMA_PCB_MT	J1 J2	SMA_JACK	Johnson Components Inc.	142-0701-301	Right Angle SMA Connector
2	NI	J3 J4	SMA_JACK	Not Installed	Not Installed	MaCom #5002-5003-10/Amphenol #901-144
1	5X2X.1	J5	5X2X.1_SMT_SOCKET	Samtec	SSW-105-22-S-D-VS	0.025" SMT Socket – Bottom side of PWB
1				Samtec	TSM-105-01-T-D-V-P	0.025" SMT Plug - Top side of PWB
1	6X2X.1	J6	6X2X.1_SMT_PLUG_&_SOCKET	Samtec	TSM-105-01-T-D-V-P	0.025" SMT Plug - Top side of PWB
1	40-PIN Header	J7	20X2X.1	Tyco Electronics/Amp	4-103149-0-20	CONN HEADR BRKWAY 0.100 40POS R/A
2	10X2X.1	P1 P3	10X2X.1_SMT_PLUG_&_SOCKET	Samtec	SSW-110-22-S-D-VS	0.025" SMT Socket - Bottom side of PWB
1	18X2X.1_SMT_PLUG_&_SOCKET	P2	18X2.1_SMT_PLUG_&_SOCKET	Samtec	SSW-118-22-S-D-VS	0.025" SMT Socket - Bottom side of PWB
1				Samtec	TSM-118-01-T-D-V-P	0.025" SMT Plug - Top side of PWB
2	SJP2	SJP5 SJP6	SJP2	NOT INSTALLED	NOT INSTALLED	
4	SJP3	SJP1–SJP4	SJP3	NOT INSTALLED	NOT INSTALLED	NOT INSTALLED NOT INSTALLED

Table 10. Bill of Materials (continued)

QTY	Value	REF DES	Footprint	MFG	MFG Part No.	Description
5	3POS_JUMPER	W1–W4 W6	3pos_jump	Samtec	TSW-103-07-L-S	3 Position Jumper _ 0.1" spacing
1	2POS_JUMPER	W5	2pos_jump	Samtec	TSW-102-07-L-S	2 Position Jumper _ 0.1" spacing
8	TP_0.025	TP3–TP7 TP9 TP11 TP12	test_point2	Keystone Electronics	5000K–ND	TEST POINT PC MINI 0.040"D RED
6	TP_0.025	TP1 TP2 TP8 TP10 TP13 TP14	test_point2	Keystone Electronics	5001K–ND	TEST POINT PC MINI 0.040"D BLACK

8 ADS8472EVM Layout

This section contains the EVM layout.

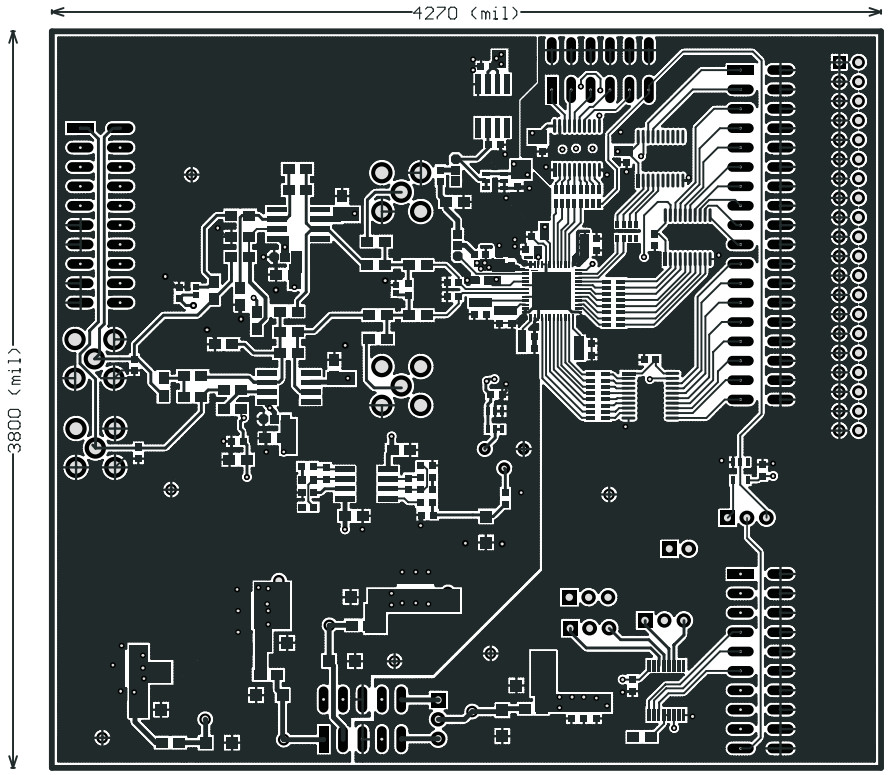


Figure 2. Top – Layer 1

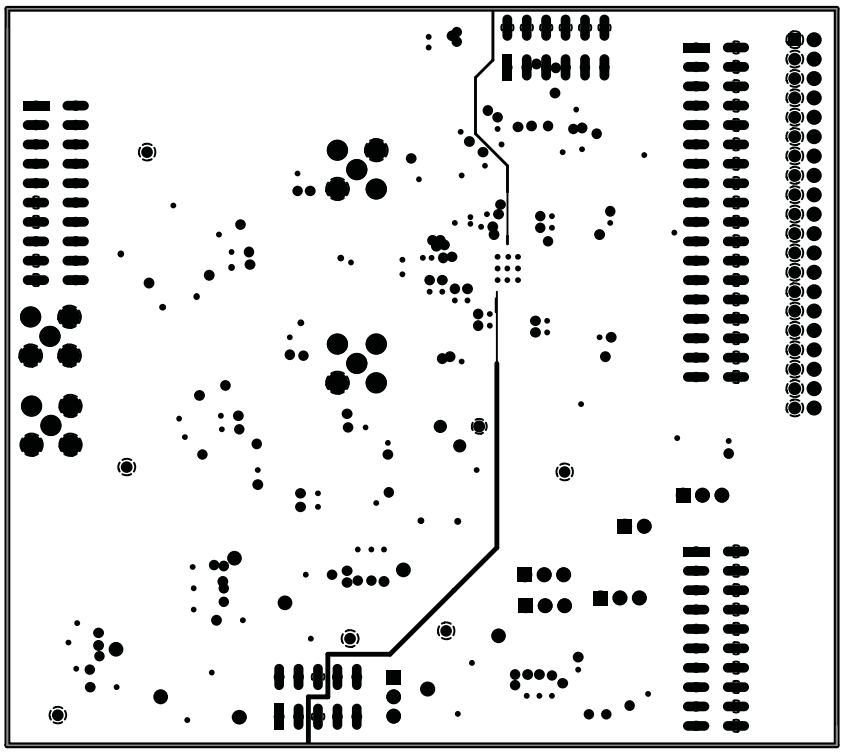


Figure 3. Ground Plane – Layer 2

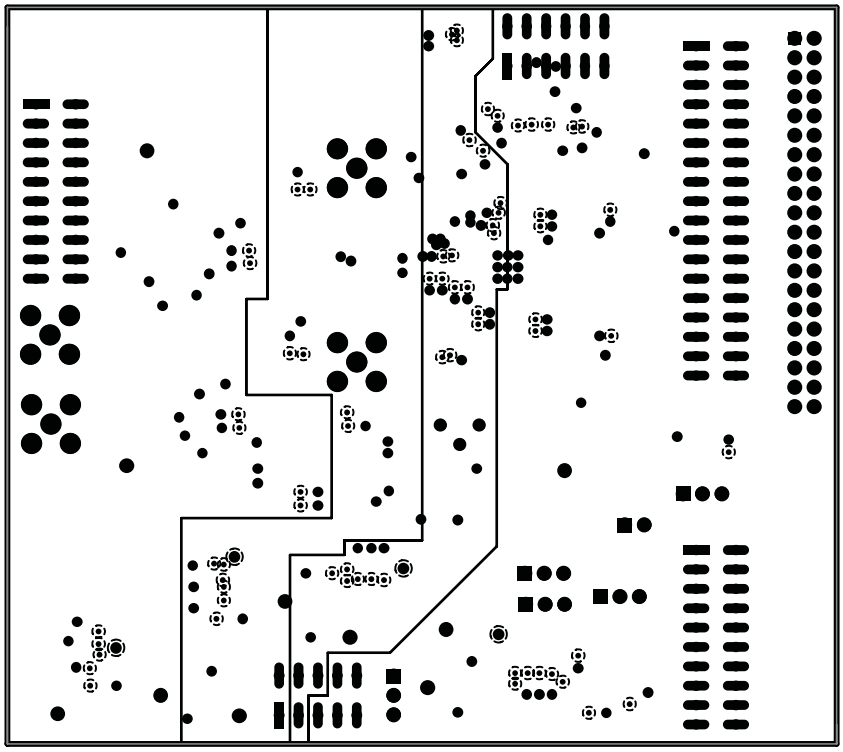


Figure 4. Power Plane – Layer 3

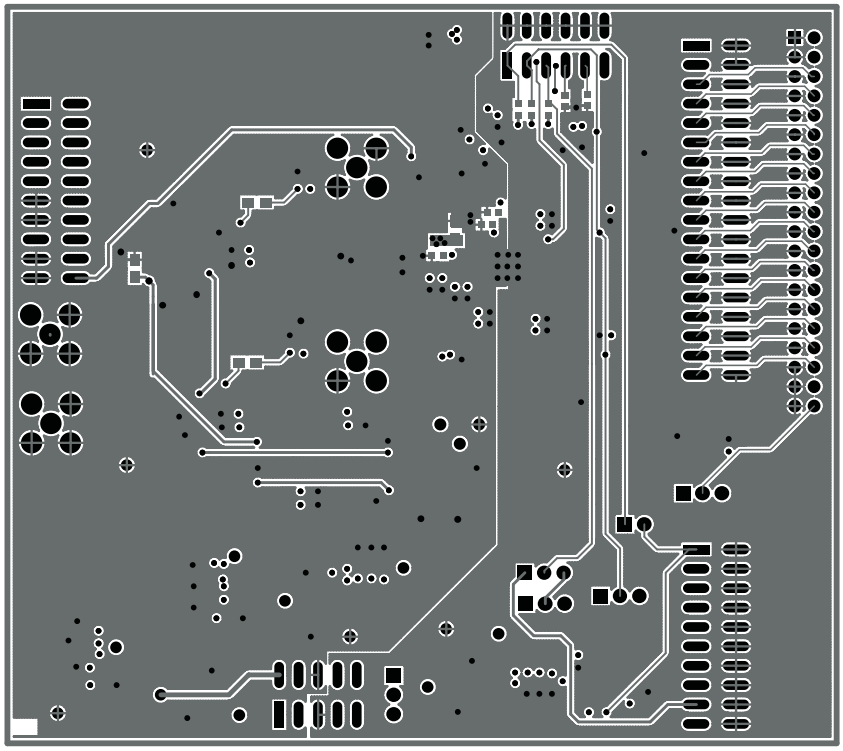


Figure 5. Bottom – Layer 4

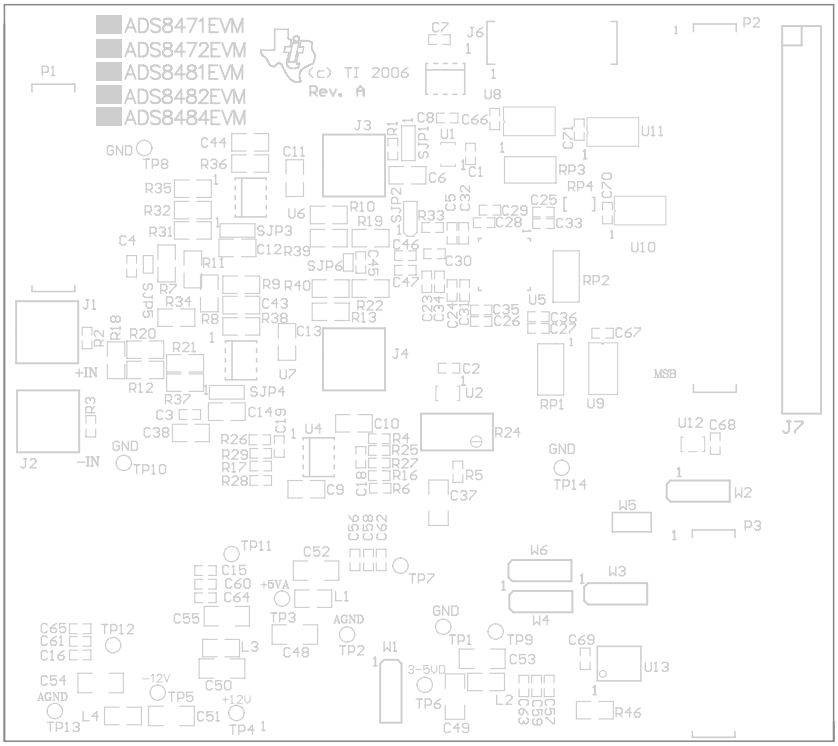


Figure 6. Top Overlay

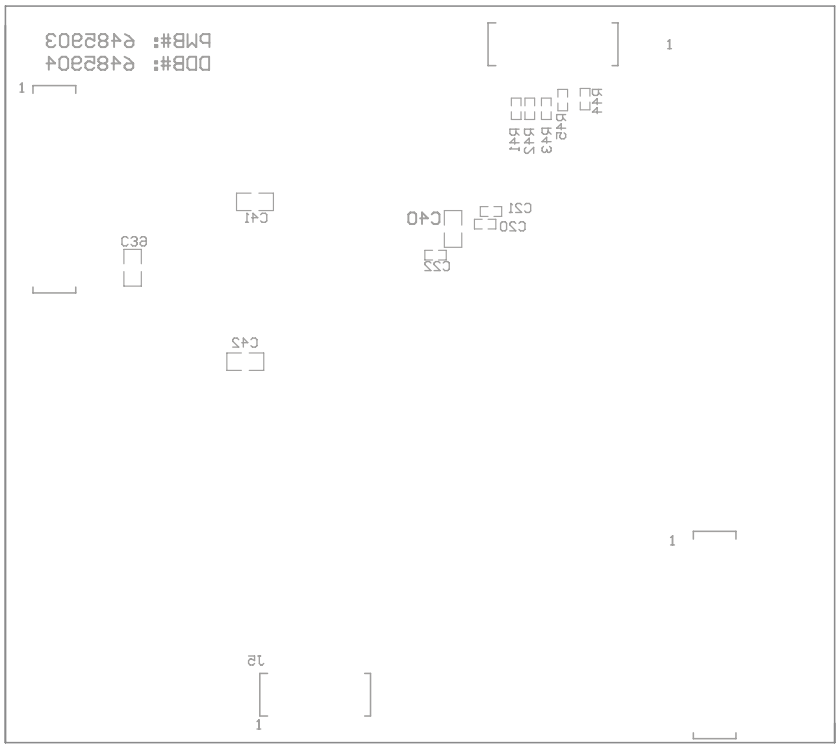
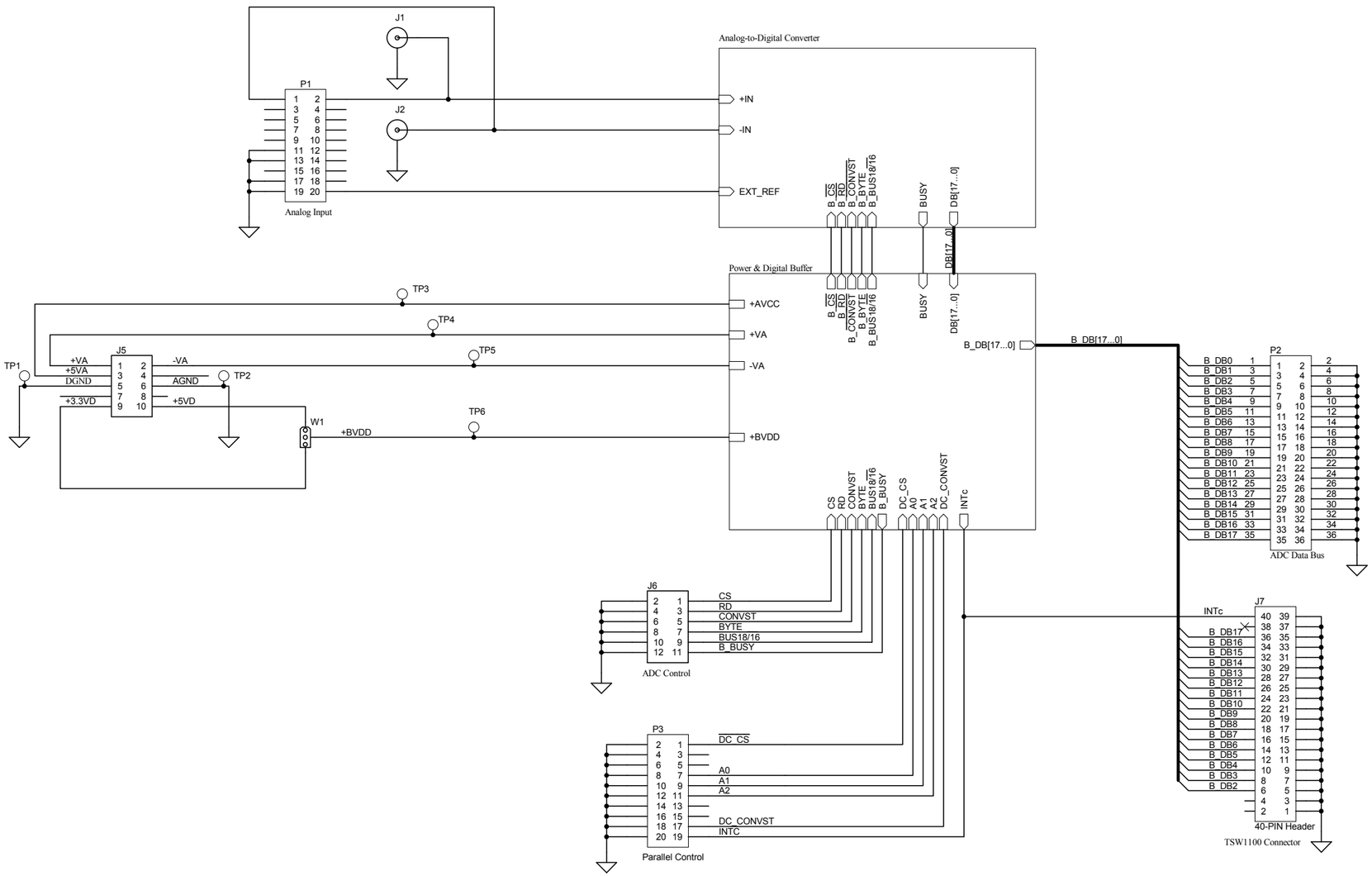


Figure 7. Bottom OverLay

9 ADS8472EVM Schematic

Schematic diagram pages are appended to this user's guide.

Revision History		
REV	ECN Number	Approved



TEXAS INSTRUMENTS

12500 TI Boulevard. Dallas, Texas 75243

TITLE: ADS8471/ADS8472EVM Block Diagram			
Engineer: Lijoy Philipose	DOCUMENT CONTROL #: 6485904		REV: A
Drawn By: Lijoy Philipose			
FILE: BlockDiagram.sch	DATE: 31-Jan-2009	SIZE:	SHEET: 1 OF: 3

Revision History		
REV	ECN Number	Approved

U3 **VRE4141**
NC, +VIN, EN, GND, NC, NC, VREF, NC
NI
C7 1uF
C8 NI
EXT_REF
SJP1
R1 49.9
C6 22uF

U1
GND_F, GND_S, ENABLE, OUT_F, OUT_S, IN
REF3230
C1 0.47uF
+5VCC

U2
GND_F, GND_S, ENABLE, OUT_F, OUT_S, IN
REF3240
C2 0.47uF
+5VCC

R24 10K
R5 33
C37 47uF
R4 300
R27 300
C18 NI
R25 33
+DC
U4B
THS4032
R16 0
R6 NI
C3 NI
C38 NI

+VCC
C10 0.1uF
R17 0
U4A
THS4032
R28 NI
R26 33
-DC
C9 0.1uF
-VCC
C19 NI
C4 NI
C39 NI
R29 300

SJP2
R33 0

+5VCC
C20 2.2uF
C21 2.2uF
C28 1000pF
C29 1000pF
C40 10uF
C5 1uF
C32 1000pF
C22 2.2uF
C30 1000pF

+VBD
C33 1000pF
C25 2.2uF

B_CS
B_RD
B_CONVST
B_BYTE
B_BUS18/16
BUSY

U5
ADS8472
REFM, REFM, +VA, AGND, AGND, +VA, CS, RD, CONVST, BYTE, BUS18/16, +VBD
REFIN, REFOUT, NC, +VA, AGND, +IN, -IN, AGND, +VA, +VA, AGND, AGND
BUSY, DB0, DB1, DB2, DB3, DB4, DB5, DB6, DB7, DB8, DB9, BDGND
+VA, AGND, AGND, DB17, DB16, DB15, DB14, DB13, DB12, DB11, DB10, +VBD
DB[17..0]

+5VCC
C23 2.2uF
C34 1000pF
C24 2.2uF
C31 1000pF
C35 1000pF
C26 2.2uF
C36 1000pF
C27 2.2uF
+VBD

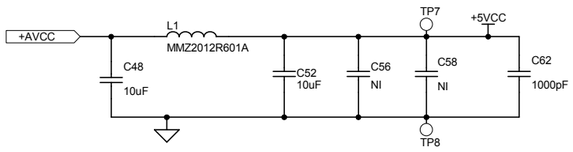
R32 NI
C11 0.1uF
J3
R10 NI
C41 1uF
U6
THS4031
R8 1k
R31 1k
+IN
R7 NI
R35 NI
R2 49.9
-DC
SJP5
R11 NI
SJP3
C12 0.1uF
-VCC
R36 75
C44 NI
R39 5.1
R19* 0
C46* NI
C45 2200pF *C0G*
C47* NI
R18 NI
R9 NI
C43 NI
R38 75
J4
R13 NI
SJP6
R34 NI
SJP4
C14 0.1uF
C42 1uF
U7
THS4031
R12 NI
R20 NI
-IN
R21 1k
R3 49.9
+DC
R37 1k
C13 0.1uF
R40 5.1
R22* 0

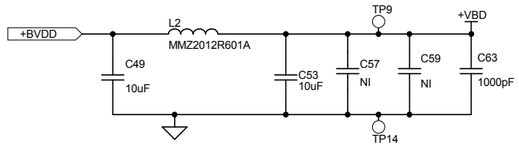
Engineer:	Lijoy Philipose
Drawn By:	Lijoy Philipose
FILE:	Analog-to-Digital Converter

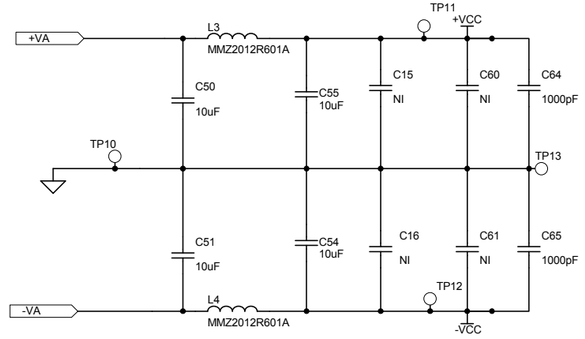
TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

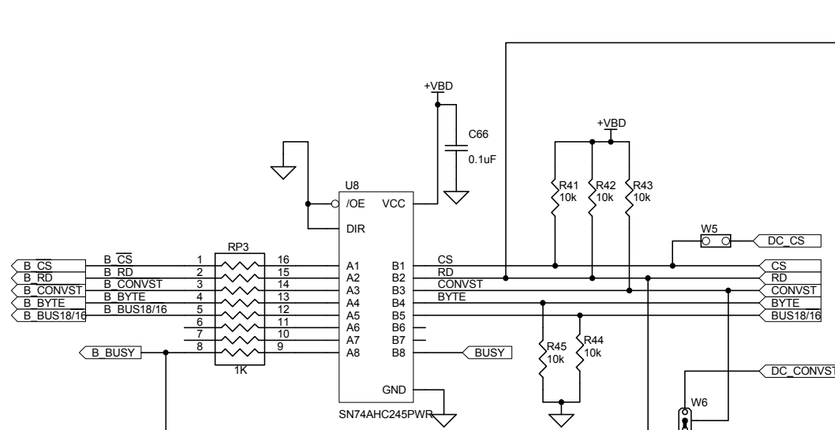
TITLE: Analog-to-Digital Converter		
DOCUMENT CONTROL #: 6485904		REV: A
DATE: 31-Jan-2009	SIZE:	SHEET: 2 OF: 3

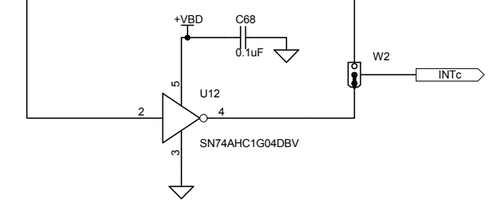
Revision History		
REV	ECN Number	Approved

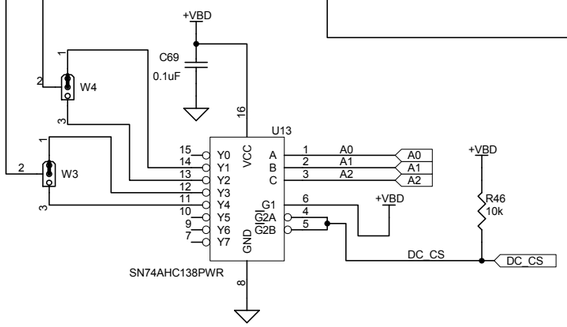


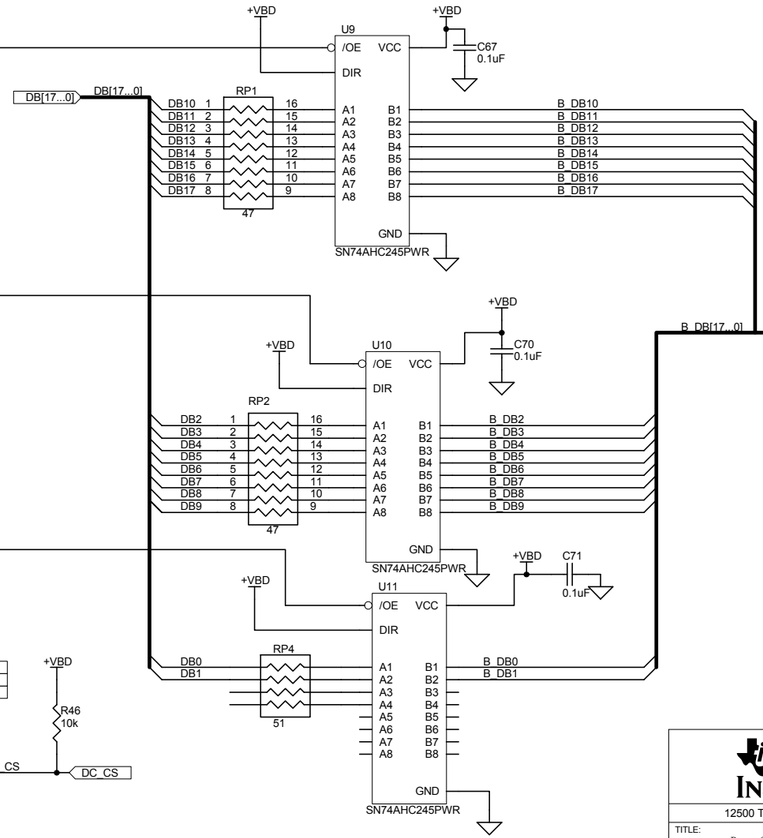












TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

TITLE:	Power Supply & Digital Buffer Circuit
DOCUMENT CONTROL #:	6485904
REV:	A
Engineer:	Lijoy Philipose
Drawn By:	Lijoy Philipose
FILE:	Power & Digital Buffer
DATE:	31-Jan-2009
SIZE:	
SHEET:	3 OF: 3

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of -6 VDC to +6 VDC, and the output voltage range of 0 to 4 VDC.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 70°C . The EVM is designed to operate properly with certain components above 70°C as long as the input and output ranges are maintained. These components include but are not limited to, switching transistors, inductor, and IC. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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