

# HEF4014B-Q100

## 8-bit static shift register

Rev. 3 — 24 November 2021

Product data sheet

## 1. General description

The HEF4014B-Q100 is an 8-bit shift register with synchronous parallel enable. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{DD}$ .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 3) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 3)
  - Specified from -40 °C to +85 °C
- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Tolerant of slow clock rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - MIL-STD-883C, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)

## 3. Applications

- Parallel-to-serial converter
- Serial data queueing
- General-purpose register

## 4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
HEF4014BT-Q100	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

### 5. Functional diagram

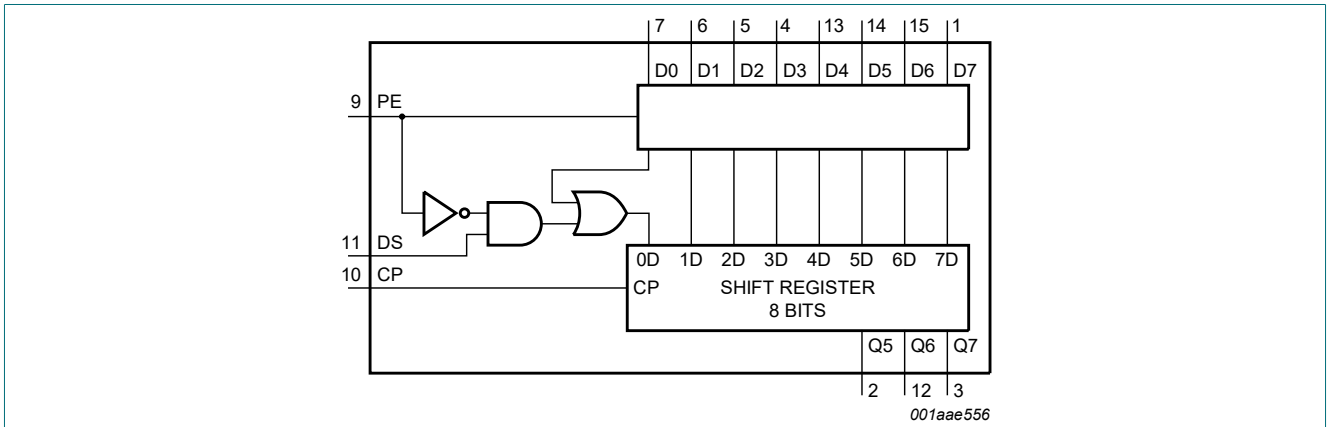


Fig. 1. Functional diagram

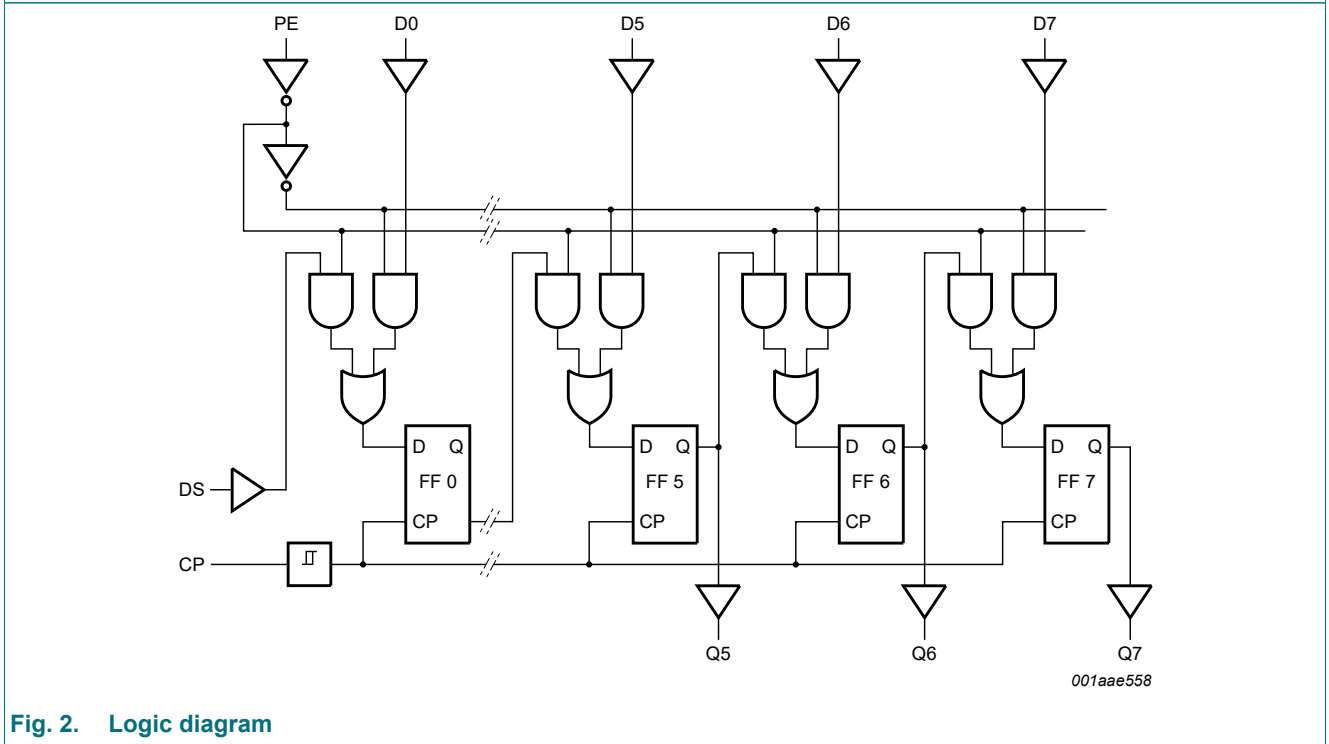
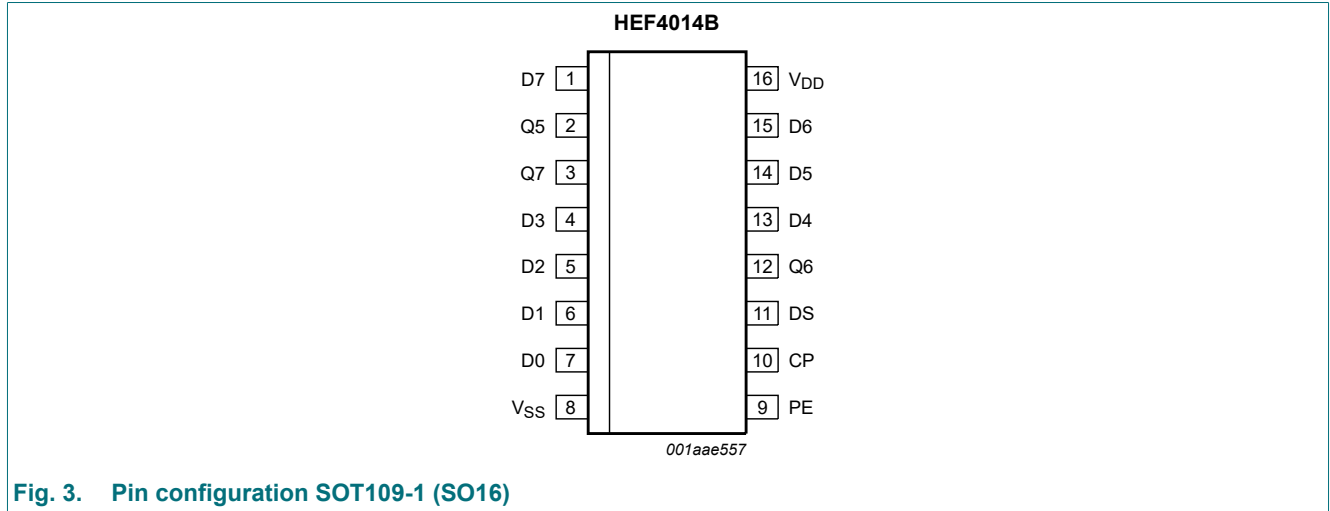


Fig. 2. Logic diagram

## 6. Pinning information

### 6.1. Pinning



### 6.2. Pin description

**Table 2. Pin description**

Symbol	Pin	Description
Q5 to Q7	2, 12, 3	output
D0 to D7	7, 6, 5, 4, 13, 14, 15, 1	parallel data input
V <sub>SS</sub>	8	ground supply voltage
PE	9	parallel enable input
CP	10	clock input (LOW-to-HIGH edge-triggered)
DS	11	serial data input
V <sub>DD</sub>	16	supply voltage

## 7. Functional description

**Table 3. Function table**

H = HIGH voltage level; L = LOW voltage level; X = don't care; nD = HIGH or LOW;  
 ↑ = LOW-to-HIGH clock transition; ↓ = HIGH-to-LOW clock transition.

Number of clock transitions	Inputs			Outputs		
	CP	DS	PE	Q5	Q6	Q7
<b>Serial operation</b>						
1	↑	1D	L	X	X	X
2	↑	2D	L	X	X	X
3	↑	3D	L	X	X	X
6	↑	X	L	1D	X	X
7	↑	X	L	2D	1D	X
8	↑	X	L	3D	2D	1D
	↓	X	X	no change	no change	no change
<b>Parallel operation</b>						
1	↑	X	H	D5	D6	D7
	↓	X	X	no change	no change	no change

## 8. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	supply voltage		-0.5	+18	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>DD</sub> + 0.5 V	-	±10	mA
V <sub>I</sub>	input voltage		-0.5	V <sub>DD</sub> + 0.5	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>DD</sub> + 0.5 V	-	±10	mA
I <sub>I/O</sub>	input/output current		-	±10	mA
I <sub>DD</sub>	supply current		-	50	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>amb</sub>	ambient temperature		-40	+85	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +85 °C	-	500	mW
P	power dissipation	per output	-	100	mW

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>DD</sub>	supply voltage		3	-	15	V
V <sub>I</sub>	input voltage		0	-	V <sub>DD</sub>	V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V <sub>DD</sub> = 5 V	-	-	3.75	μs/V
		V <sub>DD</sub> = 10 V	-	-	0.5	μs/V
		V <sub>DD</sub> = 15 V	-	-	0.08	μs/V

## 10. Static characteristics

**Table 6. Static characteristics**

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$  unless otherwise specified.

Symbol	Parameter	Conditions	V <sub>DD</sub>	T <sub>amb</sub> = -40 °C		T <sub>amb</sub> = +25 °C		T <sub>amb</sub> = +85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	I <sub>O</sub>   < 1 μA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V <sub>IL</sub>	LOW-level input voltage	I <sub>O</sub>   < 1 μA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V <sub>OH</sub>	HIGH-level output voltage	I <sub>O</sub>   < 1 μA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V <sub>OL</sub>	LOW-level output voltage	I <sub>O</sub>   < 1 μA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I <sub>OH</sub>	HIGH-level output current	V <sub>O</sub> = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		V <sub>O</sub> = 4.6 V	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		V <sub>O</sub> = 9.5 V	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		V <sub>O</sub> = 13.5 V	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I <sub>OL</sub>	LOW-level output current	V <sub>O</sub> = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V <sub>O</sub> = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V <sub>O</sub> = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I <sub>I</sub>	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	μA
I <sub>DD</sub>	supply current	I <sub>O</sub> = 0 A	5 V	-	20	-	20	-	150	μA
			10 V	-	40	-	40	-	300	μA
			15 V	-	80	-	80	-	600	μA
C <sub>I</sub>	input capacitance		-	-	-	-	7.5	-	-	pF

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $V_{SS} = 0\text{ V}$ .

Symbol	Parameter	Conditions	V <sub>DD</sub>	Extrapolation formula [1]	Min	Typ	Max	Unit		
t <sub>PHL</sub>	HIGH to LOW propagation delay	CP to Qn; see Fig. 4	5 V	103 ns + (0.55 ns/pF)C <sub>L</sub>	-	130	260	ns		
			10 V	44 ns + (0.23 ns/pF)C <sub>L</sub>	-	55	110	ns		
			15 V	32 ns + (0.16 ns/pF)C <sub>L</sub>	-	40	80	ns		
t <sub>PLH</sub>	LOW to HIGH propagation delay	CP to Qn; see Fig. 4	5 V	88 ns + (0.55 ns/pF)C <sub>L</sub>	-	115	230	ns		
			10 V	39 ns + (0.23 ns/pF)C <sub>L</sub>	-	50	100	ns		
			15 V	32 ns + (0.16 ns/pF)C <sub>L</sub>	-	40	80	ns		
t <sub>t</sub>	transition time	Qn output; see Fig. 4	5 V [2]	10 ns + (1.00 ns/pF)C <sub>L</sub>	-	60	120	ns		
			10 V	9 ns + (0.42 ns/pF)C <sub>L</sub>	-	30	60	ns		
			15 V	6 ns + (0.28 ns/pF)C <sub>L</sub>	-	20	40	ns		
t <sub>W</sub>	pulse width	CP input; minimum width; see Fig. 5	5 V		70	35	-	ns		
			10 V		30	15	-	ns		
			15 V		24	12	-	ns		
t <sub>su</sub>	set-up time	PE to CP; see Fig. 5	5 V		40	10	-	ns		
			10 V		25	5	-	ns		
			15 V		15	0	-	ns		
		DS to CP; see Fig. 5	5 V		+35	-5	-	ns		
			10 V		+25	-5	-	ns		
			15 V		25	0	-	ns		
		Dn to CP; see Fig. 5	5 V		+35	-5	-	ns		
			10 V		+25	-5	-	ns		
			15 V		25	0	-	ns		
		t <sub>h</sub>	hold time	PE to CP; see Fig. 5	5 V		+25	-5	-	ns
					10 V		20	0	-	ns
					15 V		15	0	-	ns
DS to CP; see Fig. 5	5 V				30	15	-	ns		
	10 V				20	10	-	ns		
	15 V				15	7	-	ns		
Dn to CP; see Fig. 5	5 V				30	15	-	ns		
	10 V				20	10	-	ns		
	15 V				15	7	-	ns		
f <sub>clk(max)</sub>	maximum clock frequency			see Fig. 5	5 V		6	13	-	MHz
					10 V		15	30	-	MHz
					15 V		20	40	-	MHz

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C<sub>L</sub> in pF).

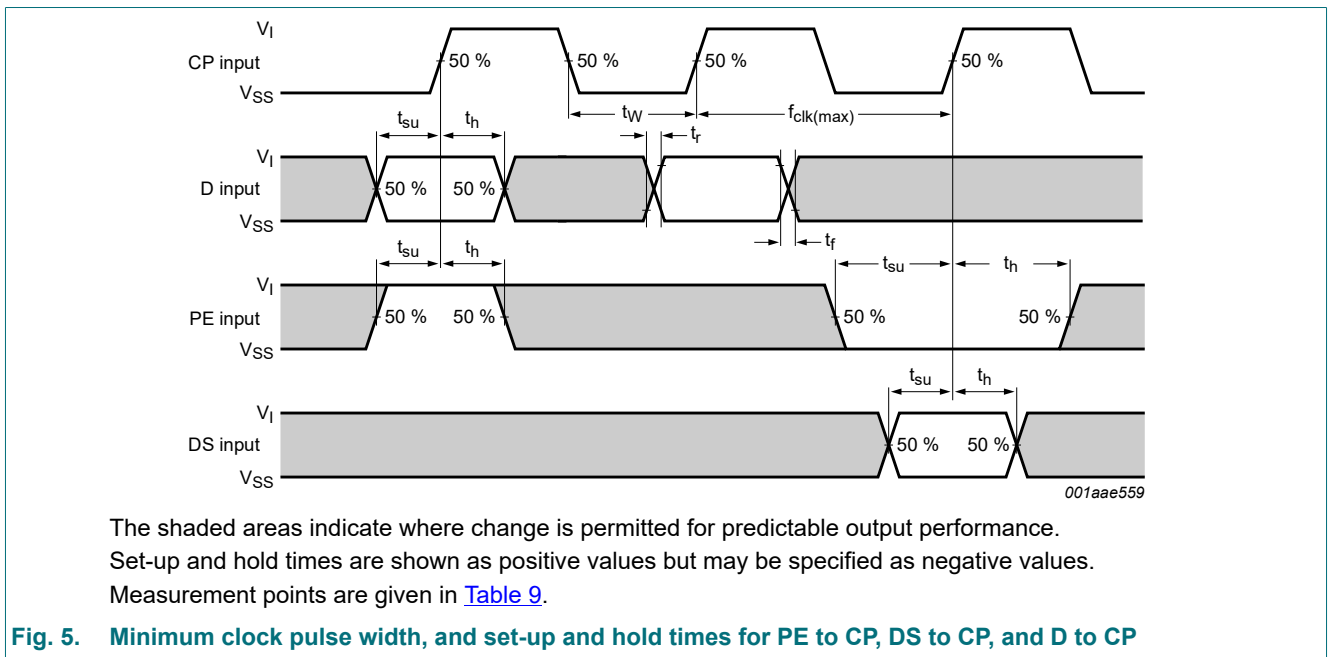
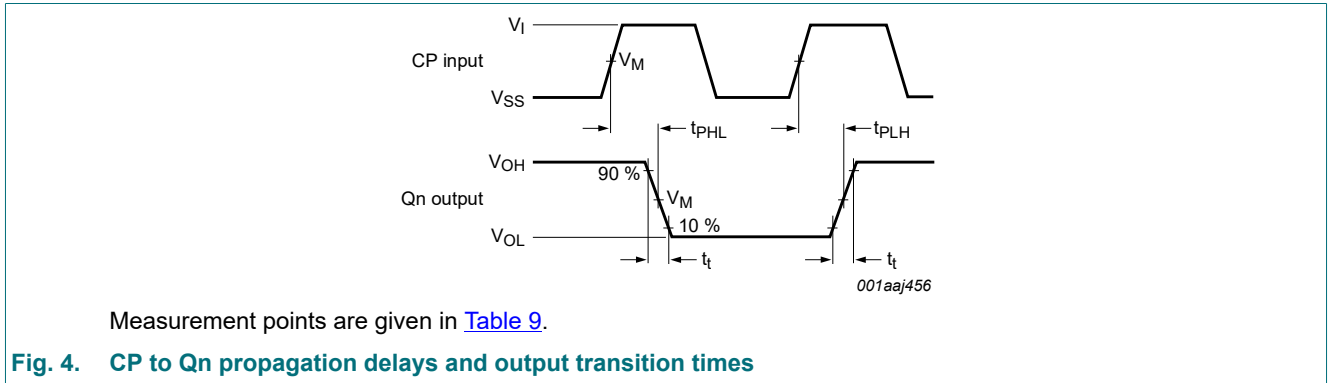
[2] t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.

**Table 8. Dynamic power dissipation  $P_D$**

$P_D$  can be calculated from the formulas shown.  $V_{SS} = 0\text{ V}$ ;  $t_r = t_f \leq 20\text{ ns}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ .

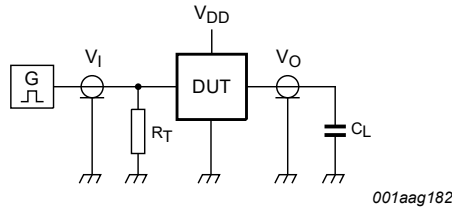
Symbol	Parameter	$V_{DD}$	Typical formula for $P_D$ ( $\mu\text{W}$ )	Where:
$P_D$	dynamic power dissipation	5 V	$P_D = 900 \times f_i + \sum(f_o \times C_L) \times V_{DD}^2$	$f_i$ = input frequency in MHz; $f_o$ = output frequency in MHz; $C_L$ = output load capacitance in pF; $V_{DD}$ = supply voltage in V; $\sum(C_L \times f_o)$ = sum of the outputs.
		10 V	$P_D = 4300 \times f_i + \sum(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 12000 \times f_i + \sum(f_o \times C_L) \times V_{DD}^2$	

**11.1. Waveforms and test circuit**



**Table 9. Measurement points**

Supply voltage	Input	Output
$V_{DD}$	$V_M$	$V_M$
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



Test data is given in [Table 10](#).

Definitions for test circuit:

$C_L$  = load capacitance including jig and probe capacitance.

$R_T$  = termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

**Fig. 6. Test circuit for measuring switching times**

**Table 10. Test data**

Supply voltage	Input		Load
$V_{DD}$	$V_I$	$t_r, t_f$	$C_L$
5 V to 15 V	$V_{SS}$ or $V_{DD}$	$\leq 20$ ns	50 pF



## 12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

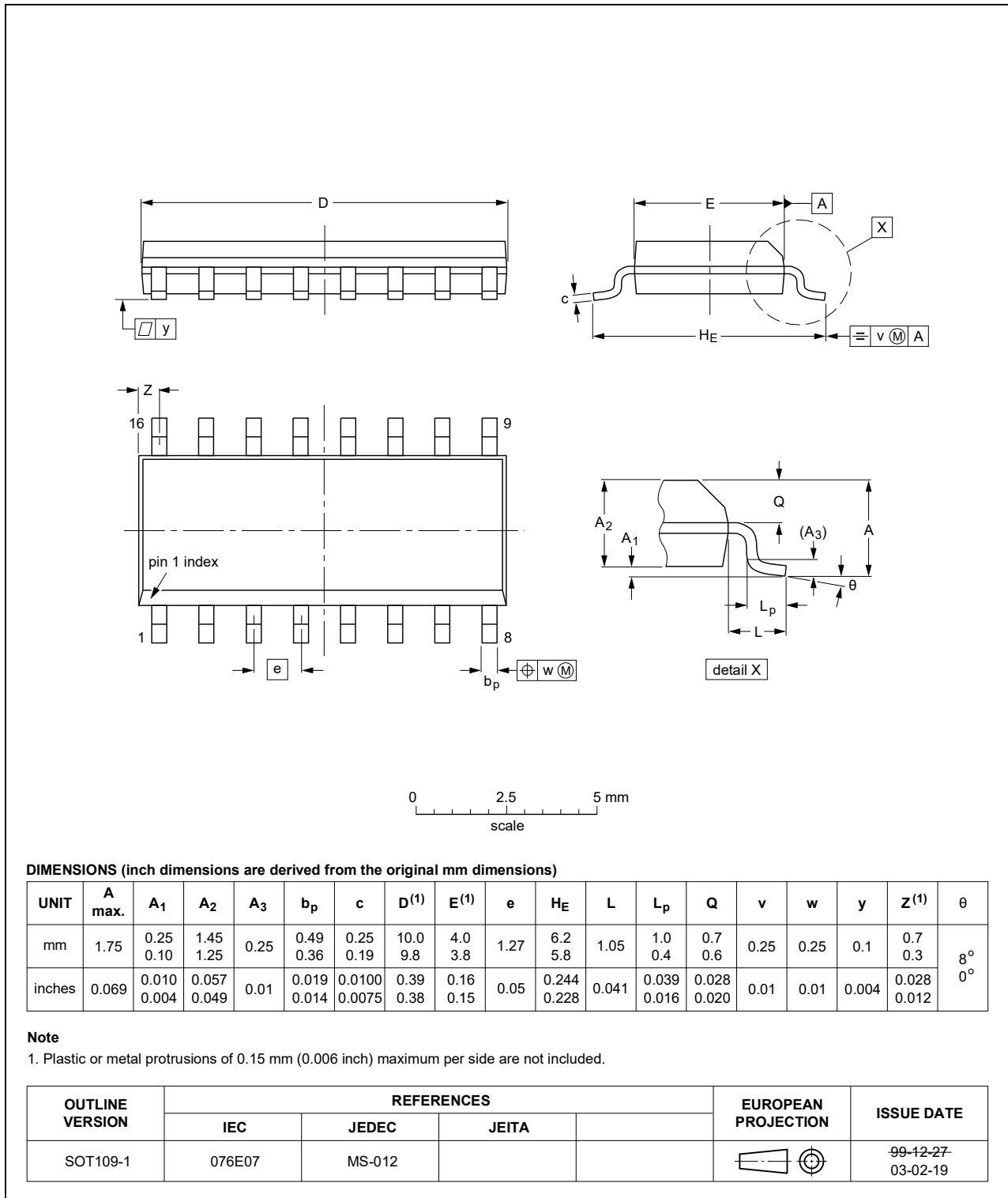


Fig. 7. Package outline SOT109-1 (SO16)

## 13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model

## 14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4014B_Q100 v.3	20211124	Product data sheet	-	HEF4014B_Q100 v.2
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> </ul>			
HEF4014B_Q100 v.2	20181017	Product data sheet	-	HEF4014B_Q100 v.1
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
HEF4014B_Q100 v.1	20130227	Product data sheet	-	-

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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