Single 2-Input OR Gate

MC74VHC1G32, MC74VHC1GT32

The MC74VHC1G32 / MC74VHC1GT32 is a single 2−input OR Gate in tiny footprint packages. The MC74VHC1G32 has CMOS−level input thresholds while the MC74VHC1GT32 has TTL−level thresholds.

The input structures provide protection when voltages up to 5.5 V are applied, regardless of the supply voltage. This allows the device to be used to interface 5 V circuits to 3 V circuits. Some output structures also provide protection when $V_{CC} = 0$ V and when the output voltage exceeds V_{CC}. These input and output structures help prevent device destruction caused by supply voltage − input/output voltage mismatch, battery backup, hot insertion, etc.

Features

- Designed for 2.0 V to 5.5 V V_{CC} Operation
- 3.7 ns t_{PD} at 5 V (typ)
- Inputs/Outputs Over−Voltage Tolerant up to 5.5 V
- I_{OFF} Supports Partial Power Down Protection
- Source/Sink 8 mA at 3.0 V
- Available in SC−88A, SC−74A, TSOP−5, SOT−953 and UDFN6 Packages
- Chip Complexity < 100 FETs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant
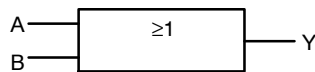
Figure 1. Logic Symbol

MARKING DIAGRAMS

Package	Marking
SC−88A DF SUFFIX CASE 419A	XX M■
SC−74A DBV SUFFIX CASE 318BQ	XXX M■
TSOP−5 DT SUFFIX CASE 483	XX M■
	XXXAYW■
SOT−953 P5 SUFFIX CASE 527AE	X M
UDFN6 1.45 x 1.0 CASE 517AQ	XM
UDFN6 1.2 x 1.0 CASE 517AA	X M
UDFN6 1.0 x 1.0 CASE 517BX	X M

XX = Specific Device Code
M = Date Code*
■ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 7 of this data sheet.
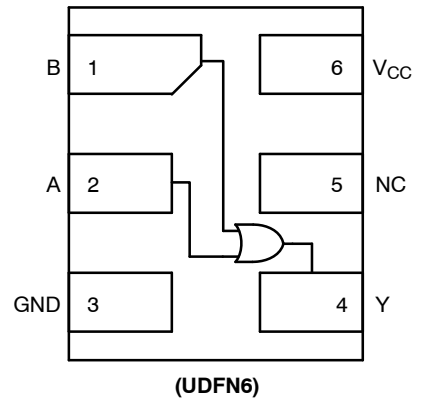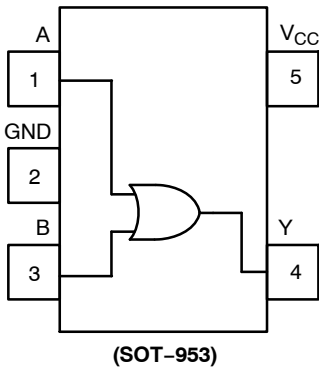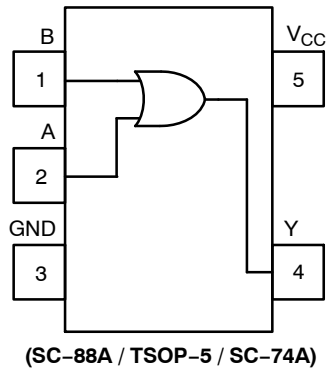
MC74VHC1G32, MC74VHC1GT32

(SC−88A / TSOP−5 / SC−74A)

(SOT−953)

(UDFN6)

Figure 2. Pinout (Top View)

PIN ASSIGNMENT
(SC−88A / TSOP−5 / SC−74A)

Pin	Function
1	B
2	A
3	GND
4	Y
5	V_{CC}

PIN ASSIGNMENT (SOT−953)

Pin	Function
1	A
2	GND
3	B
4	Y
5	V_{CC}

PIN ASSIGNMENT (UDFN)

Pin	Function
1	B
2	A
3	GND
4	Y
5	NC
6	V_{CC}

FUNCTION TABLE

Input		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	H

MAXIMUM RATINGS

Symbol	Characteristics		Value	Unit
V_{CC}	DC Supply Voltage	TSOP−5, SC−88A (NLV) SC−74A, SC−88A, UDFN6, SOT−553, SOT−953	−0.5 to +7.0 −0.5 to +6.5	V
V_{IN}	DC Input Voltage	TSOP−5, SC−88A (NLV) SC−74A, SC−88A, UDFN6, SOT−553, SOT−953	−0.5 to +7.0 −0.5 to +6.5	V
V_{OUT}	DC Output Voltage (NLV)	1Gxx	−0.5 to V_{CC} + 0.5	V
		1GTxx Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V_{CC} = 0 V)	−0.5 to V_{CC} + 0.5 −0.5 to +7.0 −0.5 to +7.0	
	DC Output Voltage	Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V_{CC} = 0 V)	−0.5 to V_{CC} + 0.5 −0.5 to +6.5 −0.5 to +6.5	V
I_{IK}	DC Input Diode Current	V_{IN} < GND	−20	mA
I_{OK}	DC Output Diode Current (NLV)	1Gxx V_{OUT} > V_{CC}, V_{OUT} < GND	±20	mA
		1GTxx V_{OUT} < GND	−20	
	DC Output Diode Current	V_{OUT} < GND	−20	mA
I_{OUT}	DC Output Source/Sink Current		±25	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin		±50	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	SC−88A SC−74A SOT−553 SOT−953 UDFN6	377 320 324 254 154	°C/W
P_D	Power Dissipation in Still Air	SC−88A SC−74A SOT−553 SOT−953 UDFN6	332 390 386 491 812	mW
MSL	Moisture Sensitivity		Level 1	−
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	−
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 1000	V
$I_{Latchup}$	Latchup Performance (Note 4)		± 100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 10mm−by−1inch, 2 ounce copper trace no air flow per JESD51−7.
3. HBM tested to ANSI/ESDA/JEDEC JS−001−2017. CDM tested to EIA/JESD22−C101−F. JEDEC recommends that ESD qualification to EIA/JESD22−A115−A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics			Min	Max	Unit
V_{CC}	Positive DC Supply Voltage			2.0	5.5	V
V_{IN}	DC Input Voltage			0	5.5	V
V_{OUT}	DC Output Voltage (NLV)	1Gxx		0	V_{CC}	V
		1GTxx	Active−Mode (High or Low State)	0	V_{CC}	
			Tri−State Mode (Note 1)	0	5.5	
			Power−Down Mode (V_{CC} = 0 V)	0	5.5	
	DC Output Voltage		Active−Mode (High or Low State)	0	V_{CC}	V
			Tri−State Mode (Note 1)	0	5.5	
			Power−Down Mode (V_{CC} = 0 V)	0	5.5	
T_A	Operating Temperature Range			−55	+125	°C
t_r , t_f	Input Rise and Fall Time	TSOP−5, SC−88A (NLV)				ns/V
		V_{CC} = 3.0 V to 3.6 V		0	100	
		V_{CC} = 4.5 V to 5.5 V		0	20	
	Input Rise and Fall Time	SC−74A, SC−88A, UDFN6, SOT−553, SOT−953				
		V_{CC} = 2.0 V		0	20	
		V_{CC} = 2.3 V to 2.7 V		0	20	
		V_{CC} = 3.0 V to 3.6 V		0	10	
		V_{CC} = 4.5 V to 5.5 V		0	5	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (MC74VHC1G32)

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C			−40°C ≤ T_A ≤ 85°C		−55°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	High−Level Input Voltage		2.0	1.5			1.5		1.5		V
			3.0	2.1			2.1		2.1		
			4.5	3.15			3.15		3.15		
			5.5	3.85			3.85		3.85		
V_{IL}	Low−Level Input Voltage		2.0			0.5		0.5		0.5	V
			3.0			0.9		0.9		0.9	
			4.5			1.35		1.35		1.35	
			5.5			1.65		1.65		1.65	
V_{OH}	High−Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA I_{OH} = −8 mA	2.0 3.0 4.5 3.0 4.5	1.9 2.9 4.4 2.58 3.94	2.0 3.0 4.5		1.9 2.9 4.4 2.48 3.80		1.9 2.9 4.4 2.34 3.66		V
V_{OL}	Low−Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA I_{OL} = 8 mA	2.0 3.0 4.5 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1 0.36 0.36		0.1 0.1 0.1 0.44 0.44		0.1 0.1 0.1 0.52 0.52	V
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND	2.0 to 5.5			±0.1		±1.0		±1.0	μA
I_{OFF}	Power Off Leakage Current (NLV)	V_{IN} = 5.5 V	0.0	−	−	1.0	−	10	−	10	μA
	Power Off Leakage Current	V_{IN} = 5.5 V or V_{OUT} = 5.5 V	0.0	−	−	1.0	−	10	−	10	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			1.0		20		40	μA

DC ELECTRICAL CHARACTERISTICS (MC74VHC1GT32)

Symbol	Parameter	Test Conditions	V_{CC} (V)	$T_A = 25°C$			$-40°C \leq T_A \leq 85°C$		$-55°C \leq T_A \leq 125°C$		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	High–Level Input Voltage		2.0	1.0			1.0		1.0		V
			3.0	1.4			1.4		1.4		
			4.5	2.0			2.0		2.0		
			5.5	2.0			2.0		2.0		
V_{IL}	Low–Level Input Voltage		2.0			0.28		0.28		0.28	V
			3.0			0.45		0.45		0.45	
			4.5			0.8		0.8		0.8	
			5.5			0.8		0.8		0.8	
V_{OH}	High–Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50$ μA $I_{OH} = -50$ μA $I_{OH} = -50$ μA $I_{OH} = -4$ mA $I_{OH} = -8$ mA	2.0 3.0 4.5 3.0 4.5	1.9 2.9 4.4 2.58 3.94	2.0 3.0 4.5		1.9 2.9 4.4 2.48 3.80		1.9 2.9 4.4 2.34 3.66		V
V_{OL}	Low–Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50$ μA $I_{OL} = 50$ μA $I_{OL} = 50$ μA $I_{OL} = 4$ mA $I_{OL} = 8$ mA	2.0 3.0 4.5 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1 0.36 0.36		0.1 0.1 0.1 0.44 0.44		0.1 0.1 0.1 0.52 0.52	V
I_{IN}	Input Leakage Current	$V_{IN} = 5.5$ V or GND	2.0 to 5.5			±0.1		±1.0		±1.0	μA
I_{OFF}	Power Off Leakage Current	$V_{IN} = 5.5$ V or $V_{OUT} = 5.5$ V	0			1.0		10		10	μA
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			1.0		20		40	μA
I_{CCT}	Increase in Quiescent Supply Current per Input Pin	One Input: $V_{IN} = 3.4$ V; Other Input at V_{CC} or GND	5.5			1.35		1.5		1.65	mA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$			$-40°C \leq T_A \leq 85°C$		$-55°C \leq T_A \leq 125°C$		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, A to Y (Figures 3 and 4)	$C_L = 15$ pF	3.0 to 3.6		4.8	7.9		9.5		11.5	ns
		$C_L = 50$ pF			6.1	11.4		13.0		15.5	
		$C_L = 15$ pF	4.5 to 5.5		3.7	5.5		6.5		8.0	
		$C_L = 50$ pF			4.4	7.5		8.5		10.0	
C_{IN}	Input Capacitance				4.0	10		10		10	pF
C_{OUT}	Output Capacitance	Output in High Impedance State			6.0						pF

			Typical @ 25°C, $V_{CC} = 5.0$ V	
C_{PD}	Power Dissipation Capacitance (Note 5)		8.0	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 Ω)
f = 1 MHz

Figure 3. Test Circuit

Test	Switch Position	C_L, pF	R_L, Ω
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table	X
t_{PLZ} / t_{PZL}	V_{CC}		1 k
t_{PHZ} / t_{PZH}	GND		1 k

X = Don't Care

Figure 4. Switching Waveforms

V_{CC}, V	V_{mi}, V	V_{mo}, V		V_Y, V
		t_{PLH}, t_{PHL}	t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}	
3.0 to 3.6	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.3
4.5 to 5.5	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.3

ORDERING INFORMATION

Device	Packages	Specific Device Code	Pin 1 Orientation (See below)	Shipping†
MC74VHC1G32DFT1G	SC−88A	V4	Q2	3000 / Tape & Reel
MC74VHC1G32DFT1G−L22038**	SC−88A	V4	Q2	3000 / Tape & Reel
MC74VHC1G32DFT2G	SC−88A	V4	Q4	3000 / Tape & Reel
MC74VHC1G32DFT2G−L22038**	SC−88A	V4	Q4	3000 / Tape & Reel
NLVVHC1G32DFT1G*	SC−88A	V4	Q2	3000 / Tape & Reel
NLVVHC1G32DFT2G*	SC−88A	V4	Q4	3000 / Tape & Reel
M74VHC1GT32DFT1G	SC−88A	VN	Q2	3000 / Tape & Reel
M74VHC1GT32DFT2G	SC−88A	VN	Q4	3000 / Tape & Reel
NLVVHC1GT32DFT2G*	SC−88A	VN	Q4	3000 / Tape & Reel
NLVVHC1GT32DFT1G*	SC−88A	VN	Q2	3000 / Tape & Reel
MC74VHC1G32DBVT1G	SC−74A	V4	Q4	3000 / Tape & Reel
MC74VHC1GT32DBVT1G	SC−74A	VN	Q4	3000 / Tape & Reel
MC74VHC1G32DTT1G**	TSOP−5	V4	Q4	3000 / Tape & Reel
NLVVHC1G32DTT1G*	TSOP−5	V4	Q4	3000 / Tape & Reel
NLV74VHC1GT32DTT1G*	TSOP−5	VN	Q4	3000 / Tape & Reel
M74VHC1GT32DTT1G**	TSOP−5	VN	Q4	3000 / Tape & Reel
MC74VHC1G32P5T5G	SOT−953	F	Q2	8000 / Tape & Reel
MC74VHC1G32P5T5G−L22088**	SOT−953	F	Q2	8000 / Tape & Reel
MC74VHC1GT32P5T5G	SOT−953	Q	Q2	8000 / Tape & Reel
MC74VHC1GT32P5T5G−L22088**	SOT−953	Q	Q2	8000 / Tape & Reel
MC74VHC1G32MU1TCG	UDFN6, 1.45 x 1.0, 0.5P	3 (Rotated 90° CW)	Q4	3000 / Tape & Reel
MC74VHC1GT32MU1TCG (In Development)	UDFN6, 1.45 x 1.0, 0.5P	T (Rotated 180° CW)	Q4	3000 / Tape & Reel
MC74VHC1G32MU2TCG	UDFN6, 1.2 x 1.0, 0.4P	3	Q4	3000 / Tape & Reel
MC74VHC1GT32MU2TCG (In Development)	UDFN6, 1.2 x 1.0, 0.4P	5	Q4	3000 / Tape & Reel
MC74VHC1G32MU3TCG	UDFN6, 1.0 x 1.0, 0.35P	F (Rotated 180° CW)	Q4	3000 / Tape & Reel
MC74VHC1GT32MU3TCG (In Development)	UDFN6, 1.0 x 1.0, 0.35P	Q	Q4	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

** Please refer to NLV specifications for this device.

Pin 1 Orientation in Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
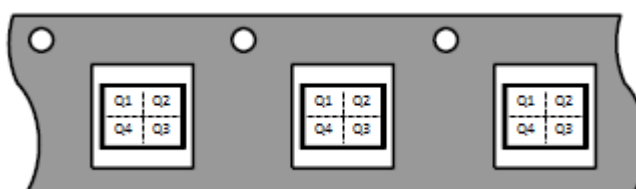
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SC−74A
CASE 318BQ
ISSUE B

DATE 18 JAN 2018

SCALE 2:1

5
1

5X **b**

⊕ | 0.20 | C | A | B

E1

5   4

o1   2   3

B

A   **D**

e

E

TOP VIEW

A

C **SEATING PLANE**

SIDE VIEW

M

▱ | 0.05

A1   **L**

DETAIL A

DETAIL A

c

END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

DIM	MILLIMETERS	
	MIN	MAX
A	0.90	1.10
A1	0.01	0.10
b	0.25	0.50
c	0.10	0.26
D	2.85	3.15
E	2.50	3.00
E1	1.35	1.65
e	0.95 BSC	
L	0.20	0.60
M	0 °	10 °

RECOMMENDED SOLDERING FOOTPRINT*

0.95 PITCH

2.40

5X 1.00

5X 0.70

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXX M▪

o   ▪

XXX = Specific Device Code
M   = Date Code
▪   = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

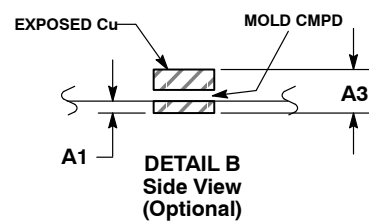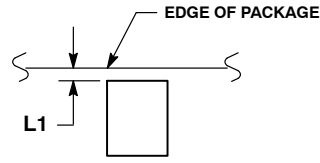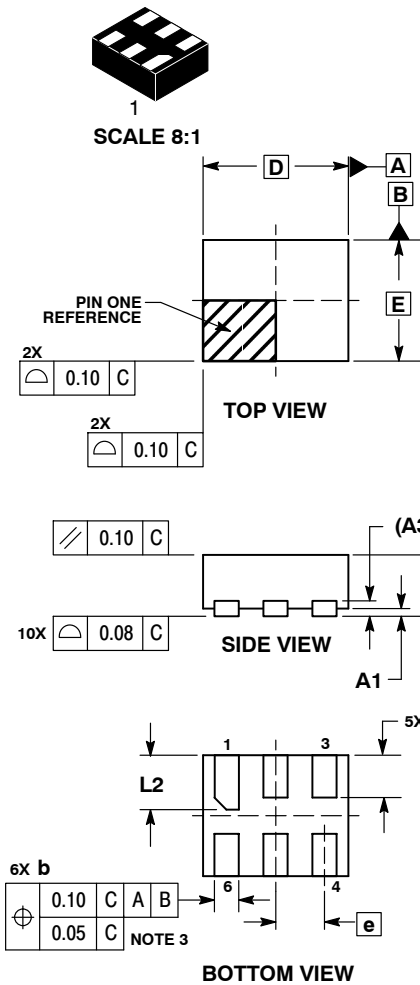| DOCUMENT NUMBER:	98AON66279G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SC−74A		PAGE 1 OF 1

onsemi™

SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE M

DATE 11 APR 2023

SCALE 2:1

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

5X b

⊕ | 0.2 Ⓜ | B Ⓜ

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30
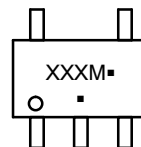
0.50
0.65
0.40
0.65
1.90

RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING
DIAGRAM*

XXXM▪

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

DOCUMENT NUMBER:	**98ASB42984B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SC−88A (SC−70−5/SOT−353)**	**PAGE 1 OF 1**

TSOP−5
CASE 483
ISSUE N

DATE 12 AUG 2020

SCALE 2:1

NOTE 5

2X | ⬠ | 0.10 | T

2X | ⬠ | 0.20 | T

D 5X

⊕ | 0.20 | C | A | B

TOP VIEW

DETAIL Z

⬠ | 0.05

SIDE VIEW

SEATING PLANE

END VIEW

DETAIL Z

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

| DIM | MILLIMETERS | |
	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

SOLDERING FOOTPRINT*

$\frac{1.9}{0.074}$

$\frac{0.95}{0.037}$

$\frac{2.4}{0.094}$

$\frac{1.0}{0.039}$

$\frac{0.7}{0.028}$

SCALE 10:1 $\left(\frac{mm}{inches}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXAYW▪

Analog

XXX M▪

Discrete/Logic

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

onsemi™

UDFN6, 1.2x1.0, 0.4P
CASE 517AA
ISSUE D

DATE 03 SEP 2010

SCALE 8:1

1

TOP VIEW

D | A | B

PIN ONE REFERENCE

E

2X △ 0.10 C

2X △ 0.10 C

SIDE VIEW

// 0.10 C

(A3)

A

10X △ 0.08 C

A1

SEATING PLANE C

BOTTOM VIEW

5X L

1 3

L2

6X b

⊕ 0.10 C A B

0.05 C NOTE 3

6 4

e

DETAIL A
Bottom View
(Optional)

EDGE OF PACKAGE

L1

DETAIL B
Side View
(Optional)

EXPOSED Cu

MOLD CMPD

A3

A1

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
---	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.20 BSC	
E	1.00 BSC	
e	0.40 BSC	
L	0.30	0.40
L1	0.00	0.15
L2	0.40	0.50

GENERIC
MARKING DIAGRAM*

X M

X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪ ", may or may not be present.

MOUNTING FOOTPRINT*

6X 0.42

6X 0.22

0.40 PITCH

1.07

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

UDFN6, 1.45x1.0, 0.5P
CASE 517AQ
ISSUE O

DATE 15 MAY 2008

SCALE 4:1

TOP VIEW

PIN ONE REFERENCE

| □ | 0.10 | C |

| □ | 0.10 | C |

SIDE VIEW

| ⌀ | 0.05 | C |

6X | □ | 0.05 | C |

DETAIL B

BOTTOM VIEW

DETAIL A

| ⊕ | 0.10 | C | A | B |
| | 0.05 | C | NOTE 3 |
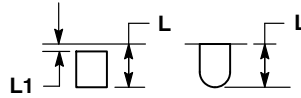
DETAIL A
OPTIONAL CONSTRUCTIONS
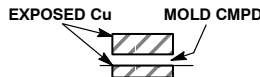
DETAIL B
OPTIONAL CONSTRUCTIONS

EXPOSED Cu   MOLD CMPD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

| DIM | MILLIMETERS | |
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A2	0.07 REF	
b	0.20	0.30
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.30	0.40
L1	---	0.15

MOUNTING FOOTPRINT

PACKAGE OUTLINE

6X 0.30

1.24

6X 0.53

1

0.50 PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
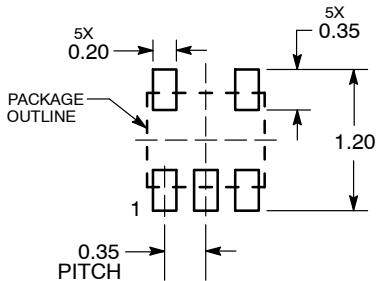
GENERIC MARKING DIAGRAM*

XM

X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

DOCUMENT NUMBER:	98AON30313E	
DESCRIPTION:	UDFN6, 1.45x1.0, 0.5P	PAGE 1 OF 1

UDFN6, 1x1, 0.35P
CASE 517BX
ISSUE O

DATE 18 MAY 2011

SCALE 4:1

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.12	0.22
D	1.00 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

PIN ONE REFERENCE

2X ⌖ 0.10 C

2X ⌖ 0.10 C **TOP VIEW**

⫽ 0.05 C

⌖ 0.05 C **SIDE VIEW**

A3, A, A1, C SEATING PLANE

e, 5X L, L1, 6X b

1, 3, 6, 4

⊕ 0.10 Ⓜ C A B
  0.05 Ⓜ C NOTE 3

BOTTOM VIEW

RECOMMENDED SOLDERING FOOTPRINT*

5X 0.48
6X 0.22
1.18
0.53
0.35
PKG OUTLINE
PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

X M
1 ∘

X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON56787E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	UDFN6, 1x1, 0.35P		PAGE 1 OF 1

ON Semiconductor®

SOT−953
CASE 527AE
ISSUE E

DATE 02 AUG 2011

SCALE 4:1

TOP VIEW

PIN ONE INDICATOR

SIDE VIEW

BOTTOM VIEW

| ⊕ | 0.08 | X | Y |

SOLDERING FOOTPRINT*

5X
0.20

5X
0.35

PACKAGE
OUTLINE

1.20

1

0.35
PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
H_E	0.95	1.00	1.05
L	0.175 REF		
L2	0.05	0.10	0.15
L3	---	---	0.15

**GENERIC
MARKING DIAGRAM***

XM

1
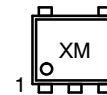
X = Specific Device Code
M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

DOCUMENT NUMBER:	98AON26457D	
DESCRIPTION:	SOT−953	PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

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