

# NLAS7242

## High-Speed USB 2.0 (480 Mbps) DPDT Switches

The NLAS7242 is a DPDT switch optimized for high-speed USB 2.0 applications within portable systems. It features ultra-low on capacitance,  $C_{ON} = 7.5$  pF (typ), and a bandwidth above 950 MHz. It is optimized for applications that use a single USB interface connector to route multiple signal types. The  $C_{ON}$  and  $R_{ON}$  of both channels are suitably low to allow the NLAS7242 to pass any speed USB data or audio signals going to a moderately resistive terminal such as an external headset. The device is offered in a UQFN10 1.4 mm x 1.8 mm package.

### Features

- Optimized Flow-Through Pinout
- $R_{ON}$ : 5.0  $\Omega$  Typ @  $V_{CC} = 4.2$  V
- $C_{ON}$ : 7.5 pF Typ @  $V_{CC} = 3.3$  V
- $V_{CC}$  Range: 1.65 V to 4.5 V
- Typical Bandwidth: 950 MHz
- 1.4 mm x 1.8 mm x 0.50 mm UQFN10
- OVT on Common Signal Pins D+/D- up to 5.25 V
- 8 kV HBM ESD Protection on All Pins
- This is a Pb-Free Device

### Typical Applications

- High Speed USB 2.0 Data
- Mobile Phones
- Portable Devices

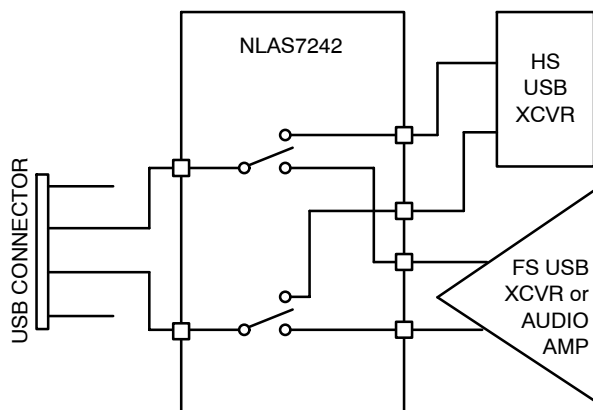


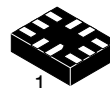
Figure 1. Application Diagram



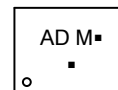
**ON Semiconductor®**

<http://onsemi.com>

### MARKING DIAGRAM



UQFN10  
CASE 488AT



AD = Device Code  
M = Date Code  
■ = Pb-Free Device

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NLAS7242MUTBG	UQFN0 (Pb-Free)	3000/Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NLAS7242

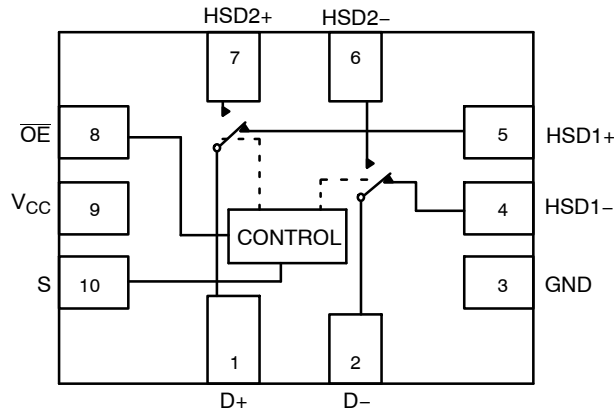


Figure 2. Pin Connections and Logic Diagram (Top View)

Table 1. PIN DESCRIPTION

Pin	Function
S	Control Input
$\overline{OE}$	Output Enable
HSD1+, HSD1-, HSD2+, HSD2-, D+, D-	Data Ports

Table 2. TRUTH TABLE

$\overline{OE}$	S	HSD1+, HSD1-	HSD2+, HSD2-
1	X	OFF	OFF
0	0	ON	OFF
0	1	OFF	ON

## MAXIMUM RATINGS

Symbol	Pins	Parameter	Value	Unit
$V_{CC}$	$V_{CC}$	Positive DC Supply Voltage	-0.5 to +5.5	V
$V_{IS}$	HSDn+, HSDn-	Analog Signal Voltage	-0.5 to $V_{CC} + 0.3$	V
	D+, D-		-0.5 to +5.25	
$V_{IN}$	S, $\overline{OE}$	Control Input Voltage, Output Enable Voltage	-0.5 to +5.5	V
$I_{CC}$	$V_{CC}$	Positive DC Supply Current	50	mA
$T_S$		Storage Temperature	-65 to +150	°C
$I_{IS\_CON}$	HSDn+, HSDn-, D+, D-	Analog Signal Continuous Current-Closed Switch	$\pm 300$	mA
$I_{IS\_PK}$	HSDn+, HSDn-, D+, D-	Analog Signal Continuous Current 10% Duty Cycle	$\pm 500$	mA
$I_{IN}$	S, $\overline{OE}$	Control Input Current, Output Enable Current	$\pm 20$	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Pins	Parameter	Min	Max	Unit
$V_{CC}$		Positive DC Supply Voltage	1.65	4.5	V
$V_{IS}$	HSDn+, HSDn-	Analog Signal Voltage	GND	$V_{CC}$	V
	D+, D-		GND	4.5	
$V_{IN}$	S, $\overline{OE}$	Control Input Voltage, Output Enable Voltage	GND	$V_{CC}$	V
$T_A$		Operating Temperature	-40	+85	°C

Minimum and maximum values are guaranteed through test or design across the Recommended Operating Conditions, where applicable. Typical values are listed for guidance only and are based on the particular conditions listed for section, where applicable. These conditions are valid for all values found in the characteristics tables unless otherwise specified in the test conditions.

## ESD PROTECTION

Symbol	Parameter	Value	Unit
ESD	Human Body Model - All Pins	8.0	kV

**DC ELECTRICAL CHARACTERISTICS**

**CONTROL INPUT, OUTPUT ENABLE VOLTAGE** (Typical: T = 25°C)

Symbol	Pins	Parameter	Test Conditions	V <sub>CC</sub> (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
V <sub>IH</sub>	S, $\overline{OE}$	Control Input, Output Enable HIGH Voltage (See Figure 11)		2.7	1.25	-	-	V
				3.3	1.3			
				4.2	1.4			
V <sub>IL</sub>	S, $\overline{OE}$	Control Input, Output Enable LOW Voltage (See Figure 11)		2.7	-	-	0.35	V
				3.3			0.4	
				4.2			0.5	
I <sub>IN</sub>	S, $\overline{OE}$	Current Input, Output Enable Leakage Current	0 ≤ V <sub>IS</sub> ≤ V <sub>CC</sub>	1.65 – 4.5	-	-	±1.0	μA

**SUPPLY CURRENT AND LEAKAGE** (Typical: T = 25°C, V<sub>CC</sub> = 3.3 V)

Symbol	Pins	Parameter	Test Conditions	V <sub>CC</sub> (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
I <sub>CC</sub>	V <sub>CC</sub>	Quiescent Supply Current	0 ≤ V <sub>IS</sub> ≤ V <sub>CC</sub> ; I <sub>D</sub> = 0 A	1.65 – 3.6	-	-	1.0	μA
			0 ≤ V <sub>IS</sub> ≤ V <sub>CC</sub> - 0.5 V	3.6 – 4.5	-	-	1.0	
I <sub>OZ</sub>		OFF State Leakage	0 ≤ V <sub>IS</sub> ≤ V <sub>CC</sub>	1.65 – 4.5	-	±0.1	±1.0	μA
I <sub>OFF</sub>	D+, D-	Power OFF Leakage Current	0 ≤ V <sub>IS</sub> ≤ V <sub>CC</sub>	0	-	-	±1.0	μA

**LIMITED V<sub>IS</sub> SWING ON RESISTANCE** (Typical: T = 25°C)

Symbol	Pins	Parameter	Test Conditions	V <sub>CC</sub> (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
R <sub>ON</sub>		On-Resistance (Note 1)	I <sub>ON</sub> = 8 mA V <sub>IS</sub> = 0 V to 0.4 V	2.7	-	6.0	8.6	Ω
				3.3		5.5	7.6	
				4.2		5.0	7.0	
R <sub>FLAT</sub>		On-Resistance Flatness (Notes 1 and 2)	I <sub>ON</sub> = 8 mA V <sub>IS</sub> = 0 V to 0.4 V	2.7	-	0.55	-	Ω
				3.3		0.30		
				4.2		0.20		
ΔR <sub>ON</sub>		On-Resistance Matching (Notes 1 and 3)	I <sub>ON</sub> = 8 mA V <sub>IS</sub> = 0 V to 0.4 V	2.7	-	0.60	-	Ω
				3.3		0.60		
				4.2		0.60		

1. Guaranteed by design.
2. Flatness is defined as the difference between the maximum and minimum value of On-Resistance as measured over the specified analog signal ranges.
3. ΔR<sub>ON</sub> = R<sub>ON(max)</sub> - R<sub>ON(min)</sub> between HSD1+ and HSD1- or HSD2+ and HSD2-.

**FULL V<sub>IS</sub> SWING ON RESISTANCE** (Typical: T = 25°C)

Symbol	Pins	Parameter	Test Conditions	V <sub>CC</sub> (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
R <sub>ON</sub>		On-Resistance	I <sub>ON</sub> = 8 mA V <sub>IS</sub> = 0 V to V <sub>CC</sub>	2.7	-	10	13.5	Ω
				3.3		8.0	9.75	
				4.2		7.0	8.50	
R <sub>FLAT</sub>		On-Resistance Flatness (Notes 4 and 5)	I <sub>ON</sub> = 8 mA V <sub>IS</sub> = 0 V to V <sub>CC</sub>	2.7	-	4.5	-	Ω
				3.3		3.0		
				4.2		2.5		
ΔR <sub>ON</sub>		On-Resistance (Note 4 and 6)	I <sub>ON</sub> = 8 mA V <sub>IS</sub> = 0 V to V <sub>CC</sub>	2.7	-	0.60	-	Ω
				3.3		0.60		
				4.2		0.60		

4. Guaranteed by design.
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance as measured over the specified analog signal ranges.
6. ΔR<sub>ON</sub> = R<sub>ON(max)</sub> - R<sub>ON(min)</sub> between HSD1+ and HSD1- or HSD2+ and HSD2-.

# NLAS7242

## AC ELECTRICAL CHARACTERISTICS

**TIMING/FREQUENCY** (Typical: T = 25°C, V<sub>CC</sub> = 3.3 V, R<sub>L</sub> = 50 Ω, C<sub>L</sub> = 35 pF, f = 1 MHz)

Symbol	Pins	Parameter	Test Conditions	V <sub>CC</sub> (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
t <sub>ON</sub>	Closed to Open	Turn-ON Time (See Figures 4 and 5)		1.65 – 4.5	–	13.0	30.0	ns
t <sub>OFF</sub>	Open to Closed	Turn-OFF Time (See Figures 4 and 5)		1.65 – 4.5	–	12.0	25.0	ns
T <sub>BBM</sub>		Break-Before-Make Time (See Figure 3)		1.65 – 4.5	2.0	–	–	ns
BW		-3 dB Bandwidth (See Figure 10)	C <sub>L</sub> = 5 pF	1.65 – 4.5	–	950	–	MHz

**ISOLATION** (Typical: T = 25°C, V<sub>CC</sub> = 3.3 V, R<sub>L</sub> = 50 Ω, C<sub>L</sub> = 5 pF)

Symbol	Pins	Parameter	Test Conditions	V <sub>CC</sub> (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
O <sub>IRR</sub>	Open	OFF-Isolation (See Figure 6)	f = 240 MHz	1.65 – 4.5	–	-22	–	dB
X <sub>TALK</sub>	HSDn+ to HSDn-	Non-Adjacent Channel Crosstalk	f = 240 MHz	1.65 – 4.5	–	-24	–	dB

**CAPACITANCE** (Typical: T = 25°C, V<sub>CC</sub> = 3.3 V, R<sub>L</sub> = 50 Ω, C<sub>L</sub> = 5 pF)

Symbol	Pins	Parameter	Test Conditions	-40°C to +85°C			Unit
				Min	Typ	Max	
C <sub>IN</sub>	S, $\overline{OE}$	Control Pin, Output Enable Input Capacitance	V <sub>CC</sub> = 0 V, f = 1 MHz	–	1.5	–	pF
			V <sub>CC</sub> = 0 V, f = 10 MHz	–	1.0	–	
C <sub>ON</sub>	D+ to HSD1+ or HSD2+	ON Capacitance	V <sub>CC</sub> = 3.3 V; $\overline{OE}$ = 0 V, f = 1 MHz S = 0 V or 3.3 V	–	7.5	–	pF
			V <sub>CC</sub> = 3.3 V; $\overline{OE}$ = 0 V, f = 10 MHz S = 0 V or 3.3 V	–	6.5	–	
C <sub>OFF</sub>	HSD1n or HSD2n	OFF Capacitance	V <sub>CC</sub> = V <sub>IS</sub> = 3.3 V; $\overline{OE}$ = 0 V, S = 3.3 V or 0 V, f = 1 MHz	–	3.8	–	pF
			V <sub>CC</sub> = V <sub>IS</sub> = 3.3 V; $\overline{OE}$ = 0 V, S = 3.3 V or 0 V, f = 10 MHz	–	2.0	–	

# NLAS7242

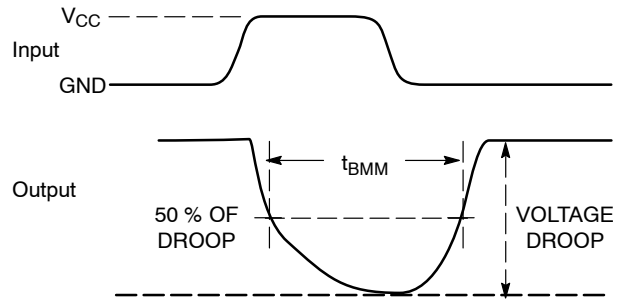
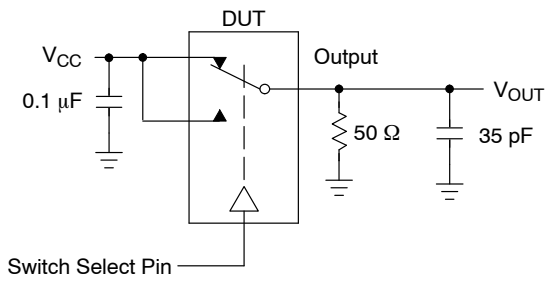


Figure 3.  $t_{\text{BMM}}$  (Time Break-Before-Make)

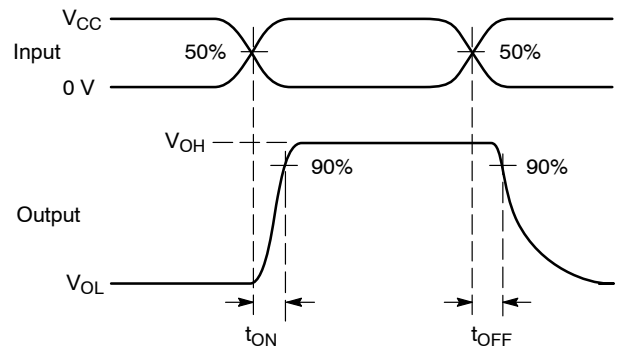
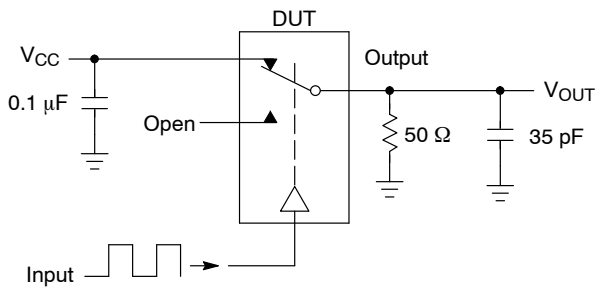


Figure 4.  $t_{\text{ON}}/t_{\text{OFF}}$

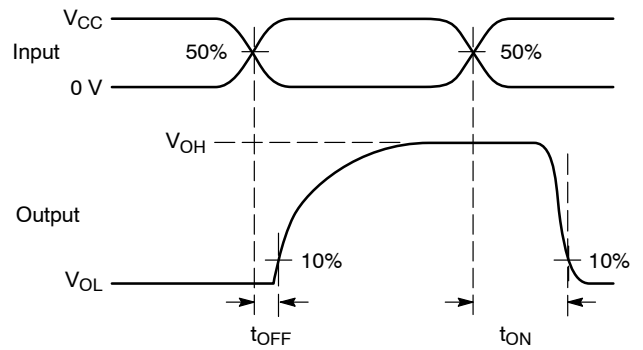
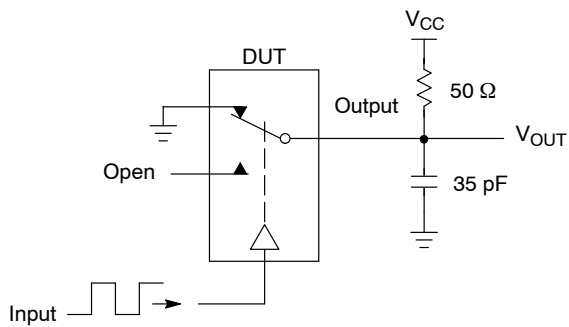
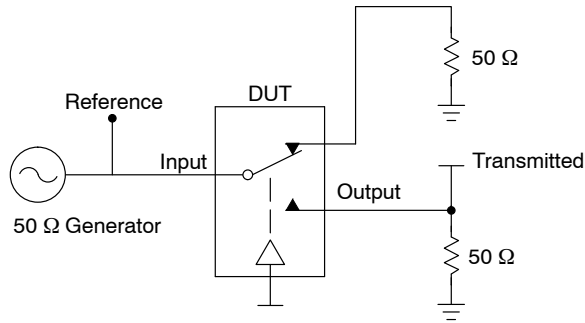


Figure 5.  $t_{\text{ON}}/t_{\text{OFF}}$

## NLAS7242



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch.  $V_{ISO}$ , Bandwidth and  $V_{ONL}$  are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left( \frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left( \frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below  $V_{ONL}$

$V_{CT}$  = Use  $V_{ISO}$  setup and test to all other switch analog input/outputs terminated with 50  $\Omega$

**Figure 6. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ $V_{ONL}$**

### DETAILED DESCRIPTION

#### High Speed (480Mbps) USB 2.0 Optimized

The NLAS7242 is a DPDT switch designed for USB applications within portable systems. The  $R_{ON}$  and  $C_{ON}$  of both switches are maintained at industry-leading low levels in order to ensure maximum signal integrity for USB 2.0 high speed data communication. The NLAS7242 switch can be used to switch between high speed (480Mbps) USB signals and a variety of audio or data signals such as full speed USB, UART or even a moderately resistive audio terminal.

#### Over Voltage Tolerant

The NLAS7242 features over voltage tolerant I/O protection on the common signal pins D+/D-. This allows the switch to interface directly with a USB connector. The D+/D- pins can withstand a short to  $V_{BUS}$ , up to 5.25 V, continuous DC current for up to 24 hours as specified in the USB 2.0 specification. This protection is achieved without the need for any external resistors or protection devices.

# NLAS7242

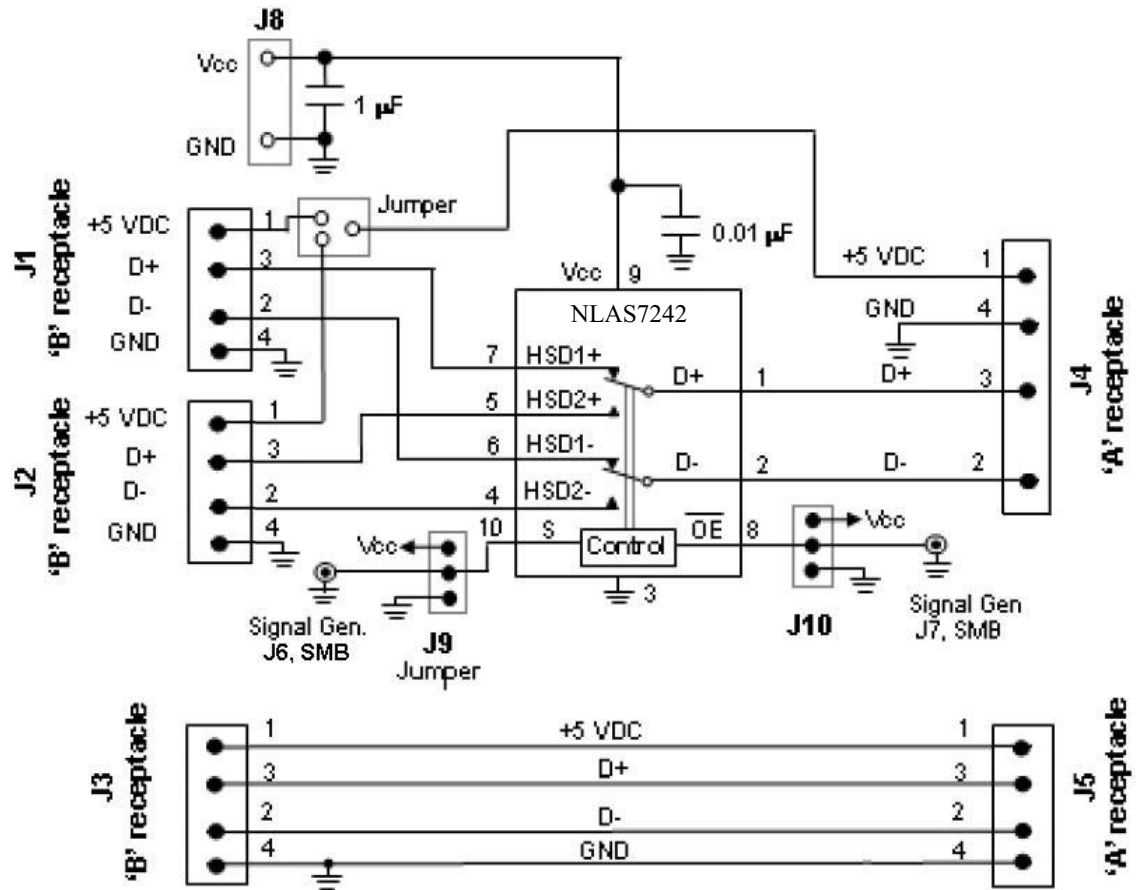


Figure 7. Board Schematic

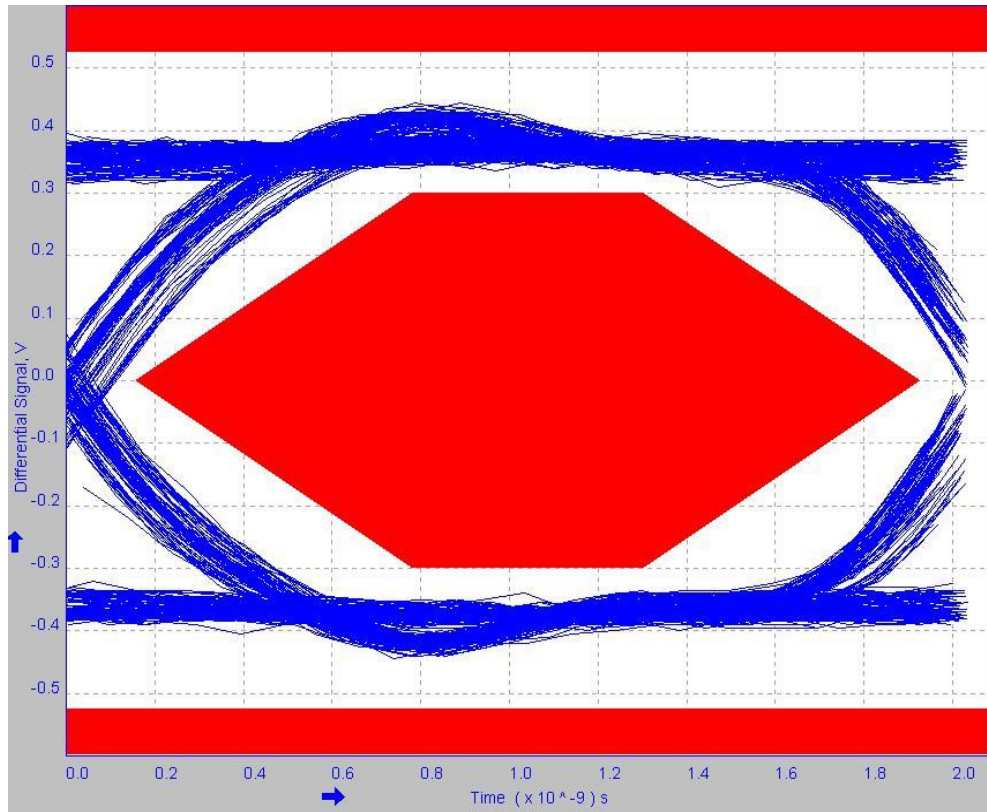


Figure 8. Signal Quality

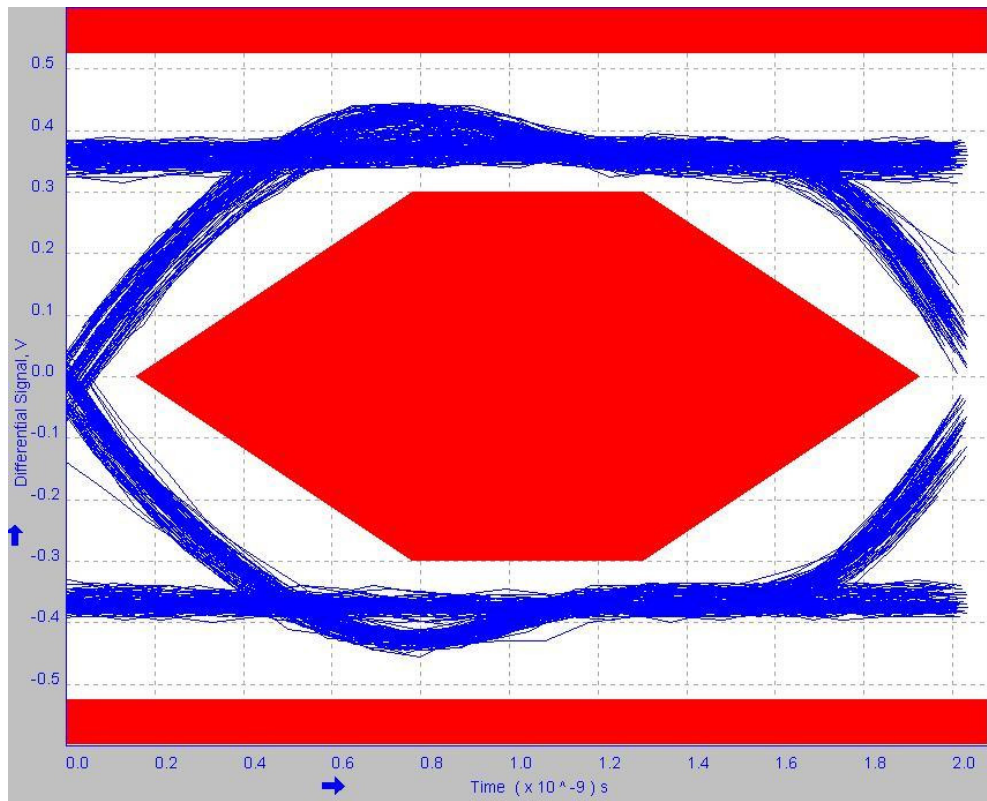
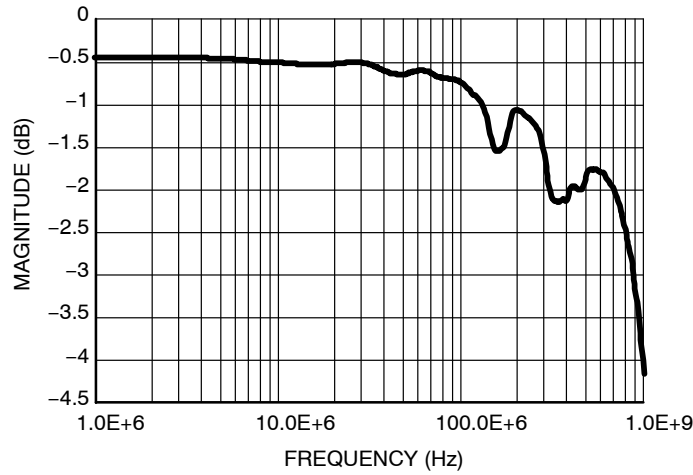


Figure 9. Near End Eye Diagram



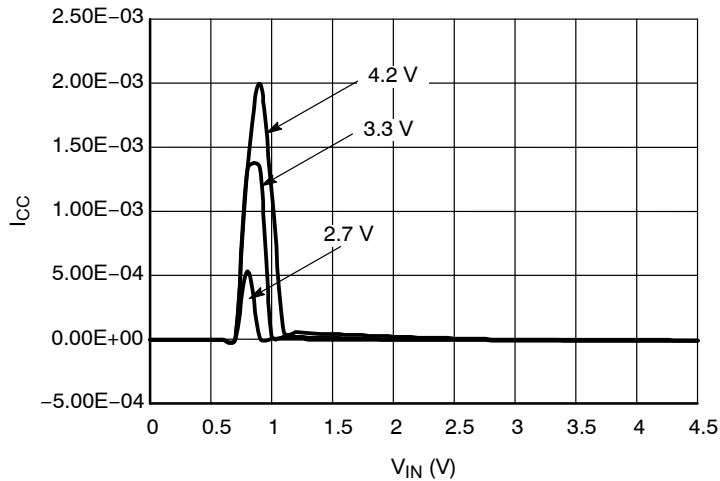
# NLAS7242

Near End Test Data:					Min	Max
Std.	Consecutive jitter range	-54.37	73.21	ps	-200 ps	+200 ps
	Paired JK jitter range	-59.14	59.56	ps		
	Paired KJ jitter range	-50.79	34.57	ps		
N.C.	Consecutive jitter range	-74.43	81.65	ps	-200 ps	+200 ps
	Paired JK jitter range	-61.60	58.55	ps		
	Paired KJ jitter range	-55.31	48.43	ps		
N.O.	Consecutive jitter range	-82.55	80.33	ps	-200 ps	+200 ps
	Paired JK jitter range	-53.50	71.65	ps		
	Paired KJ jitter range	-62.60	47.30	ps		



**Figure 10. Magnitude vs. Frequency  
@ V<sub>CC</sub> = 3.3 V, All Temperatures**

## I<sub>CC</sub> Leakage Current as a Function of V<sub>IN</sub> Voltage (25°C)



**Figure 11. I<sub>CC</sub> vs. V<sub>IN</sub>, Select Pin, All V<sub>CC</sub>'s, 25°C**

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

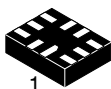
ON Semiconductor®



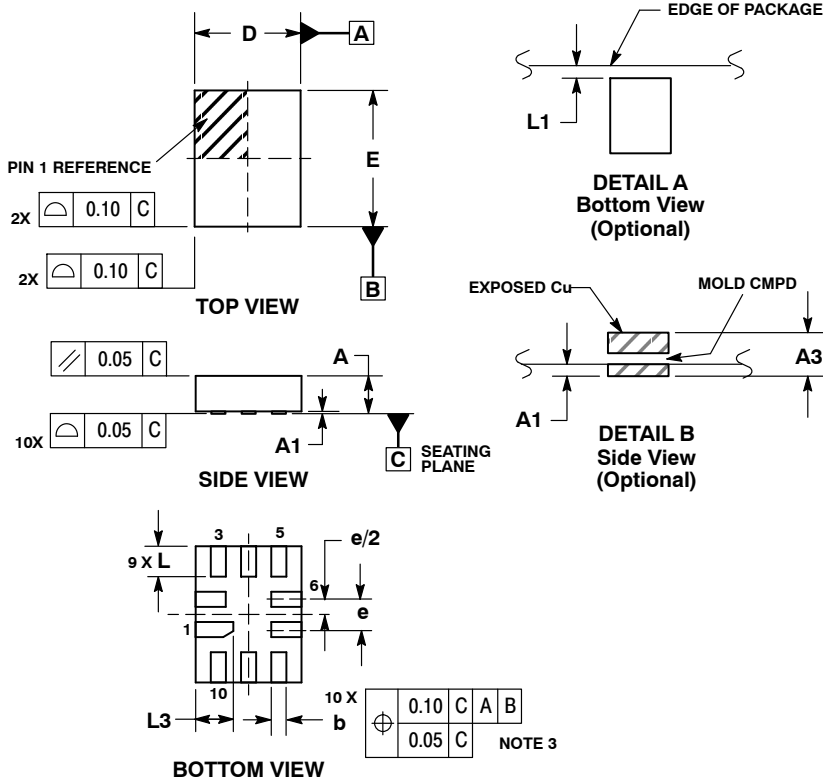
### UQFN10 1.4x1.8, 0.4P

CASE 488AT-01  
ISSUE A

DATE 01 AUG 2007

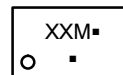


SCALE 5:1



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS
  3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
  4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

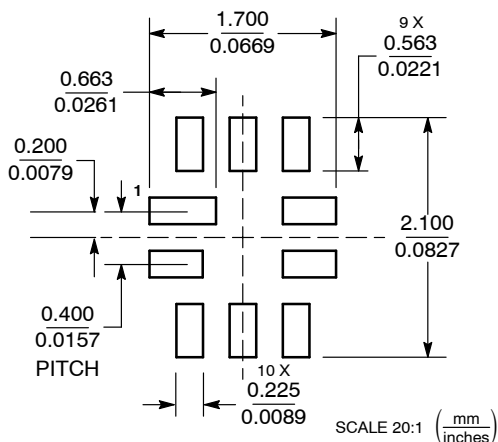
### GENERIC MARKING DIAGRAM\*



- XX = Specific Device Code
  - M = Date Code
  - = Pb-Free Package
- (Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

### MOUNTING FOOTPRINT



<b>DOCUMENT NUMBER:</b>	<b>98AON22493D</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>10 PIN UQFN, 1.4 X 1.8, 0.4P</b>	<b>PAGE 1 OF 1</b>

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**onsemi Website:** [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

**North American Technical Support:**

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative