UM1557
User manual

VIPower MO-5T: high-side switches for 24V systems

Introduction

The aim of this document is to give the design engineer a comprehensive “tool kit” to better understand the behavior of VIPower high side switches, allowing easier design and saving time and money.

This document expands on the existing VIPower user manual UM1556 rev.1 covering high side switches suited to 12 V (passenger car) automotive systems, by focusing on the new family of VIPower components for 24 V (truck) applications.

The drivers concerned derive from existing state-of-the-art M0-5 technology, but cover the even harsher environmental conditions found in truck applications.

Not only is the battery voltage doubled (which goes hand in hand with the increased ISO pulse levels), but the stray inductance of the wire harness is also significantly higher compared to passenger cars. The temperature range is the same as for passenger cars, but the required lifetime of the electronics is significantly higher due to the longer average life time of a truck.

The wires on a truck with a trailer can be as long as 30–40 meters, from the rear lights of the trailer to the ECU, located at the front of the truck. Due to the larger number of bulbs driven by the high side switch in a typical truck application, the typical load current is in the same range or even higher than in 12 V systems, despite the higher battery voltage.

The High Side Drivers in 24 V systems are therefore faced with high currents in combination with a high level of stray inductance during turn-off, as experienced in short circuit conditions of the load. This causes a high level of stress at that condition, necessitating new solutions to achieve short circuit robustness at the same or even higher levels than those achieved for current 12 V systems.

This document explains the function of the VIPower drivers for 24 V systems that cover the identified requirement profile.

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1 New features of 24 V drivers

In addition to the established family of M0-5*Enhanced* drivers, STMicroelectronics has introduced a new set of drivers for 24 V applications. On top of the M0-5*Enhanced* functions and protection mechanisms are the following additional features:

- Programmable Latch-off functionality (INx pin(s) high):
  - FR_Stby pin = low or left open:
    The drivers behave like M0-5*Enhanced* devices (autorestart in case of overload or thermal shutdown).
  - FR_Stby pin = high:
    The drivers latch-off in case of overload or thermal shutdown. In order to unlatch the channel(s), a low level pulse on FR_Stby pin is required for minimum duration of $t_{RESET.}$
- Programmable stand-by mode (INx pins(s) low):
  - FR_Stby pin=low or left open:
    A permanent low level on both the INx and fault reset standby pin disables all outputs and sets the devices in standby mode (open load diagnostic in off-state is disabled).
  - FR_Stby pin=high:
    The drivers behave like M0-5*Enhanced* devices (open load diagnostic in off-state enabled).

1.1 Programmable latch-off functionality

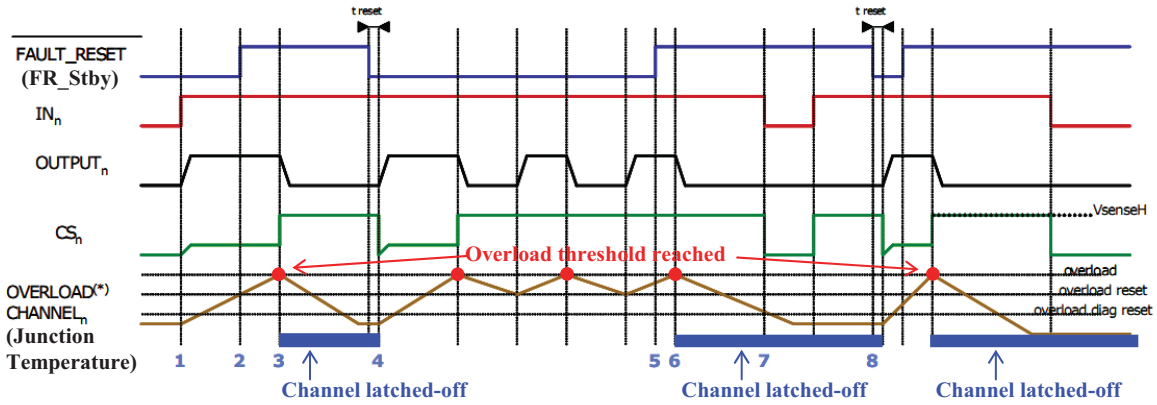
The latch-off functionality is available when the FR_Stby pin (logic input) is set high. This pin is common for all device channels.

In case of an overload, the related channel is automatically latched-off at the first intervention of either power limitation or thermal shutdown. The latch condition is indicated by V_{SENSEH} level on the related current sense pin (only if the input pin is set high).

All latched channels can be restarted by setting the FR_Stby pin low for a minimum time of t_{RESET} (> 24 µs).

A graphical explanation of the latch-off functionality can be seen in *Figure 1* and *Figure 2*.

Figure 1. Latch functionality – behavior in overload condition



1: $OUTPUT_n$ and CS_n controlled by IN_n.

2: FAULT_RESET from '0' to '1' →no action on CS_n pin

3: Overload latch-off. INn high →CS_n high

4: FAULT_RESET low AND Temp channeln < overload_reset →Overload latch reset after t_reset

4 to 5: FAULT_RESET low AND IN_n high →thermal cycling, CS_n high

5: FAULT_RESET high →latch-off reset disabled

6 to 7: Overload event and FAULT_RESET high →latch-off, no thermal cycling

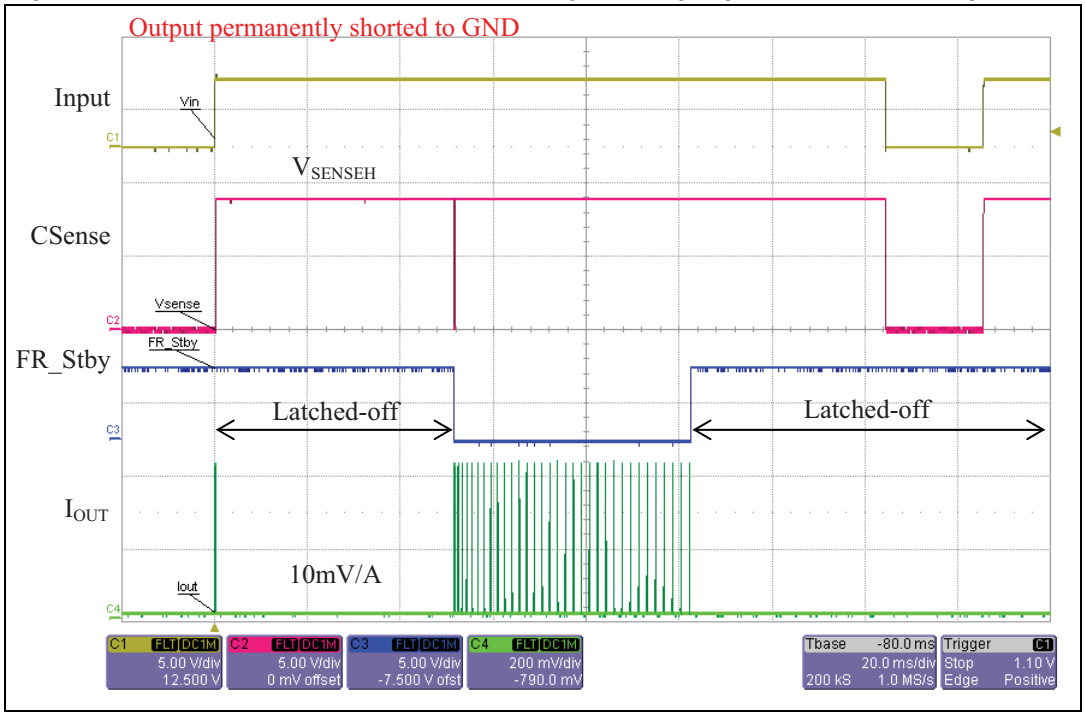
7 to 8: Overload diagnostic disabled/enabled by the input

8: Overload latch-off reset by FAULT_RESET

(*) OVERLOAD = Thermal shutdown OR Power Limitation

GAPGMS00140

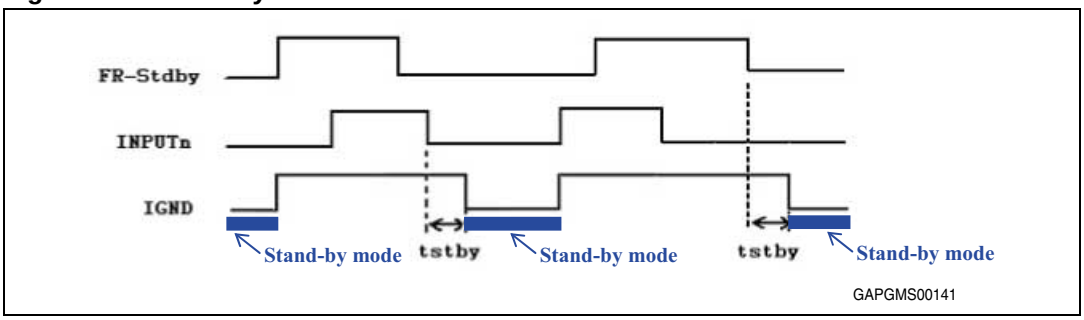
Figure 2. VND5T035AK – latch functionality check (output shorted to GND)



1.2 Programmable stand-by mode

The Stand-by mode is available when the FR_Stby pin and all INx pins are set low (or left open). In this condition, the supply current drops down to 2 µA (typically) with a typical delay of t_{stby} = 500 µs (see *Figure 3*). The open load diagnostic in off-state is disabled since the FR_Stby pin is pulled low (or left open).

Figure 3. Stand-by mode activation



The device exits Stand-by mode when any FR_Stby pin or INx pin is set high. When the FR_Stby pin is high, the open load diagnostic in off-state is available. Thus the CS pin(s) provides V_{SENSEH} in case of $V_{OUT} > V_{OL}$ (same behaviour as M0-5*Enhanced* devices).

Table 1. Diagnostic truth table

Conditions	Fault reset standby	Input	Output	Sense
Standby	L	L	L	0
Normal operation	X X	L H	L H	0 Nominal
Overload	X X	L H	L H	0 >Nominal
Overtemperature/ short to ground	X L H	L H H	L Cycling Latched	0 V_{SENSEH} V_{SENSEH}
Undervoltage	X	X	L	0
Short to V_{BAT}	L H X	L L H	H H H	0 V_{SENSEH} <Nominal
Open load off-state (with pull-up)	L H X	L L H	H H H	0 V_{SENSEH} 0
Negative output voltage clamp	X	L	Negative	0

2 General items

2.1 Application schematic (monolithic and hybrid analogue HSD)

In comparison with the established M0-5*Enhanced* drivers (12 V), there is a new FR_Stby pin (there is no CS_DIS pin) used for fault reset and mode selection (autorestart/latch-off, standby/open load in off-state).

Figure 4. Monolithic analogue HSD–application schematic

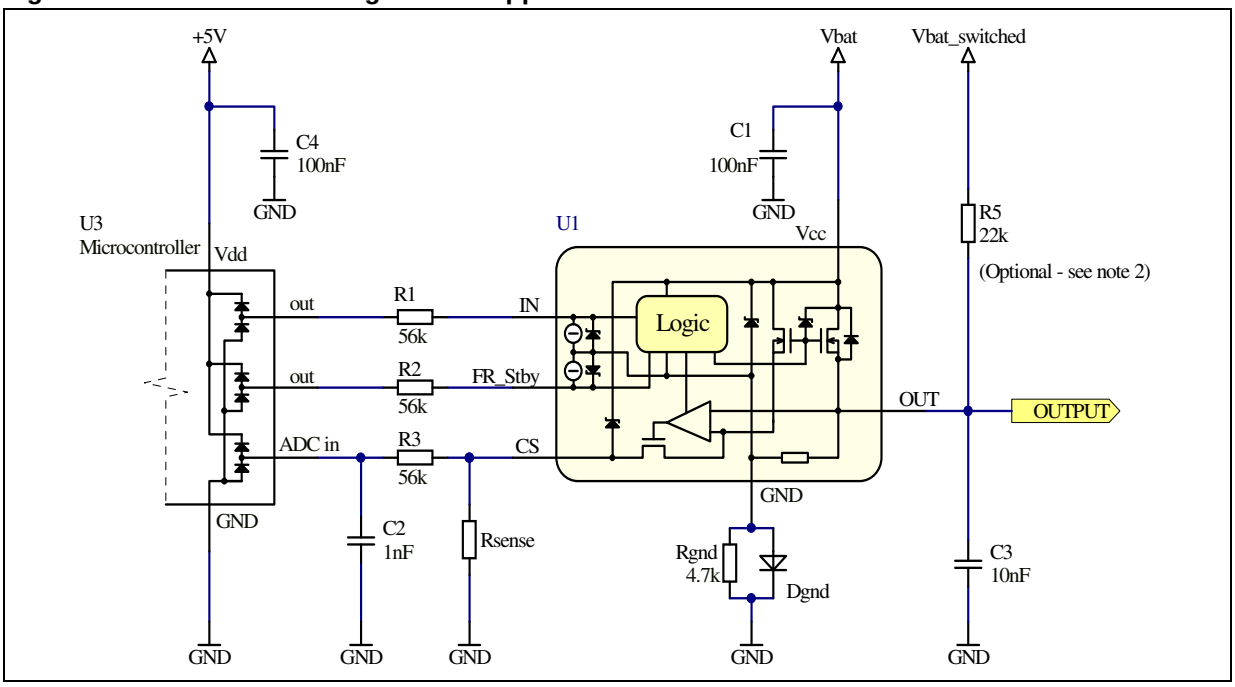
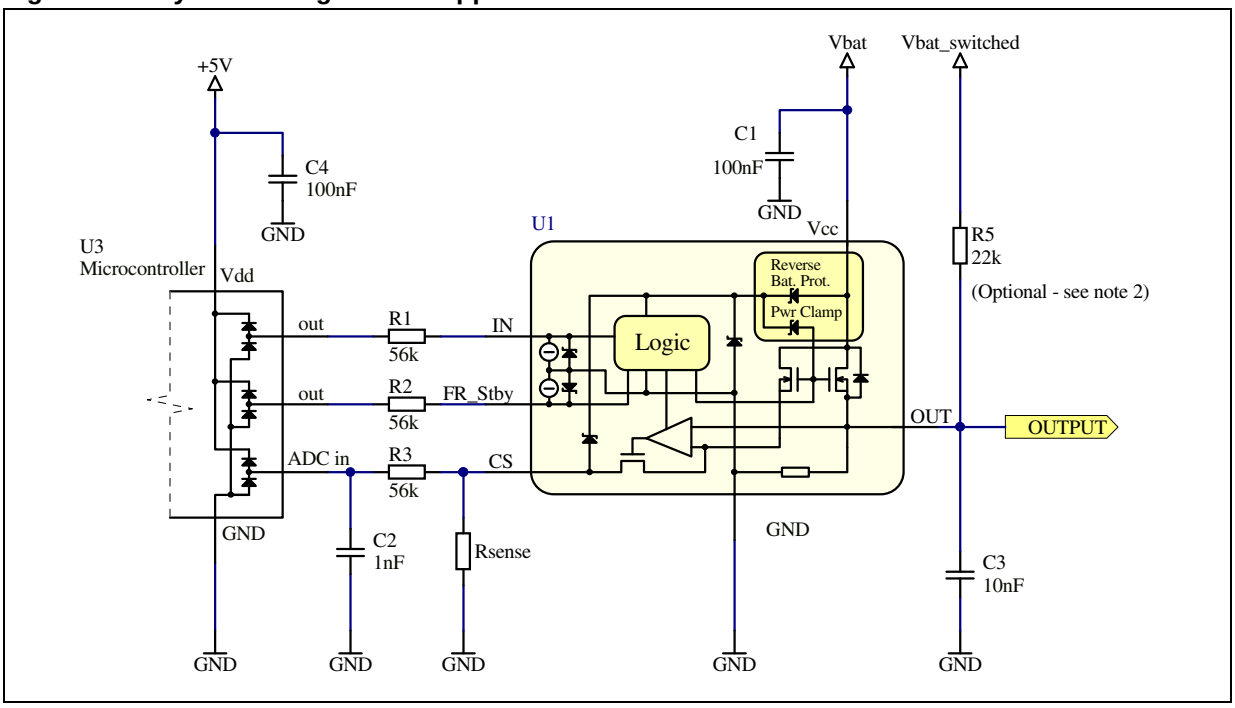


Figure 5. Hybrid analogue HSD–application schematic



1. If latch functionality or open load detection in off-state is not required, the FR_Stby pin should be left open or connected to ground through a resistor (~56 k). Direct connection to ground is not safe (ISO pulses clamped through FR_Stby pin can damage the device).

– ISO pulses refered to ISO 7637-2: 2004(E)

2. Pull-up R5 is optional (open load detection in off-state)

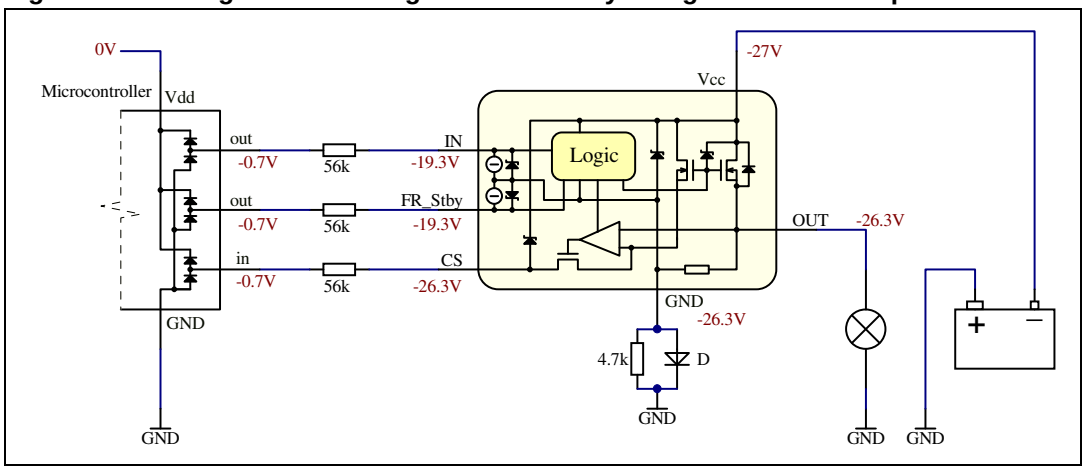
2.2 Reverse battery protection

2.2.1 Reverse battery protection of monolithic HSDs

The reverse battery protection is applied to the GND terminal of the driver. There are several possible solutions: diode, resistor plus diode or MOSFET circuitry. As there is a relatively low current in the GND path, no high power components are needed. However, this protection circuit still must be able to handle the clamped ISO pulse current as well as the ISO pulse voltage. We also have to consider the fact that this simple “ground” circuitry doesn’t provide any protection of the connected load. If a reverse battery condition occurs, the load is supplied in reverse polarity through the internal body diode of the HSD and the power dissipation on the HSD can become critical (depending on connected load and thermal connection of the HSD). The typical voltage drop on the internal body diode is about 0.7 V. The resulting power dissipation $P_D = 0.7\ I_{LOAD}$ [W].

Reverse battery protection using diode plus resistor

Figure 6. Voltage levels during reverse battery using diode-resistor protection



A diode at the GND terminal prevents a short circuit through the internal substrate diode of the HSD during a reverse battery condition.

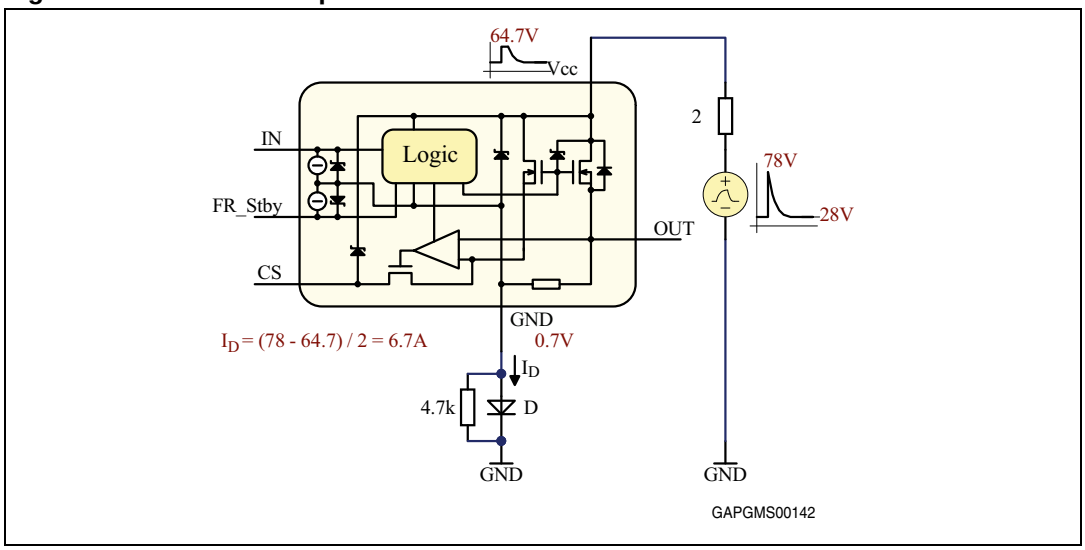
A resistor (max. 4.7 kΩ) connected in parallel to the diode is recommended (not mandatory) in case the device drives a high inductance load with a demagnetization time longer than t_{stby}. The purpose of this resistor is to suppress a negative voltage on the GND pin during standby mode if the demagnetization phase is still ongoing. Without this resistor, the low supply current in standby mode (2 µA typically) allows the GND pin to be pulled negative by the demagnetization voltage on the output (~ -40 V) via an internal pull-down resistor (~120 kΩ, not specified) on the output (see *Figure 9*, *Figure 10*). If the negative ground shift exceeds the input high level threshold (V_{IH} = 2,1 V min.), the device leaves standby mode and tends to turn on. The GND pin is immediately pulled high (~600 mV) by the increased supply current so that standby mode is activated again after t_{stby} delay. As a result, we may see short negative peaks on the GND pin with a period of t_{stby} during the whole demagnetization phase. These peaks are not long enough to activate the HSD output, which means the device works safely even without the GND resistor. However, this resistor is still recommended in order to suppress the described parasitic oscillations (if T_{DEMAG} > t_{stby}).

This ground network can be safely shared amongst several different HSDs. The presence of the ground network produces a shift (~ 600 mV) in the input threshold. This shift does not vary if more than one HSD share the same diode/resistor. A diode at the GND terminal allows the High-Side Driver to clamp positive ISO pulses above 64 V (the typical clamping voltage of the HSD). Negative ISO pulses still pass GND and logic terminals. The diode should withstand clamped ISO currents in case of positive ISO pulses and reverse voltages in case of negative ISO pulses.

Dimensioning of the diode[a] :

The most severe positive ISO pulse to consider is test pulse 2 at level IV (50 V@50 µs). This voltage is considered on top of the nominal supply voltage of 28 V – so the total voltage is 78 V. The VIPower has a clamping voltage of typ. 64 V (min. 58 V/max. 70 V). For a typical device, the remaining voltage is 78 V - 64 V - 0.7 V = 13.3 V. The ISO pulse generator interior resistance is given with 2 Ω. Hence, the resulting peak current through the diode is 6.7 A for a duration of 50 µs.

Figure 7. Positive ISO pulse

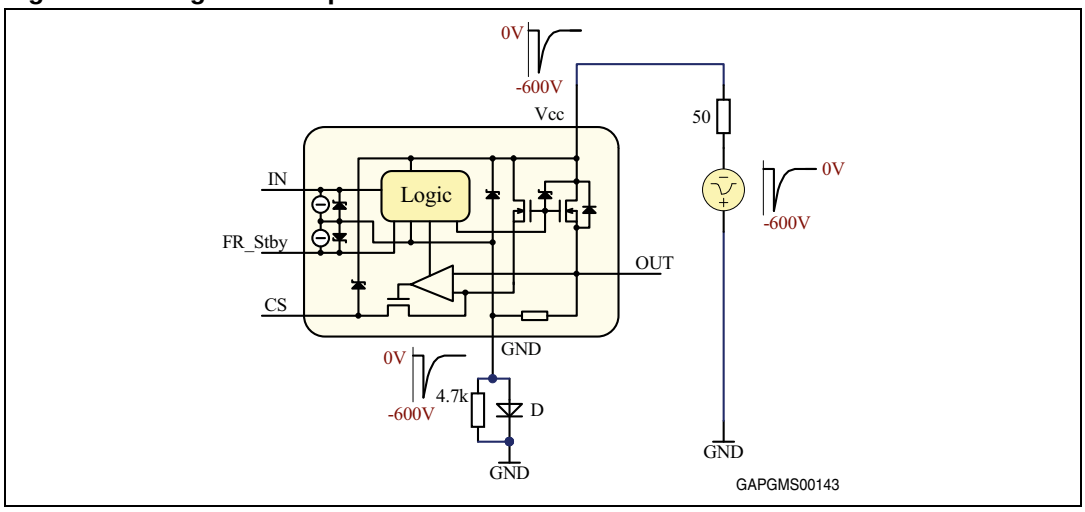


The most severe negative ISO pulse we have to consider is test pulse 1 at level IV (-600 V@1 ms). This pulse is directly transferred to the GND pin via the internal clamping. Hence, the maximum peak reverse voltage of the diode should be at least 600 V.

Note: The diode works in avalanche mode if the pulse level is above the rated reverse voltage.

a. Result:
Max. peak forward current: 6.7 A @ 50 µs
Max. reverse voltage: -600 V

Figure 8. Negative ISO pulse



Note: As seen from the above explanation, the HSD with a diode protection at the GND pin doesn't clamp negative ISO pulses on the supply line. Therefore an appropriate serial protection resistor should be used between the µC and HSD. The resistor value should be calculated according to the maximum injected current to the I/O pin of the used microcontroller.

Note: Diode parameters can be lower if an external clamping circuitry is used (e.g., the HSD module is supplied from a protected power supply line).

Dimensioning of the resistor [(b)]:

The GND resistor is recommended in case of a high inductivity load. To determine whether the resistor is needed, we need to know the demagnetization time (T_{DEMAG}). The resistor is recommended if T_{DEMAG} is higher than the standby delay time (t_{stby}).

A minimum t_{stby} value of 120 µs (as specified in the datasheet) is considered in this comparison.

b. Summary – dimensioning of the resistor:

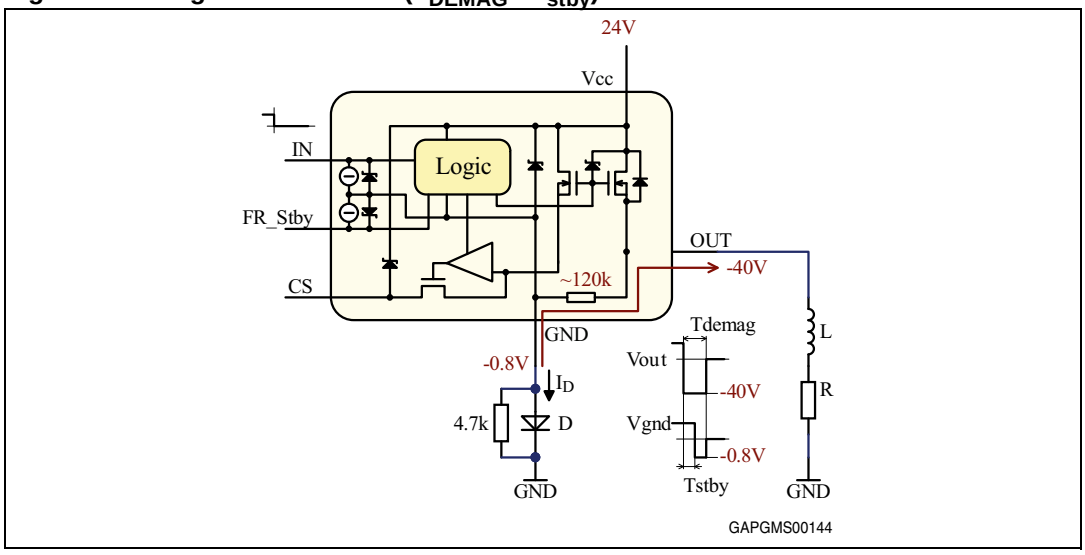
Resistor recommended if:$T_{DEMAG} > t_{stby}$

Resistance:4.7 k (or lower)

Voltage capability:min. 600 V (ISO pulse 1 at level IV)

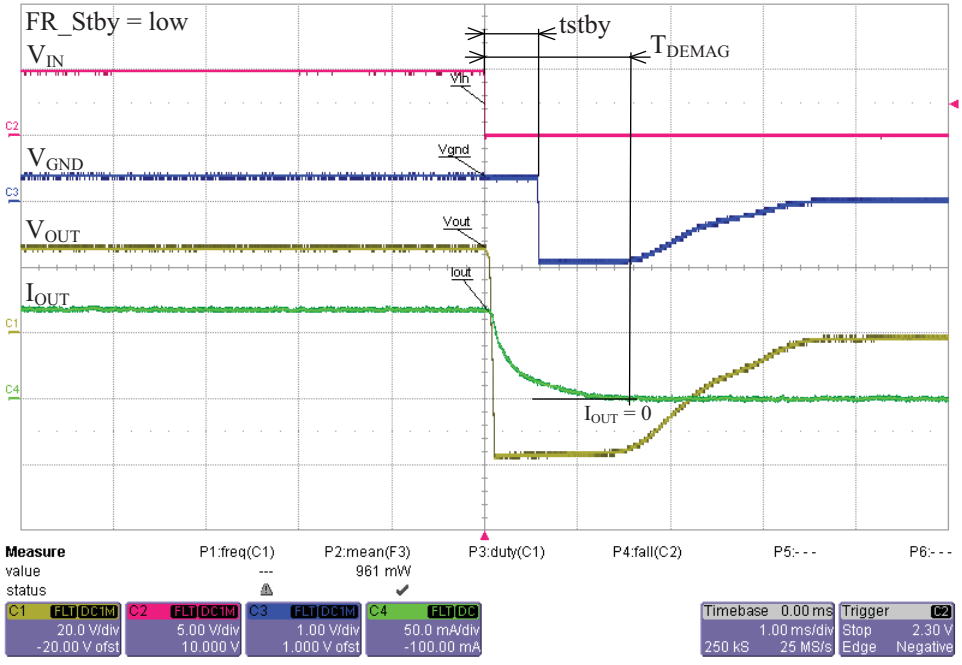
Power dissipation (reverse batt.):min. 167 mW (4.7 k) => Package 1206

Figure 9. Negative GND shift (T_{DEMAG} > t_{stby})



T_{DEMAG} can be determined either by measurement (*Figure 10*) or calculation using *Equation 1* and *Equation 2*.

Figure 10. Measurement example – T_{DEMAG} > t_{stby} (R_{GND} = 6.8 k, relay 880 mH/280 Ω)



The value of the resistor should be low enough to ensure that the negative voltage at the GND pin is suppressed as much as necessary to keep the device off. This means the V_{GND} should be kept above -2.1 V (assuming V_{IN} = 0 V, minimum input high level voltage V_{IH} = 2.1 V). Assuming the value of the internal pull-down at the output (R_{OUT}) of 120 kΩ and neglecting the device standby current, the maximum value of the GND resistor is given by a simple resistor divider calculation:

$$R_{GND} < R_{OUT} \cdot \frac{V_{GND}}{V_{DEMAG} - V_{GND}} = 120k \cdot \frac{-2.1V}{-40V + 2.1V} = 6.6k$$

→ considering a certain safety margin, a maximum 4.7 kΩ value is recommended

The minimum resistor value is determined by the maximum DC reverse ground pin current of the HSD in a reverse battery condition:

$$R_{GND} \geq \frac{V_{BAT(reverse)}}{I_{GND(reverse)\max}} = \frac{28V}{200mA} = 140ohm$$

In order to keep the power dissipation on the resistor during a reverse battery condition as low as possible, it is better to select the resistor value close to the maximum value (4.7 kΩ).

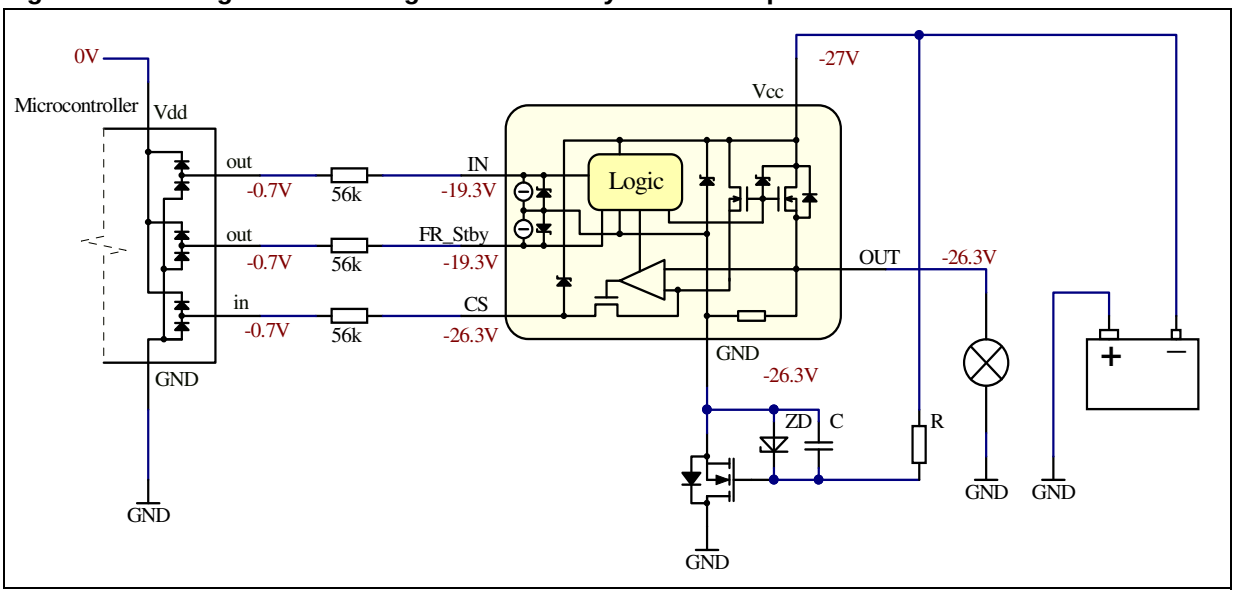
$$P_D = \frac{V_{BAT(reverse)}^{\ 2}}{R_{GND}} = \frac{28V^2}{4.7k} = 0.167W$$

→ Package 1206

(Power rating of 1206 is 0.25 W@70 °C)

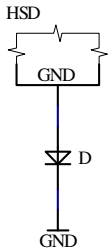
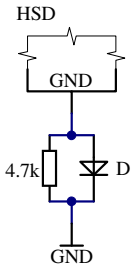
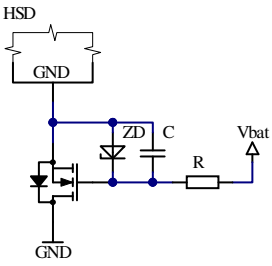
Reverse battery protection using MOSFET

Figure 11. Voltage levels during reverse battery – MOSFET protection



The HSD is protected by a MOSFET which is switched-off during a reverse battery condition. This MOSFET circuitry also provides full ISO pulse clamping at supply line and causes no ground level shift. A capacitor between gate and source keeps the gate charged even during negative ISO pulses. The time constant given by RC values should be longer than 1 ms (duration of the negative ISO7637 pulse 1).

Table 2. Reverse battery protection (of monolithic HSDs only) – comparison

Protection type (monolithic HSD)	+	-
1) Diode 	Fixed voltage drop. Positive ISO-pulse clamping (>64 V). Any type of load.	Negative ISO-pulse transfer to input and diagnostics pin (serial protection resistors necessary). Possibility of parasitic oscillations on the GND pin during turn-off of the high inductivity load (when $T_{DEMAG} > t_{stby}$).
2) Resistor and Diode 	Fixed voltage drop Positive ISO-pulse clamping (>64V). Any type of load.	Negative ISO-pulse transfer to input and diagnostics pin (serial protection resistors necessary).
3) MOSFET 	Any type of load. No voltage drop. No ISO-pulse transfer to input and diagnostics pin.	Higher cost (more external components needed).

2.2.2 Reverse battery protection of hybrid HSDs

In contrast to monolithic devices, all hybrid VIPower HSDs do not need any external components to protect the internal logic in case of a reverse battery condition. The protection is provided by internal structures (see “Reverse Battery Protection” in *Figure 12*).

Also, due to the fact that the output MOSFET automatically turns on in reverse battery mode and thus provides the same low ohmic path as in regular operation conditions, no additional power dissipation has to be considered.

Furthermore, if for example, a diode is connected to the GND of a hybrid HSD the output MOSFET is unable to turn on and thus the unique feature of the driver is disabled (see *Figure 13*).

Figure 12. Hybrid HSD – reverse battery protection with self switch-on of the MOSFET

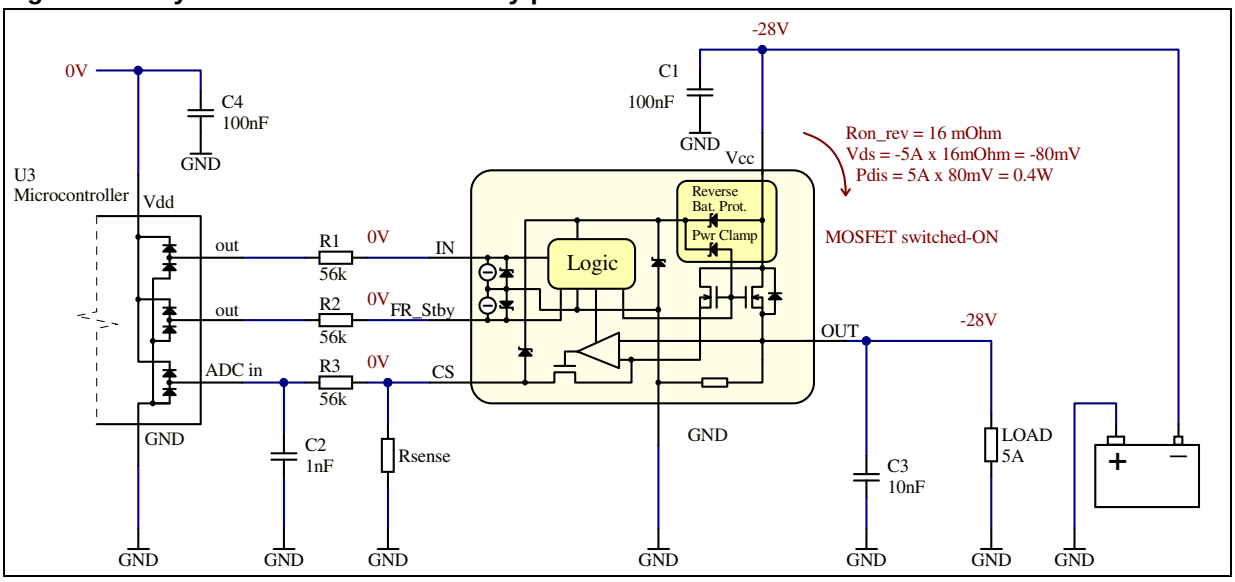
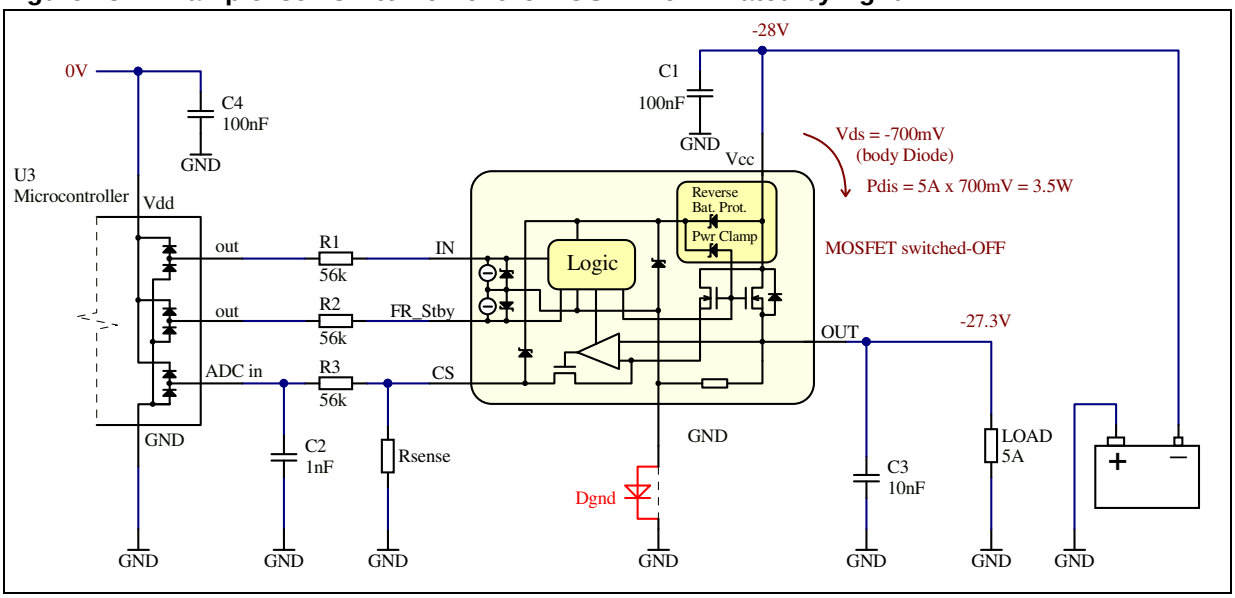


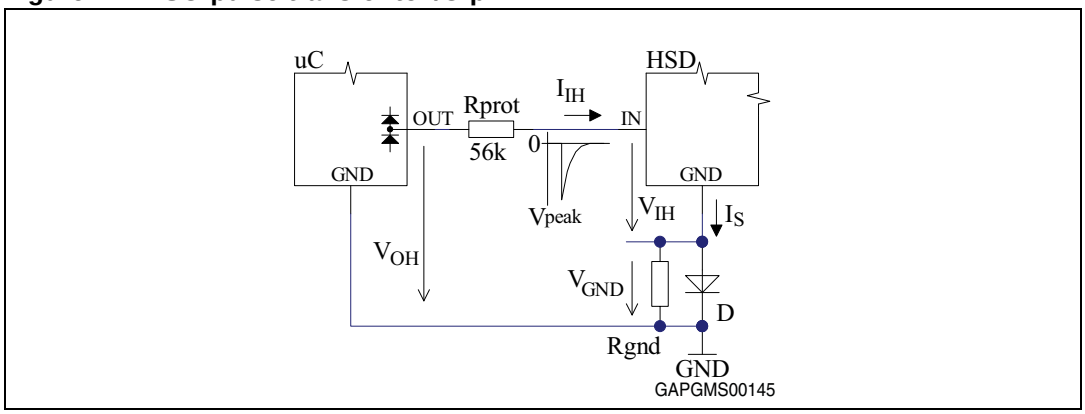
Figure 13. Example–self switch-on of the MOSFET eliminated by Dgnd



2.3 Microcontroller protection

If ISO pulses or a reverse battery condition appears, the HSD control pins can be pulled to dangerous voltage levels due to the internal HSD structure and ground protection network (as seen in *Section 2.2: Reverse battery protection*).

Figure 14. ISO-pulse transfer to I/O pin



Therefore, each microcontroller I/O pin connected to a HSD must be protected by a serial resistor to limit the injected current. The value of R_{PROT} must be high enough to ensure that the injected current is always below the latch-up limit of the microcontroller I/O. We should also consider the voltage drop on R_{PROT} because the current required by the HSD input is typically 10 µA. The following condition must be fulfilled:

$$\frac{V_{PEAK}}{I_{(\mu C)LATCHUP}} \leq R_{PROT} \leq \frac{V_{OH} - (V_{IH} + V_{GND})}{I_{IH}}$$

Example:

$$\frac{600V}{20mA} \leq R_{PROT} \leq \frac{4.5V - (2.1V + 0.6V)}{10\mu A}$$

$$30k\Omega \leq R_{PROT} \leq 180k\Omega$$

Recommended R_{PROT} value is 56 kΩ (safe value for most automotive microcontrollers).

3 Analogue current sense

3.1 Introduction

With the introduction of the VIPower M0-5 technology, important improvements have been introduced in the analog current sense operation.

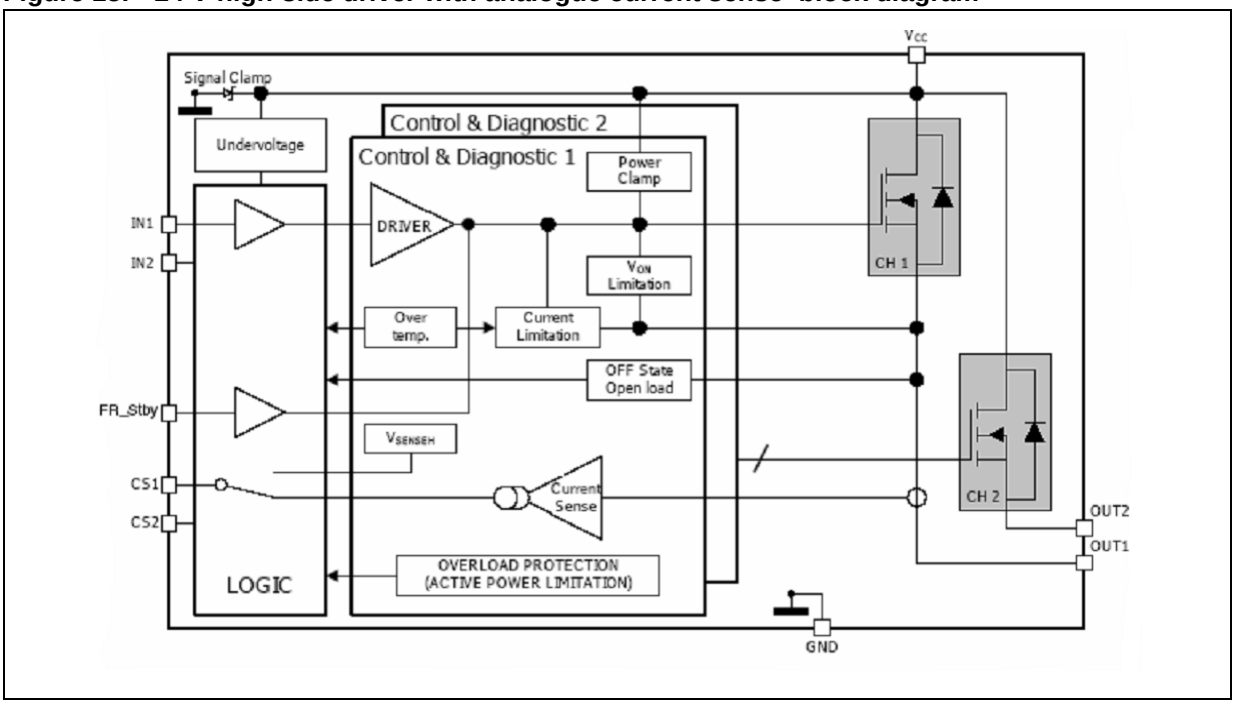
The block diagram of a M0-5 high-side driver with analog current sense is shown in *Figure 16*.

As with the previous generations, the current sense block has a double function:

- Current mirror of the load current in normal operation, delivering a current proportional to the load current according to a known ratio named K;
- Diagnostics flag in fault conditions, delivering a fixed voltage with a certain current capability in case of overload and open load in off-state condition.

The current delivered by the current sense circuit can be easily converted to a voltage by means of an external sense resistor, thus allowing continuous load monitoring and fault condition detection.

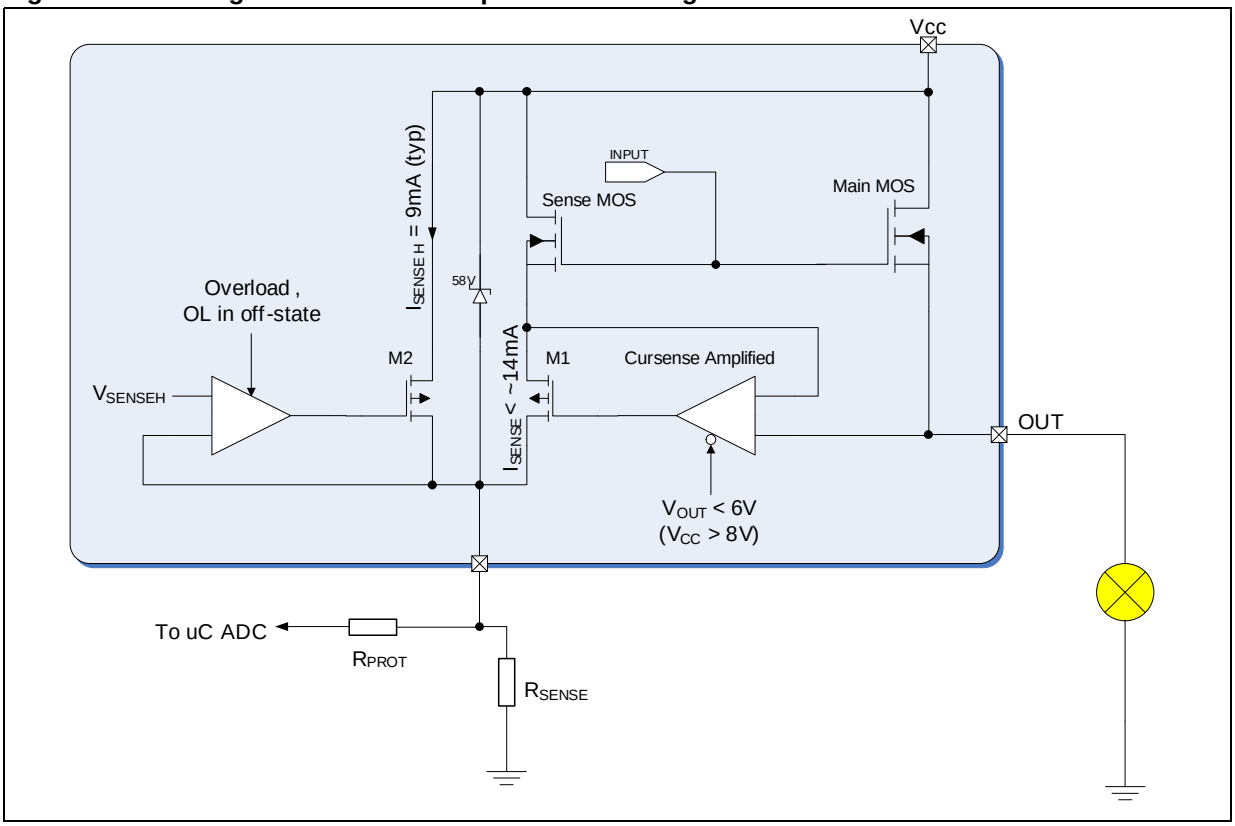
Figure 15. 24 V high-side driver with analogue current sense–block diagram



3.2 Principle of operation

The simplified block diagram of the analog current sense is illustrated in *Figure 16*.

Figure 16. Analog current sense simplified block diagram



The SenseMOS is a scaled down copy of the MainMOS according to a defined geometric ratio, driven by the same gate control circuit as the MainMOS.

The current flowing through the MainMOS is mirrored by the SenseMOS.

The current delivered by the current sense pin is regulated by the current sense amplifier through the P channel MOSFET M1 so that:

$$V_{DS\_Main} = V_{DS\_Sense} \rightarrow R_{ds\_sense} \cdot I_{sense} = R_{DS\_Main} \cdot I_{out}$$

and consequently

$$V_{sense} = R_{sense} \cdot I_{out} / K$$

where

$$K \propto R_{ds\_sense} / R_{DS\_Main}$$

encloses the geometric ratio, the current sense amplifier offset and various process parameter spreads.

Care must be taken in order to ensure the I_{sense} is proportional to I_{OUT}. Indeed, the maximum drop across the R_{SENSE} is internally limited to approx. 8.5 V as specified in the

datasheet by the parameter V_{SENSE} “maximum analog sense output voltage” (5 V minimum @ 8 V< Vcc < 36 V; -40 °C < Tj < 150 °C).

Example 1 – V_{SENSE} saturation (8.5 V typ.):

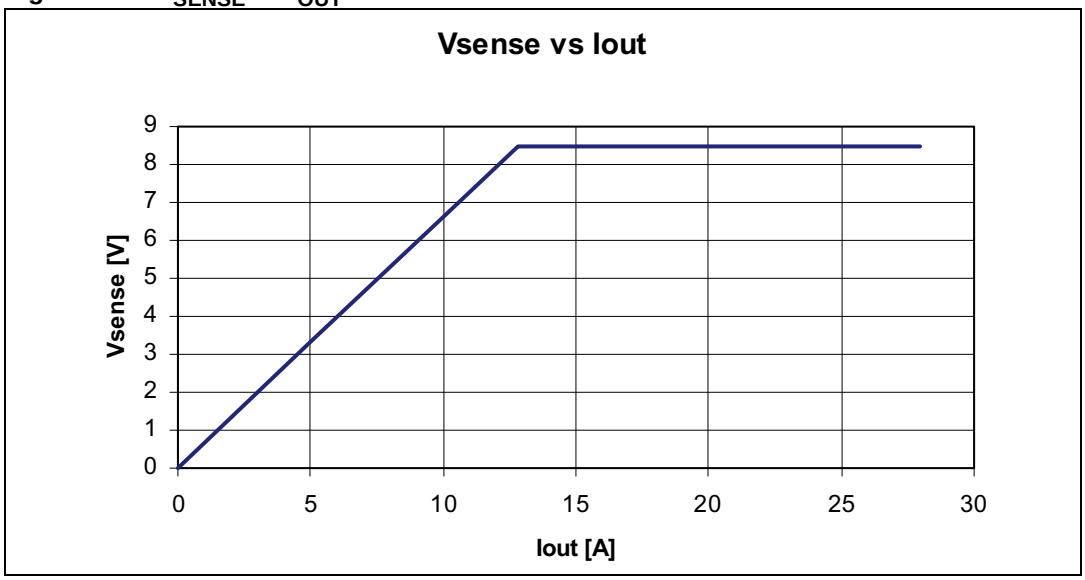
VND5T035AK with R_{SENSE} selected in order to have V_{SENSE}=2 V @ Iout = 3 A

Considering (for sake of simplicity) K_2 @ 3 A = 2870 (typical value) → I_{SENSE} = ~1 mA → R_{SENSE} = ~1.9 k

Assuming a typical V_{SENSE} saturation of 8.5 V → maximum I_{SENSE} = 4.5 mA to maintain linearity → maximum I_{OUT} = 12.8 A.

In other words, with the selected R_{SENSE} any load current higher than 12.8 A produces the same V_{SENSE} (see *Figure 17*).

Figure 17. V_{SENSE} vs I_{OUT}



On the other hand, care must be taken to prevent the P channel MOSFET M1 from saturation, causing the I_{SENSE} to again be disproportional with I_{OUT}. This normally happens when the maximum current that M1 is able to supply is reached (~14 mA).

This value is consistent with the current sense operating range and current limitation value.

Example 2 – I_{SENSE} saturation (~14 mA):

VND5T035AK with R_{SENSE} selected in order to have V_{SENSE}=1.5 V @ Iout = 10 A

Considering (for sake of simplicity) K_3 @ 10 A = 2895 (typical value) →

I_{SENSE} = 3.45 mA → R_{SENSE} = 430 Ω

Assuming a typical I_{SENSE} saturation of 14 mA and K to remain approx. 2895 for I_{OUT} > 10 A, the maximum load current which can be detected is

$$I_{OUT} = I_{SENSE\_MAX} \cdot K \cong 40.5A$$

This value is compatible with the typical I_{LimH}.

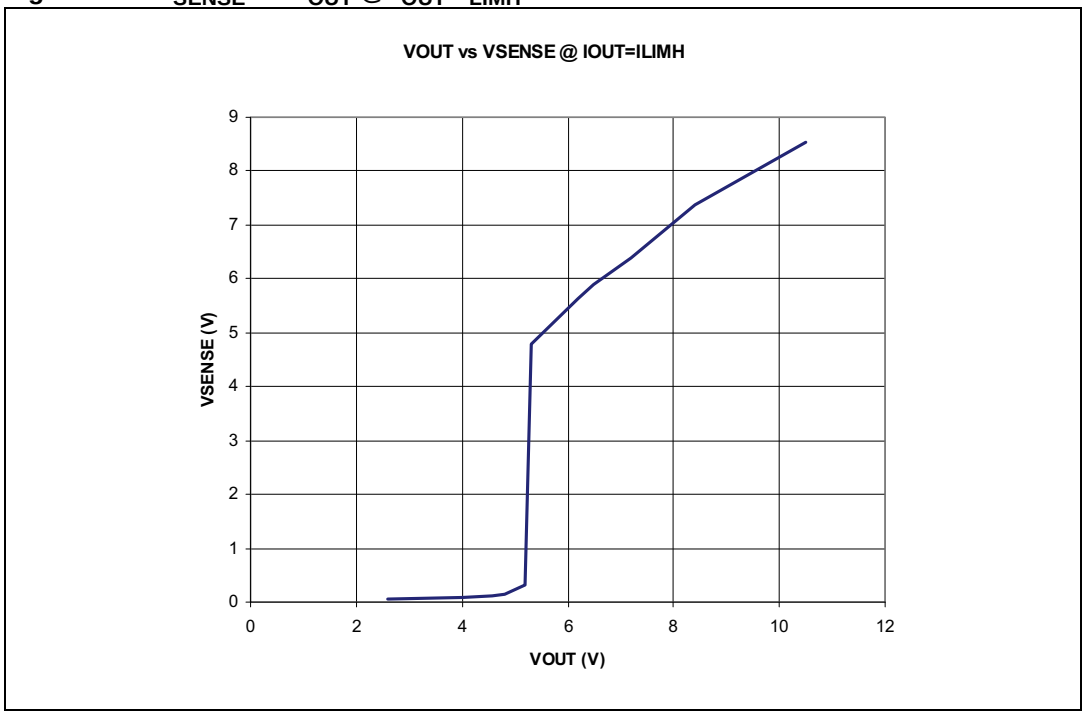
With the selected R_{SENSE}, the maximum V_{SENSE} which can be developed to maintain linearity is approx. 6.02 V.

However, the current sense operation for load current approaching the current limitation is neither guaranteed nor predictable. Indeed, because of the intervention of the current limiter, the output voltage can drop significantly: up to approximately 0 V in the extreme case of a hard short circuit.

As the whole circuit is referred to V_{OUT}, ambiguous and unreliable current values can derive from the CS under such conditions.

In order to bring the CS into a well defined state, a dedicated internal circuit shuts down the current sense when V_{OUT} drops below a certain threshold (6 V typ, see *Figure 18*).

Figure 18. V_{SENSE} vs V_{OUT} @ I_{OUT}=I_{LIMH}



Once again, this value is consistent with the current sense operating range and current limitation value.

Example: VND5T035AK

At the edge of the current limitation I_{OUT} = I_{LimH} = 30 A the maximum drop on the output MOSFET is

$$V_{DS} = R_{DS\_MAX} \cdot I_{LimH} \cong 70mOhm \cdot 30A = 2.1V$$

Therefore, at Vcc = 8 V, V_{OUT} is still sufficient to ensure correct CS function up to the current limited region.

In conclusion, in normal operation the current sense works properly within the described border conditions. For a given device, the I_{SENSE} is a single value monotonic function of the I_{OUT} until the maximum V_{SENSE} (1st example) or the current sense saturation (2nd example) are reached, i.e. there's no chance of having the same I_{SENSE} for different I_{OUT} within the given range.

3.3 Indication of power limitation and overtemperature

The principle:

in case of *Power Limitation*/overtemperature, the fault is indicated by the CS pin which is switched to a “current limited” voltage source.

Indeed, with reference to *Figure 16*, whenever a *Power Limitation*/overtemperature condition is reached, the M2 switch on the left side is activated.

The P channel MOSFET M2 is controlled in such a way as to develop 8.5 V typ (V_{SENSEH} in the datasheet) across the external sense resistor.

In any case, the current sourced by the CS in this condition is limited to 9 mA typ (I_{SENSEH} in the datasheet). In order to allow the current sense pin to develop V_{SENSEH} of 5 V minimum, the sense resistor value must not be below a certain value as shown in the following example:

Example: VND5T035AK calculation of minimum sense resistor for V_{SENSEH} > 5 V

Considering a typical I_{SENSEH} =9 mA → R_{SENSE_MIN} = 556 Ω

The typical behavior of a 24 V driver in case of overload or hard short circuit is shown in the following figures (FR_Stby set low = autorestart mode):

Figure 19. Example–overload (350 mΩ to GND)

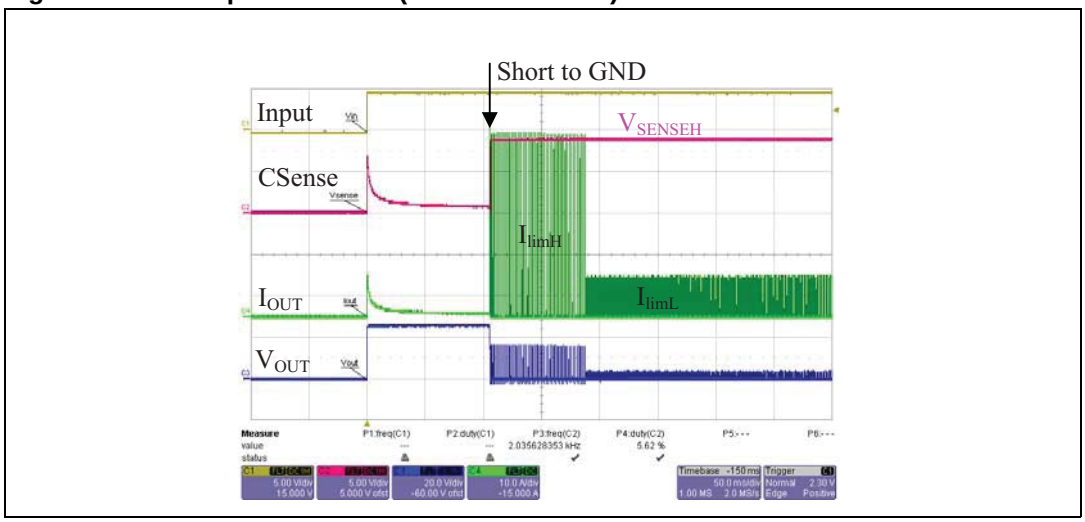
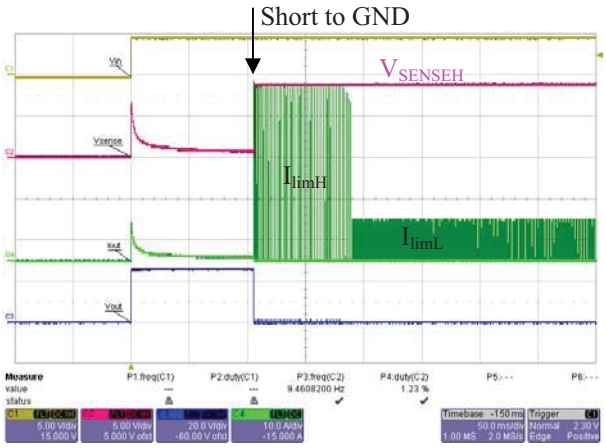


Figure 20. Example–hard short to GND



- Diagnostics reacts as soon as *Power Limitation* is reached without waiting for thermal shut down (see *Figure 19*)
- No ambiguity of diagnostics between open load and overload
- Fast and secure detection of short circuit/overload also for intermittent loads (for example turn-indicator lamps or loads driven with PWM)
- Intermittent short circuit detection covered as well

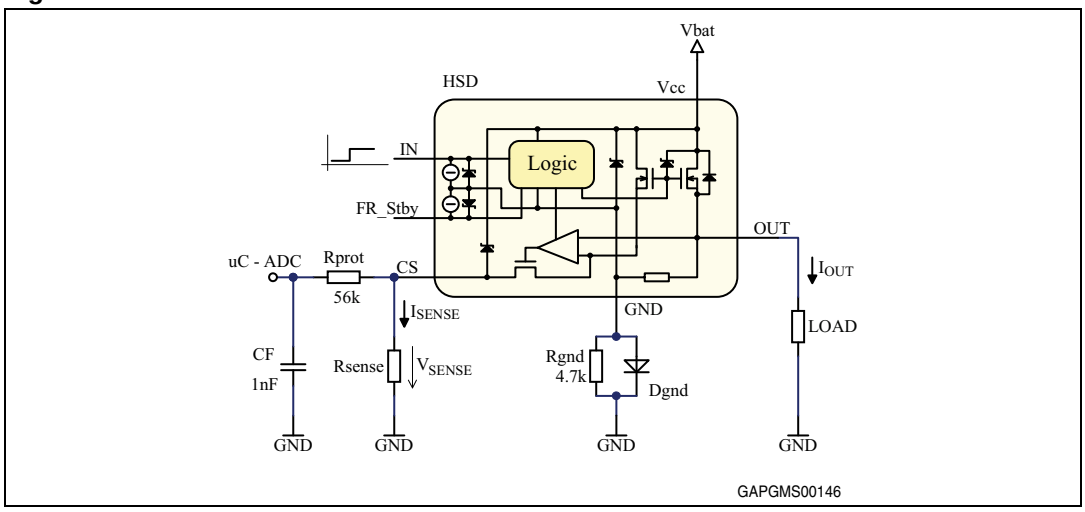
3.4 Current sense resistor calculation

The 24 V HSDs integrate a current sense which under normal circumstances provides a voltage across an external shunt resistor (R_{SENSE}), which is proportional to the load current with an N/n ratio (so-called K-Factor, specified in the datasheet):

$$V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \frac{I_{OUT}}{K} \quad [V]$$

This allows monitoring of the current which flows through the load and the detection of fault conditions, such as open load, overload, short-circuit to GND leading to a thermal shutdown. In case of a thermal shutdown or *Power Limitation*, the CS pin is switched to a voltage source V_{SENSEH} (V_{SENSEH} = 8.5 V typ, $I_{SENSEHtyp}$ = 9 mA) for as long as the device remains in the thermal shutdown (*Power Limitation*) mode.

Figure 21. Current sense resistor



The current sense voltage is usually connected through a 56 kΩ protection resistor to the ADC input of the µC. For the V_{SENSEH} level, the voltage is limited by the µC internal ESD protection (~5.6 V) while the ADC shows maximum value (0xFF in case of 8-bit resolution). The capacitor CF is used to improve the accuracy of the V_{SENSE} measurement. This capacitor acts as a low impedance voltage source for the ADC input during the sampling phase. Together with a 56 kΩ serial resistor, it creates a low pass filter (with cutoff frequency of ~3 kHz) for potential HF noise on the CS line (especially if a long wire is routed to the µC). This capacitor should be connected close to the µC.

The R_{SENSE} value definition example:

Let's consider the VND5T035AK (35 mΩ) with a nominal load current I_N = 3 A@V_{SENSE} = 2 V and typ K_2 = 2870 (datasheet):

$$R_{SENSE} = K \cdot \frac{V_{SENSE}}{I_{OUT}} = 2870 \cdot \frac{2}{3} = 1.9k\Omega$$

3.5 Diagnostics

3.5.1 Diagnostics with paralleled loads

A HSD with current sensing allows the detection of individual bulb failures when in a parallel arrangement. However, if we consider the bulb wattage spread, the HSD K-factor tolerance, the variation of bulb currents vs. V_{BAT} and ADC resolution, it is clear that accurate failure determination can be difficult in some cases. For example, if there are larger and smaller bulbs paralleled, the detection limit for the lowest power bulb is lost in the tolerances.

Table 3. Paralleling bulbs-overview

5+5 W	OK without calibration
21+21 W	
27+27 W	
21+5 W	Calibration and V_{BAT} monitoring recommended
21+21+5 W	Calibration and V_{BAT} monitoring necessary

In order to achieve a better current sense accuracy one or both of the strategies listed below can be adopted:

1. Current sense calibration (K-factor measurement) of each HSD
2. V_{BAT} measurement $\Rightarrow$ bulb current compensation by appropriate software

3.5.2 Diagnostics with different load options

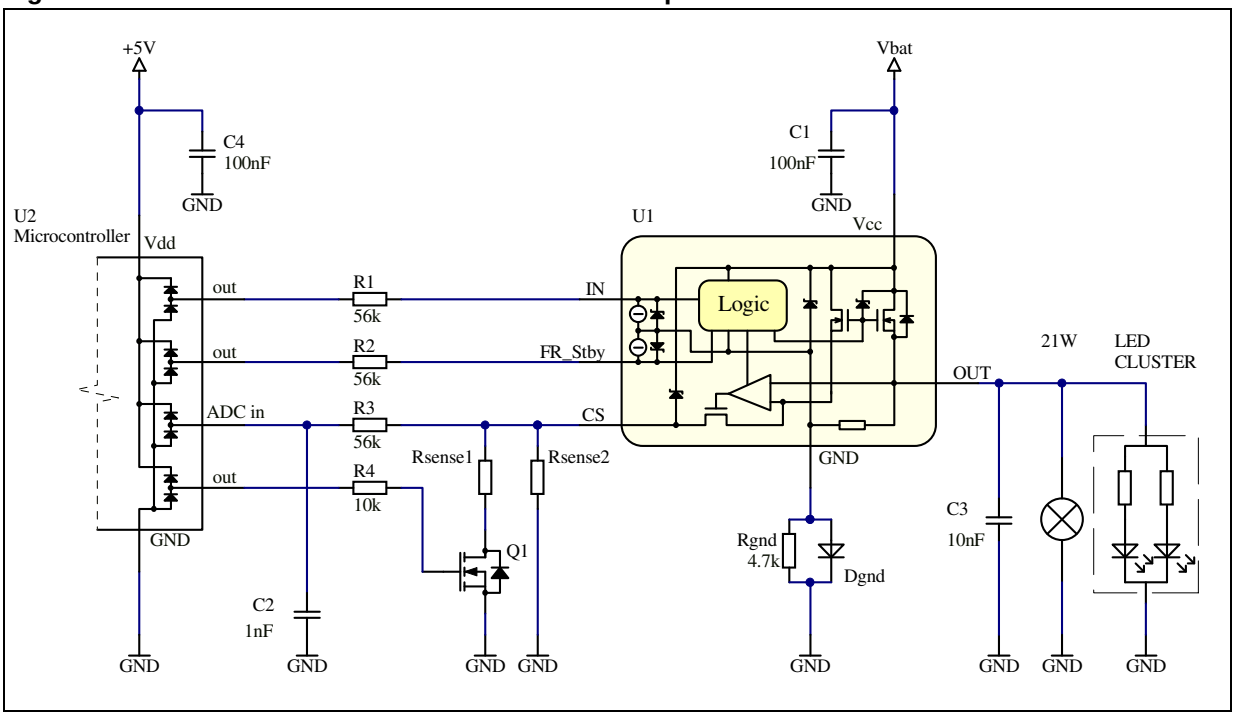
In some cases the requirement profile asks for alternative loads driven with one and the same high-side driver. This can be a bulb lamp with the alternative of an LED (- cluster). In this case the driver:

- Has to handle the high inrush current of the bulb load
- Must provide sufficiently low power dissipation during continuous operation
- Must not indicate an open load in case an LED (-cluster) is applied instead of a bulb.

In the case of different load options (bulb/LED), there is the possibility to use two different (switchable) sense resistors in order to use the current sense band in the appropriate range matching the different load currents.

An example of a current sense resistor switching circuit can be seen in the *Figure 22*. The measured scale can be extended by R_{sense1} switched in parallel to R_{sense2} by MOSFET Q1.

Figure 22. Switchable current sense resistor–example



3.5.3 K-factor calibration method

In order to reduce the Vsense spread, it is possible to reduce the K spread and eliminate the Rsense variation by adding a simple test (calibration test) at the end of the module production line.

How the calibration works:

“To calibrate” on a specific device soldered in a module signifies measuring the K ratio at a given output current by a V_{SENSE} reading. Since the relation of $I_{OUT} = I_{SENSE} \times K$ is known, it is straightforward to calculate the K ratio. However, even if the K ratio measured at a single point eliminates the parametric spread, it doesn't eliminate the V_{SENSE} variation due to the K variation produced by the output current variation.

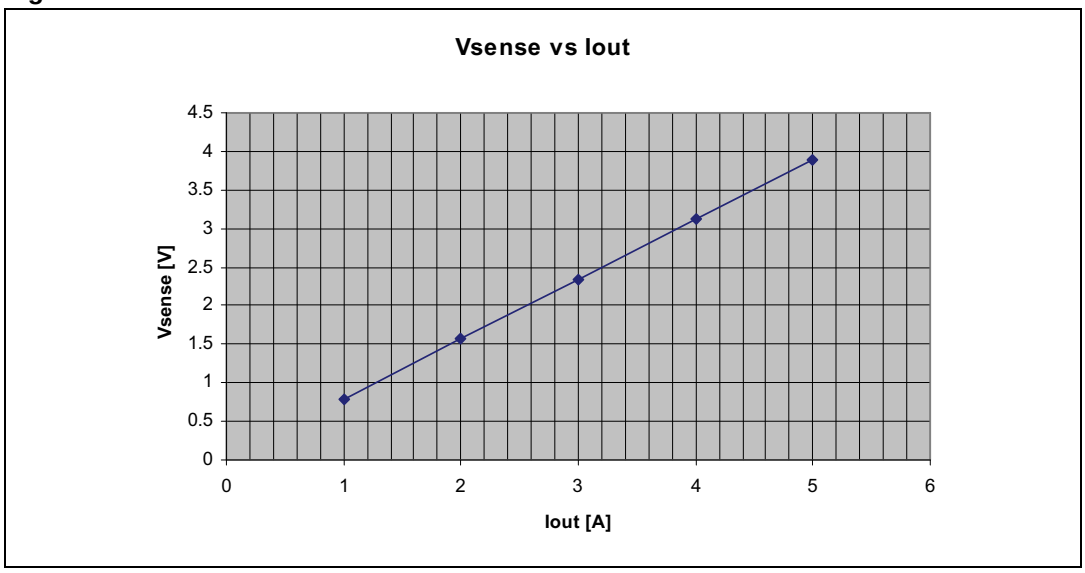
This variation can be eliminated according to the following considerations:

Table 4 and *Figure 23* show a V_{SENSE} measurement on a random VND5T035AK with R_{SENSE} = 2.2 kΩ.

Table 4. Vsense measurement

Iout[A]	Vsense[V]
1	0.783
2	1.563
3	2.344
4	3.115
5	3.898

Figure 23. Vsense measurement



The trend is almost linear in the application range so we can approximate the Vsense trend with the following equation:

Vsense=*m**Iout+*a* (1)

Where *m* [ohm] is the rectangular coefficient and *a* is a constant.

The output current can be calculated by inverting this equation:

Iout = M*Vsense + b (2)

Instead of $I_{OUT} = I_{SENSE} \times K$, once M [S] and b are known, it is possible to evaluate the I_{OUT} with a high accuracy, leaving only the spread due to temperature variation.

The current sense fluctuation due to temperature variation is expressed in the datasheet with the parameter dK/K.

How to calculate M and b:

To calculate M and b two simple measurements performed at the end of the production line are required. Chose two reference output currents (I_{ref1} and I_{ref2}) and measure the respective V_{SENSE1} and V_{SENSE2}. These four values must then be stored in an EEPROM in order to let the µC use this information to calculate K and b using the simple formulas reported below.

Since we defined Iout = M*Vsense + b it is also true that:

Iref1 = M*Vsense1+b

and (3)

Iref2 = M*Vsense2+b

Solving these two equations we get the following relations:

M = (Iref1-Iref2)/(Vsense1-Vsense2) (4)

b = (Iref2*Vsense1 –Iref1*Vsense2)/(Vsense1-Vsense2)

Example for the chosen device:

Setting Iref1 = 2 A and Iref2 = 4 A according to *Table 4* we get Vsense1 = 1.563 V and Vsense2 = 3.115 V then

M=1.289 [S]

b= -0.014 [A]

Iout is then:

Iout = 1.289*Vsense - 0.014 (5)

After calibration, the current sense variation is still influenced by the device temperature. Equation (5) is still affected by an error proportional to the sense current thermal drift.

This drift is reported in the datasheet as dK/K. The drift decreases when increasing the output current.For example, in the VND5T035AK datasheet, the drift is +/-15 % at 2 A and it decreases down to +/-5 % when the output current is 10 A.

3.5.4 Open load detection in off-state

- Available if FR_Stby pin is set high
- Indicated by V_{SENSEH} on CS pin
- External pull-up on the output needed
- Possibility to distinguish between open load in off-state and short to V_{BAT} using switchable pull-up resistor.

Figure 24. Analogue HSD–open load detection in off-state

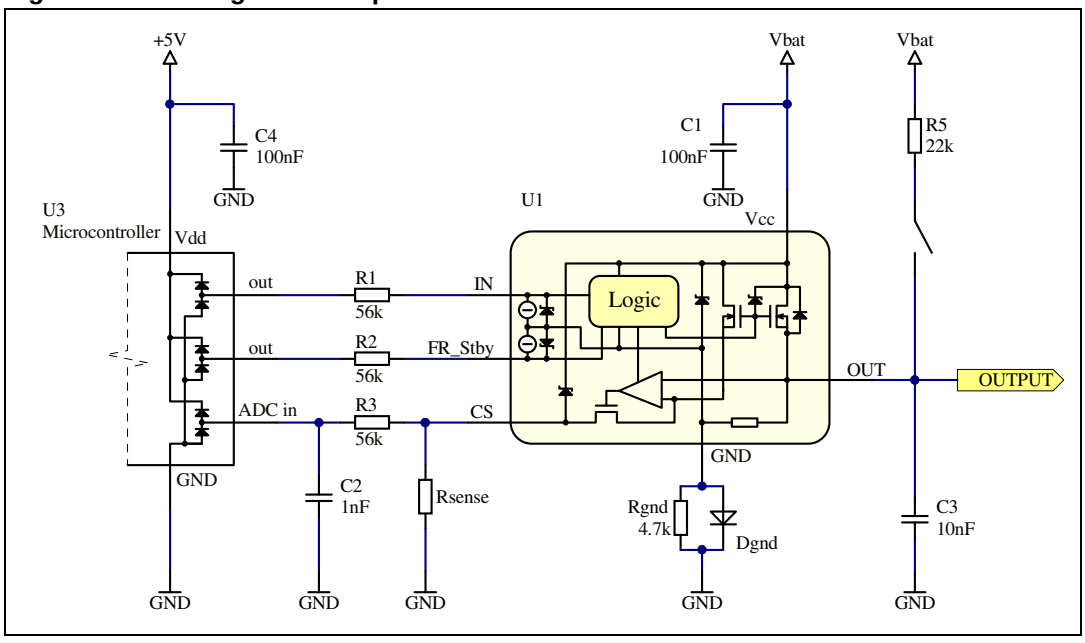
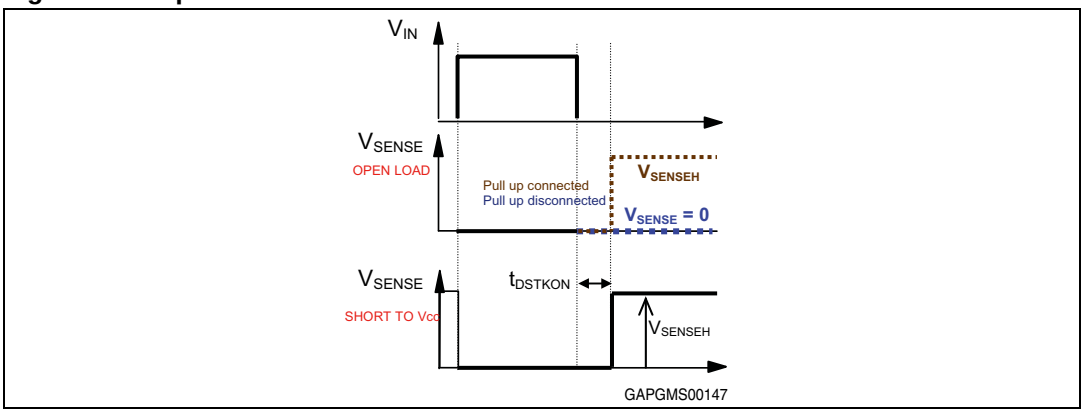


Table 5. CS pin levels in off-state

Condition	Pull up	CS	FR_Stby
Open load	Yes	0	L
		V_{senseH}	H
	No	0	L
		0	H
Short to Vcc	Yes	0	L
		V_{senseH}	H
	No	0	L
		V_{senseH}	H
Nominal	Yes	0	L
		0	H
	No	0	L
		0	H

Figure 25. Open load/short to Vcc condition



3.5.5 Diagnostic summary

Table 6 summarizes all failure conditions, the V_{SENSE} signal behavior and recommendations for diagnostics sampling.

Table 6. Diagnostics–overview

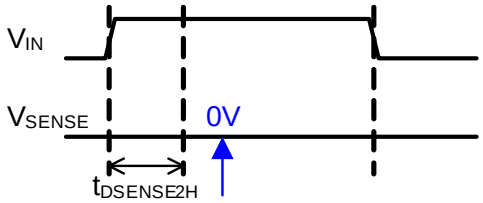
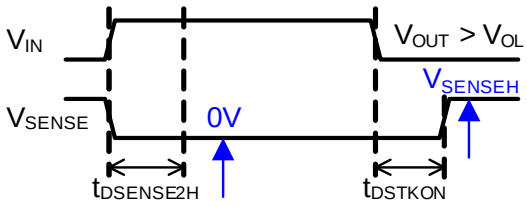
Fault condition	Signal	Value		
Open load (without pull-up)	V_{IN}	L		H
	FR_Stby	L or H		L or H
	V_{SENSE}	0 V		0 V
	Notes			Current sense delay response time from rising edge of IN pin must be considered ($t_{DSENSE2H}$).
	Waveforms Sampling			
Open load (with pull-up)	V_{IN}	L		H
	FR_Stby	L	H	L or H
	V_{SENSE}	0 V	V_{SENSEH}	0 V
	Notes	Diagnostic in off-state disabled	Delay time from falling edge of IN pin must be considered (t_{DSTKON}).	Current sense delay response time from rising edge of IN pin must be considered ($t_{DSENSE2H}$).
	Waveforms Sampling			

Table 6. Diagnostics–overview

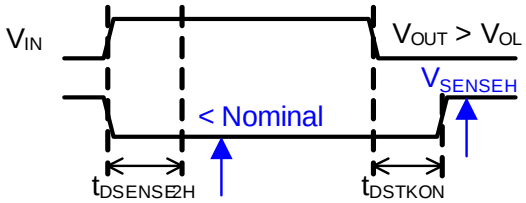
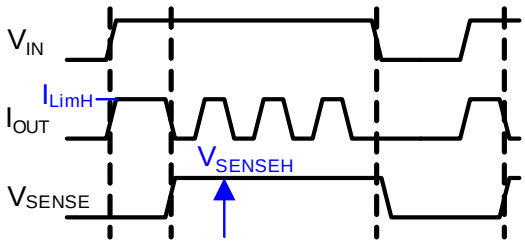
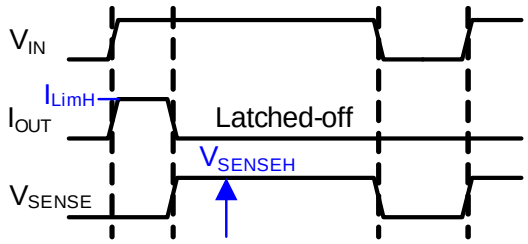
Fault condition	Signal	Value		
Short circuit to V_{BAT}	V_{IN}	L		H
	FR_Stby	L	H	L or H
	V_{SENSE}	0 V	V_{SENSEH}	< Nominal
	Notes	Diagnostic in off-state disabled	Delay time from falling edge of IN pin must be considered (t_{DSTKON}).	Current sense delay response time from rising edge of IN pin must be considered ($t_{DSENSE2H}$).
	Waveforms Sampling			
Power limitation or over temperature (Autorestart mode)	V_{IN}	L		H
	FR_Stby	L		L
	V_{SENSE}	0 V		V_{SENSEH}
	Notes	Diagnostic in off-state disabled		Current sense delay response time from rising edge of IN pin must be considered ($t_{DSENSE2H}$).
	Waveforms Sampling			

Table 6. Diagnostics–overview

Fault condition	Signal	Value	
Power limitation or over temperature (Latch mode)	V_{IN}	L	H
	FR_Stby	H	H
	V_{SENSE}	0 V	V_{SENSEH}
	Notes	Diagnostic in off-state enabled	Current sense delay response time from rising edge of IN pin must be considered ($t_{DSENSE2H}$). Output latched-off after the first intervention of power limitation or thermal shutdown. Can be unlatched by a low level pulse on the FR_Stby pin ($T_{PULSE} > T_{RESET}$).
	Waveforms Sampling		

4 Switching inductive loads

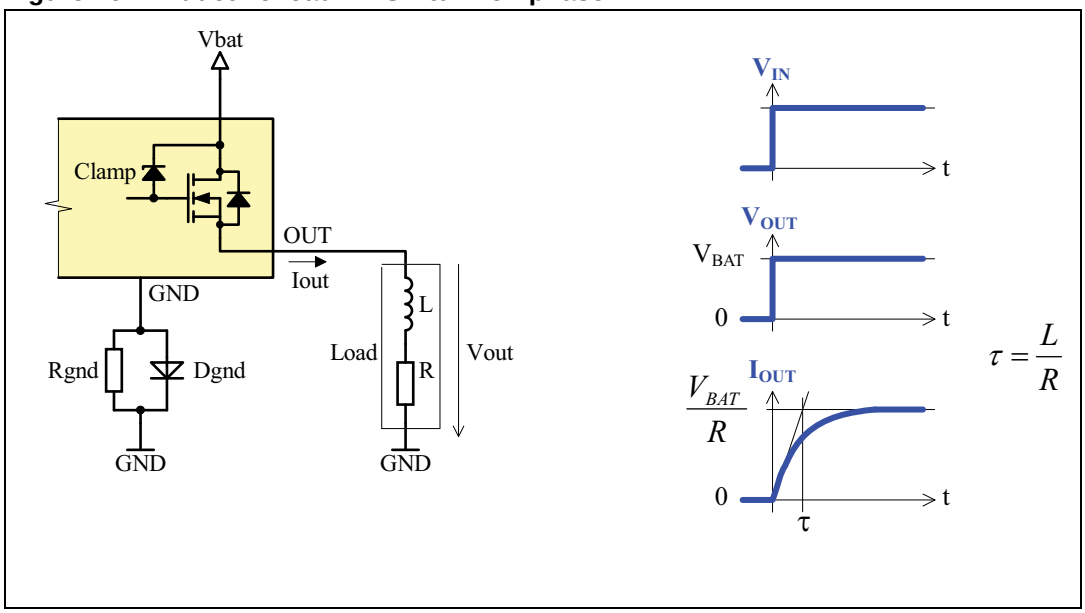
Switching inductive loads such as relays, solenoids, motors etc. can generate transient voltages of many times the steady-state value. For example, turning off a 24 volt relay coil can easily create a negative spike of several hundred volts. The ST high-side drivers are well designed to drive such loads, in most cases without any external protection. Nevertheless there are physical limits for each component that have to be respected in order to decide whether external protection is necessary or not.

An attractive feature of the ST high-side drivers is that a relatively high output voltage clamping leads to a fast demagnetization of the inductive load.

The purpose of this chapter is to provide a simple guide on how to check the conditions during demagnetization and how to select a proper HSD (and the external clamping if necessary) according to the given load.

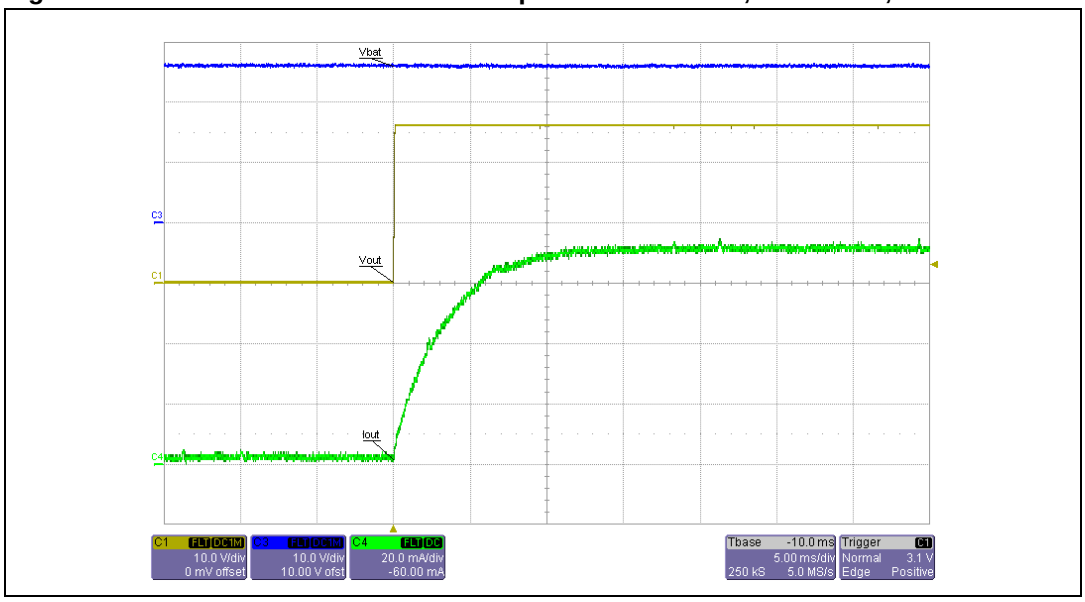
4.1 Turn-on phase behavior

Figure 26. Inductive load – HSD turn-on phase



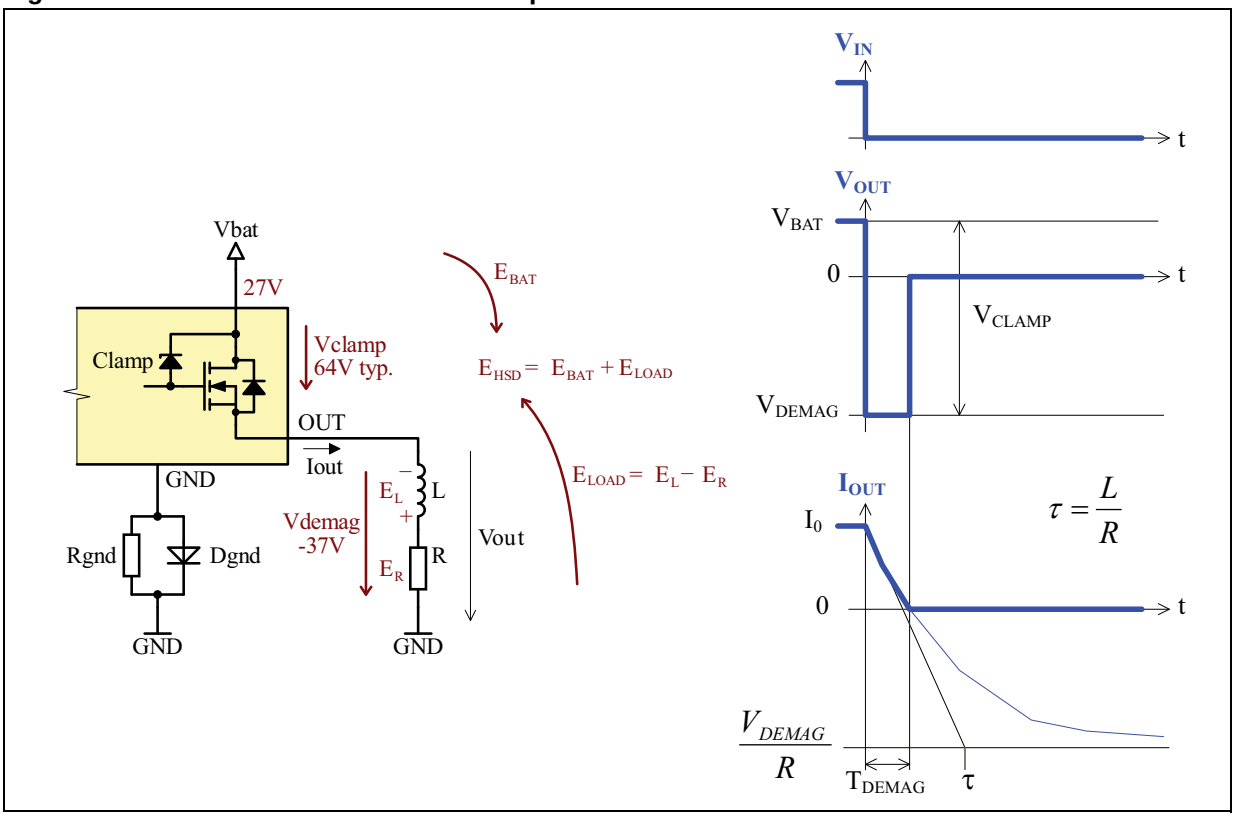
When a HSD turns on an inductive load the current increases with a time constant given by the L/R values, so the nominal load current is not reached immediately. This fact should be considered in the diagnostics software (i.e. to avoid a false open load detection).

Figure 27. Inductive load–turn-on example: VND5T035AK, L=880 mH, R=370 Ω



4.2 Turn-off phase behavior

Figure 28. Inductive load – HSD turn-off phase



The HSD turn-off phase with an inductive load is explained in *Figure 28*. The inductance reverses the output voltage in order to be able to continue driving the current in the same

direction. This voltage (so called demagnetization voltage) is limited to the value given by the clamping voltage of the HSD and the battery voltage:

Equation 1

$$V_{DEMAG} = V_{BAT} - V_{CLAMP} = 27V - 64V = -37Vtyp$$

The load current decays exponentially (linearly if R → 0) and reaches zero when all energy stored in the inductor is dissipated in the HSD and the load resistance.

Since the HSD output clamp is related to the V_{BAT} pin, the energy absorbed by the HSD increases with increasing battery voltage (the battery is in series with the high-side switch and load so the energy contribution of the battery increases with the battery voltage).

4.2.1 Calculation of energy dissipated in the HSD

The energy dissipated in the high-side driver is given by the integral of the actual power on the MOSFET through the demagnetization time:

$$E_{HSD} = \int_0^{T_{DEMAG}} V_{CLAMP} \cdot i_{OUT}(t)dt$$

To solve the above formula we need to know the current response $i_{OUT}(t)$ and the demagnetization time T_{DEMAG}. The $I_{OUT}(t)$ can be obtained from the well known formula of the R/L circuit current response using the initial current I_0 and the final current V_{DEMAG}/R considering i_{OUT} >= 0 condition (see *Figure 28*):

$$i_{OUT}(t) = I_0 - \left(I_0 + \frac{|V_{DEMAG}|}{R} \right) \cdot \left(1 - e^{\frac{-t \cdot R}{L}} \right)$$

($0 < t < T_{DEMAG} \Rightarrow i_{OUT} >= 0$)

Putting

$$i(t) = 0$$

we can calculate the demagnetization time by using**:**

Equation 2

$$T_{DEMAG} = \frac{L}{R} \cdot \ln\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|} \right)$$

Equation 3

$$\lim_{R \to 0} T_{DEMAG} = L \cdot \frac{I_0}{V_{DEMAG}}$$

(simplified for R→0)

Substituting the T_{DEMAG} and $i_{OUT}(t)$ by the formulas above we can calculate the energy dissipated in the HSD:

$$E_{HSD} = \int_0^{T_{DEMAG}} V_{CLAMP} \cdot i_{OUT}(t)dt = \int_0^{T_{DEMAG}} \left(V_{BAT} + |V_{DEMAG}|\right) \cdot i_{OUT}(t)dt$$

$\Rightarrow$

Equation 4

$$E_{HSD} = \frac{V_{BAT} + |V_{DEMAG}|}{R^2} \cdot L \cdot \left[R \cdot I_0 - |V_{DEMAG}| \cdot \ln\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|} \right) \right]$$

Equation 5

$$\lim_{R \to 0} E_{HSD} = \frac{1}{2} \cdot L \cdot I_0^2 \cdot \frac{V_{BAT} + |V_{DEMAG}|}{|V_{DEMAG}|}$$

(simplified for $R \to 0$)

4.2.2 Calculation example

This example shows how to use above equations to calculate the demagnetization time and the energy dissipated in the HSD.

Conditions:

- Battery voltage: V_{BAT} = 27 V
- HSD: VND5T035AK
- Clamping voltage: V_{CLAMP} = 64V (typical value)
- Load resistance: R = 370 Ω
- Load inductance: L = 880 mH
- Load current (before turn-off event): $I_0 = V_{BAT}/R$ = 73 mA

Step 1) Demagnetization voltage calculation using *Equation 1: on page 38*:

$$V_{DEMAG} = V_{BAT} - V_{CLAMP} = 27 - 64 = -37V$$

Step 2) Demagnetization time calculation using *Equation 2: on page 38:*

$$T_{DEMAG} = \frac{L}{R} \cdot \ln\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|}\right) = \frac{0.880}{370} \cdot \ln\left(\frac{37 + 0.073 \cdot 370}{37}\right) = 1.3ms$$

Step 3) Calculation of energy dissipated in the HSD using *Equation 4: on page 39*:

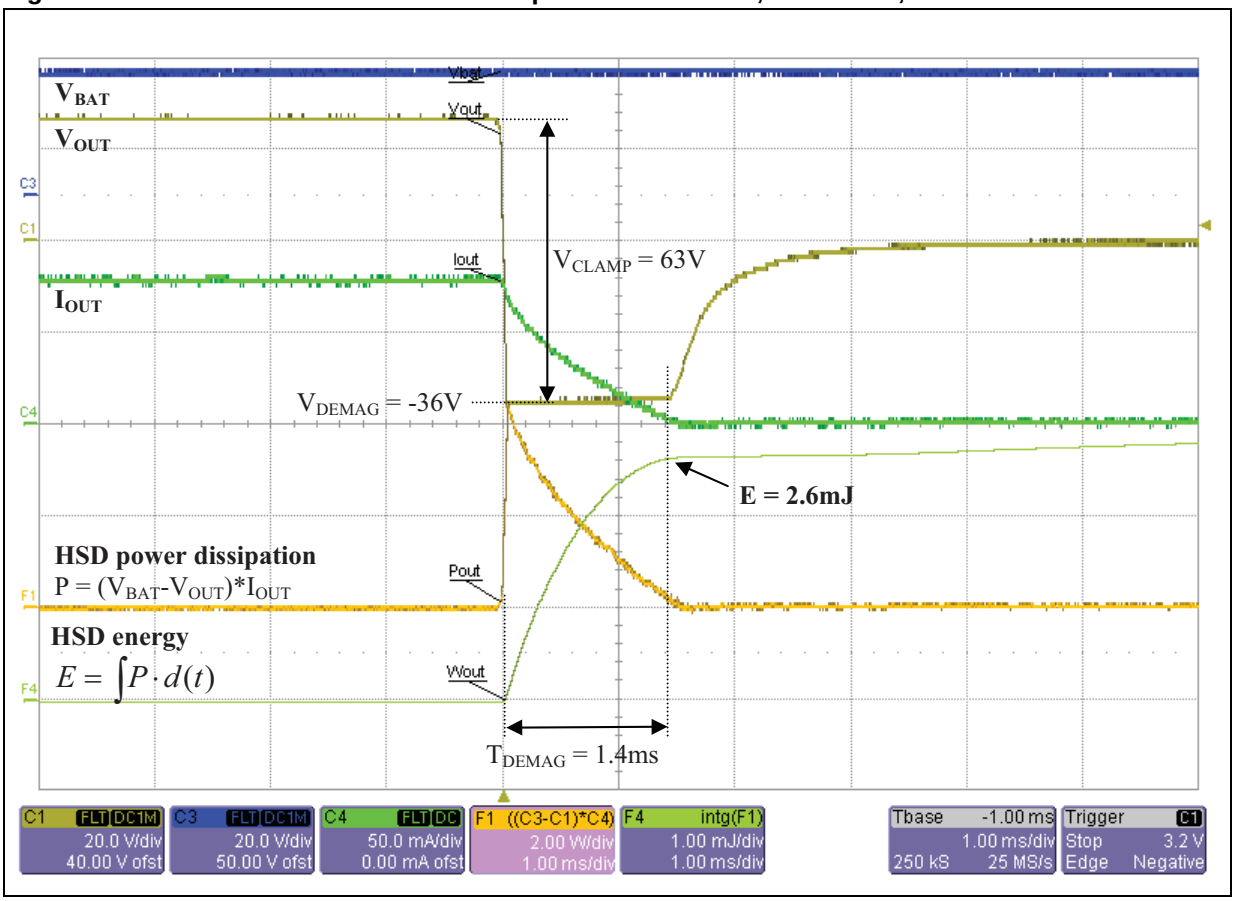
$$E_{HSD} = \frac{V_{BAT} + |V_{DEMAG}|}{R^2} \cdot L \cdot \left[R \cdot I_0 - |V_{DEMAG}| \cdot \ln\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|}\right)\right] =$$

$$= \frac{27 + 37}{370^2} \cdot 0.880 \cdot \left[370 \cdot 0.073 - 37 \cdot \ln\left(\frac{37 + 0.073 \cdot 370}{37}\right)\right] = 2.77mJ$$

Step 4) Measurement (comparison with theory):

(see oscillogram on *Figure 29*).

Figure 29. Inductive load - Turn off example: VND5T035AK, L=880 mH, R=370 Ω



The demagnetization energy dissipated in the HSD was measured by an oscilloscope with mathematical functions. The first function F1 shows the actual power dissipation on the HSD $(V_{BAT} - V_{OUT})*I_{OUT}$, the second function (F4) shows the HSD energy (integral of F1).

As seen from the oscillogram the measured values are close to the theoretical calculations (2.77 mJ@1.3 ms calculated versus 2.6 mJ@1.4 ms measured).

4.3 Proper HSD selection

Even if the device is internally protected against break down during the demagnetization phase, the energy capability is limited and has to be taken into account during the design of the application.

It is possible to identify two main mechanisms that can lead to a device failure:

1. The temperature during the demagnetization rises quickly (depending on the inductance) and the uneven energy distribution on the power surface can lead to a hot spot causing the device failure with a single shot.
2. As in normal operation, the life time of the device is affected by the fast thermal variation as described by the Coffin-Manson law. Repetitive demagnetization energy causing temperature variations above 60K causes a shorter life time.

These considerations lead to two simple design rules:

1. The energy has to be below the energy the device can withstand at a given inductance.
2. In case of a repetitive pulse the average temperature variation of the device should not exceed 60 K at turn-off.

To fulfill these rules the designer has to calculate the energy dissipated in the HSD at turn-off and then compare this number with the datasheet values as shown in the following examples.

4.3.1 Example of VND5T100AJ driving relays

The purpose of this example is to evaluate if a VND5T100AJ device can safely drive a relay under following conditions:

- Battery voltage: V_{BAT} = 27 V
- HSD: VND5T100AJ
  - Clamping voltage: V_{CLAMP} = 64 V (typical)
- Relay: HFKP024-1Z3T
  - Resistance: R = 280ohm @ -40 °C(see note 1)
  - Inductance (coil not powered): L = 880 mH(see note 2)
- Load current (before turn-off event): $I_0 = V_{BAT}/R$ = 96 mA

Note 1: *The relay datasheet usually specifies a coil resistance at 20 °C. For the worst case evaluation we should consider the resistance at -40 °C which can be calculated as:*

Equation 6

$$R_{-40} = R_{20} \cdot \left(1 + 0.0039 \cdot (-40 - 20)\right)$$

Note 2: *Not every relay datasheet specifies the coil inductance. In this case it can be determined by measurement. The inductance value with the armature seated (relay powered) is different to the one when unseated (relay not powered). The measurement should be done with relay powered (armature seated) because this better represents the application conditions. The inductance of a typical 24 V automotive relay is around 1 H.*

Step 1) Demagnetization voltage calculation using *Equation 1: on page 38*:

$$V_{DEMAG} = V_{BAT} - V_{CLAMP} = 27 - 64 = -37V$$

Step 2) Demagnetization time calculation using *Equation 2: on page 38*:

$$T_{DEMAG} = \frac{L}{R} \cdot \ln\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|}\right) = \frac{0.880}{280} \cdot \ln\left(\frac{37 + 0.096 \cdot 280}{37}\right) = 1.72ms$$

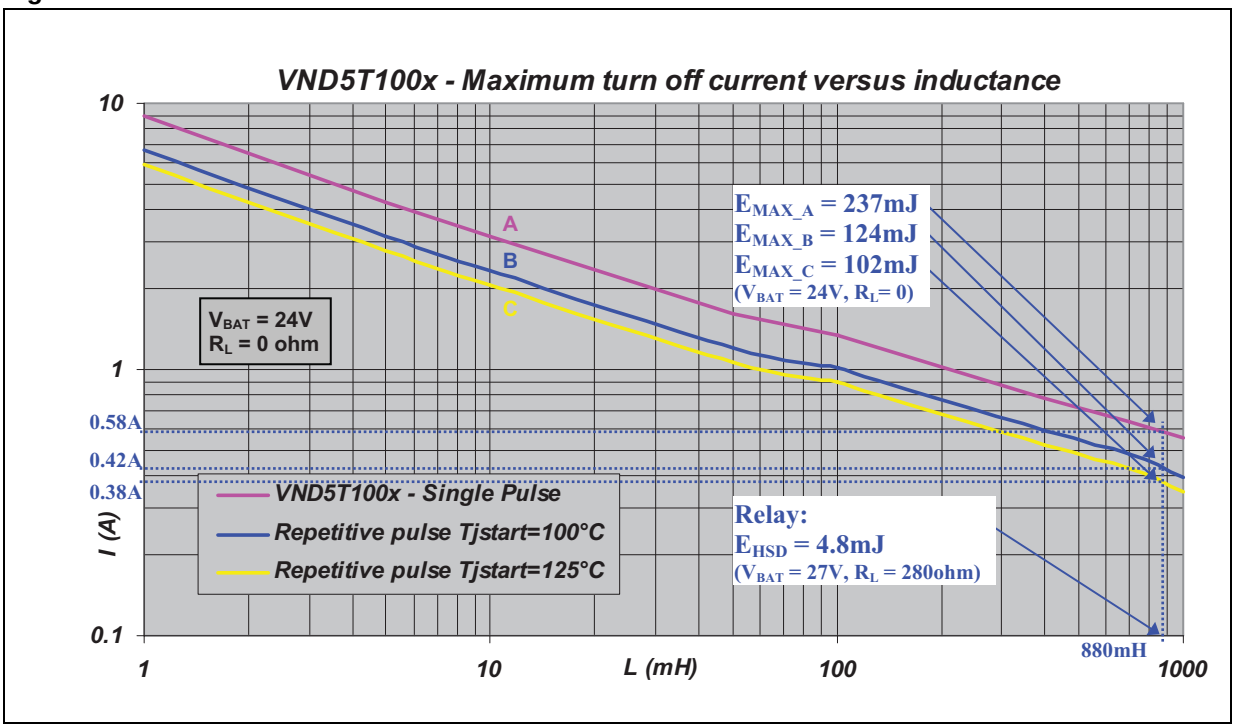
Step 3) Calculation of energy dissipated in the HSD using *Equation 4: on page 39*:

$$E_{HSD} = \frac{V_{BAT} + |V_{DEMAG}|}{R^2} \cdot L \cdot \left[R \cdot I_0 - |V_{DEMAG}| \cdot \ln\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|} \right) \right] =$$

$$= \frac{27+37}{280^2} \cdot 0.880 \cdot \left[280 \cdot 0.096 - 37 \cdot \ln\left(\frac{37 + 0.096 \cdot 280}{37} \right) \right] = 4.8mJ$$

Step 4) HSD datasheet analysis:

Figure 30. Maximum turn-off current versus inductance–VND5T100AJ datasheet



In the I/L diagram in the datasheet (see *Figure 30*), the maximum turn-off current with 880 mH inductance is 0.58 A for a single pulse, 0.42 A for a repetitive pulse at T_{jstart} = 100 °C and 0.38 A for a repetitive pulse at T_{jstart} = 125 °C. These current limits are 4–6 times higher than the worst case load current in our example (96 mA), so it is obvious that the device can safely drive the load.

Nevertheless, we should take into account that the I/L diagram shown in the datasheet is specified for V_{BAT} = 24 V and R_L = 0 Ohm. These conditions are different from the conditions considered in our example (V_{BAT} = 27 V, R_L = 280 Ohm). Thus direct comparison of the load current with the I/L diagram might be inaccurate. In this case it is better to convert the current limits taken from the I/L diagram to the energy limits using *Equation 5* and compare these limits with the calculated energy dissipated in the HSD:

$$E_{MAX-A} = \frac{1}{2} \cdot L \cdot I^2_{MAX} \cdot \frac{V_{BAT} + |V_{DEMAG}|}{|V_{DEMAG}|} = \frac{1}{2} \cdot 0.88 \cdot 0.58^2 \cdot \frac{24+40}{40} = 237mJ$$

(single pulse)

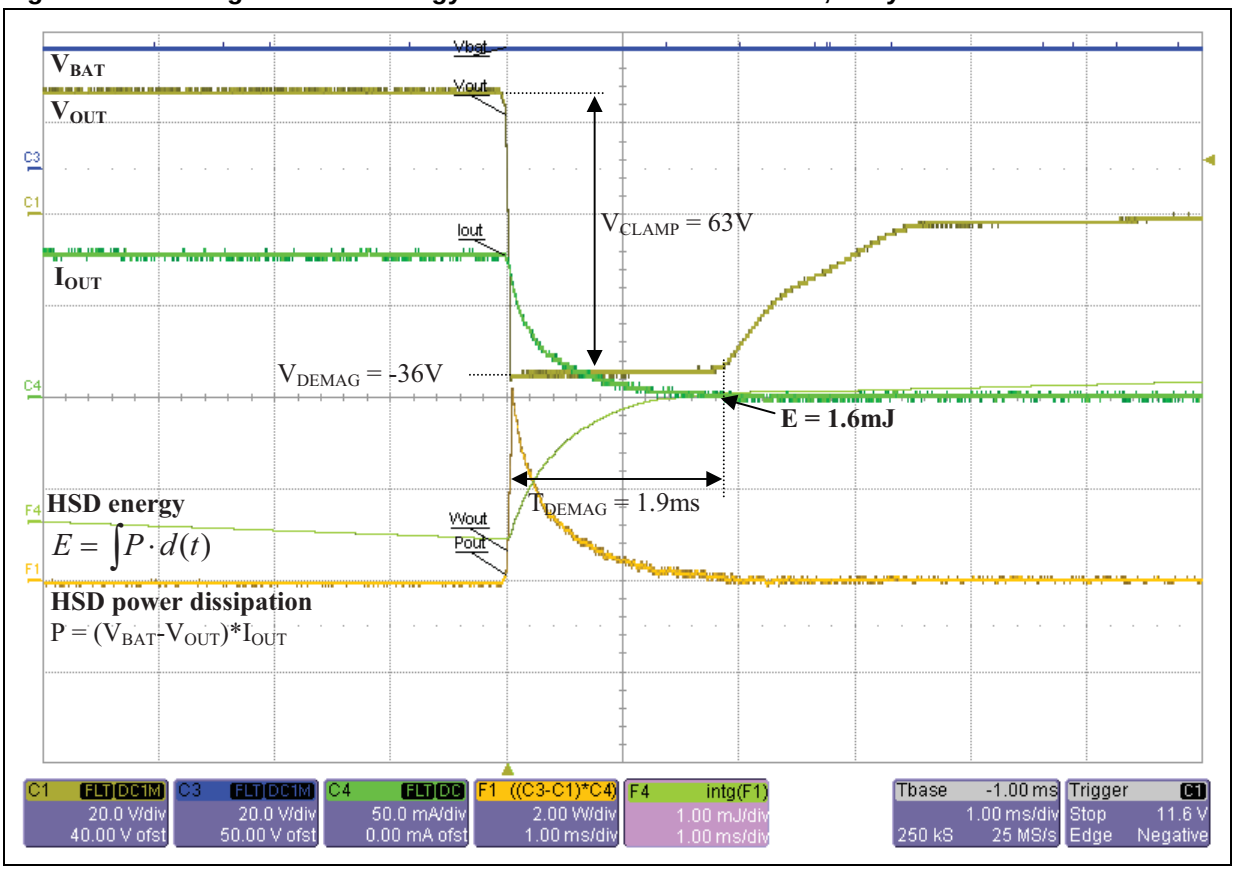
E_{MAX_B} = 124 mJ(repetitive pulse @ T_{jstart} = 100 °C)

E_{MAX_C} = 102 mJ(repetitive pulse @ T_{jstart} = 125 °C)

We can confirm that energy dissipated in the HSD (4.8 mJ – calculated in Step 3) is below these energy limits.

Step 5) Measurement (calculation check):

Figure 31. Demagnetization energy measurement–VND5T100AJ, relay 880 mH



The measured energy is lower by a factor of three than calculated (1.6 mJ measured versus 4.8 mJ calculated). This difference can be explained by a decrease of the coil inductance due to the magnetic saturation. The inductance value used in the calculation was measured on an un-powered coil using a small signal (120 Hz). Another factor is the coil resistance, the measurement was performed at room temperature when the coil resistance is ~25 % higher than the value used in the calculations (at -40 °C).

Conclusion:

The device can safely drive the load without additional protection. The worst case demagnetization energy is clearly below the device limit.

4.4 External clamping selection

The main function of external clamping circuitry is to clamp the demagnetization voltage and to dissipate the demagnetization energy in order to protect the HSD. It can be used as a cost effective alternative in case the demagnetization energy exceeds the energy capability of a given HSD. A typical example is driving DC motors (high currents in combination with high inductance).

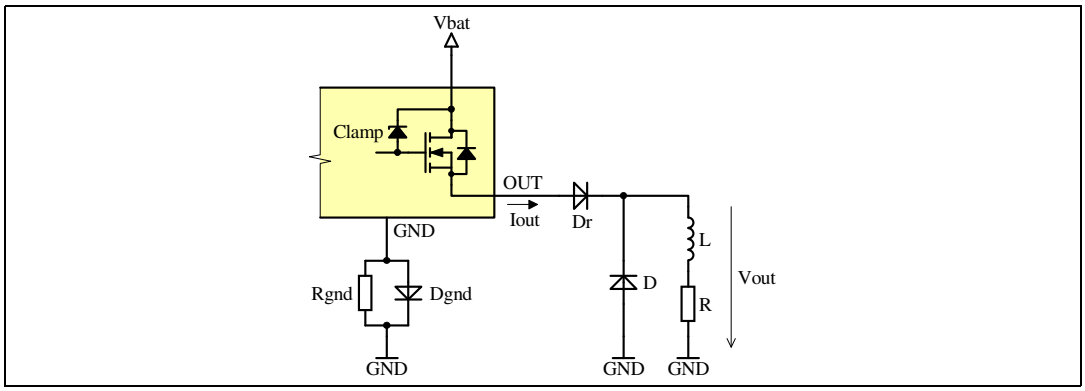
During the selection of a suitable HSD for such an application, we usually end up in the situation that a given HSD fits perfectly in terms of current profile, but the worst case demagnetization energy is too high (turn-off from stall condition at 32V, -40°C). Rather than selecting a larger HSD the use of an external clamp can be the more economical choice.

External clamping circuitry – requirements summary:

- Proper negative output voltage clamping to protect the HSD
- No conduction at:
  - Normal operation (0-32 V)
  - a reverse battery condition (-28 V@5 minutes)
  - Jump start (48 V@15 minutes)
  - Load Dump (58 V@600 ms)
- Proper energy capability
  - Single demagnetization pulse
  - Repetitive demagnetization pulse

4.4.1 Clamping circuitry examples

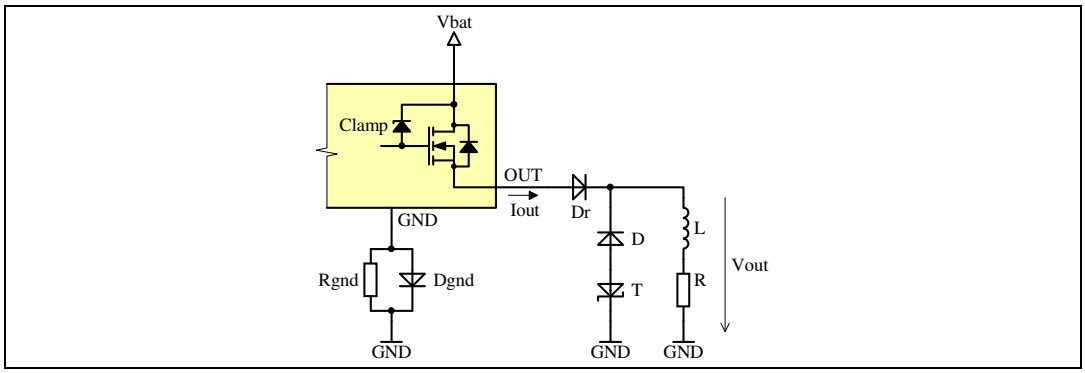
1) Freewheeling diode and reverse battery diode



A general purpose diode (D) connected in parallel with the load provides a conductive path for proper demagnetization. A relatively low demagnetization voltage (1 diode voltage drop in forward direction) leads to a very slow demagnetization. This can have a negative influence when driving the relay, for example. A slow movement of the armature (slow opening of contacts) may reduce the lifetime of the relay contacts (depending on the switching current).

In order to protect the freewheeling diode against the reverse battery condition there is an additional diode (Dr) required in series with the output. This circuitry is suitable only for small loads due the permanent voltage drop (⇒ power dissipation) on Dr during normal operation.

2) Transil and diode (in parallel with the load):

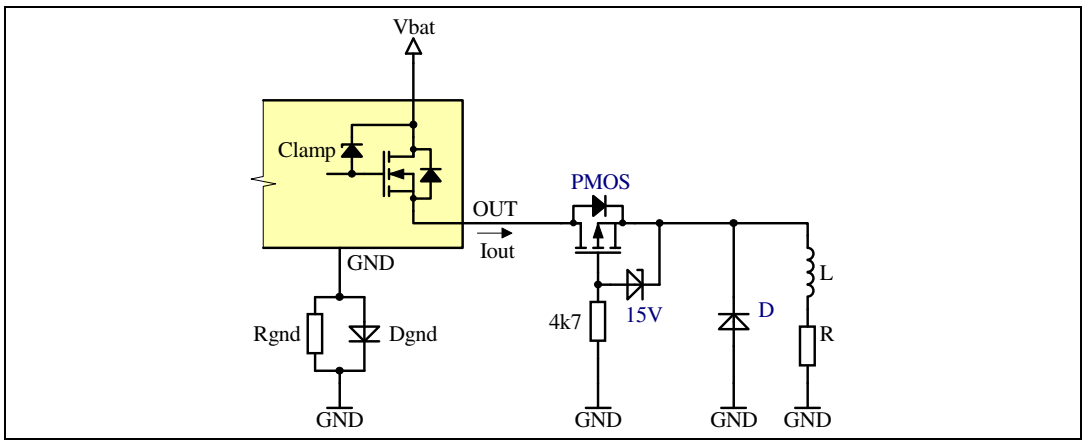


This circuitry is an improvement of the previous example 1. The demagnetization voltage is increased by the transil (T) inserted in series with diode (D). This diode is still necessary to decouple the transil during normal operation. A higher demagnetization voltage (in comparison with example 1) leads to a faster demagnetization of inductive loads (the main advantage of this circuitry).

The protection clamping voltage (V_{CLProt}) should be selected in a way that the voltage across the HSD channel stays below its minimum specified clamping voltage (58 V). Considering the worst case battery voltage (32 V), the minimum V_{CLProt} is -26 V (32 V - 58 V).

Since this voltage level (-26 V) is not compliant with the reverse battery requirement (-28 V), an additional diode (Dr) is included to protect the clamping circuitry during a reverse battery condition (with the same drawbacks as in the previous example 1).

3) Freewheeling diode and reverse battery P-channel MOS circuitry

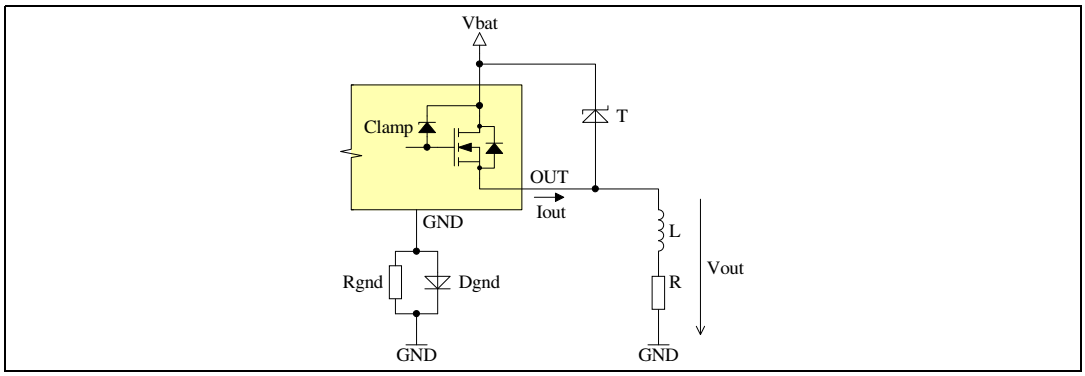


This circuitry is an improvement of the previous example 1. The reverse battery protection of the freewheeling diode (and load) is solved by PMOS circuitry with negligible voltage drop at nominal current (to avoid undesired power dissipation in on-state)

The peak power dissipation of the freewheeling diode during the demagnetization phase is very low in comparison with the transil protection because of the low demagnetization voltage (1 diode voltage drop). Furthermore, the average power dissipation is much lower assuming a non-zero load resistance. Thanks to the low demagnetization voltage, a significant part of the demagnetization energy is dissipated in the load resistance.

Therefore this circuitry is suitable for high current inductive loads such as DC motors, where the transil protection is usually not able to handle the average power dissipation caused by repetitive turn-on/off cycles (the HSD usually goes in thermal cycling when the motor is blocked so there are a lot of demagnetization cycles in a short time).

4) Transil protection circuitry (in parallel with the HSD)



The HSD channel is protected directly by a transil connected in parallel. The clamping voltage of the transil should be below the minimum clamping voltage of the HSD (58 V). Such transils (V_{CL} < 58 V) usually start conducting at ~40 V, which is not compatible with the clamped load dump requirement (58 V). Once the transil is activated during the load dump pulse, there is a high probability that it is damaged (overheated) by current flow through the load. For that reason it is usually better to use one of the previously described solutions (depending on the application).

External clamping circuitry examples

Table 7. External clamping circuitry examples(1/2)

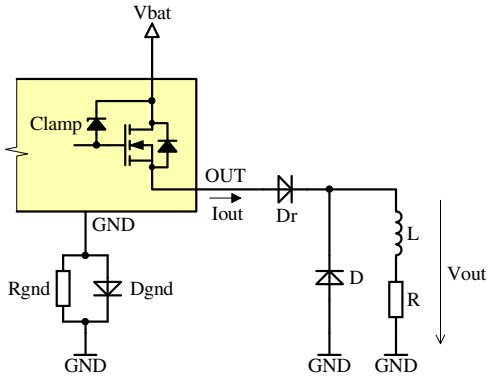
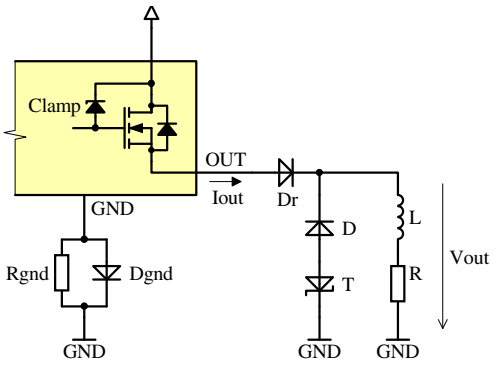
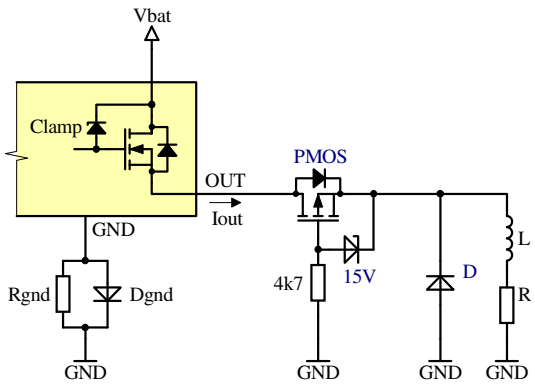
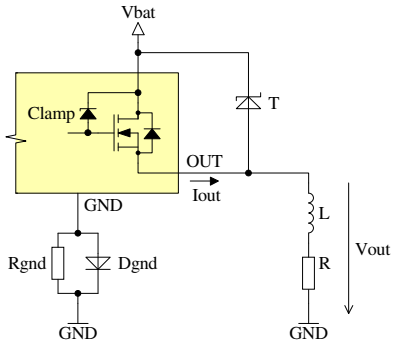
External clamping circuitry	+	–
1) Freewheeling diode and reverse battery diode) 	Low cost Load is reverse battery protected	Only for small loads (voltage drop and power dissipation on reverse battery protection diode Dr) Slow demagnetization
2) Transil and diode (in parallel with the load) 	Fast demagnetization Load is reverse battery protected	Only for small loads (voltage drop and power dissipation on reverse battery protection diode Dr)
3) Freewheeling diode and reverse battery FET 	Load is reverse battery protected Low peak power dissipation on D during demag. phase Suitable for high current inductive loads such as DC motors	High number of ext. components (cost) Slow demagnetization

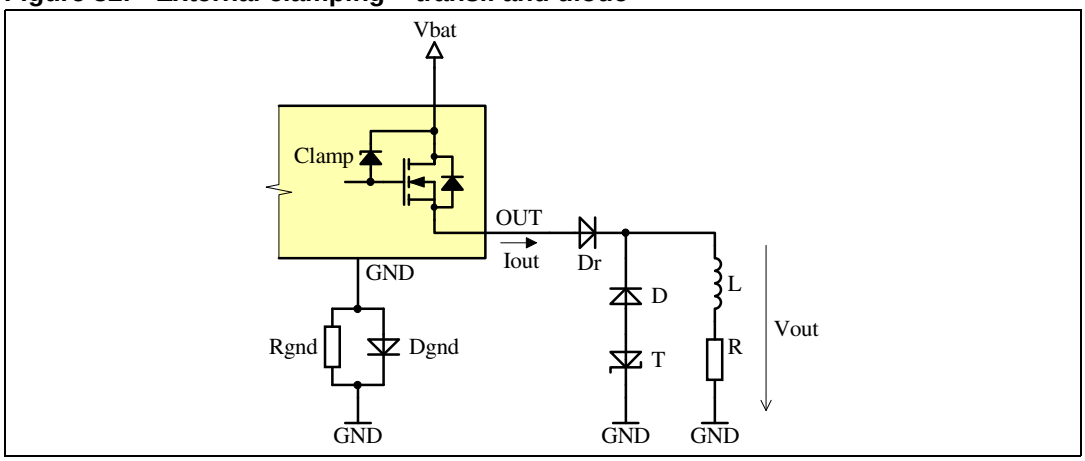
Table 8. External clamping circuitry examples(2/2)

External clamping circuitry	+	–
4) Transil (in parallel with the HSD) 	Fast demagnetization Direct (parallel) protection of the HSD - independent from V_{BAT}	Load dump pulse: (The transil with V_{CL} < 58 V is starting to conduct already at ~40 V ⇒ transil can be damaged during the load dump pulse) Higher peak power dissipation on transil in comparison with circuitry 2) (contribution of power supply)

4.4.2 Component selection guide for external transil-diode clamping

This chapter shows how to select properly a diode (D) and transil (T) for external clamping circuitry 2).

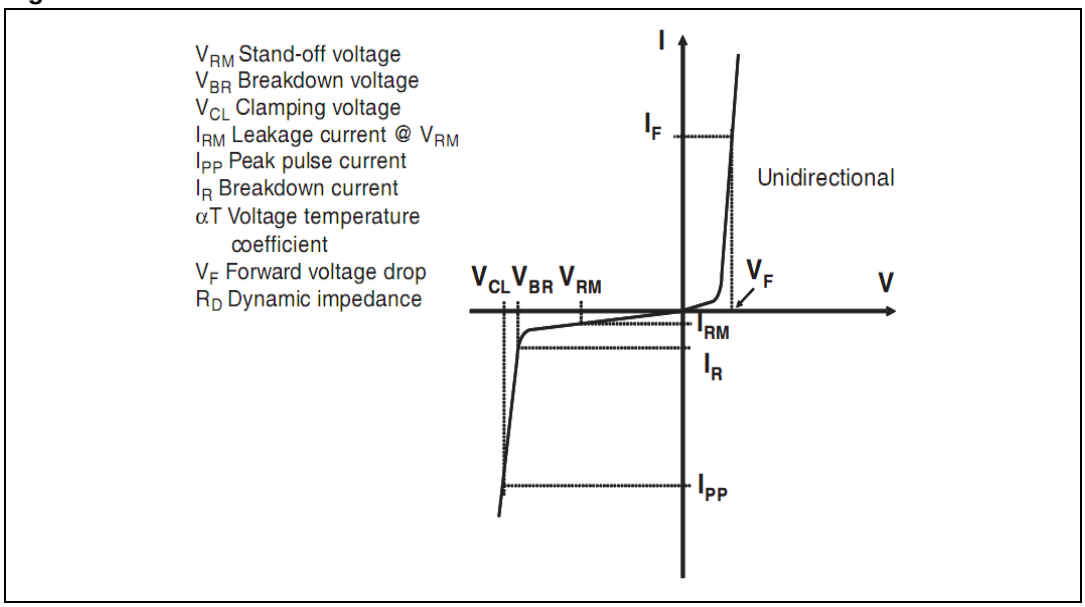
Figure 32. External clamping – transil and diode



Transil selection:

- Clamping voltage, V/A characteristic

Figure 33. Transil – V/A characteristic



Considering the worst case values (V_{BATmax} = 32 V, $V_{HSDClampMin}$ = 58 V) the voltage on the HSD output should be limited to a level above 32 V – 58 V = –26 V in order not to activate the HSD clamp structure. Assuming 1 V voltage drop on the protection diode (D) we need a transil with V_{CL} < 25 V at a given current level (load current at switch-off event). The clamping voltage is usually specified only at the maximum peak power limit of the device. The voltage at a given current level can be determined from the datasheet, either by calculation (linear approximation of V_{BR}/I_R and V_{CL}/I_{PP} values) or by reading the V/A diagram.

⇒ Transil clamping voltage requirement:

Equation 7

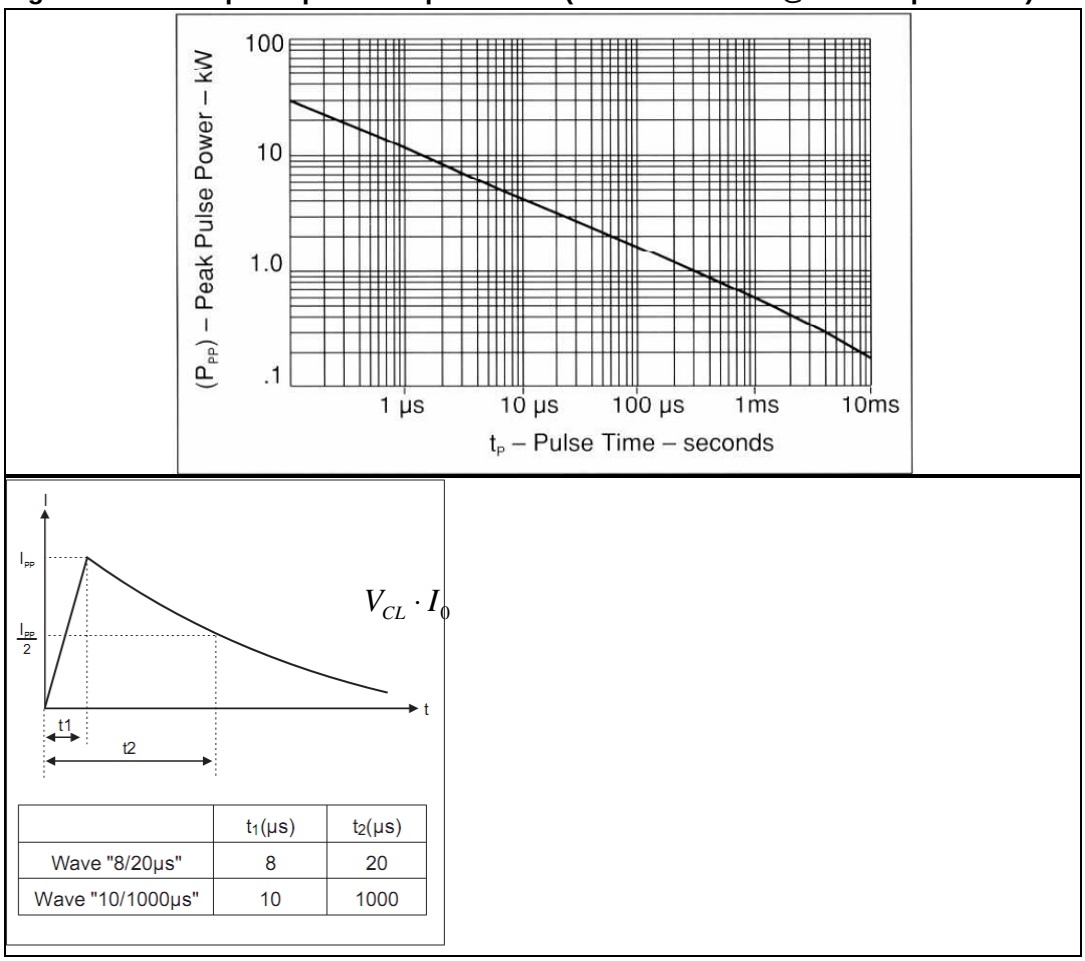
$$V_{CL} < V_{HSDClampMin} - V_{BAT\,max} \quad -1$$

(V_{CL} - clamping voltage at given I_0, where I_0 = load current at turn-off event)

- Single pulse energy capability

The maximum non repetitive transient power and current capability of transils is specified mostly for a 10/1000 µs exponential pulse at 25 °C. A real application condition is usually different. In our case the pulse length is given by the demagnetization time while the current waveform is close to the sawtooth shape (depending on L/R ratio of the load). To check if the transil can safely operate under the desired conditions, we can use the translation diagrams in *Figure 34*, *Figure 35* and *Figure 36*.

Figure 34. Peak pulse power vs pulse time (for transil 600 W@10/1000 µs series)



	t_1(µs)	t_2(µs)
Wave "8/20µs"	8	20
Wave "10/1000µs"	10	1000

Figure 35. Equivalent pulses giving the same power dissipation

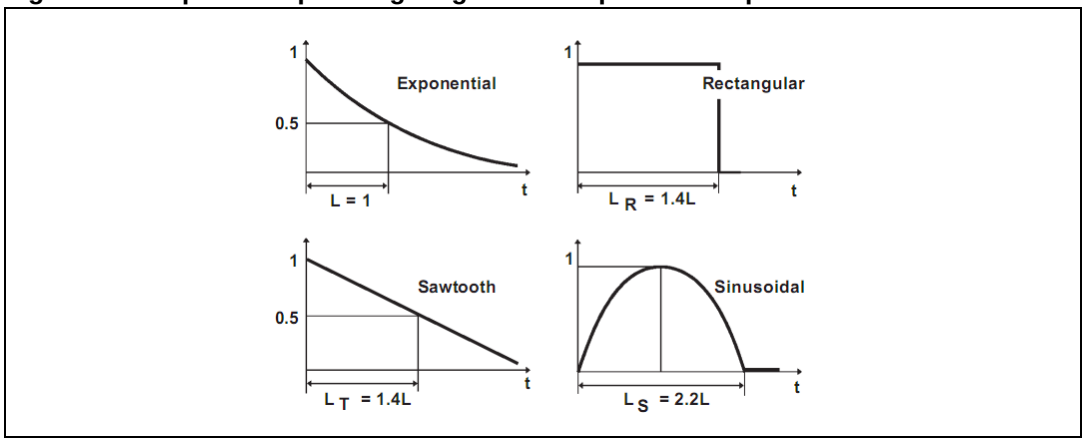
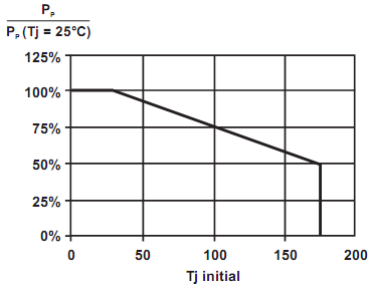


Figure 36. Maximum peak power as function of the initial temperature of the transil



- Repetitive pulse energy capability

Depending on the application (PWM, HSD thermal cycling), the transil should be able to withstand repetitive operation and the most important parameter is the average power dissipation:

Equation 8

$$P_{AVG} = f \cdot E$$

valid when

$$T_{DEMAG} < \frac{1}{f}$$

(*f*: switching frequency, E: energy dissipated in the transil at each demag. pulse)

Equation 9

$$E = \frac{|V_{CL}|}{R^2} \cdot L \cdot \left[R \cdot I_0 - |V_{CL}| \cdot \ln\left(\frac{|V_{CL}| + I_0 \cdot R}{|V_{CL}|} \right) \right]$$

(V_{CL}: transil clamping voltage, R: load resistance, L: load inductance, I_0: load current at turn-off event)

The junction temperature T_J calculated from P_{AVG} should never exceed the specified maximum junction temperature:

Equation 10

$$T_J = T_{Amb} + R_{th(j-a)} \cdot P_{AVG}$$

(T_{Amb}: ambient temperature, $R_{th(j-a)}$: thermal resistance between junction and ambient, P_{AVG}: average power dissipation)

Transil selection summary:

1. Determine maximum clamping voltage (*Equation 7*)
2. Determine length of equivalent exponential pulse:

$$T_P = 0.5 \cdot \frac{T_{DEMAG}}{1.4}$$

(*Figure 35* – sawtooth pulse)

3. Determine max. peak power (P_P) for T_P (using *Figure 34*)
4. Correct P_P value according to worst case T_j (using *Figure 36*)
5. Check if corrected

$$P_P > V_{CL} \cdot I_0$$

6. Check P_{AVG} and T_J in repetitive operation (*Equation 8*-*Equation 10*)

Diode selection criteria (diode in series with transil):

- Reverse voltage > 78 V
  (The diode must not conduct during positive voltage on the HSD output
  ⇒ ISO pulse 2 at level IV (50 V@50 µs) considered on top of the nominal supply voltage of 28 V when HSD is turned on).
- Peak forward current > I_0 @ T_{DEMAG}
  (I_0: load current at switch-off event, T_{DEMAG}: demagnetization time)

4.4.3 Example of VND5T035AJ for DC motor driving with external clamp

The purpose of this example is to evaluate if a VND5T035AJ can safely drive a given DC motor in terms of demagnetization energy or to determine a suitable external clamping circuitry if needed.

- Battery voltage: V_{BAT} = 27 V
- HSD: VND5T035AJ
  - Clamping voltage: V_{CLAMP} = 64 V (typical)
- DC Motor (truck front wiper):
  - Nominal current: I_{nom} = 2 A
  - Resistance: R = 0.89 Ω @ 25 °C
  - Inductance: L = 3.56 mH
  - Stall current: I_0 = 27 A @ 25 °C, 24 V

Step 1) Demagnetization voltage calculation using *Equation 1*:

$$V_{DEMAG} = V_{BAT} - V_{CLAMP} = 27 - 64 = -37V$$

Step 2) Demagnetization time calculation using *Equation 2:*

$$T_{DEMAG} = \frac{L}{R} \cdot \ln\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|}\right) = \frac{0.00356}{0.89} \cdot \ln\left(\frac{37 + 27 \cdot 0.89}{37}\right) = 2ms$$

Step 3) Calculation of energy dissipated in the HSD using *Equation 4:*

$$E_{HSD} = \frac{V_{BAT} + |V_{DEMAG}|}{R^2} \cdot L \cdot \left[R \cdot I_0 - |V_{DEMAG}| \cdot \ln\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|}\right)\right] =$$

$$= \frac{27 + 37}{0.89^2} \cdot 0.00356 \cdot \left[0.89 \cdot 27 - 37 \cdot \ln\left(\frac{37 + 27 \cdot 0.89}{37}\right)\right] = 1.59J$$

Step 4) HSD datasheet analysis:

Looking at the I/L diagram in the datasheet (see *Figure 37*), the maximum turn-off current specified for 3.56 mH inductance is 10 A (single pulse, V_{BAT} = 24 V, R_L = 0). The worst case current in our example is much higher (27 A - stall condition of the motor) so it is obvious that the device cannot safely drive this load without external protection (clamping).

For better comparison of the calculated energy (1.59J) with the device limits it is useful to translate the maximum current values at 3.56 mH (I_{MAX_A} = 10 A, I_{MAX_B} = 7.5 A, I_{MAX_C} = 6.5 A) to energy values using *Equation 5:*

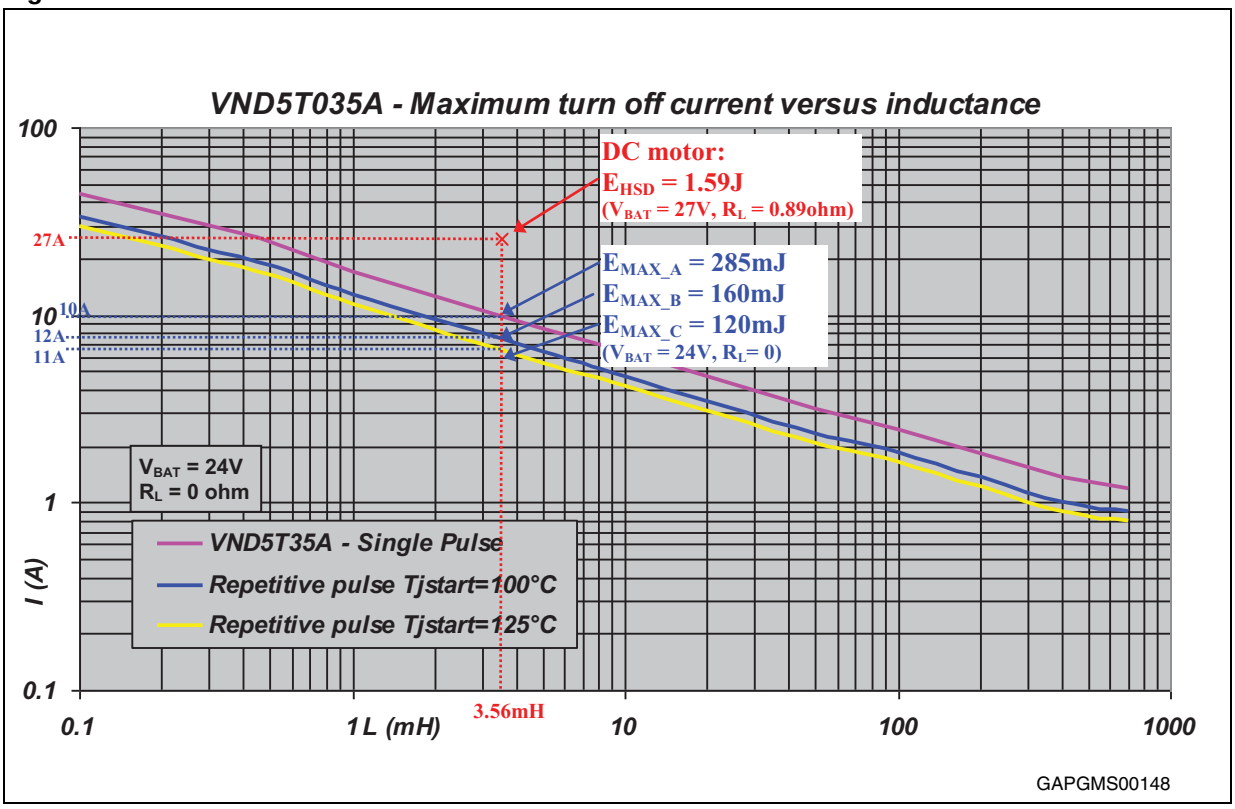
$$E_{MAX\_A} = \frac{1}{2} \cdot L \cdot I_{MAX}^2 \cdot \frac{V_{BAT} + |V_{DEMAG}|}{|V_{DEMAG}|} = \frac{1}{2} \cdot 0.00356 \cdot 10^2 \cdot \frac{24 + 40}{40} = 285mJ$$

single pulse

E_{MAX_B} = 160 mJ repetitive pulse @ T_{jstart} = 100 °C

E_{MAX_C} = 120 mJ repetitive pulse @ T_{jstart} = 125 °C

Figure 37. Maximum turn-off current versus inductance – VND5T035AJ datasheet



The demagnetization energy is by a factor of 6 higher than the device is able to withstand, therefore additional protection/clamping is necessary.

The evaluation of an appropriate protection/clamping is described in the following Step 5).

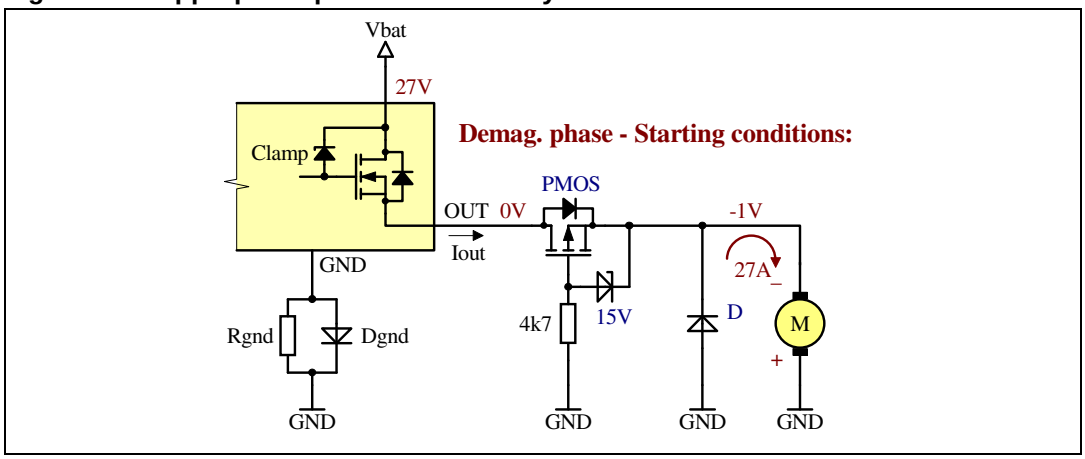
Step 5) External clamping selection:

The external clamping circuitry is selected according to *Table 7*. Respecting the load characteristics (DC motor), the circuitry 3 with a freewheeling diode (as shown in *Figure 38*) is considered the best choice. The demagnetization voltage is about -1 V, therefore most of the energy stored in the load inductance is dissipated in the load resistance (0.89 Ω). This allows us to use a relatively small freewheeling diode.

Nevertheless, an additional reverse battery protection circuit should be included to protect the freewheeling diode and to prevent the activation of the DC motor in reverse direction. The example of such a protection (with P-channel MOSFET) can be seen in *Figure 38*.

There are several ways to solve reverse battery protection (depending on application requirements). But as this chapter deals with inductive load switching, the next section only focuses on dimensioning of the freewheeling diode.

Figure 38. Appropriate protection circuitry for VND5T035A with DC motor



Demagnetization time - *Equation 2* (assuming V_{DEMAG} = -1 V) :

$$T_{DEMAG} = \frac{L}{R} \cdot \ln\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|}\right) = \frac{0.00356}{0.89} \cdot \ln\left(\frac{1 + 27 \cdot 0.89}{1}\right) = 12.9ms$$

Freewheeling diode selection criteria:

- Reverse voltage > 70 V
  (Must not conduct during positive voltage on the output
  $\Rightarrow$ max. possible output voltage is determined by $V_{HSDClampMax}$ = 70 V
- Peak forward current: > 27 A @ 12.9 ms
  (I_0 @ T_{DEMAG})
- Average power dissipation (repetitive turn-off):

Assuming that the HSD is in thermal shutdown condition with autorestart (frequency assumed to be ~500 Hz) and $I_0 = I_{limL} \Rightarrow$ 10.5 A.

The energy dissipated in the freewheeling diode - *Equation 9:*

(HSD turn off: $I_0 = I_{limL}$ = 10.5 A):

$$E = \frac{|V_{CL}|}{R^2} \cdot L \cdot \left[R \cdot I_0 - |V_{CL}| \cdot \ln\left(\frac{|V_{CL}| + I_0 \cdot R}{|V_{CL}|}\right)\right]$$

$$E = \frac{1}{0.89^2} \cdot 0.00356 \cdot \left[0.89 \cdot 10.5 - 1 \cdot \ln\left(\frac{1 + 10.5 \cdot 0.89}{1}\right)\right]$$

E = 31.5 mJ

Demagnetization time for $I_0 = I_{limL}$ = 10.5 A - *Equation 2*:

$$T_{DEMAG} = \frac{L}{R} \cdot \ln\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|}\right) = \frac{0.00356}{0.89} \cdot \ln\left(\frac{1 + 10.5 \cdot 0.89}{1}\right)$$

T_{DEMAG} = 9.3 ms

The demagnetization time (9.3 ms) is higher than the assumed HSD cycling frequency period (2 ms). Therefore, the average power dissipation on the freewheeling diode cannot be easily calculated using *Equation 8*:

$$P_{AVG} = f \cdot E$$

$\Rightarrow$ 500 × 0.0315 = 15.8 W (the real value is significantly lower).

Then, as a rough estimation, we can use the average power dissipation during one demagnetization pulse:

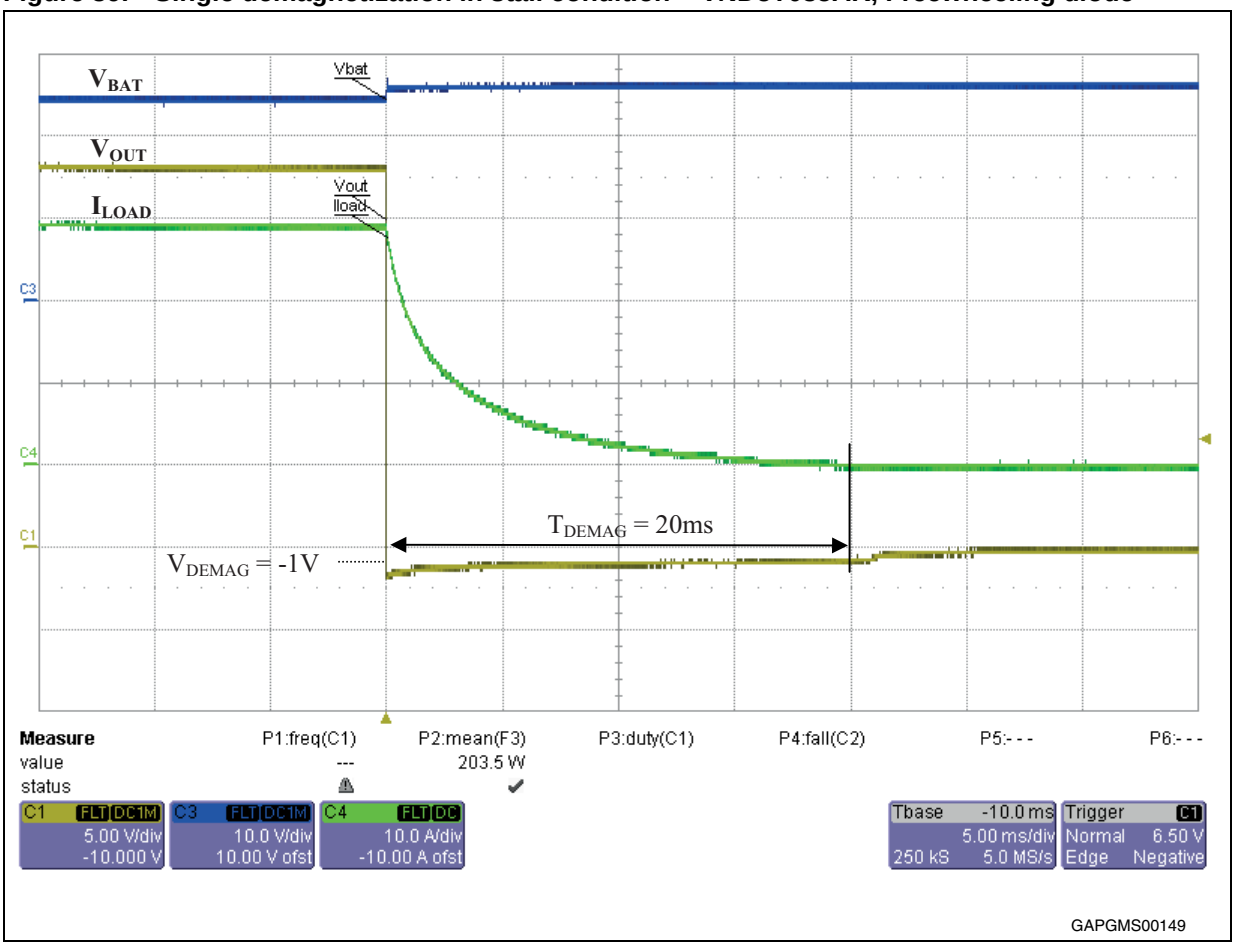
$$P_{AVG} = \frac{E}{T_{DEMAG}} = \frac{0.0315}{0.0093} = 3.4W$$

Step 6a) Single pulse measurement (verification of the theoretical analysis)

The measurement was done at room temperature on VND5T035AK loaded with a blocked DC motor (as specified in the beginning) and with an external freewheeling diode.

(The reverse battery protection circuitry was not applied during this measurement.)

Figure 39. Single demagnetization in stall condition – VND5T035AK, Freewheeling diode

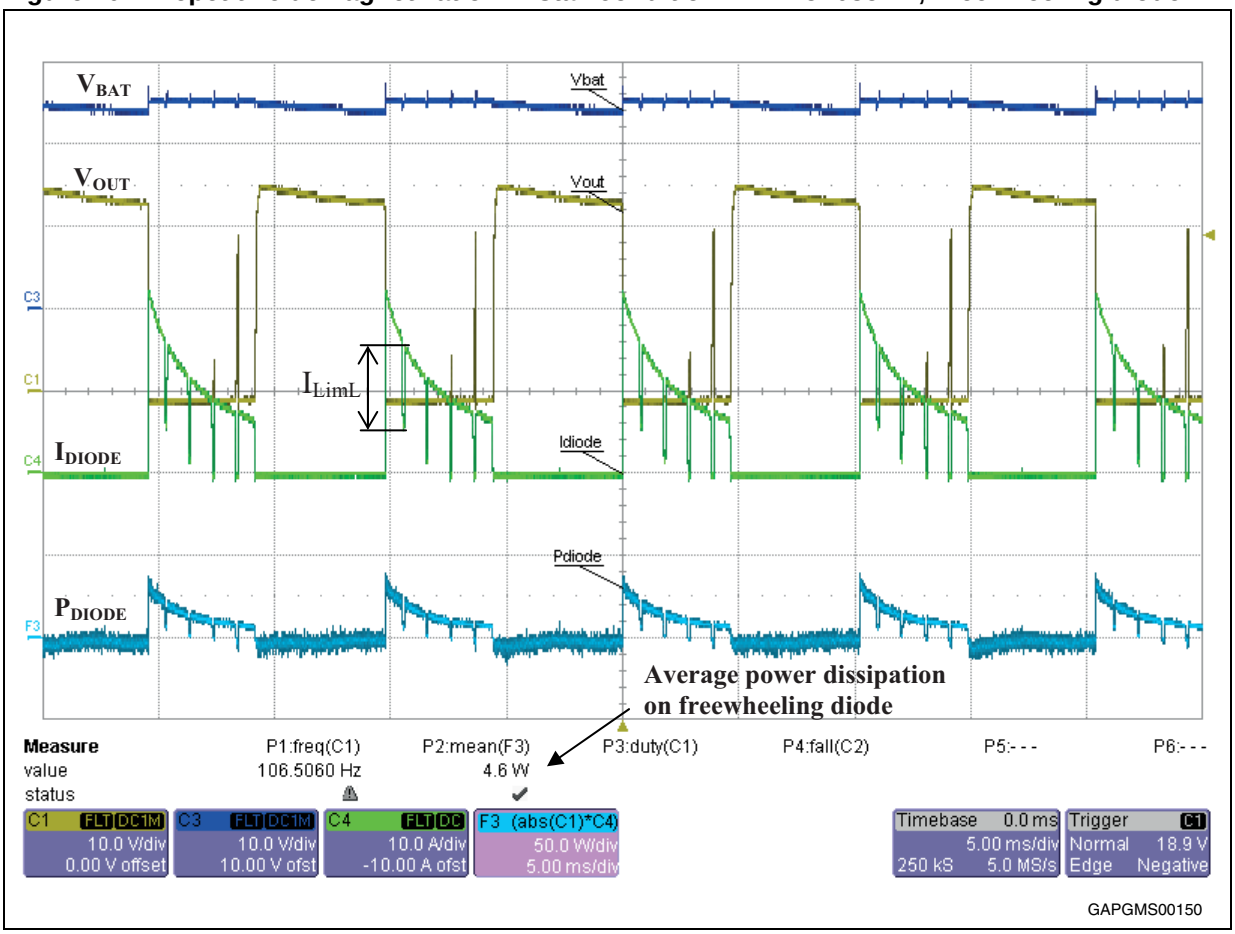


The measurement shows a significantly higher demagnetization time (20 ms) compared to the calculated one (12.9 ms).

This difference can be caused by an inappropriate inductance value of the motor used in the calculations. The inductance value was evaluated by a small signal measurement at 120 Hz (3.56 mH) and 1 kHz (1.9 mH). For the calculations, the inductance value measured at 120 Hz (3.56 mH) was used, while the conditions during the demagnetization phase are different.

Step 6b) Repetitive pulse measurement (verification of theoretical analysis)

Figure 40. Repetitive demagnetization in stall condition – VND5T035AK, Freewheeling diode



The average power dissipation measured on the freewheeling diode during the HSD thermal cycling (stall condition) was 4.6 W.

The HSD cycling is influenced by the relatively slow demagnetization of the load, so there are two cycling periods (~10 ms and ~1 ms) visible on the oscillogram:

When the HSD is turned-on, the load current increases while the junction temperature rises due to the high current of the blocked motor. When the temperature reaches the TSD threshold, the HSD output switches off. Then the output voltage is reversed by the inductive load and the load current is passed via the freewheeling diode (green waveform). When the junction temperature falls to T_{RESET}, the output turns on again. If the demagnetization current is still high enough (higher than I_{LimL}), the HSD output voltage remains at ~-1 V due

to the I_{LimL} limitation (TSD condition). Then the HSD is immediately switched off due to the high power dissipation (visible as short ~10 A peaks on the I_{DIODE} waveform). When the demagnetization current falls below I_{LimL}, the device may recover from TSD condition. Then the output is turned-on and the load current again increases until TSD is reached (~5.5 ms in our case) and so on.

Conclusion:

The demagnetization energy is 6 times higher than the device is able to withstand, therefore additional protection/clamping is necessary.

External protection circuitry with a freewheeling diode and a P-channel MOSFET as reverse battery protection was analyzed. A freewheeling diode in parallel with the DC motor is sufficient to protect the HSD in case of single as well as repetitive demagnetization events.

5 Paralleling of HSDs

5.1 Paralleling of FR_Stby (fault reset/standby) or IN (input)

The following chapters describe the paralleling of FR_Stby and IN pins of HSDs, taking into account device technology (monolithic HSDs or hybrid HSDs) and supply line configurations (either the same or separate supply lines for each HSD).

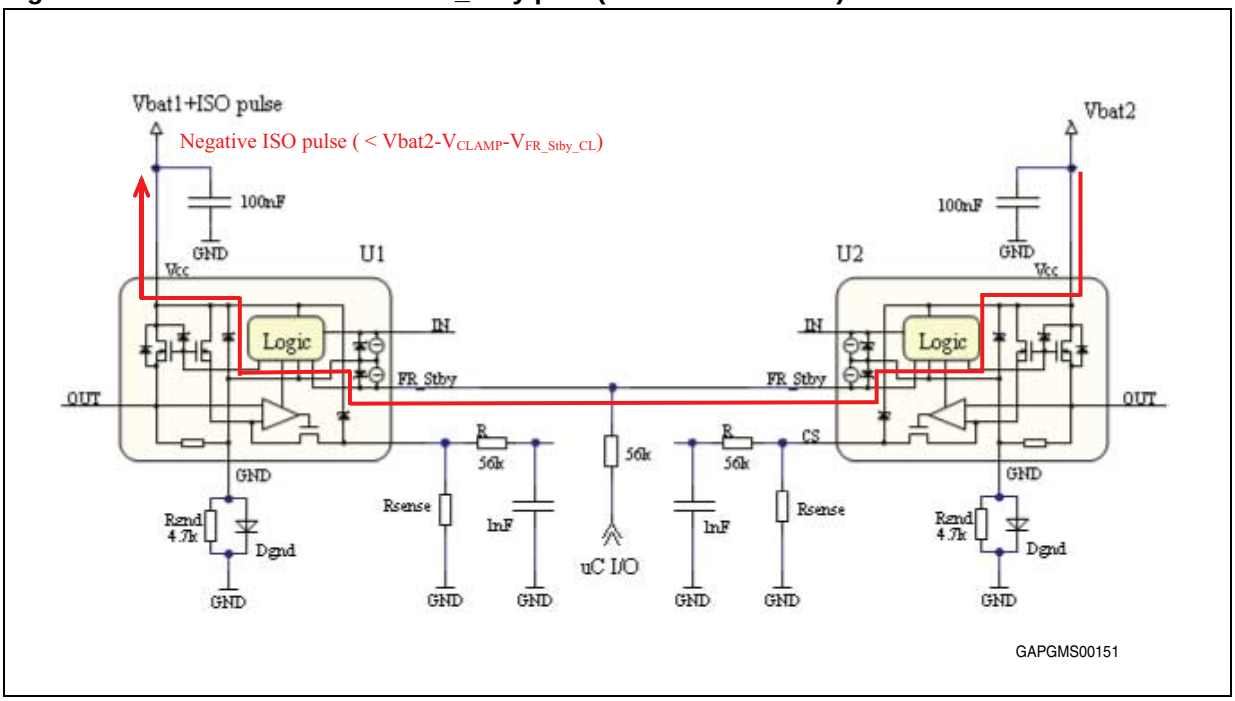
Direct connection of FR_Stby pins or IN pins is generally an allowed operation for devices designed in the same technology (monolithic or hybrid) supplied from one common supply line. In all other cases (such as the combination of monolithic with hybrid technology and different supply lines, or both) we should use additional components to ensure safe operation under any conditions in an automotive environment (including ISO pulses, reverse battery …).

The clamp structure on FR_Stby pins is similar to that on IN pins, therefore all the explanations related to the paralleling of FR_Stby pins are applicable to paralleling of IN pins as well.

5.1.1 Monolithic HSDs supplied from different supply lines

Paralleling FR_Stby pins of monolithic HSDs is possible, however some precautions in the schematic should be applied if the HSDs are supplied from different supply lines. In this case the direct connection of FR_Stby pins (as shown in *Figure 41*) is not safe.

Figure 41. Direct connection of FR_Stby pins (not recommended)



Direct connection of FR_Stby pins is not safe in following cases:

- Negative voltage surge on either Vbat1 or Vbat2
- Positive voltage surge either on Vbat1 or Vbat2 while:
  - Device GND pin disconnected;
  - Dgnd not used (resistor protection only);
  - Positive pulse energy higher than HSD (or Dgnd) capability - all paralleled devices can be damaged

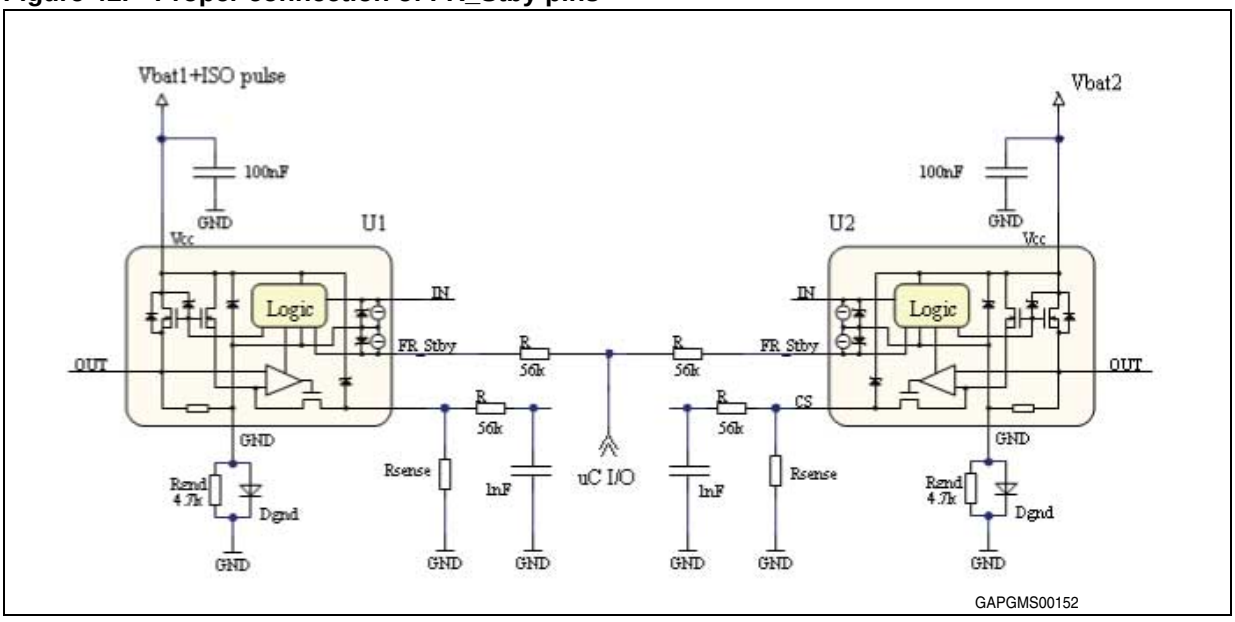
A negative voltage surge (ISO7637-2 pulse 1, 3a) either on Vbat1 or Vbat2 is directly coupled to the HSD GND pin through the involved Vcc-GND clamp structure. As soon as this occurs and the negative voltage on the GND pin is large enough to activate all involved clamp structures, there may be an unlimited current flow through both FR_Stby pins (supported by current from Vcc through the associated parasitic bipolar structure). This current can lead to malfunction or even failure of one or both of the HSDs.

A positive voltage surge (ISO7637-2 pulse 2a, 3b) either on Vbat1 or Vbat2 can lead to a HSD GND pin rise in voltage (in case of missing Dgnd, Dgnd failure or GND pin disconnected). As soon as this occurs, the voltage on FR_Stby pin also rises (the FR_Stby pin clamp structure is linked with the GND). If the voltage on FR_Stby line reaches ~12.6 V (clamp voltage on FR_Stby pin) there may be an unlimited current flow through both FR_Stby pins (supported by current from Vcc through the associated parasitic bipolar structure). This current can lead to malfunction or even failure of one or both of the HSDs.

In order to avoid such failures add a 56KΩ resistor in series to each FR_Stby pin (see *Figure 42*).

In principle the same applies to the input pins (the clamp structure is similar to that on the FR_Stby pins).

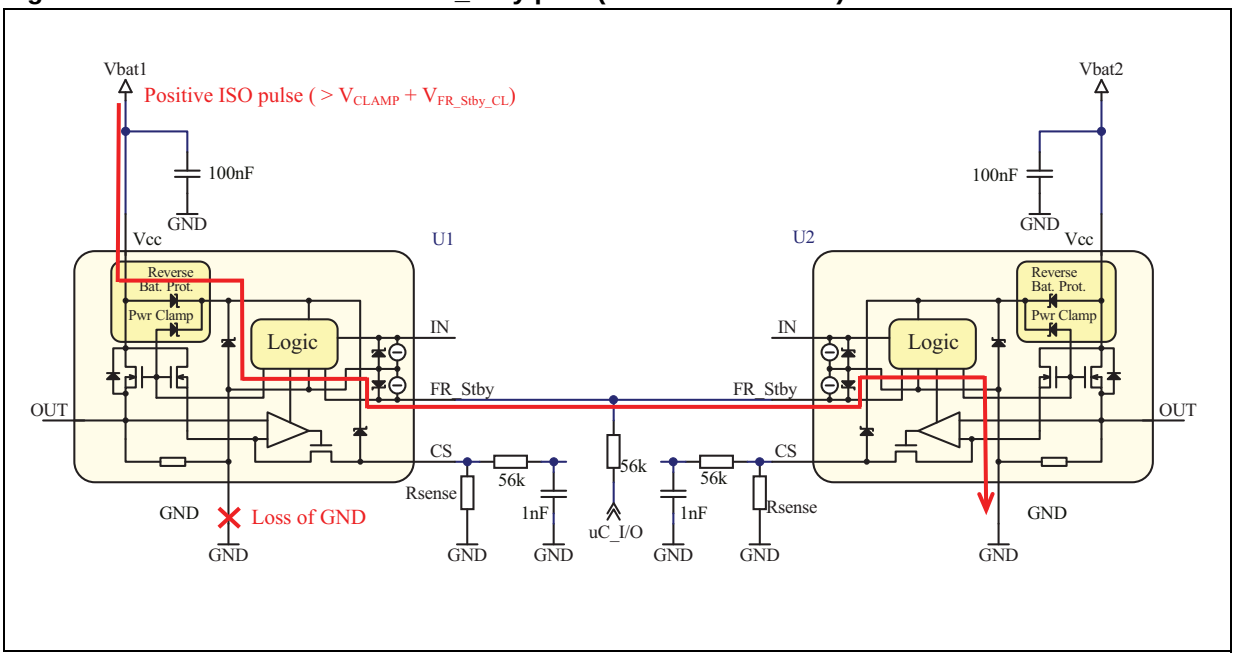
Figure 42. Proper connection of FR_Stby pins



5.1.2 Hybrid HSDs supplied from different supply lines

Paralleling of FR_Stby pins of hybrid HSDs is possible, however some precautions in the schematic should be applied if the HSDs are supplied from different supply lines. Direct connection of FR_Stby pins (as shown in *Figure 43*) is not safe.

Figure 43. Direct connection of FR_Stby pins (not recommended)



Direct connection of CS pins is not safe in the following cases:

- Loss of GND connection

If the GND connection of one device is lost, positive as well as negative ISO pulses on the associated supply line are no longer clamped (considering no other devices connected to this supply line). If the transient voltage is large enough to activate involved clamp structures, there may be unlimited current flow between both supply lines through FR_Stby pins. This current can lead to malfunction or even failure of one or both of the HSDs.

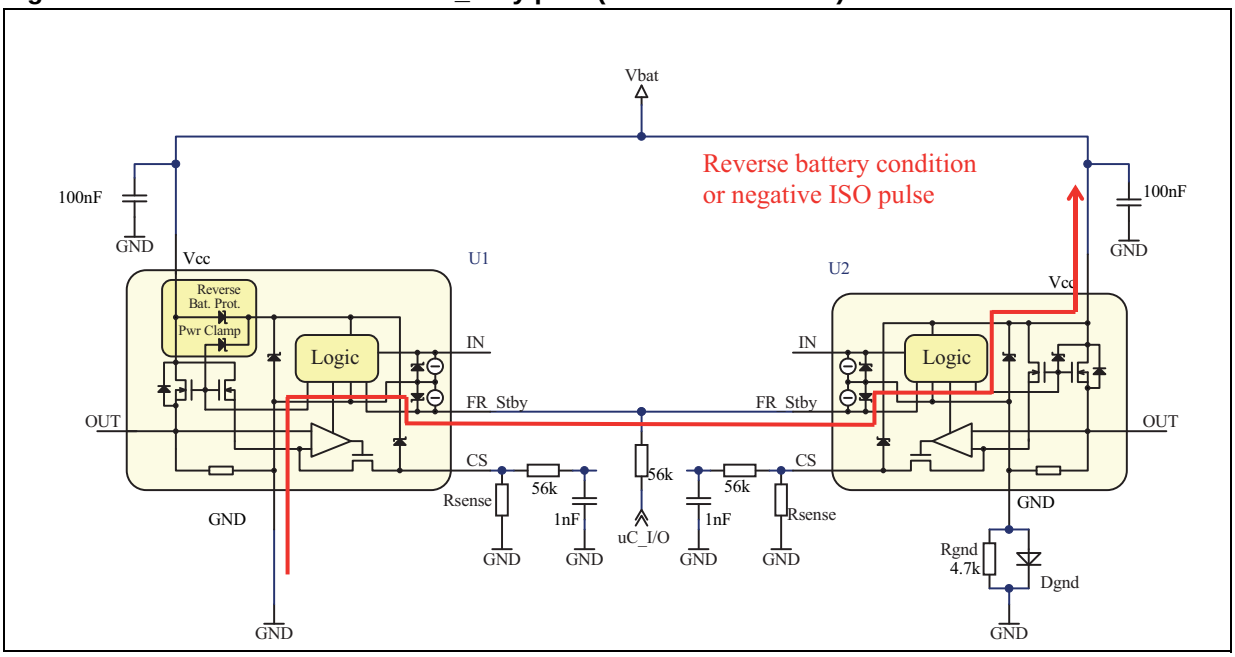
In order to avoid such failures add a 56 kΩ resistor in series to each FR_Stby pin (as previously described in case of monolithic devices – see *Section 5.1.1: Monolithic HSDs supplied from different supply lines*).

In principle, the same applies to the input pins as well (the clamp structure is similar to that on FR_Stby pins).

5.1.3 Mix of monolithic and hybrid HSDs

Paralleling of FR_Stby pins of monolithic and hybrid HSD is possible, however some precautions in the schematic should be applied. The direct connection of FR_Stby pins (as shown in *Figure 44*) is not safe (even if we consider the same power supply for both devices).

Figure 44. Direct connection of FR_Stby pins (not recommended)



Direct connection of FR_Stby pins is not safe in the following cases (single supply line considered):

- Reverse battery
- Negative ISO pulse

Due to the different concepts of reverse battery protection of hybrid and monolithic devices, there is a way for unlimited current flow between both devices in case of a reverse battery condition. The hybrid device has integrated reverse battery protection circuitry in the Vcc line, while the monolithic device needs an external diode/resistor in series with the GND pin (refer to chapter Reverse battery protection of this document). The different potential on each GND pin (hybrid: ~ 0 V, monolithic: V_{BAT} - 0.7 V) leads to the activation of both FR_Stby clamp structures when V_{BAT} is below ~ -14 V (V_{FR_StbyCL} + two diodes voltage drop). The resulting current can lead to malfunction or even failure of one or both of the HSDs.

In order to avoid such a failure add a 56 kΩ resistor in series to each FR_Stby pin (as previously described in case of paralleling of monolithic devices – see *Section 5.1.1: Monolithic HSDs supplied from different supply lines*).

In principle the same applies to the input pins (the clamp structure is similar to that on FR_Stby pins).

5.2 Paralleling of CS pins (current sense)

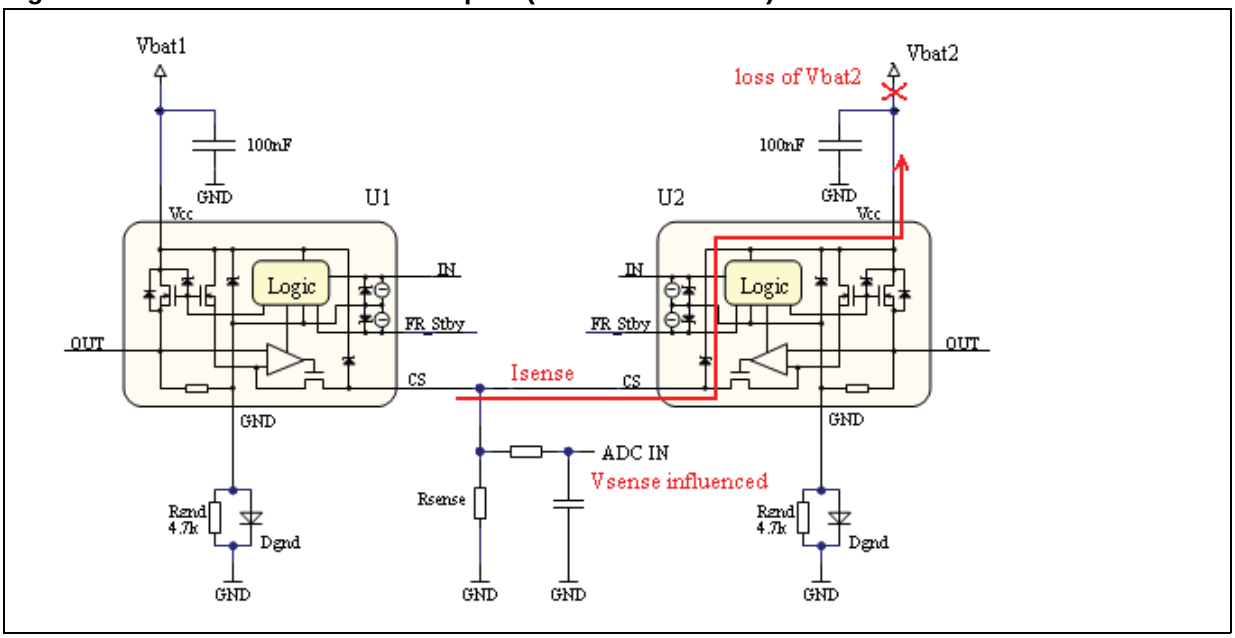
The following chapters describe the paralleling of CS pins of HSDs, taking into account device technology (monolithic HSDs or hybrid HSDs) and supply line configurations (either the same or separate supply line for each HSD).

Direct connection of CS pins is generally allowed when the devices are supplied from one common supply line. In case of separate supply lines, we should use additional components to ensure safe operation under any conditions in an automotive environment (including ISO pulses, reverse battery …).

5.2.1 Monolithic HSDs supplied from different supply lines

Paralleling of CS pins of monolithic HSDs is possible, however some precautions in the schematics should be applied if the HSDs are supplied from different supply lines. Direct connection of CS pins (as shown in *Figure 45*) is not safe.

Figure 45. Direct connection of CS pins (not recommended)



Direct connection of CS pins is not safe in the following cases:

- Negative voltage surge on either on Vbat1 or Vbat2
- Positive voltage surge either on Vbat1 or Vbat2 while:
  - Device GND pin disconnected;
  - Dgnd not used (resistor protection only);
  - Positive pulse energy higher than the HSD (or Dgnd) capability - all paralleled devices can be damaged
- Loss of Vbat1 or Vbat2

A negative voltage surge (ISO7637-2 pulse 1, 3a) either on Vbat1 or Vbat2 is directly coupled to the CS pin through the internal Vcc-CS clamp structure. If the negative voltage on the CS line is high enough to activate the Vcc-CS clamp structure, there may be an unlimited current flow through both CS pins. This current can lead to malfunction or even failure of one or both of the HSDs.

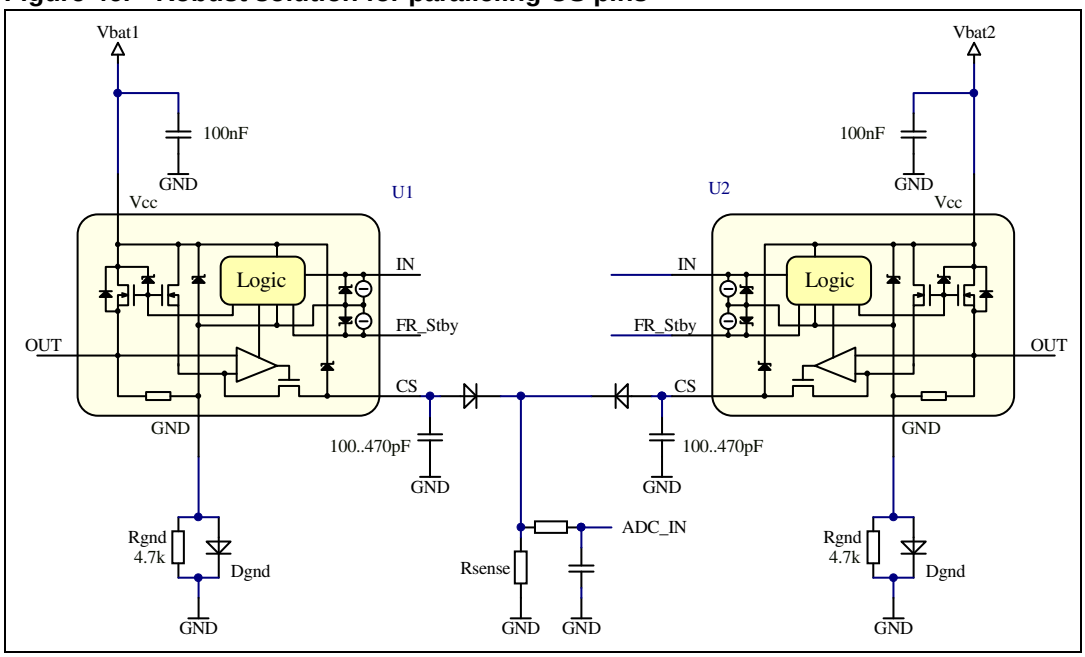
A positive voltage surge (ISO7637-2 pulse 2a, 3b) either on Vbat1 or Vbat2 together with a missing Dgnd (Dgnd not used, Dgnd failure or GND pin disconnected) can activate the Vcc-CS clamp structure (clamp voltage similar to Vcc-GND clamp). As soon as this occurs, there may be an unlimited current flow through both CS pins. This current can lead to malfunction or even failure of one or both of the HSDs.

Loss of either Vbat1 or Vbat2 leads to an incorrect current sense signal. If Vbat2 is lost, U2 (and other components connected to Vbat2) is supplied by the U1 current sense signal through the internal Vcc-CS clamp structure. Consequently the voltage on the CS bus drops to almost 0 V resulting in an invalid V_{SENSE} reading.

In order to protect the devices during ISO pulses and to ensure a valid current sense signal, we may add a diode in series to each CS pin (as shown in the following schematics). In order to suppress the rectification of noise injected to the sense line, add a ceramic filter capacitor between each CS pin and ground.

However, the voltage drop on the diode in series with the CS pin can have an influence on the dynamic range of current sense.

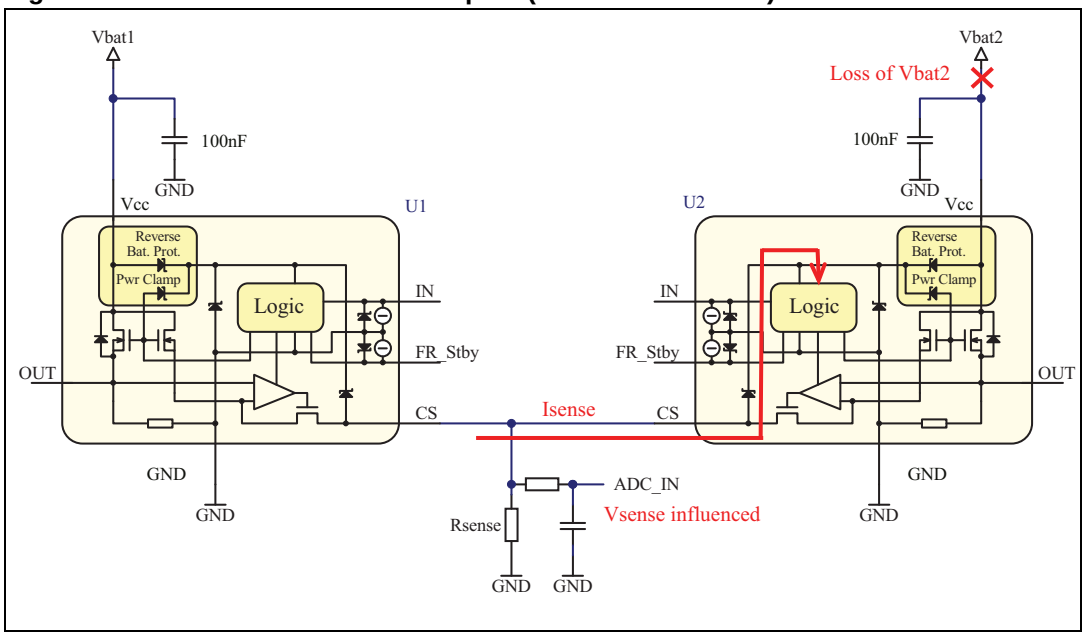
Figure 46. Robust solution for paralleling CS pins



5.2.2 Hybrid HSDs supplied from different supply lines

Paralleling CS pins of hybrid HSDs is possible, however some precautions in the schematic should be applied if the HSDs are supplied from different supply lines. Direct connection of CS pins (as shown in *Figure 47*) is not safe.

Figure 47. Direct connection of CS pins (not recommended)



Direct connection of CS pins is not safe in the following cases:

- Loss of Vbat1 or Vbat2
- Loss of GND connection

Loss of either Vbat1 or Vbat2 leads to an incorrect current sense signal. If Vbat2 is lost, the U2 logic part is supplied by the U1 current sense signal through the internal Vcc-CS clamp structure. Consequently the voltage on the CS bus drops, resulting in an inaccurate V_{SENSE} reading.

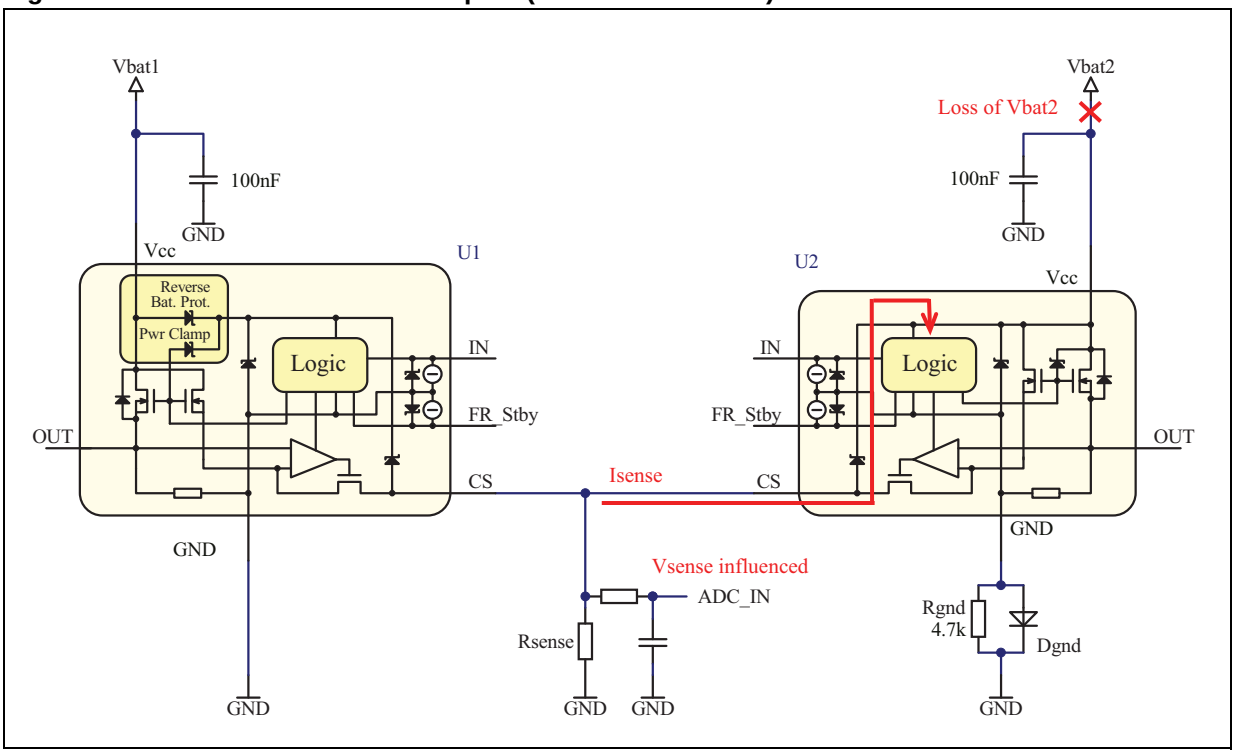
If the GND connection of one device is lost, positive as well as negative ISO pulses on the associated supply line are no longer clamped (considering no other devices connected on this supply line). If the transient voltage is high enough to activate the involved clamp structures, there may be an unlimited current flow between both supply lines through the CS pins. This current can lead to malfunction or even failure of one or both of the HSDs.

In order to ensure a valid current sense signal and to protect devices in all previously described cases, we may add a diode in series to each CS pin (as previously described in the case of monolithic devices – see *Section 5.1.1: Monolithic HSDs supplied from different supply lines*).

5.2.3 Mix of monolithic and hybrid HSDs supplied from different supply lines

Paralleling CS pins of monolithic and hybrid HSDs is possible, however some precautions in the schematic should be applied if the HSDs are supplied from different supply lines. Direct connection of CS pins (as shown in the next picture) is not safe.

Figure 48. Direct connection of CS pins (not recommended)



Direct connection of CS pins is not safe in following cases:

- Negative ISO pulse on Vbat2
- Loss of Vbat1 or Vbat2
- Loss of GND connection

A negative voltage surge (ISO7637-2 pulse 1, 3a) on Vbat2 is directly coupled to the CS pin through the internal Vcc-CS clamp structure. If the negative voltage on the CS line is high enough to activate the Vcc-CS clamp structure, there may be an unlimited current flow through both CS pins. This current can lead to malfunction or even failure of one or both of the HSDs.

Loss of either Vbat1 or Vbat2 leads to an incorrect current sense signal. If Vbat2 is lost, the U2 logic part is supplied by the U1 current sense signal through the internal Vcc-CS clamp structure. Consequently the voltage on the CS bus drops, resulting in an inaccurate V_{SENSE} reading.

If the GND connection of one device is lost, positive as well as negative ISO pulses on the associated supply line are no longer clamped (considering no other devices connected to this supply line). If the transient voltage is high enough to activate the involved clamp structures, there may be an unlimited current flow between both supply lines through the CS pins. This current can lead to malfunction or even failure of one or both of the HSDs.

In order to ensure a valid current sense signal and to protect the devices in all previously described cases, we may add a diode in series to each CS pin (as previously described in case of monolithic devices – see *Section 5.1.1: Monolithic HSDs supplied from different supply lines*).

5.3 Paralleling of outputs

Paralleling output channels should be restricted to exceptional cases. Due to the significant stray inductance of the wire harness in truck applications, a paralleling of output channels implies the exposure to a critical high demagnetization energy in case of short circuit conditions, impacting the component lifetime. Therefore, whenever a paralleled output configuration is considered, one should add an external freewheeling circuit to protect the HSD from excessive demagnetization energy.

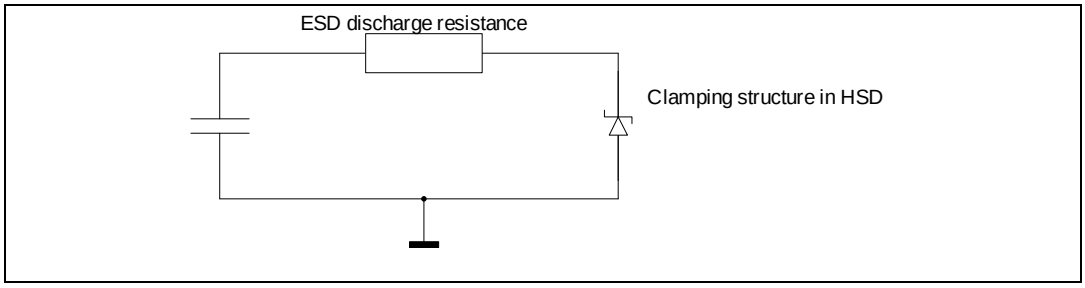
Other technical subjects linked with paralleling outputs is treated in a future release of this HWDG.

6 ESD protection

6.1 ESD protection of HSD – calculations

The ESD robustness of a typical HSD is rated at 5000 V on the Output - as well as on the Vcc-pin - according to the Human Body Model (100 pF, 1.5 kΩ). This applies to positive as well as negative ESD pulses. For any ESD pulse beyond these values an external protection is required.

Calculation of the energy capability of the HSD output without external protection (negative ESD pulse)



The energy content of the ESD pulse is:

Equation 11*:*

$$W_{ESD} = 1/2 * C_{ESD} * V_{ESD}^2$$

The energy dissipated by the resistance is:

Equation 12

$$W_R = 1/2 * C_{ESD} * (V_{ESD} - V_{DEMAG})^2$$

The energy dissipated by the HSD is:

Equation 13

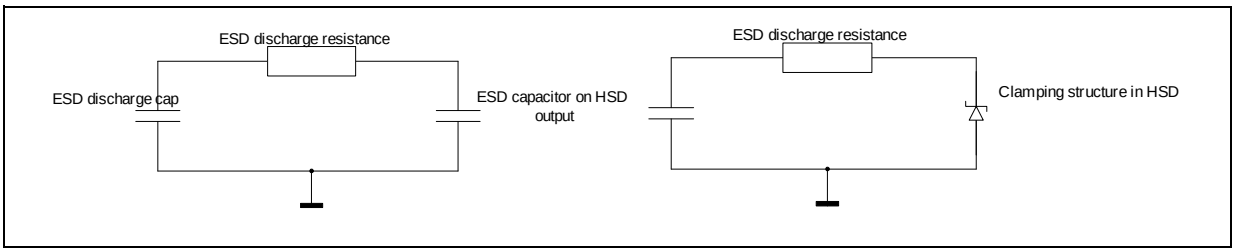
$$W_{HSD} = (V_{ESD} - V_{DEMAG}) * V_{clamp} * C_{ESD}$$

The maximum ESD pulse energy capability of the HSD can be calculated using *Equation 13* and the data sheet parameters (typical example):

$$W_{HSDMAX} = 4936V * 64V * 100\,pF \cong 32\mu J$$

Calculation of external protection (negative ESD pulse)

When the ESD pulse amplitude or the ESD capacitance is increased or the discharging resistance is decreased, the HSD needs external protection, because the energy discharged in the HSD exceeds the limit calculated in *Equation 13*. If we add a ceramic capacitor on the output, the ESD pulse initially only charges the capacitor without impacting the HSD until the voltage reaches the HSD active clamping voltage. Then the voltage stays constant (without further impact on the capacitor), and excessive energy is absorbed by the ESD discharge resistance and by the HSD.



If in the first step we neglect the HSD, the final voltage becomes:

Equation 14*:*

$$V_{Final} = V_{ESD} * (\frac{C_{ESD}}{C_{ESD} + C_{EXT}})$$

With

$$V_{ESD} = 8kV$$

$$C_{ESD} = 330\,pF$$

and

$$V_{Final} = 64V$$

C_{EXT} should be >41nF. But since the HSD can absorb some ESD energy on its own, the external capacitor can actually be smaller.

The time t_1 defines the point in time when the external capacitor reaches the demagnetisation voltage of the HSD and does not charge further.

The time constant for discharging the ESD capacitor is:

Equation 15

$$\tau = R_{ESD} * C_{ESD} * \frac{C_{EXT}}{C_{EXT} + C_{ESD}}$$

with $C_{EXT} >> C_{ESD} \rightarrow$

$$\tau \approx R_{ESD} \cdot C_{ESD}$$

Equation 16

$$I(t) = \frac{V_{ESD}}{R_{ESD}} * e^{-t/\tau}$$

Equation 17

$$V_{C_{ESD}}(t) = V_{ESD} * e^{-t/\tau} + V_{Final} * (1 - e^{-t/\tau})$$

Equation 18:

$$V_{C_{EXT}}(t) = V_{Final} * (1 - e^{-t/\tau})$$

Equation 19

$$t_1 = -\tau * \ln(1 - \frac{V_{DEMAG}}{V_{Final}})$$

The residual voltage at the ESD capacitor, when the external capacitor is charged to the HSD clamping voltage becomes:

Equation 20

$$V_{C_{ESD}}(t1) = V_{ESD} - V_{DEMAG} * \frac{C_{EXT}}{C_{ESD}}$$

Therefore, the energy absorbed by the HSD becomes:

Equation 21

$$W_{HSD} = (V_{ESD} - V_{DEMAG} * (1 + \frac{C_{EXT}}{C_{ESD}})) * V_{clamp} * C_{ESD}$$

Once we know the maximum ESD energy capability of the HSD (calculated with *Equation 13*), we can calculate the necessary external capacitor:

Equation 22

$$C_{EXT} > \frac{(V_{ESD} - V_{DEMAG})}{V_{DEMAG}} * C_{ESD} - \frac{W_{HSDMAX}}{V_{DEMAG} * V_{clamp}}$$

Of course the external capacitor needs a voltage capability larger than the maximum clamping voltage of the HSD.

In addition it must be ensured, that the ESD discharge current cannot exceed the maximum current capability of the HSD:

Equation 23:

$$I(t_1) =< I_{LIMH\,\max}$$

and therefore

Equation 24*:*

$$C_{EXT} > C_{ESD} * (\frac{(V_{ESD} - R_{ESD} * I_{LIMH\ max})}{V_{DEMAG}} - 1)$$

Example 1: Contact discharge 8 kV, 330 pF, 2 kΩ, $I_{LIMH\ max}$=55 A (VND5T035AK HSD), battery not supplied (Vcc=0 V)

→ according to *Equation 22*: C_{EXT} > 33 nF

→ according to *Equation 24*: C_{EXT} > -526 nF

→ C_{EXT} > 33 nF fulfils both requirements.

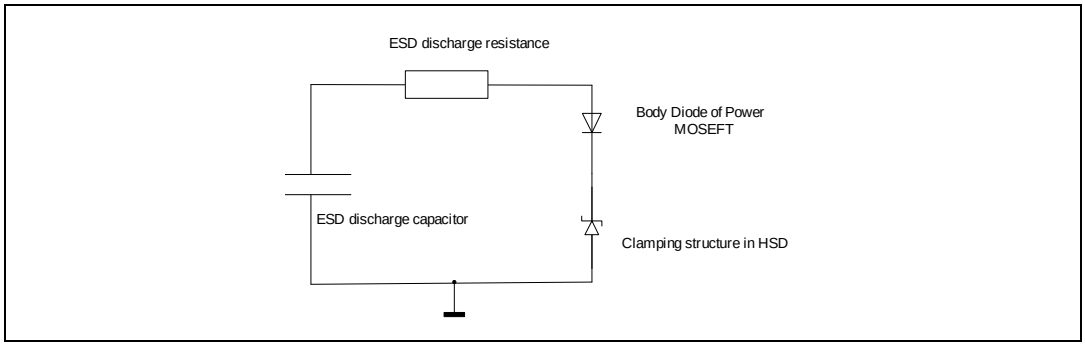
Example 2: Contact discharge 6 kV, 150 pF, 330 Ω, battery not supplied (Vcc = 0 V)

→ according to *Equation 22*: C_{EXT} > 6.1 nF

→ according to *Equation 24*: C_{EXT} > -28.6 nF

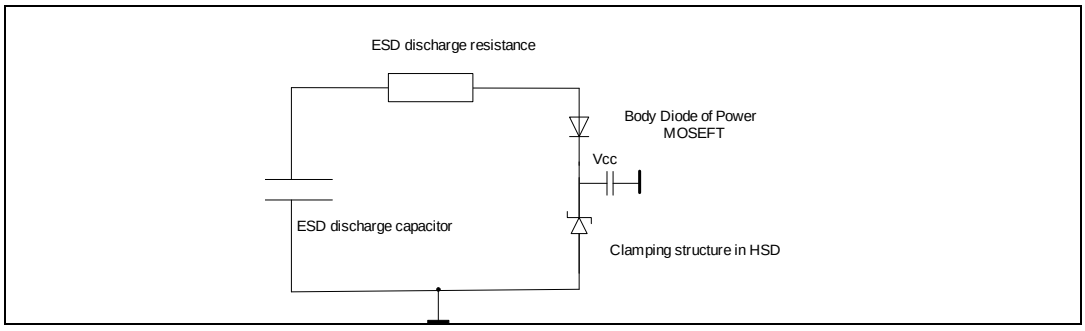
→ C_{EXT} > 6.1 nF fulfils both requirements.

Positive ESD pulses without external protection



A positive ESD pulse on the output is transferred through the body diode of the power MOSFET to the Vcc pin of the HSD, stressing the Vcc-GND clamping structure. The ESD ratings of the Vcc-GND clamping structure is the same for the output clamping structure. Therefore the same considerations and calculations apply for negative ESD pulses on the output.

Positive ESD pulses with external protection

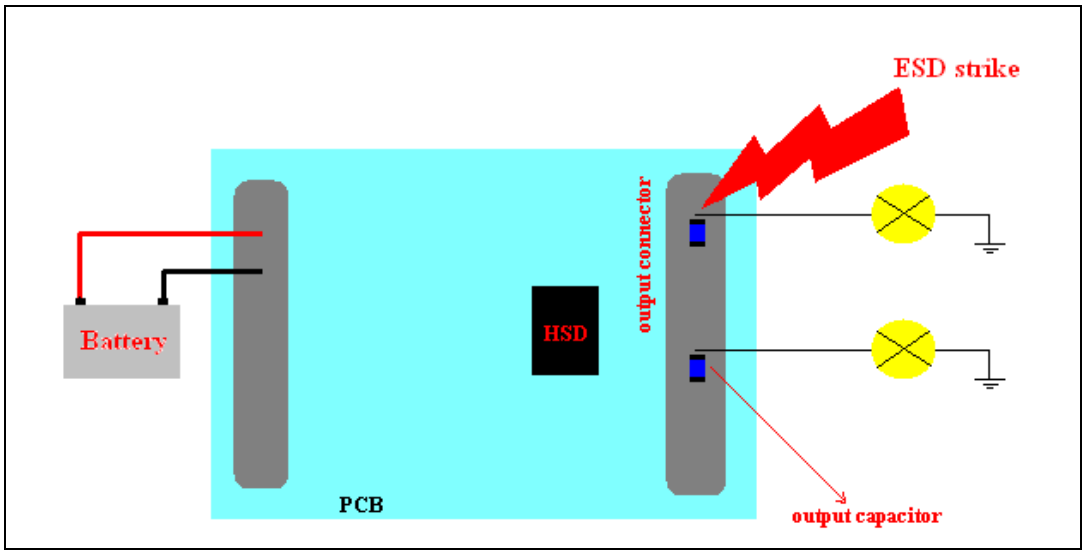


A positive ESD pulse on the output is transferred through the body diode of the power MOSFET to the Vcc pin of the HSD, so the same requirements to dimension the external capacitor apply as the negative ESD pulses on the output.

6.2 ESD protection – ECU level (layout consideration)

An ESD pulse on a powered ECU output connector is an expected event during the life of a car.

Typically contact and air discharge tests are performed during module qualification. (Ref. IEC61000-4-2). The possible risk at application level is an early failure of the HSD with following resistive short circuit between Vcc and OUT. The ESD pulse destruction value strongly depends on the module layout. In order to make the module pass the required stress level, add a ceramic capacitor with a value in the order of tens of nF to the output close to the connector. This capacitor decreases both the applied dv/dt and the maximum output voltage seen by the HSD.



7 Robust design

7.1 Design suggestions for HSDs and relays on the same PCB

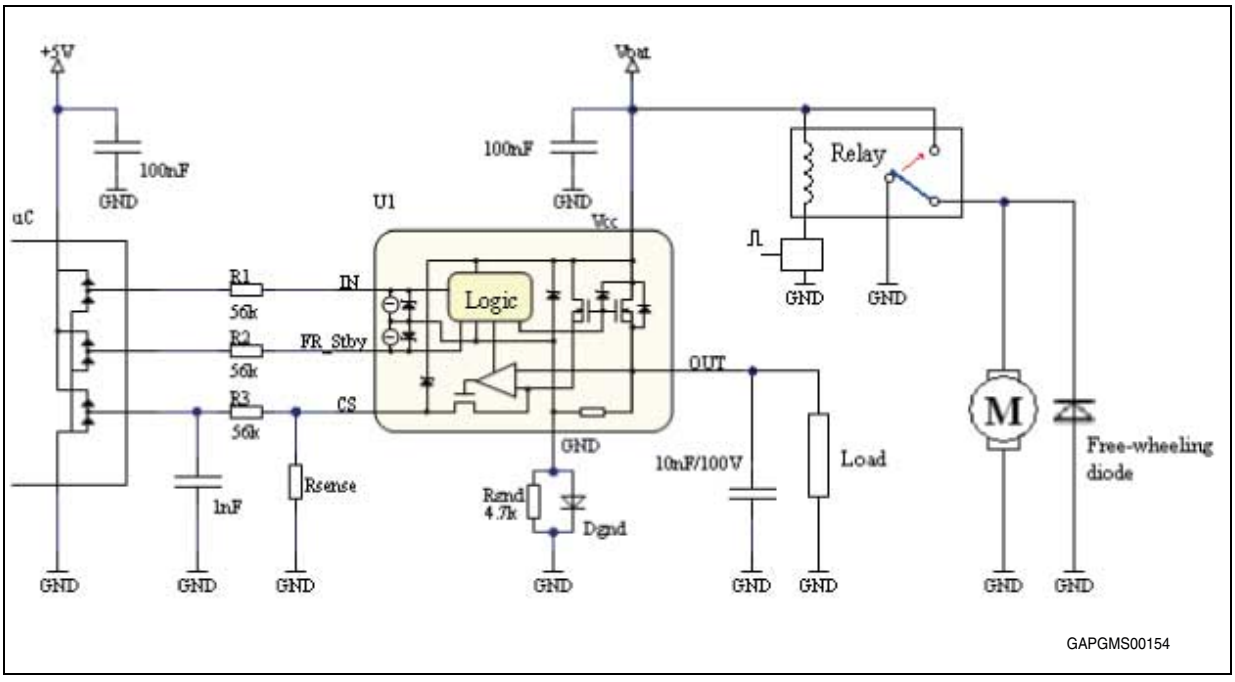
A typical ECU today still employs, along with the smart power HSDs and LSDs, a certain number of electromechanical relays. The activation of these relays, being on the same PCB and supplied by the same battery line as the HSDs, may lead to fast dv/dt on the battery line due to bouncing of the contacts when inductive loads are driven. Even a standard high frequency capacitor (typ. value 100 nF) across the local battery and ground is not enough to smoothen these pulses. The possible risk at application level is an early failure of the HSD with a following resistive short between Vcc and OUT. In order to avoid this, add a free-wheeling diode across the inductive load terminals (see below diagram) in order to minimize the effects of the relay bouncing.

Applicative hints, on top of the above, that would help to make the HSDs less sensitive when used with relays on the same board are:

a) The usage of four-layer PCBs where the inner layers are used as low resistance shield (one should be connected to module GND, the other to the battery connector)

b) The CS pin circuitry as recommended in the datasheet

c) The use of separate connectors to supply the HSDs



8 Operation with AMICO

8.1 Introduction on AMICO

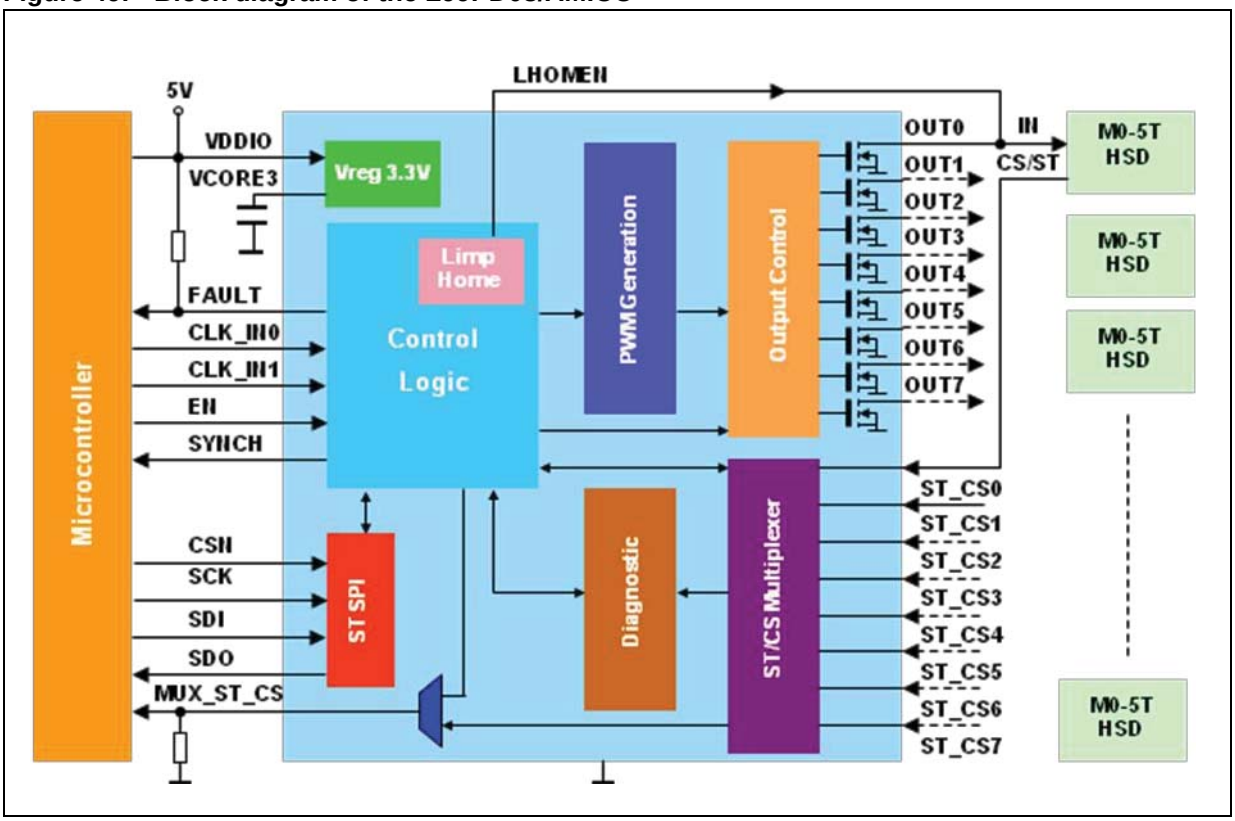
The L99PD08, also called AMICO (Advanced Multiplexed and Integrated Co-processor), interfaces between the microntroller and the high-side drivers (*Figure 50*). It is an intelligent multiplexer which controls and performs the diagnostic of 8 HSD channels from the M0-5T/M0-5 and M0-5E families.

The device integrates several functions which reduce the workload of the microcontroller and the number of required I/Os.

The main features of the device are:

- Control and diagnostic of HSDs via ST SPI interface (16 bit)
- Synchronous and detailed diagnostic
- PWM generation (8-bit resolution) for 8 independent channels with phase shift
- Programmable open load and overload detection thresholds
- On board filtered diagnostic (64µs to 96µs)
- Programmable inrush blanking time
- Time out watchdog with limp home mode
- Current sense multiplexer

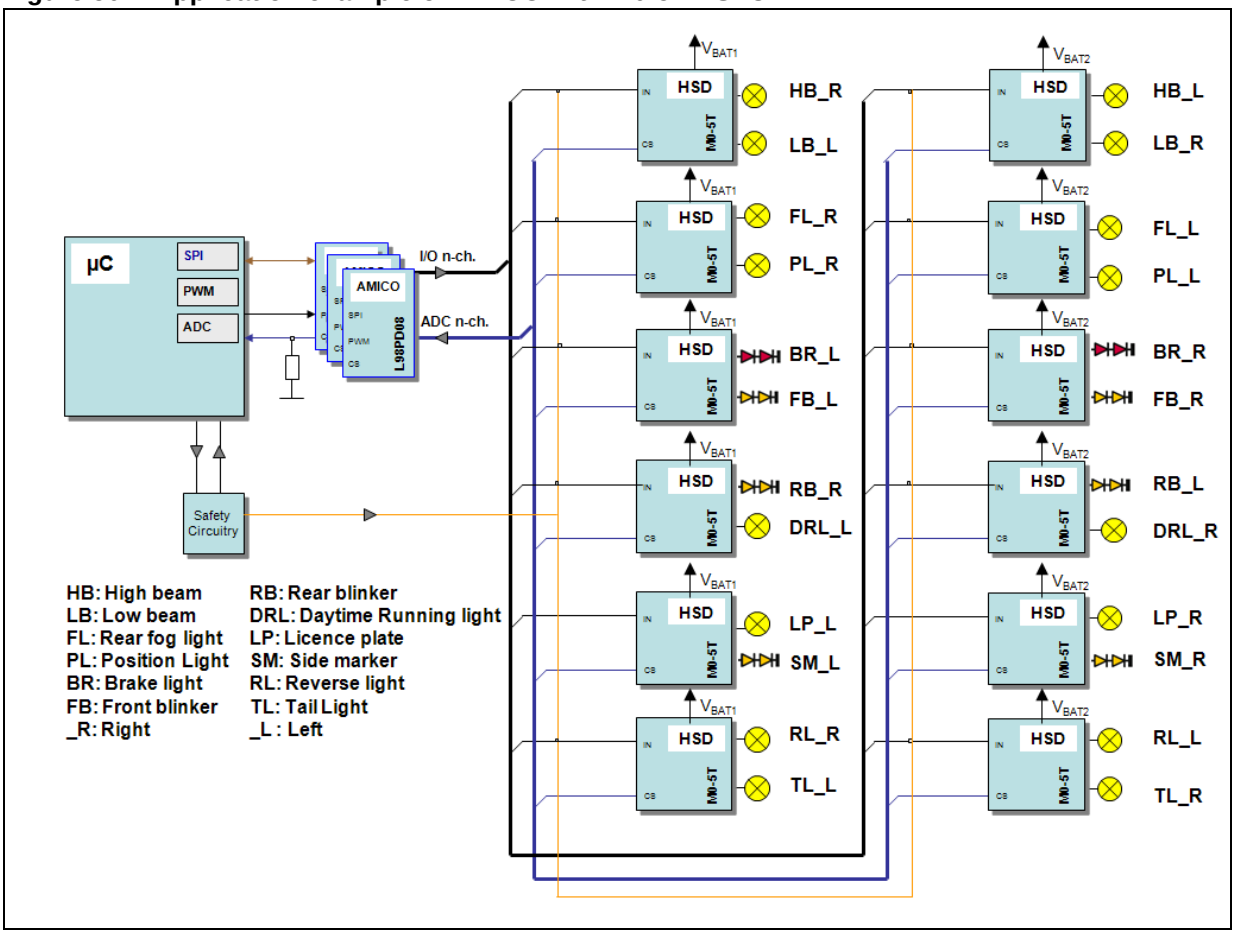
Figure 49. Block diagram of the L99PD08/AMICO



The application benefits are:

- Enhanced short-circuit robustness of the HSDs by fast reaction time
- Detailed and synchronous diagnostic without intervention of the µC
- Extremely low µC workload with simplified software
- µC pin count reduction by SPI interface
- Full partitioning flexibility thanks to the compatibility with any M0-5T HSDs, regardless of their Rdson, supply lines and number of channels per device
- LED and Bulb compatibility without external components
- Enhanced system reliability
- Cost reduction at system level
- Rejection of failure notification caused by transients with a duration below 50 µs

Figure 50. Application example of AMICO with M0-5T HSDs



8.2 Control and diagnostic function

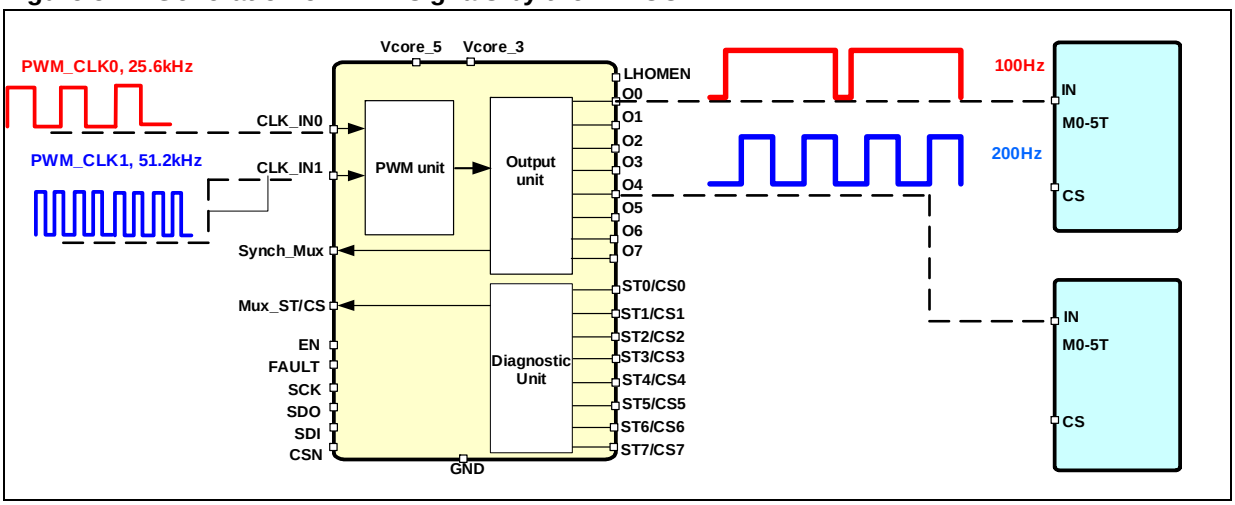
The following chapter describes the control of the HSD by the AMICO as well as its diagnostic functions.

8.2.1 PWM control

The L99PD08 can control the M0-5T HSDs in PWM. These PWM signals are generated from two PWM clock inputs (PWM_CLK_0/1). The duty cycle of each channel is programmed via SPI with a step of 0.4 % or 8-bit resolution.

For instance, an output driven at 100 Hz or 200 Hz, requires a PWM clock frequency of 25.6 kHz or 51.2 kHz respectively (see *Figure 51*).

Figure 51. Generation of PWM signals by the AMICO



8.2.2 HSD control in normal conditions

AMICO's outputs Ox are open drains. In normal operation, the Ox actively turn off the HSDs by pulling down the HSD's input (see O7, *Figure 53*).

To turn on the HSDs, the Ox are disabled and a pull-up source sets the HSD's input to High. The pull-up sources can be either LHOMEN (see O0, *Figure 53*) or another pull up source.

Note that LHOMEN stands for Limp Home Not. This signal is High (~ VDDIO) when the device is in normal mode and Low in limp home mode (*Figure 52*). In the particular case of loss of VDD, LHOMEN is in high impedance, therefore a pull down on this pin e.g. ~ 10 kΩ should be used.

Figure 52. Behaviour of the LHOMEN signal

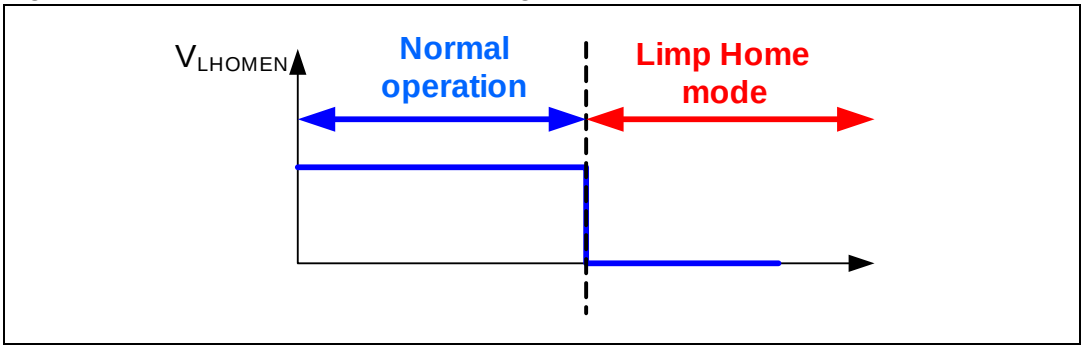
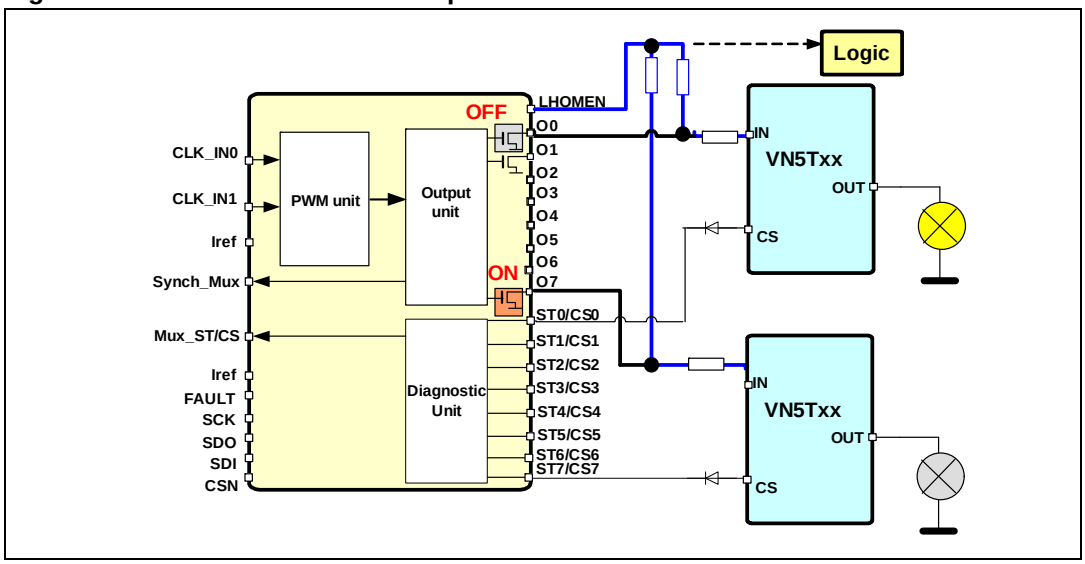


Figure 53. Control of the HSDs' inputs



8.2.3 HSD control in limp home mode

The AMICO enters limp home mode if one of the following events occur:

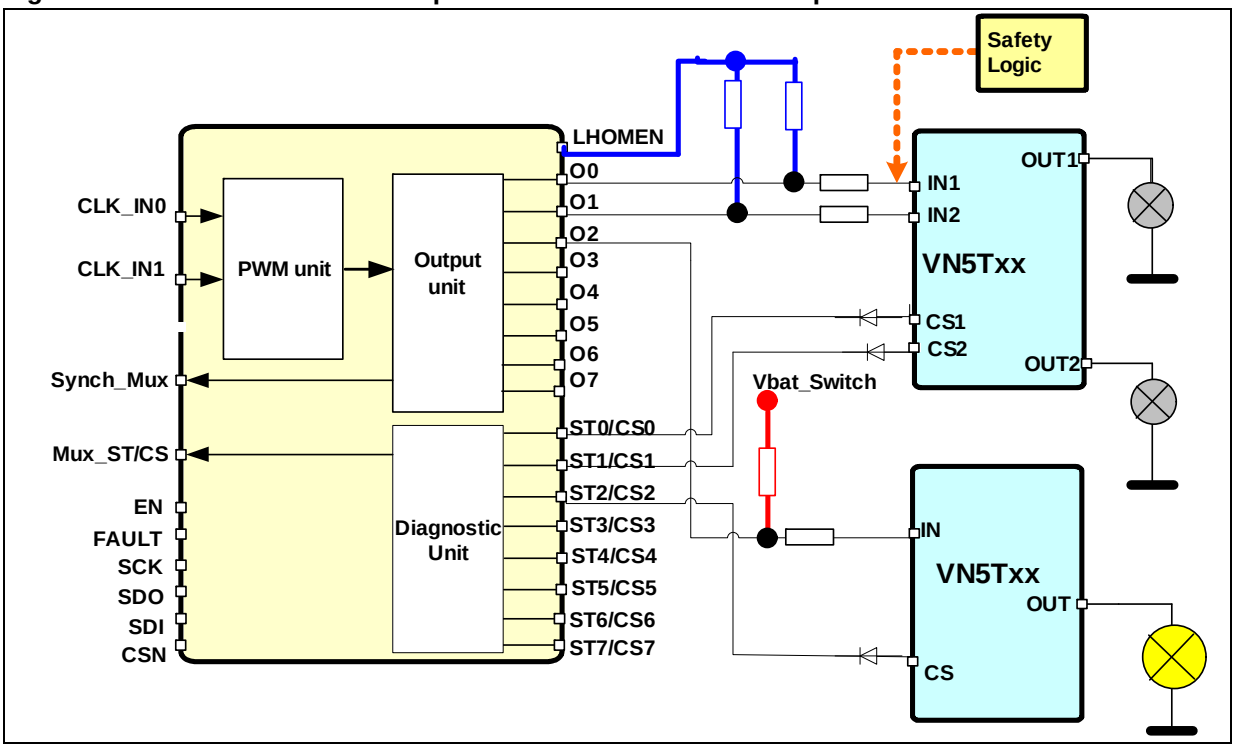
- Loss of VDDIO supply
- Watchdog timeout
- SPI commands Ox00 or OxFF are interpreted as a short circuit of SDI to GND or to the supply
- Special SPI command (software reset)
- Power on reset of the AMICO (default state)

In this case, the content of the registers are reset to their default value and the outputs 0x of the AMICO are turned off. Hence, the behaviour of the HSD depends on the chosen pull-up source.

Three configurations are possible:

- If the pull-up source is LHOMEN, the corresponding HSD channel is turned off, as LHOMEN goes Low (e.g. for high beams, O2 in the example on *Figure 54*). In the particular case of loss of VDD, LHOMEN is in High impedance, and the HSD channel is pulled down by the weak current sink of the HSD's input. A pull down (e.g. 10 kΩ) on the LHOMEN can also be used.
- If the pull-up source is V_{bat} or a derived signal from V_{bat} (noted V_{bat} _switch on *Figure 54*), the HSD channel turns on, as long as the pull-up source is High (e.g., for low beams, O2 on *Figure 54*)
- If the pull-up source is a safety logic, e.g., for blinker, hazard lights or brake lights, the corresponding HSD's output follows the pull-up source (see O0 *Figure 54*)

Figure 54. State of the HSDs' outputs while the AMICO is in limp home mode



8.2.4 Diagnostic principle of the HSDs by the AMICO

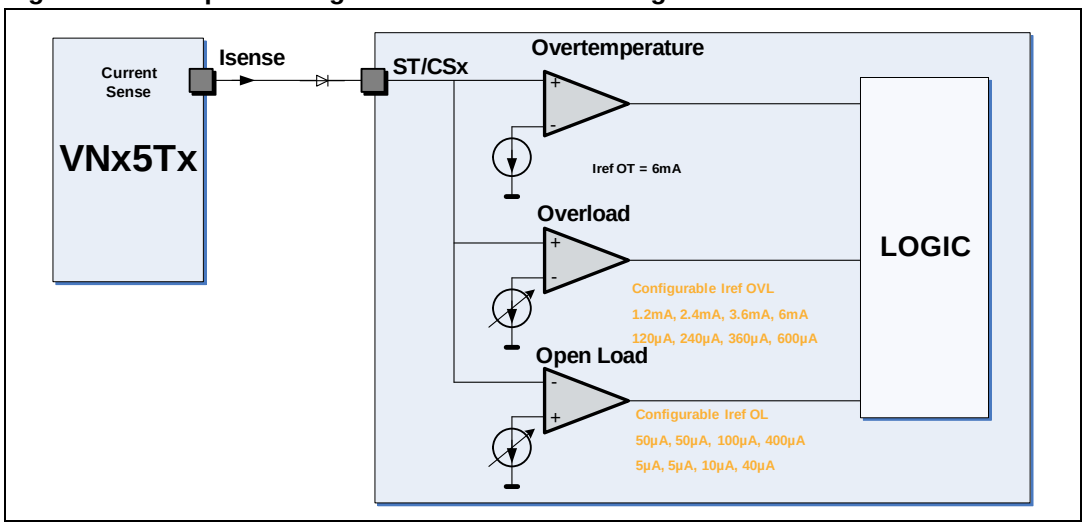
Principle of internal diagnostic

The AMICO processes the currents coming from the current sense pins of the connected M0- 5T HSDs. These currents are noted I_{SENSE} in the rest of the document. The *Figure 55* shows the principle. Moreover, the AMICO provides a synchronous and detailed diagnostic with a short-time filter of 64µs to 96µs.

Indeed, the device distinguishes between:

- Normal operation
- Open load in on-state
- Short circuit to V_{bat} in off-state or open load in off-state
- Overload
- Power limitation or thermal shutdown

Figure 55. Simplified diagram on the on-board diagnostic



I_{SENSE} is compared with configurable current references of the AMICO. These current references can be configured in order to adjust the open load (in on-state) and the overload detection threshold. Note that the threshold for open load in on-state and overload are coupled (refer to the datasheet of the L99PD08).

The threshold for power limitation, overtemperature, short circuit to V_{bat} and open load in off-state is fixed to ~ 6 mA typ.

Condition	Effect/failure reporting
Isense < current reference for open load	Failure flag for open load
Isense > current reference for overload	Failure flag for overload
Isense > 6 mA in on-state	Failure flag for overtemperature/power limitation
Isense > 6 mA in off-state	Failure flag for open load short to Vbat in off-state

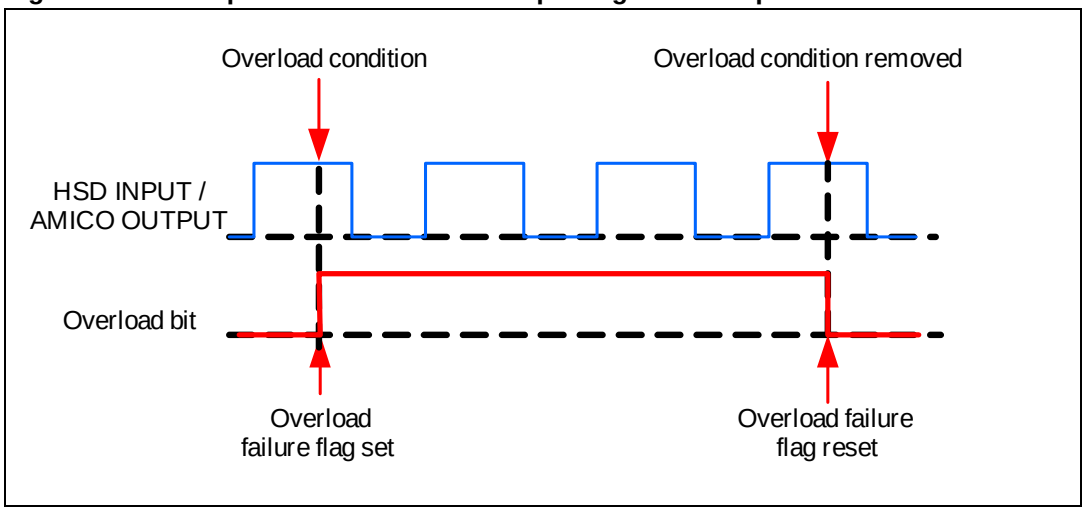
A general diagnostic is reported in the global status register as well as the AMICO's fault pin, whereas detailed diagnostics are reported in the corresponding status registers (refer to the datasheet of the L99PD08 for more details).

Failure reporting during PWM operation

The AMICO provides a real time diagnostic, which means that the failure flags are not latched: If a normal operation is detected, the failure flags in the status registers are removed.

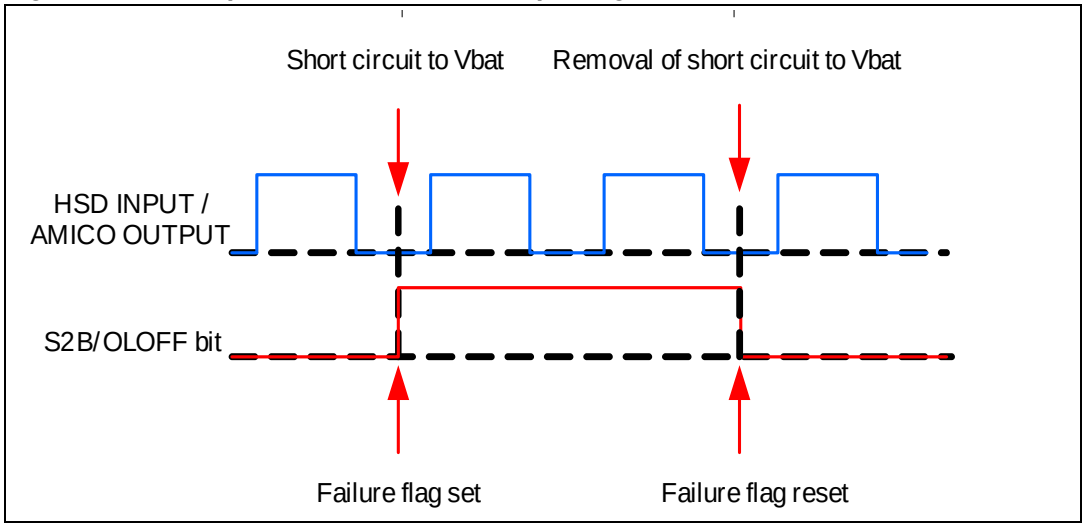
In PWM operation, however, the on-state relevant diagnostics are latched during the off-state and refreshed in the next on-phase in order to avoid a toggling of the failure flags with the PWM operation (*Figure 56*). The on-state relevant diagnostics are: open load in on-state, overload, power limitation or thermal shutdown.

Figure 56. Example of overload failure reporting in PWM operation



The same behaviour also applies to the off-state relevant diagnostics: open load in off-state (noted OLOFF) or short circuit to V_{bat} (noted S2B). For example, if a short circuit to V_{bat} is detected during the off-phase of the PWM, the failure flag is kept set during the next on-state cycle. An update of the corresponding status register occurs in the next off-phase if the failure has been removed (*Figure 57*).

Figure 57. Example of overload failure reporting in PWM conditions



8.3 Load compatibility

In the following section, we consider the compatibility between a given HSD, the settings of the AMICO and the load to be driven. Compatibility is attained by the following conditions:

- The activation of a cold bulb may not result in the latch-off of the HSD
- For proper diagnostic, the ratio between overload and nominal current should be about 2:1 (assumption)

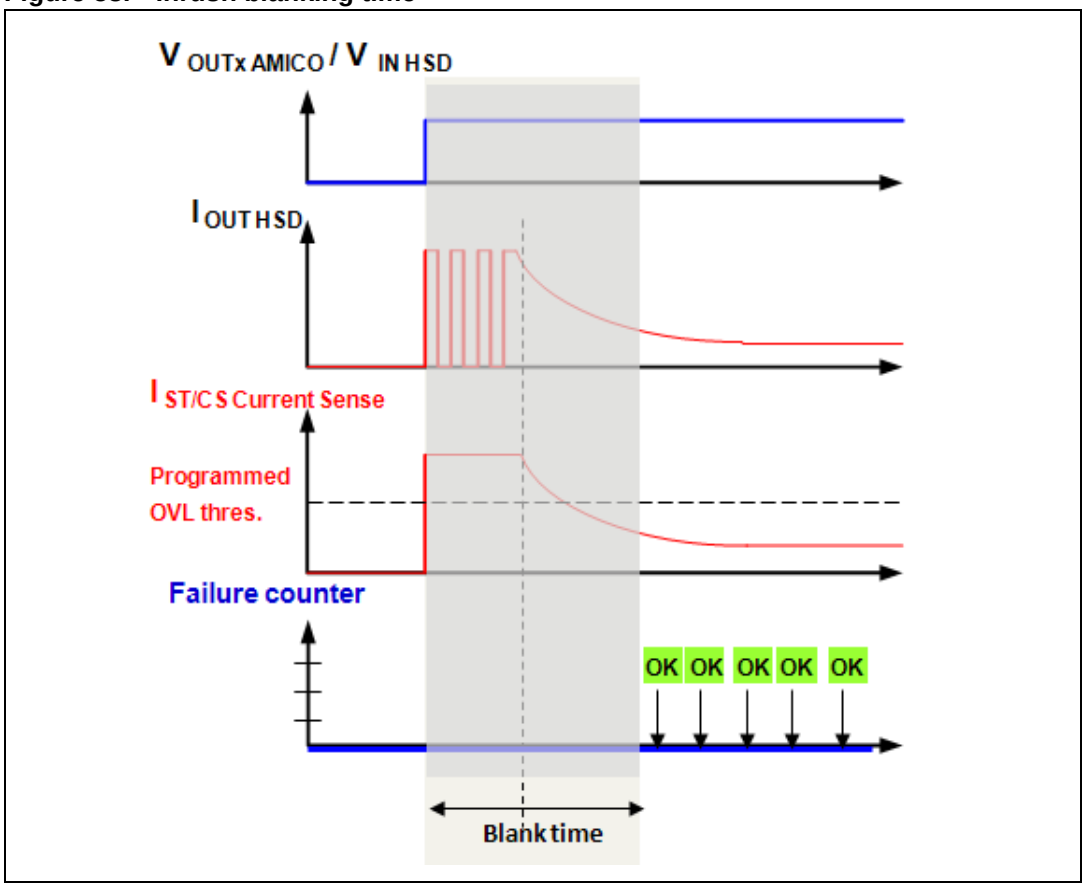
8.3.1 Inrush blanking time

The AMICO has a configurable inrush blanking time. During this time, any new failure related to overload conditions or power limitation/thermal shutdown is ignored. The latter fault condition does not lead to a latch off of the HSD by the AMICO, even though its Automatic Shutdown function is activated (see *Figure 58*).

This feature avoids an incorrect overload detection, e.g. during the inrush phase of a cold bulb.The duration of the blanking time can be selected in four steps: 0 ms, 15 ms, 70 ms, 200 ms. The blanking time starts when a channel is activated for the first time via SPI (i.e. write command to set the ON/OFF bit). The selection of the right inrush blanking time depends on the combination of the type of lamp or motor/HSD/battery voltage and load temperature at the time of activation.

The inrush blanking time of any of the 8 HSD channels can be configured independently of the others.

Figure 58. Inrush blanking time



For enhanced robustness of the HSDs in short circuit conditions, set:

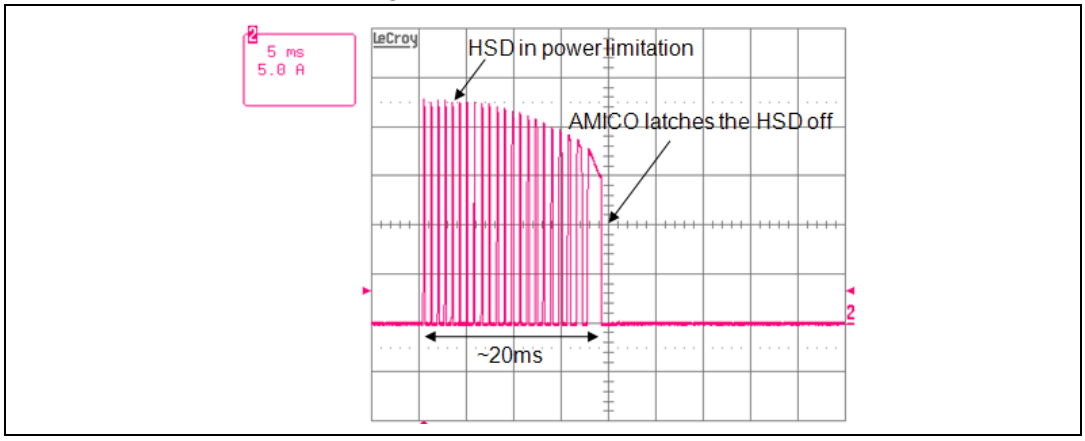
- The AMICO channel as Automatic Shut Down with a blanking time (see datasheet for the settings of the control registers)
- The HSD in Autorestart mode (The STBY_FR pin of the HSD is set to Low)

In this case the system behaves as follows:

- During the blanking time, the system AMICO + HSD are in autorestart mode. This avoids that the AMICO latches off because of the inrush current caused by a cold bulb
- Once the blanking time has elapsed, the AMICO latches off the faulty channel if the HSD still operates in thermal cycling or in power limitation (see *Figure 59*).

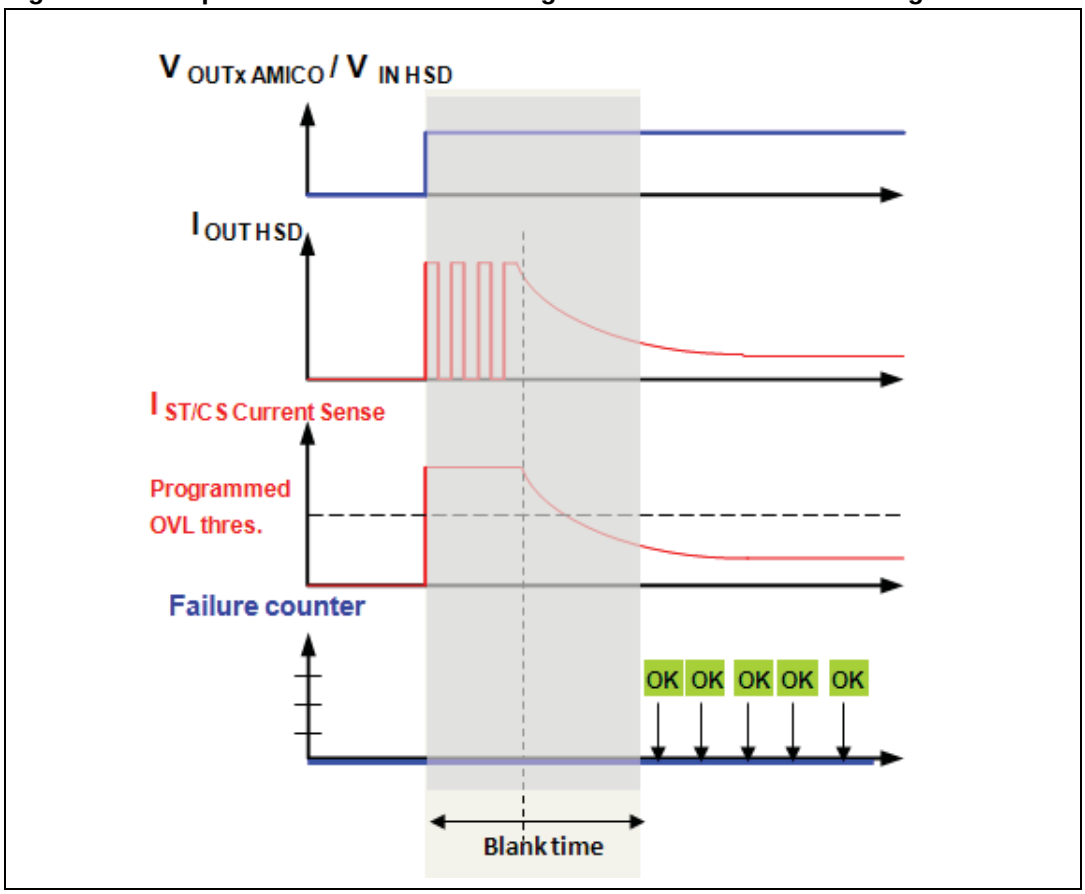
The following example shows the output current of the HSD if a blanking time of 20ms is selected. The output of the HSD has been connected to a heavy overload (VND5T100AJ driving 2x55W bulbs).

Figure 59. HSD output current if the duration of the power limitation is longer than the inrush blanking time



The following example (*Figure 60*) shows a latch off by the AMICO if the blanking time is disabled. Note that although no blanking time is set, the AMICO nevertheless delays the diagnostic by 400µs–500µs in order to take into account the current sense delay of the HSD and to filter out transients.

Figure 60. Output current of a HSD driving a cold bulb without blanking time



8.3.2 Overload and open load detection

As mentioned previously, the AMICO performs the diagnostic of the HSDs by processing the I_{SENSE} currents .This paragraph deals with load compatibility of the HSD/AMICO in terms of overload thresholds and provides some example settings of the AMICO's control register.

The following table displays the typical current of some loads and the typical K-factors of some M0-5T devices.

Table 9. Typical load currents and HSDs' K-factors

Lamp type	DC current@Vbat=24 V [A]
5W LAMP Wega BA15s	0.24
10W LAMP Jahn	0.41
21W LAMP Wega BA15s	0.88
70W LAMP Wega (H4) P43T	2.42
75W LAMP Wega (H4) P43T	2.53
70W LAMP Wega (H3) PK22s	2.39
11W LAMP 168LF TK4	0.46

Table 9. Typical load currents and HSDs' K-factors

Lamp type	DC current@Vbat=24 V [A]
Device	**Typical K-factor**
VN5T006ASP	10000
VN5T016ASP	5000
VND5T035AKLamp type	2870
VND5T100AJ	1500

The following tables display some recommended AMICO settings for the open load and overload thresholds of the internal diagnostic, as well as the resulting ratio between I_{MUX} and I_{SENSE}. I_{SENSE} is the current sense of the HSD and I_{MUX} is the current supplied by the AMICO on the MUX_ST/CS pin.

Several combinations of load/HSD are considered. The green-highlighted rows are recommended settings, based on the assumption that the ratio between overload and nominal current at V_{bat} = 24 V is about 2:1.

Table 10. Amico's typical on-board open load and overload thresholds

Device/Load	Inom @ 24V [A]	Typ. OVL level [A]	Typ. ratio Iovl/Inom	Typ. OPL level [A]	Typ. ratio I_{OPL}/Inom	Typ. ratio Imux/ Isense	Vmux [V] @Inom,Ktyp	CFL Bit	OLOVL [1,0]
VN5T006ASP Bulb 5x21W	4.40	12.0	2.73	0.50	0.11	0.83	0.59	0	0,0
	4.40	24.0	5.45	0.50	0.11	0.50	0.35	0	0,1
	4.40	36.0	8.18	1.00	0.23	0.33	0.23	0	1,0
	4.40	60.0	13.64	4.00	0.91	0.17	0.12	0	1,1
VN5T006ASP Bulb 6x21W	5.28	12.0	2.27	0.50	0.09	0.83	0.70	0	0,0
	5.28	24.0	4.55	0.50	0.09	0.50	0.42	0	0,1
	5.28	36.0	6.82	1.00	0.19	0.33	0.28	0	1,0
	5.28	60.0	11.36	4.00	0.76	0.17	0.14	0	1,1
VN5T006ASP Bulb 2x70W+2x21W	6.60	12.0	1.82	0.50	0.08	0.83	0.88	0	0,0
	6.60	24.0	3.64	0.50	0.08	0.50	0.53	0	0,1
	6.60	36.0	5.45	1.00	0.15	0.33	0.35	0	1,0
	6.60	60.0	9.09	4.00	0.61	0.17	0.18	0	1,1
VN5T016ASP 4x21W + 10W	3.93	6.00	1.53	0.25	0.06	0.83	1.05	0	0,0
	3.93	12.0	3.05	0.25	0.06	0.50	0.63	0	0,1
	3.93	18.0	4.58	0.50	0.13	0.33	0.42	0	1,0
	3.93	30.0	7.63	2.00	0.51	0.17	0.21	0	1,1

Table 10. Amico's typical on-board open load and overload thresholds

Device/Load	Inom @ 24V [A]	Typ. OVL level [A]	Typ. ratio Iovl/Inom	Typ. OPL level [A]	Typ. ratio I_{OPL}/Inom	Typ. ratio Imux/ Isense	Vmux [V] @Inom,Ktyp	CFL Bit	OLOVL [1,0]
VN5T016ASP 3x21W	2.64	6.00	2.27	0.25	0.09	0.83	0.70	0	0,0
	2.64	12.0	4.55	0.25	0.09	0.50	0.42	0	0,1
	2.64	18.0	6.82	0.50	0.19	0.33	0.28	0	1,0
	2.64	30.0	11.36	2.00	0.76	0.17	0.14	0	1,1
VN5T016ASP 5x21W	4.40	6.0	1.36	0.25	0.06	0.83	1.17	0	0,0
	4.40	12.0	2.73	0.25	0.06	0.50	0.70	0	0,1
	4.40	18.0	4.09	0.50	0.11	0.33	0.47	0	1,0
	4.40	30.0	6.82	2.00	0.45	0.17	0.23	0	1,1

OVL: overload

OPL: open load

I_{NOM}: nominal HSD's output current

Imux: current from MUX ST_CS pin

Isense: current sense from HSD

CFL and OLOVL: AMICO's configuration bits

	Recommended setting for CFL and OLOVL bits, so that the ratio typical OVL threshold/nominal current @Vbat=24V≈2

Table 11. Amico's typical on-board open load and overload thresholds

Device/Load	Current @ 24V [A]	Typ. OVL level [A]	Typ. ratio Iovl/Inom	Typ. OPL level[A]	Typ. Ratio Iopl/Inom	Typ. ratio Imux/Isense	Vmux [V] @Inom,Ktyp	CFL Bit	OLOVL [1,0]
VND5T035AK 2x21W	1.76	3.4	1.96	0.144	0.08	0.83	0.82	0	0,0
	1.76	6.8	3.91	0.144	0.08	0.50	0.49	0	0,1
	1.76	10.3	5.87	0.287	0.16	0.33	0.33	0	1,0
	1.76	17.2	9.78	1.148	0.65	0.17	0.16	0	1,1
VND5T035AK 3x21W	2.64	3.4	1.30	0.144	0.05	0.83	1.23	0	0,0
	2.64	6.8	2.61	0.144	0.05	0.50	0.74	0	0,1
	2.64	10.3	3.91	0.287	0.11	0.33	0.49	0	1,0
	2.64	17.2	6.52	1.148	0.43	0.17	0.25	0	1,1

Table 11. Amico's typical on-board open load and overload thresholds

Device/Load	Current @ 24V [A]	Typ. OVL level [A]	Typ. ratio Iovl/Inom	Typ. OPL level[A]	Typ. Ratio Iopl/Inom	Typ. ratio Imux/Isense	Vmux [V] @Inom,Ktyp	CFL Bit	OLOVL [1,0]
VND5T100AJ 21W+10W	1.29	1.8	1.40	0.075	0.06	0.83	1.15	0	0,0
	1.29	3.6	2.79	0.075	0.06	0.50	0.69	0	0,1
	1.29	5.4	4.19	0.150	0.12	0.33	0.46	0	1,0
	1.29	9.0	6.98	0.600	0.47	0.17	0.23	0	1,1
VND5T100AJ 10W	0.41	0.18	0.44	0.008	0.02	8.33	3.64	1	0,0
	0.41	0.36	0.88	0.008	0.02	5.00	2.19	1	0,1
	0.41	0.54	1.32	0.015	0.04	3.33	1.46	1	1,0
	0.41	0.90	2.20	0.060	0.15	1.67	0.73	1	1,1

OVL: overload

OPL: open load

Inom: nominal HSD's output current

Imux: current from MUX ST_CS pin

Isense: current sense from HSD

CFL and OLOVL: AMICO's configuration bits

	Recommended setting for CFL and OLOVL bits, so that the ratio typical OVL threshold/nominal current @Vbat=24V≈2

8.4 Combining inrush blanking time and diagnostic of open load in off-state

As described in the previous section, the turning on of a cold incandescent bulb results in an inrush current due to the low resistance of the bulb's filament. This inrush current might activate the HSD's power limitation. However, this may not be considered as a fault condition and may not trigger a latch off of the HSD.

The following chapter describes a proposal which allows both the blanking of the inrush current and open load or short circuit to V_{bat} diagnostic in off-state (noted OLOFF and S2B).

8.4.1 Description of the principle

As explained in the section Inrush blanking time set:

- The AMICO channel in Automatic Shut Down mode with a blanking time
- The HSD in Autorestart mode (The FR_Stby pin of the HSD is set to Low)

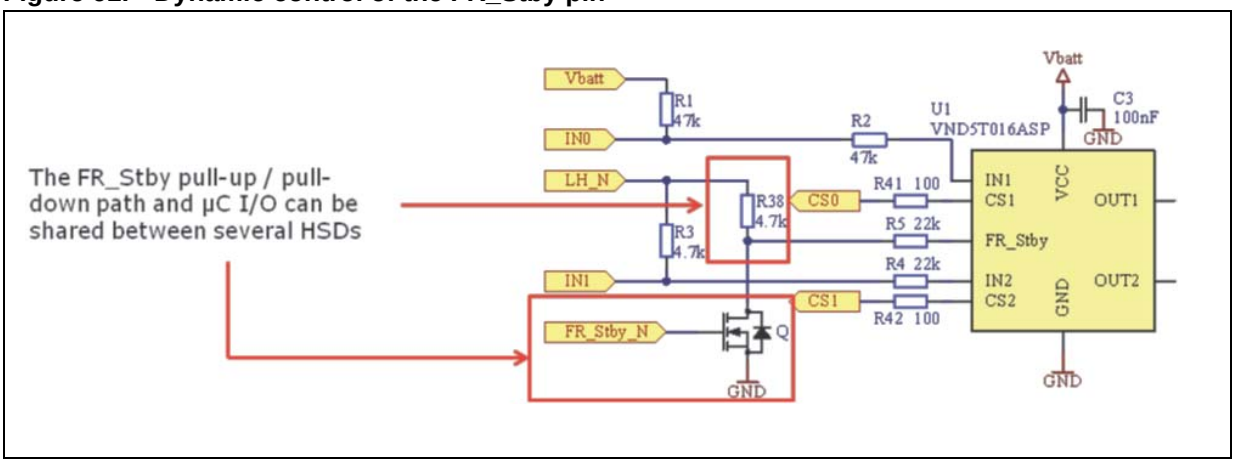
However, the second point is not compatible with the diagnostic of an open load in off-state or a short circuit of the HSD's output to V_{bat} (refer to*Table 1*). Indeed, the diagnostic in off-state is possible only if FR_Stby is High.

Therefore, the µC has to dynamically control the FR_stby pin in order to enable (see proposed circuitry *Figure 61*):

- Either FR_Stby = Low (default) and the HSD is in auto-restart during the inrush blanking time
- Or FR_Stby = High (on demand) and the OLOFF/S2B detection is enabled

Note that the diagnostic in off-state can be performed for several HSD channels at the same time, when FR_Stby pin(s) of the HSD(s) is (are) High.

Figure 61. Dynamic control of the FR_Stby pin



Two cases are considered:

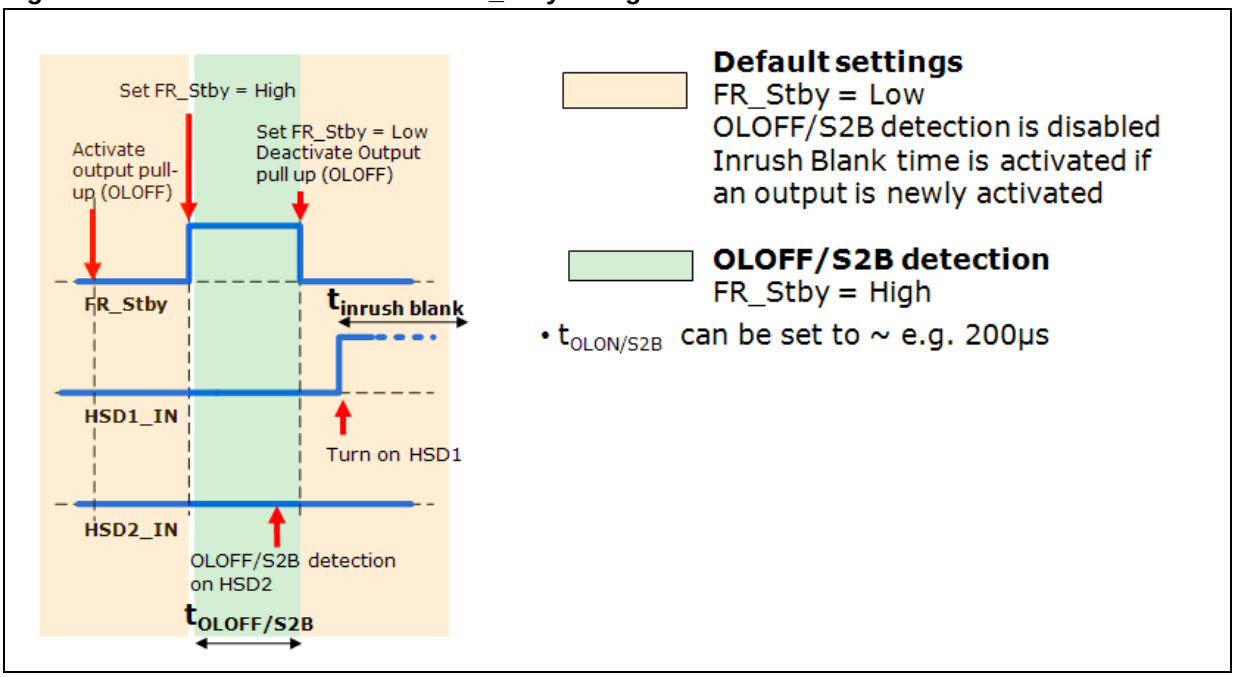
- Case 1: there is no new activation of any HSD when the FR_Stby of the HSDs is set to High
- Case 2: an inrush current on a HSD occurs while the FR_Stby pin of the HSDs is High

Case 1: no new activation of any HSD during the off-state diagnostic

Let's consider the case where no new activation (i.e. no SPI write command to address Ox01 of AMICO's control register) of any HSD occurs while the FR_Stby pin is set to High (*Figure 62*).

– No inrush current occurs and the diagnostic in off-state has no side effect on any channel.

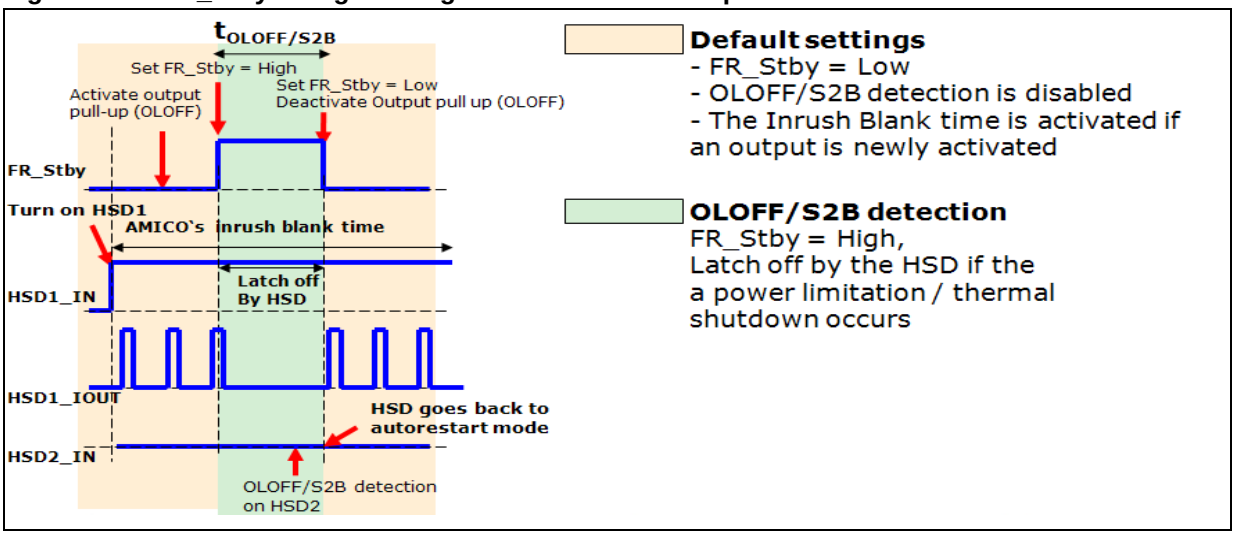
Figure 62. No new activation while Fr_Stby is High



Case 2: inrush current of a HSD during the off-state diagnostic

Let's consider now the case where a new activation of one or several HSDs occurs while the FR_Stby pin is set to High. In this case the channels which operate in power limitation are latched off by the HSD itself (*Figure 63*).

Figure 63. FR_Stby is High during the activation of the power limitation



Even if the HSD Ch1 is latched off by the HSD during $t_{OLON/S2B}$ while the inrush blanking time is activated, the auto-restart function of the HSD is reactivated as soon as FR_Stby is set back to Low.

Setting FR_Stby to High for $t_{OLOFF/S2B}$ = 200 µs is sufficient to ensure a reliable diagostic. Actually, around 100µs are required until the diagnostic in off-state is completed (*Figure 64*). 200 µs are recommended for margin.

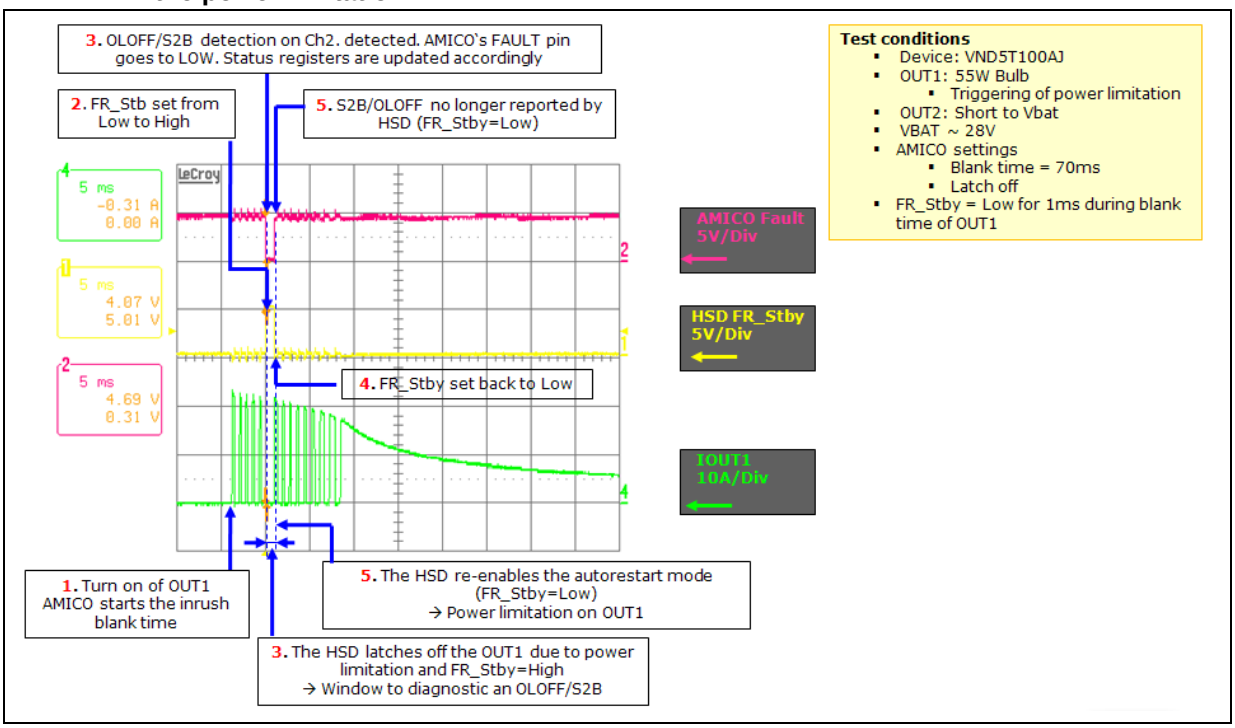
An interruption of the turning on of a cold bulb of 200 µs has a negligible effect for two reasons:

- The bulb's filament has a large thermal inertia. An interruption of the inrush current for 200 µs does not cause any substantial decrease of the filament's temperature and therefore does not further delay its turn on.
- The delay between the activation of a cold incandescent bulb and the moment when the bulb provides its nominal brightness is in the range of several tens of milliseconds to several hundred of milliseconds. Therefore a maximum interruption of the power limitation of 200 µs has a negligible impact on the turn on of a cold bulb.

The following figure (*Figure 64*) shows an oscillogram when an off-state diagnostic is performed on Ch2 while an inrush current on Ch1 occurs. The FR_Stby signal is set High for 200 µs. The inrush current leads to the activation of the power limitation and therefore Ch1 is latched off by the HSD.

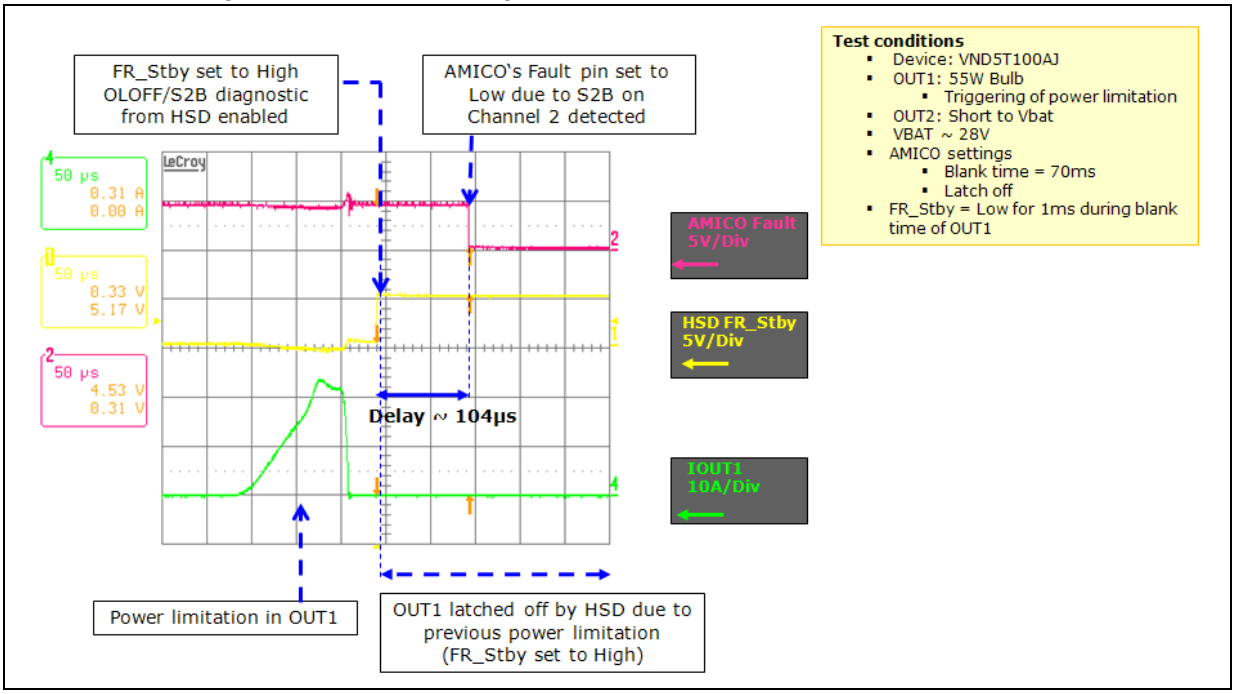
As soon as the FR_Stby is set back to Low, the Ch1 is in Autorestart mode. Since the AMICO's blanking time is still valid, Ch1 operates in power limitation without latch off until the blanking time has elapsed.

Figure 64. Plot of output current and AMICO's fault pin. FR_Stby is high during the activation of the power limitation



The following figure provides a zoom on the Fault pin.

Figure 65. Plot of output current and AMICO's fault pin (zoom of *Figure 64*). FR_Stby is High during the activation of the power limitation



Set FR_STBY pin to High for 200 µs and perform the OLOFF/S2B diagnostic at the end of these 200 µs. After the diagnostic, the FR_STBY pin should be set back to Low.

Summary

Case 1 and case 2 have no substantial effect on the activation of a cold bulb, even if this activation occurs while FR_Stby is High. This is true as long as the FR_Stby is kept High for a short time. 200 µs are compatible for a reliable diagnostic in off-state and does not substantially increase the turn on delay of a cold bulb.

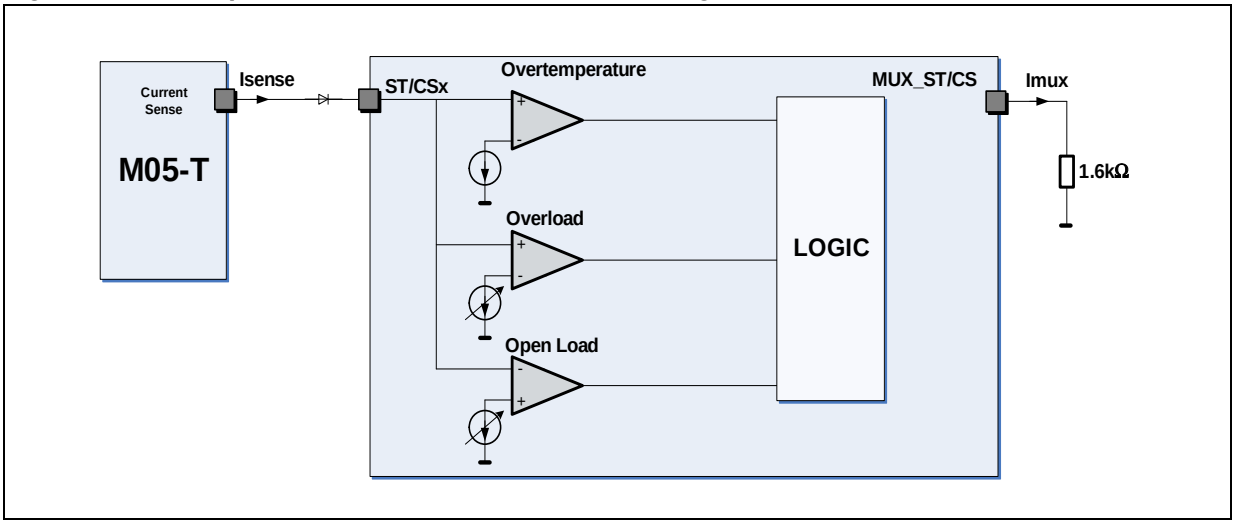
8.5 Direct current sense reading

On top of its internal diagnostic, the AMICO also enables the µC to monitor an image of I_{SENSE} via its MUX_ST/CS pin, referred to as “direct current sense reading”.

This pin provides the sense current of the M0-5T channel multiplied by a certain gain or divider. The ratio between I_{MUX} and I_{SENSE} (see *Figure 66*) can be set between 0.166 and 8.33 (refer to*Table 12* and the datasheet for more details). A resistor between MUX_ST/CS and GND translates I_{MUX} into a voltage, which can be monitored by a µC’s ADC channel.

This output is multiplexed, so that the microcontroller can select one of the eight HSD channels.

Figure 66. Principle of the direct current sense reading



The gain/divider between I_{MUX} and I_{SENSE} is selected by the control registers. There are individual gains and dividers for each device. See the table below.

Table 12. Settings of the ratio Imux/Isense

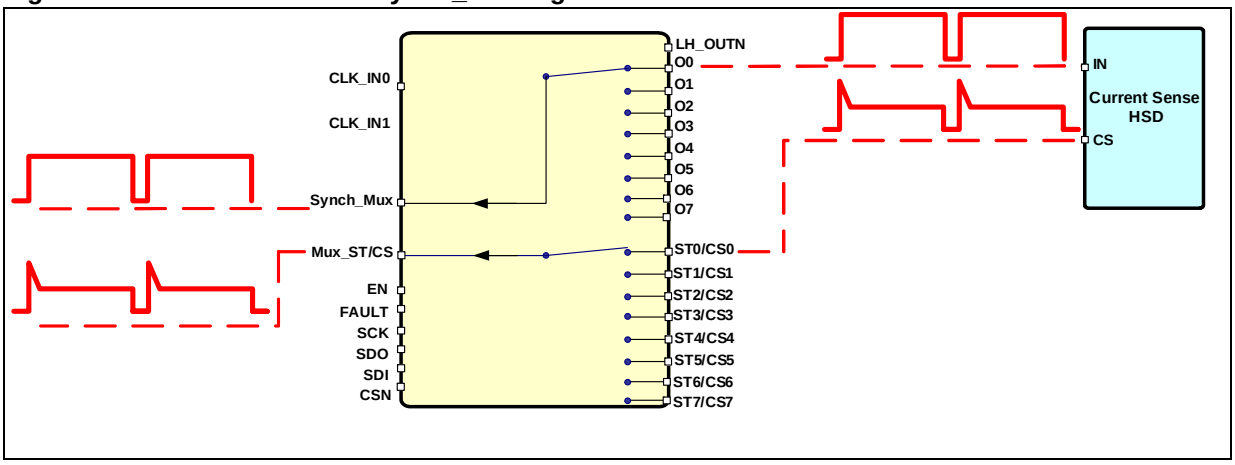
CFL	OLOVL1	OLOVL0	Imux/Isense ratio
0	0	0	0.83
0	0	1	0.50
0	1	0	0.33
0	1	1	0.16

Table 12. Settings of the ratio Imux/Isense (continued)

CFL	OLOVL1	OLOVL0	Imux/Isense ratio
1	0	0	8.33
1	0	1	4.99
1	1	0	3.33
1	1	1	1.67

The AMICO generates the PWM signal internally. Nevertheless, the µC can perform a synchronous reading of the MUX_ST/CS pin with the on-phase or off-phase of the PWM signal, as the input signal of the selected HSD channel is replicated on the Synch_Mux pin (*Figure 67*).

Figure 67. Behaviour of the Synch_Mux signal



8.6 Impact on the accuracy of the current sense reading

The tolerance of the ratio I_{MUX}/I_{SENSE} increases the overall tolerance of the current sense reading, when the µC monitors the MUX_ST/CS signal. This also affects the tolerance of the overload and open load thresholds. We can see in the following section that the additional tolerance from the AMICO is quite small when we apply a statistical approach to the tolerance calculation.

The main tolerances are due to the tolerance of the K-factor of the HSD and the tolerance of the ratio I_{MUX}/I_{SENSE} of the AMICO. The tolerance of the current sense resistor can be neglected as resistance with a tolerance of 1 % or even lower can be used.

The expression for I_{MUX} is:

$$\text{Imux} = \frac{Iout}{Kmux} = \frac{G}{K} * Iout$$

With:

G: the mux gain

K: HSD's current sense ratio

K_{MUX}: K-factor resulting from the combination AMICO/HSD

Naturally, G and K have a statistical spread and it can be represented as:

$$k = k_{mean} \pm \delta_k = k_{mean} \pm x\% * k_{mean}$$
$$G = G_{typ} \pm \delta_g = G_{mean} \pm y\% * G_{mean}$$

The uncertainty of K_{MUX} is then a function of the uncertainty of K and the uncertainty of G, and it can be represented as:

$$k_{mux} = \frac{k_{mean}}{G_{mean}} \pm \delta_{Ikg}$$

Both parameters are statistically independent. If we consider that they follow a gaussian distribution, the tolerance of K_{MUX} is:

$$\delta_{Ikg} = \sqrt{\delta_{Ig}^{\ 2} + \delta_{Ik}^{\ 2}} = \frac{k_{mean}}{G_{mean}} * \sqrt{(x\%^2 + y\%^2)}$$

Where x % is the tolerance of the K-factor of the HSD and y % is the tolerance of the ratio between I_{MUX} and I_{SENSE}.

Example:

Let's calculate the tolerance of Kmux under the following conditions:

One channel of the VND5T100AJ drives an output current of 0.8A

The AMICOs ratio Imux/Isense is set to ~3.33 ($K_{1\ 10,}$ *Table 14*)

The tolerance of the HSD's K-factor is +/-20 % at the considered load current (K2 parameter, *Table 13*).

Table 13. Specification of the current sense ratio of the VND5T100AJ

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 350 mA; V_{SENSE} = 1 V; T_j = -40 °C to 150 °C T_j = 25 °C to 150 °C	930 1050	1547 1547	2185 2020	
dK_1/K_1(1)	Current sense ratio drift	I_{OUT} = 350 A; V_{SENSE} = 1 V; T_j = -40 °C. to 150 °C	-15		15	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 0.8 A; V_{SENSE} = 2 V; T_j = -40 °C. to 150 °C T_j = 25 °C to 150 °C	1225 1310	1528 1528	1835 1745	
dK_2/K_2(1)	Current sense ratio drift	I_{OUT} = 0.8 A; V_{SENSE} = 2 V; T_j = -40 °C. to 150 °C	-12		12	%

1. Parameter guaranteed by design; it is not tested.

Isense, which comes from the HSD is typically 0.8/1528 = 524 µA. Considering this current, the tolerance of the AMICO current sense ratio is +/- 7 % (see *Table 14*).

Table 14. Specification of AMICO's Imux/Isense ratio

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
k_{1_10}	current MUX_ST/CS ratio@I_{CS} = 510 µA	CFL = 1, OLOVL[1,0]=1,0	3.10	3.33	3.50	-
	current MUX_ST/CS ratio@I_{CS} = 70 %* 510 µA		3.10	3.33	3.50	-
	current MUX_ST/CS ratio@I_{CS} = 35 %* 510 µA		3.10	3.33	3.50	-
	current MUX_ST/CS ratio@I_{CS} = 5 %* 510 µA		3.10	3.33	3.50	-
	current MUX_ST/CS ratio@I_{CS} = 5 µA		2.80	3.33	3.70	-

The tolerance of K_{MUX} is

$$\sqrt{(20\%^2 + 7\%^2)} = 21.2\%$$

compared to 20 % without AMICO.

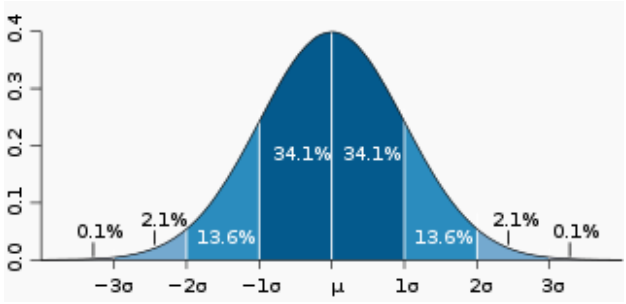
Therefore, the additional tolerance caused by the AMICO to the current sense reading is actually small if we consider a statistical approach.

Without statistical considerations, one would arrive at 27 % by simply adding the tolerances of both components. However, this calculation is very pessimistic as demonstrated below.

In general, the min/max tolerance is specified at least with:

- Mean value + 6 Sigma (max)
- Mean value - 6 Sigma (min)

Figure 68. Probability density function of a gaussian distribution



µ is the mean value of the distribution

Sigma is the standard deviation, also noted σ

The probability to have a parameter outside the limits [μ – 6σ , μ + 6σ] is 0.002 ppm or 2.10^{-9}.

Simply adding the tolerances of each devices, means that the probability to observe a combination AMICO/HSD with the resulting min/max limits have a probability of (2.10^{-9}) = 4.10^{-18} of ocurring, which is not realistic.

References:

– Wolfram Mathematica:

http://reference.wolfram.com/applications/eda/ExperimentalErrorsAndErrorAnalysis.html

– http://physicslabs.cwru.edu/MECH/Manual/Appendix_V_Error%20Prop.pdf

8.7 Functional safety aspects

Functional safety aspects are essential for automotive exterior lighting applications. Some loads are considered as safety relevant functions such as low beams, blinker, tail lights or brake lights. These aspects been considered by the AMICO, so that the system fulfils the requirements of the ISO 26262 norm.

8.7.1 Limp home mode

The AMICO device enters limp home mode if one of the following events occur:

- Loss of VDD supply
- Watchdog timeout
- Invalid SPI commands interpreted as a short of CSN to GND/Supply
- Special SPI command

In this mode, the state of the high-side drivers is predefined by the choice of the pull up on the input of the HSD. This enables, for example, the turn-on of low beams or position lights and the deactivation of the high beams.

8.7.2 Timeout Watchdog

In general, malfunction of the μC is detected by a system watchdog which may or may not be integrated in a power management device.

Local failures such as SDI shorted to GND, can be detected by the timeout watchdog of the L99PD08. The AMICO's watchdog is refreshed at each rising edge of the CSN signal. The timeout can be configured to 100 ms or 200 ms.

8.7.3 Functional safety considerations through ST SPI

The standardized ST SPI protocol has been defined in order to offer a robust communication interface which supports fail-safe concepts, and to rapidly provide the microcontroller with global information about the L99PD08 and the connected high-side drivers. Failures on the SPI bus, such as a shorted SDI or SDO, can be detected.

The ST SPI standard also detects and reports if communication with a wrong number of clock pulses has been detected during a SPI communication.

8.7.4 Full flexibility of the output stages and supply rails

In order to comply with the functional safety requirements of ISO26262, the supply voltage of the HSDs is generally split into 2 to 4 supply rails. It is also possible that only one safety relevant load is controlled by one multichannel HSD. In addition to these constraints, the optimal adaptation of the Rdson to the loads and the variants within a car platform lead to a HSD partitioning with many single and dual channel devices.

Thanks to the L99PD08, the µC is able to drive and perform the diagnostic of standard HSDs using the SPI interface. This advantage comes from the fact that the L99PD08 is compatible with any HSD of the M0-5T family, regardless of the number of channels and of the supply rail the HSD is connected to.

8.8 Hardware guidelines

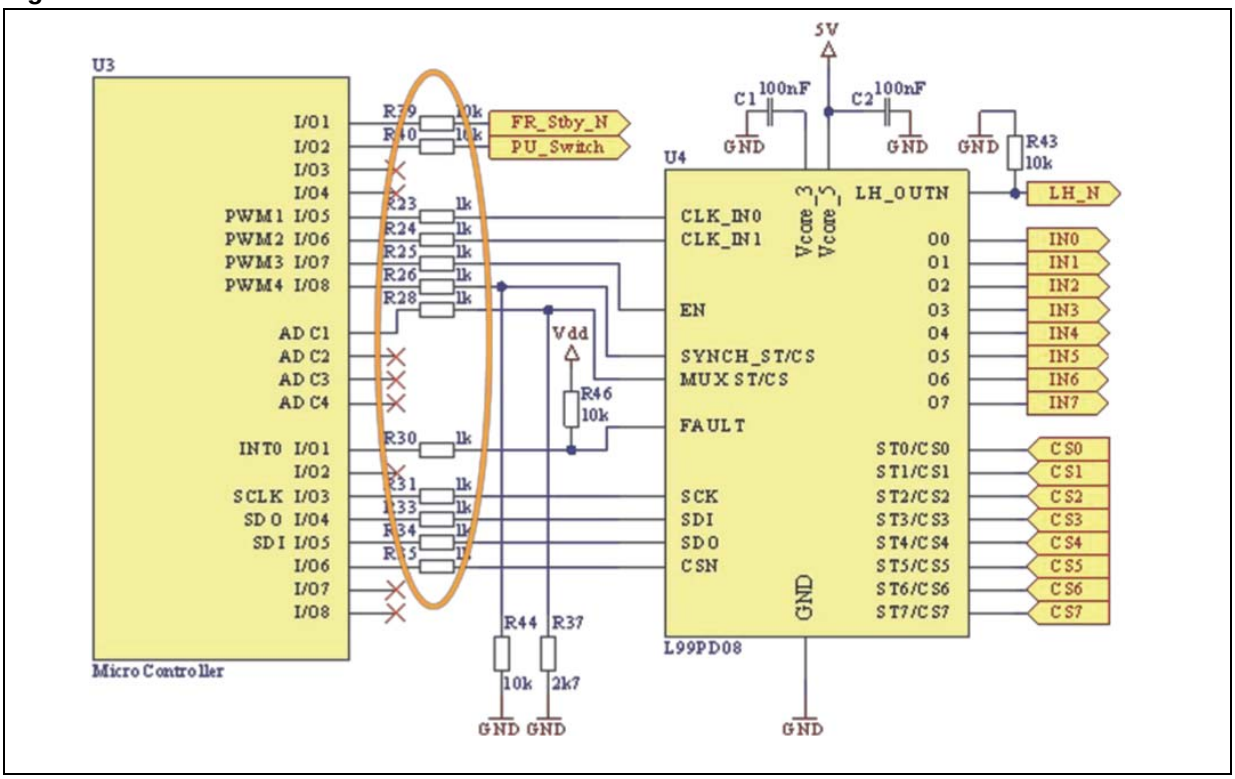
This section provides recommendations on the dimensionning of external components around the L99PD08. Requirements like reverse battery conditions and ISO pulses are considered.

8.8.1 Interface microcontroller/AMICO

For a robust design, series resistors between each µC/AMICO connection are recommended so that local failures of the AMICO, such as a shorted pin to GND or to VDD, do not cause critical effects on the further operation of the devices, which are connected to the same SPI bus.

For CLK_Inx, EN, FAULT, SYNCH_ST/CS, MUX_ST/CS: 1 kΩ to 10 kΩ is suitable. The higher the value, the better the decoupling.

Figure 69. Recommendations for series resistors between the AMICO and the microcontroller



For the same reason, series resistors on SDI, SDO, CSN, SCK are required. These resistors should be placed as close as possible to each AMICO device.

The SPI interface is considered as a high speed bus compared to the above mentioned signals. In this case, a too high value of the series resistance, in conjunction with stray capacitances (e.g. input capacitances of SDI, SCK etc.,…) can prevent the SPI bus from working properly at certain SPI clock frequencies.

The oscillograms on *Figure 70* show edge shaping of the original square wave signal which is generated by the µC. The distorted incoming signal on SCK and SDI of the AMICO device is due to the 4.7 kΩ series resistors in conjunction with stray capacitors.

The higher the serial resistance, the lower the max. SPI speed (*Table 15*)

Figure 70. Distortion of the SPI signal by a too high series resistor

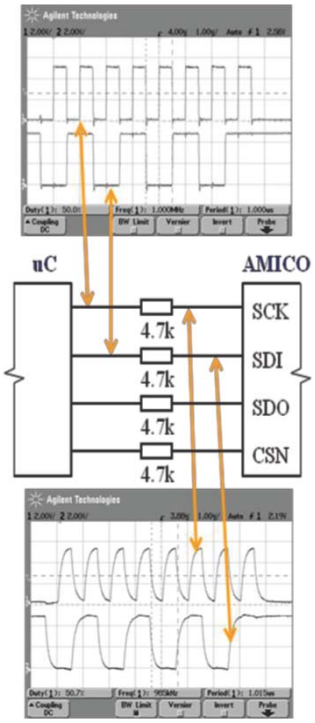


Table 15. Recommended max. SPI clock frequency as a function of the series resistance

Resistor value	Max. recommended SPI clock frequency
1 k	1 MHz
2.2 k	1 MHz
4.7 k	500 kHz
10 k	250 kHz

A 1 kΩ series resistor on these pins is generally a good compromise between the data rate and decoupling between µC/AMICO.

8.8.2 Interface HSD/AMICO

This section deals with external components between the HSD and AMICO, in order to protect the devices against ISO transients and reverse battery conditions. A differentiation between monolithic (VND5T035Ax, VND5T050Ax, VND5T100Ax) and hybrid devices is done (VN5T006ASP, VND5T016ASP, VN5T016AH).

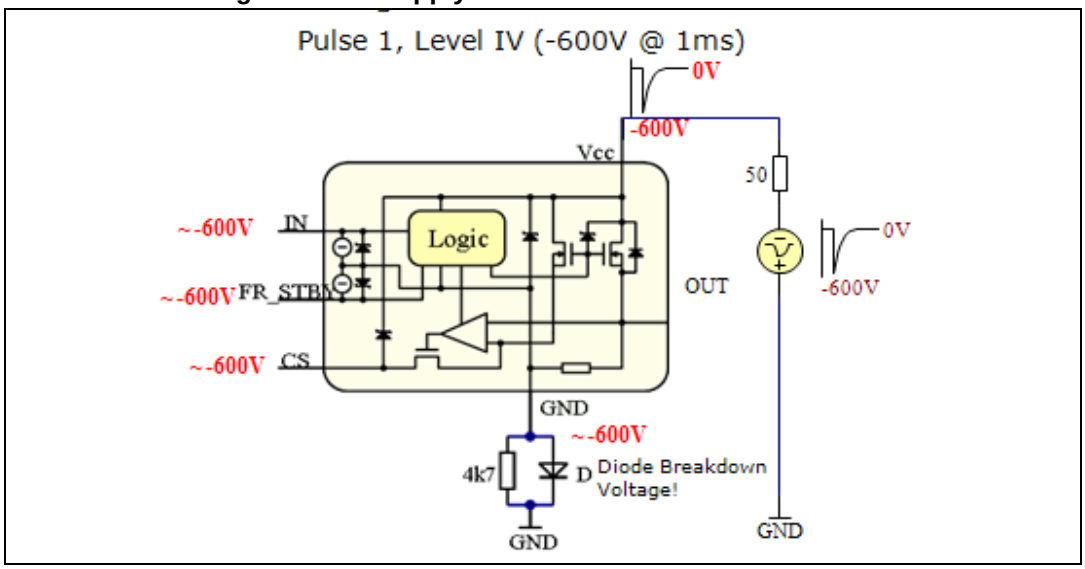
ISO pulses on monolithic devices

Negative ISO pulses are directly transferred to the HSD's input pin (noted IN) and the FR_Stby and CS pins of monolithic devices. The worst case is when no load is connected to

any of the HSD outputs, which share the same supply line (*Figure 71*). Therefore, a 22 kΩ to 47kOhm series resistor on IN and FR_Stby are required.

The STx/CSx pin cannot be decoupled from the CS pin with such a high resistor value, because of the too high voltage drop, which is caused by the Isense in normal conditions. Therefore, a decoupling diode with a minimum breakdown voltage of 600 V is required.

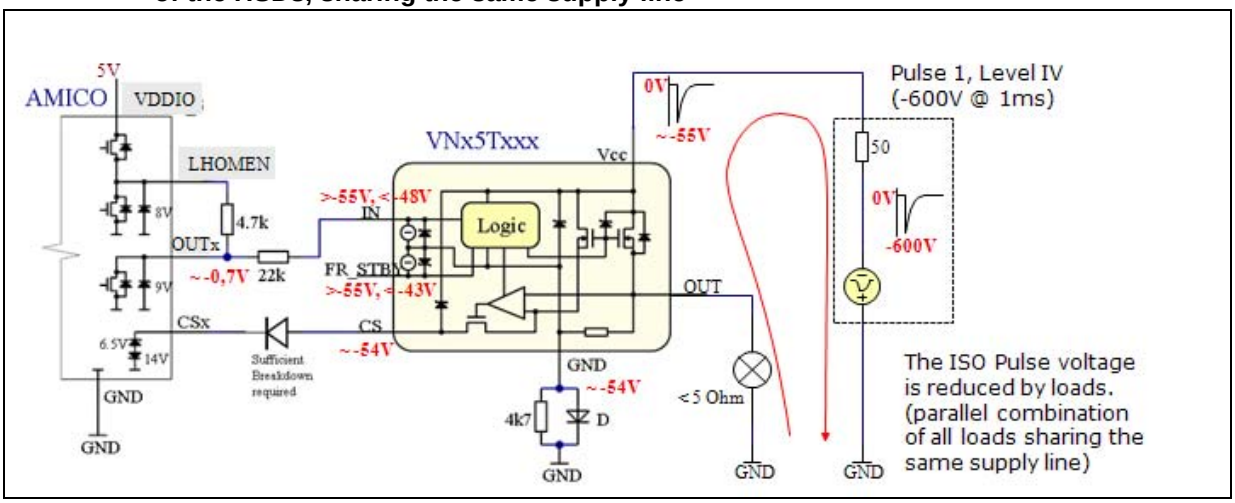
Figure 71. Effect of an ISO pulse 1 on Vcc, if no load is connected to any HSD sharing the same supply line



If at least one load is connected to one of the output of a HSD, then, the negative voltage on the CS/FR_Stby and INx pins are much less severe (see *Figure 72*). This would enable to use a diode between CS and STx/CSx, with a lower breakdown voltage.

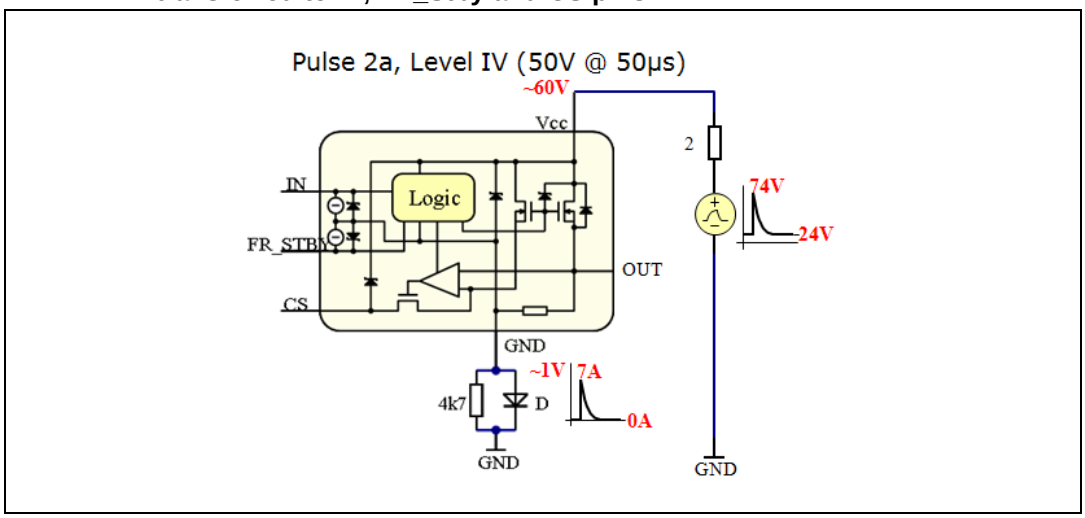
In this example one load with 5 Ω is connected, the negative voltage at the IN, FR_Stby and CS pins are only ~ - 55 V, compared to the -600 V if no load is connected.

Figure 72. Effect of an ISO pulse 1 on Vcc with at least one connected load to one of the outputs of the HSDs, sharing the same supply line



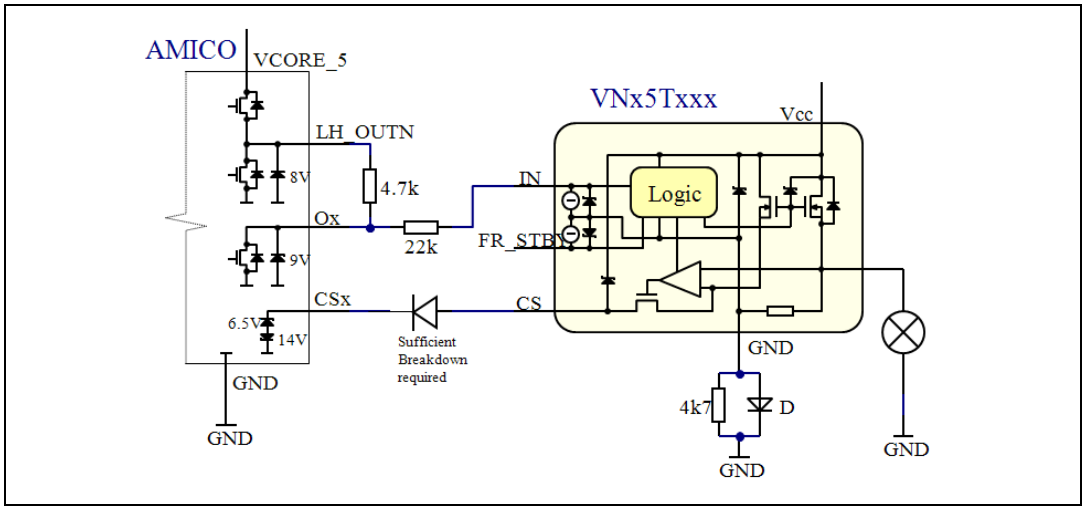
Positive ISO pulses on the supply of a monolithic device are not transferred to IN, FR_Stby and CS pins (*Figure 73*).

Figure 73. Positive ISO pulses on the supply of monolithic devices are not transferred to IN, FR_Stby and CS pins



The *Figure 74* sums up the recommendations at the interface between the AMICO and the monolithic HSDs.

Figure 74. Recommended external components between a monolithic HSD and the AMICO

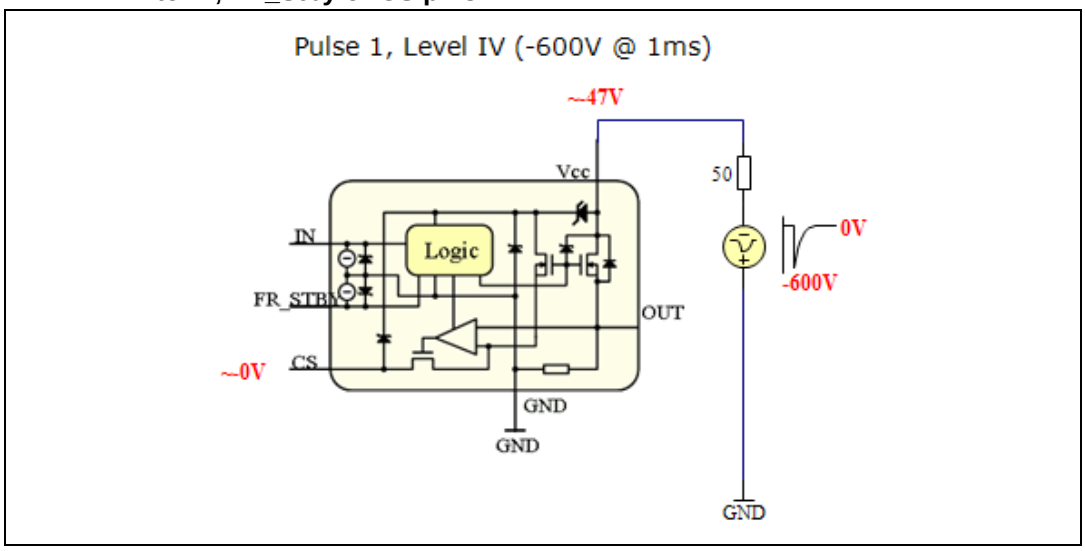


ISO pulses on hybrid devices

Negative ISO pulses 1 are not transferred directly to the IN pins and FR_Stby but through parasitic structures. 22 kΩ series resistors on these pins are nevertheless recommended, to protect the AMICO in reverse battery conditions (see Reverse battery protection).

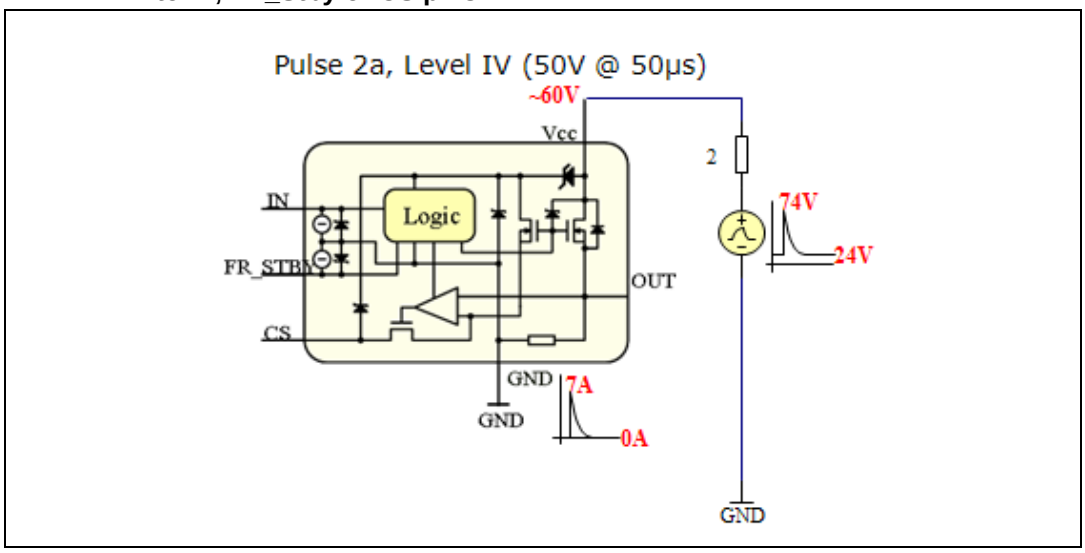
The CS pin is ~ GND during the ISO pulse 1. A 100 Ω series resistor to the STx/CSx pin is nevertheless recommended for a robust design. Indeed, this diode decouples the CS pin of the HSD and the AMICO's STx/CSx pin. On the other hand the drop voltage across this resistor in normal conditions is compatible with the AMICO's diagnostic.

Figure 75. Negative ISO pulses on the supply of the hybrid HSD are not transferred to IN, FR_Stby or CS pins



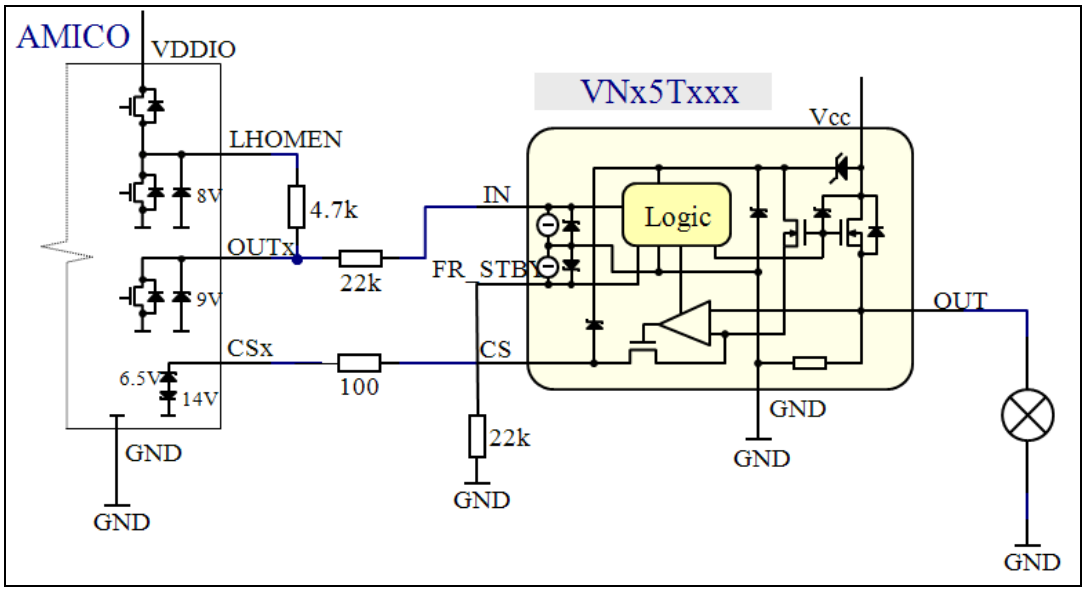
Positive ISO pulses 2a are clamped by the hybrid device and are not transferred to the IN/FR_Stby or CS pins.

Figure 76. Positive ISO pulses on the supply of the hybrid HSD are not transferred to IN, FR_Stby or CS pins



The following figure sumarizes the recommendations at the interface between the AMICO and the hybrid HSDs.

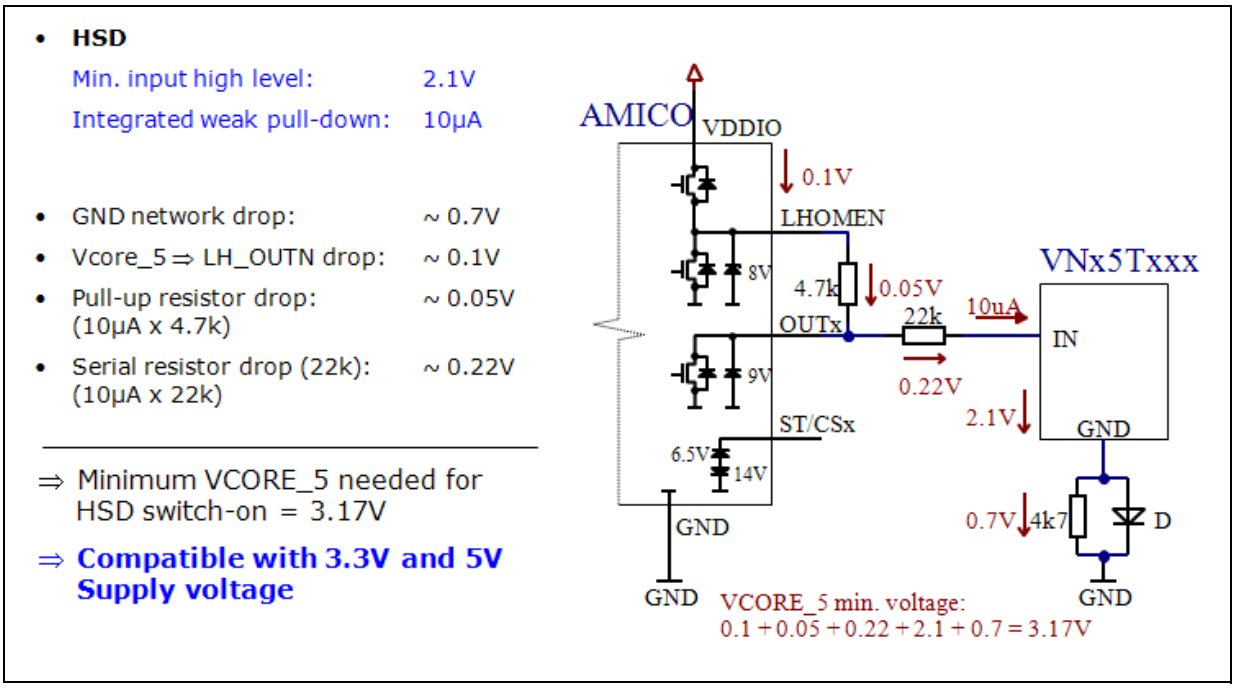
Figure 77. Recommended external components between a hybrid HSD and an AMICO



Input level verification

At this stage we shall verify the min. required supply voltage of the AMICO, which ensures correct control of the HSDs. We consider that the min. High level for the HSD is 2.1 V and the max. input current consumption is 10 µA at 2.1 V. The calculation below (*Figure 78*) shows that the monolithic HSD is correctly turned on if the supply voltage of the AMICO is above 3.17 V. This min. value is ~ 2.47 V for a hybrid HSD, since the HSD's GND pin is directly connected to the system GND.

Figure 78. Verification of the correct activation of a monolithic HSD, despite the voltage drop across the series resistor



8.8.3 Reverse battery protection

The following chapter deals with the reverse battery protection. We consider that the reverse battery voltage of -28 V can be applied between the positive supply and the module GND.

Here again, we distinguish between monolithic HSDs (VND5T035Ax, VND5T050Ax, VND5T100Ax) and hybrid HSDs (VN5T006ASP, VND5T016ASP, VN5T016AH).

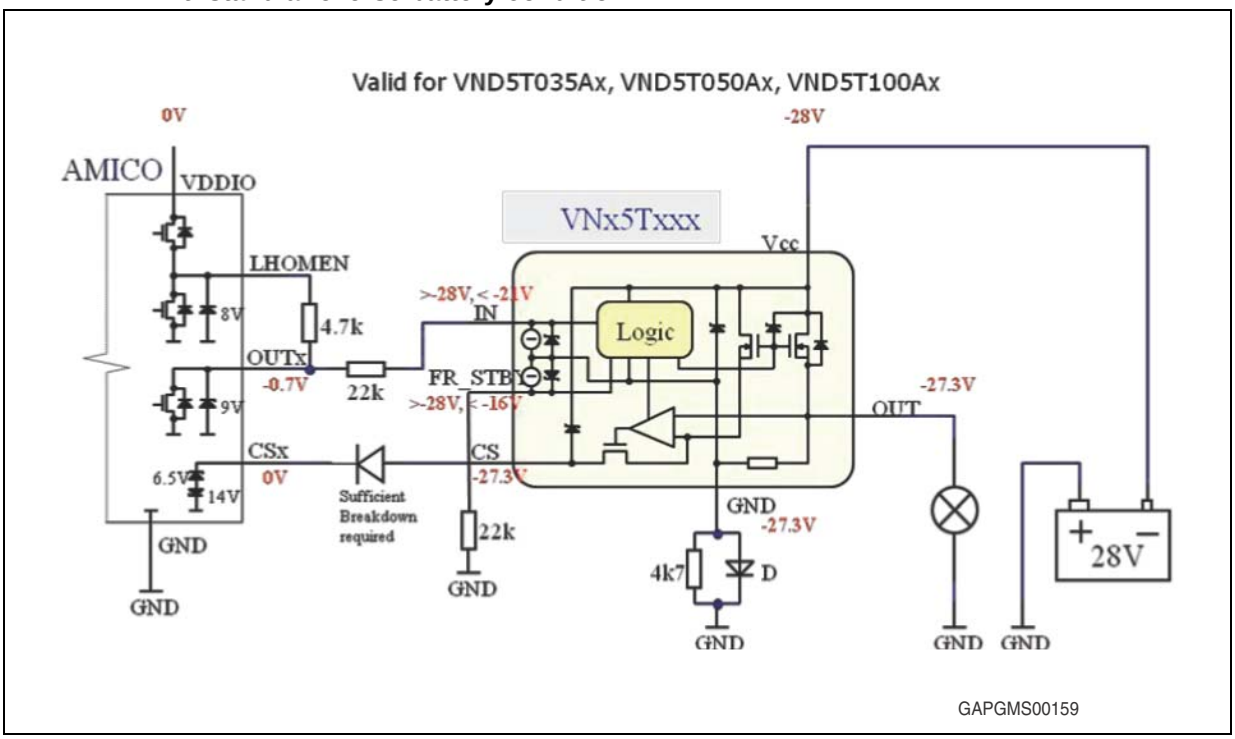
Reverse battery protection with monolithic devices

Monolithic devices such as VND5T035Ax, VND5T050Ax or VND5T100Ax have a voltage at their IN, CS and FR_STBY pins which is almost equal to the reverse battery voltage.

INx pins: a series resistor of ~ 22 kΩ between the HSD's INx pin and the AMICO's OUTx pin, limits the current flow from the AMICO's GND to the AMICO's OUTx pin via the body diode or the output clamping structure to approximatively 1 mA. This current does not cause any damage to the AMICO.

CS Pins: a series resistor of 22 kΩ on this pin cannot be used. It would result in too high a voltage drop between the CS pin of the HSD and the STx/CSx pin of the AMICO. Therefore, a protection diode with a reverse capability of at least 28 V is required for the reverse battery protection. However, a breakdown voltage of min. 600 V might be required if the module must withstand negative ISO pulses with all loads disconnected (refer to paragraph *ISO pulses on monolithic devices*).

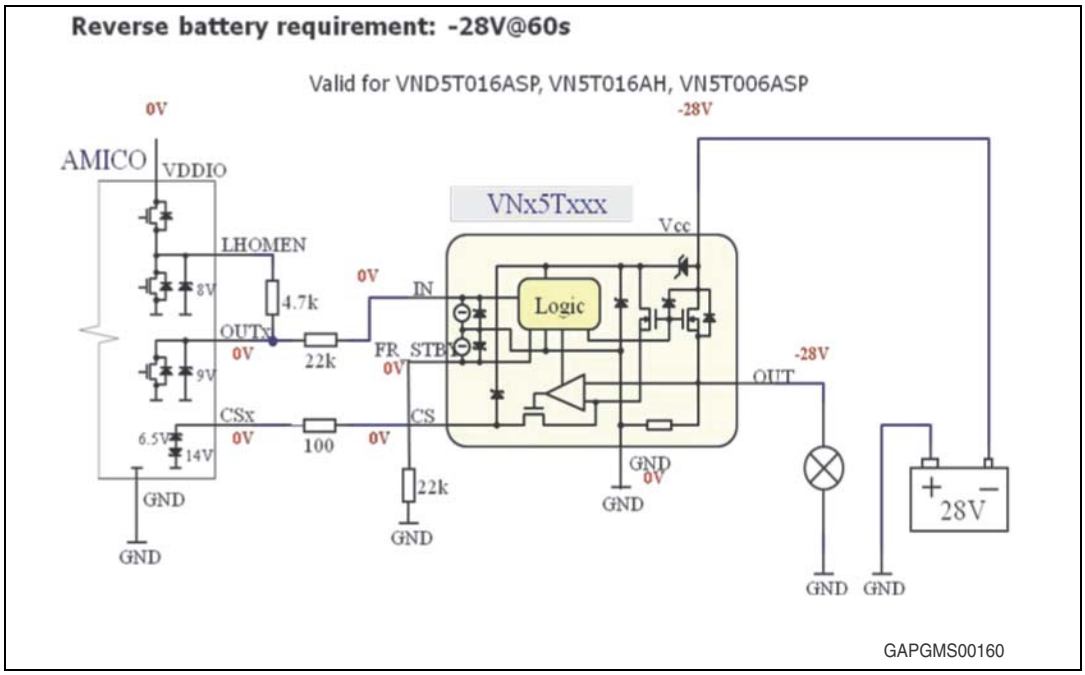
Figure 79. Recommended external components between a monolithic HSD and the AMICO to withstand a reverse battery condition



Reverse battery protection with hybrid devices

Hybrid HSDs such as VND5T016ASP, VN5T016AH or VN5T006ASP have a different behaviour in reverse battery conditions than the monolithic devices (Note that the HSD GND pin must be connected directly to the signal GND, without a resistor or a protection diode). Indeed, the potential at FR_STBY, IN and CS pins is GND during the a reverse battery condition.

Figure 80. Recommended external components between a monolithic HSD and the AMICO



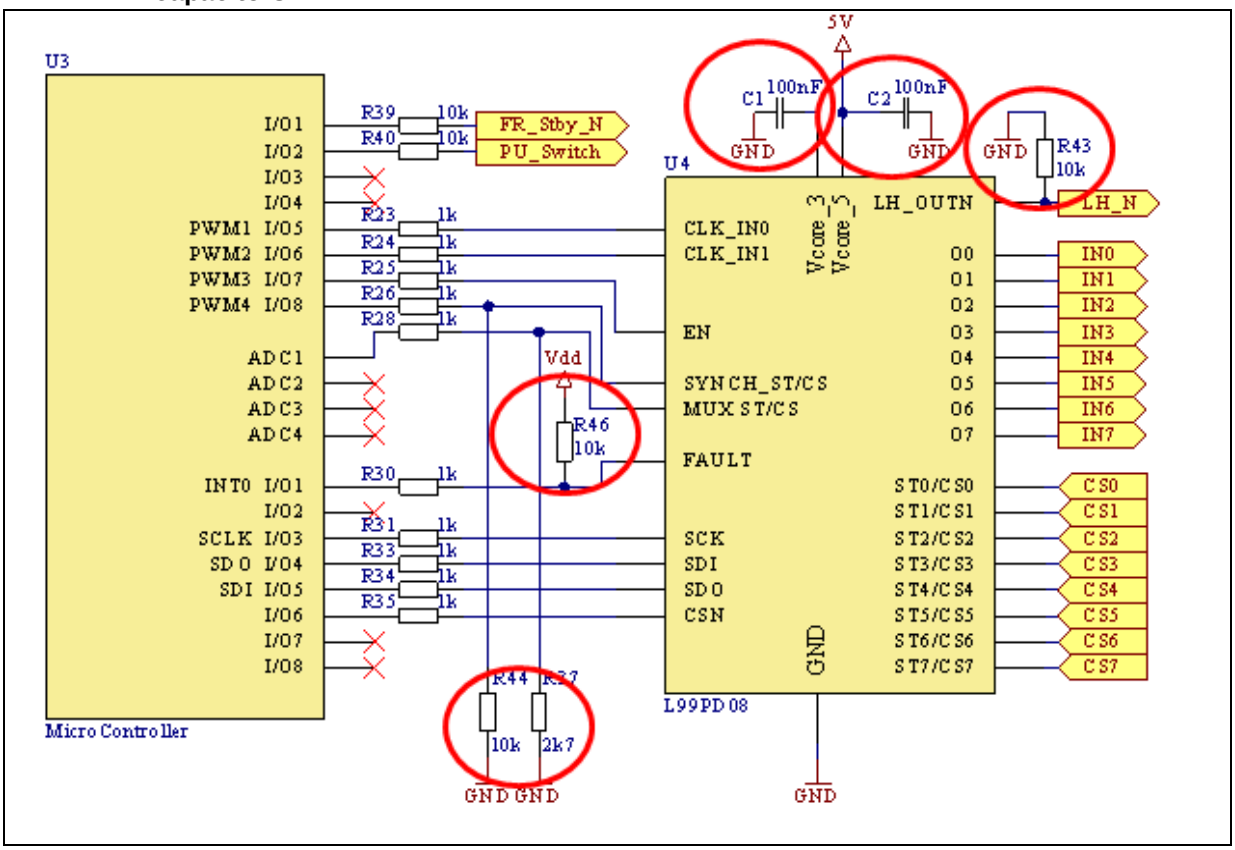
8.8.4 Pull-up/pull-down and decoupling capacitors for AMICO

Decoupling capacitors: A 100 nF capacitor should be placed on Vcore_3 and Vcore_5, as these pins are internally connected to high frequency switching blocks such as the internal oscillator of the AMICO or the SDO block.

Pull-up/pull-down resistors:

- A 10 kΩ pull down resistor is required on the LHOMEN pin if the application cannot rely solely on the weak pull down of the HSD input if the VDD of the AMICO is lost
- A 10 kΩ pull-up resistor is required on the FAULT pin of the AMICO, as the internal structure is an open drain
- A 10 kΩ series resistor on the Synch ST/CS should be placed on the SYNCH_ST/CS pin
- The sense resistor at the MUX_ST/CS can be from 1.6 kΩ to 2.7 kΩ. The optimal value depends on the load/HSD combinations.

Figure 81. Recommendations for pull-up resistors, pull-down resistors and decoupling capacitors



Appendix A Reference documents

- *VIPower M0-5 and M0-5Enhanced high-side drivers* (UM1556, Doc ID 023520)
- *SPI control diagnosis interface device for VIPower™ M0-5 and M0-5E high side drivers* (L99PD08, Doc ID 15872)

Revision history

Table 16. Document revision history

Date	Revision	Changes
03-Dec-2012	1	Initial release.
18-Sep-2013	2	Updated disclaimer.

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