LDO Parallel Design Evaluation Module

This user's guide describes the characteristics, operation, and use of the *LDO Parallel Design* evaluation module (EVM) and includes setup instructions, board layouts, schematics, and the bill of materials (BOM).

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1 Introduction

TI's *LDO Parallel Design* evaluation module (EVM) helps designers evaluate the operation and performance of the LDO parallel application with the TPS7B6750-Q1 and TPS7B4253-Q1 in parallel. For more information on the TPS7B6750-Q1 and TPS7B4253-Q1 devices, see the data sheets (SLVSCB2 and SLVSCP3, respectively).

The EVM contains three linear regulators (see Table 1).

Table 1. Device and Package Configurations

Designator	Devices	Package
U1	TPS7B6750QPWPRQ1	20-pin HTSSOP
U2, U3	TPS7B4253QPWPRQ1	20-pin HTSSOP

For more details about this *LDO Parallel Design*, see the TI reference design TIDA-00863.

2 Connector Descriptions, Setup, and Operation

This section describes the jumpers and connectors on the EVM as well and how to properly connect, set up, and use the *LDO Parallel Design* EVM.

2.1 Input and Output (I/O) Connector Descriptions

J1/VBAT connector – This connector connects the regulator IN pin to the input power supply through a diode.

J2/VOUT connector – This connector provides the output of the regulator to allow the user to attach a load to the EVM.

2.2 Bench Setup

The input voltage range for both the TPS7B6750-Q1 and TPS7B4253-Q1 is 4 V to 40 V. The EVM can support up to a 900-mA load current. Use the following steps to setup the test bench for the EVM:

1. Set the power supply for input (VBAT) to 12 V and set the current limit to 1 A.
2. Connect the power supply positive lead to the V_{IN} (J1 VBAT) and the negative lead to GND (J1 GND).
3. Apply the load between OUT (J2 VOUT) and GND (J2 GND).

2.3 Operation

The *LDO Parallel Design* EVM powers up after the V_{IN} voltage exceeds the UVLO rising threshold of both the TPS7B6750-Q1 and TPS7B4253-Q1.

3 Board Layout

The PCB offers footprints for the *LDO Parallel Design* EVM as shown in Figure 1, Figure 2, and Figure 3.

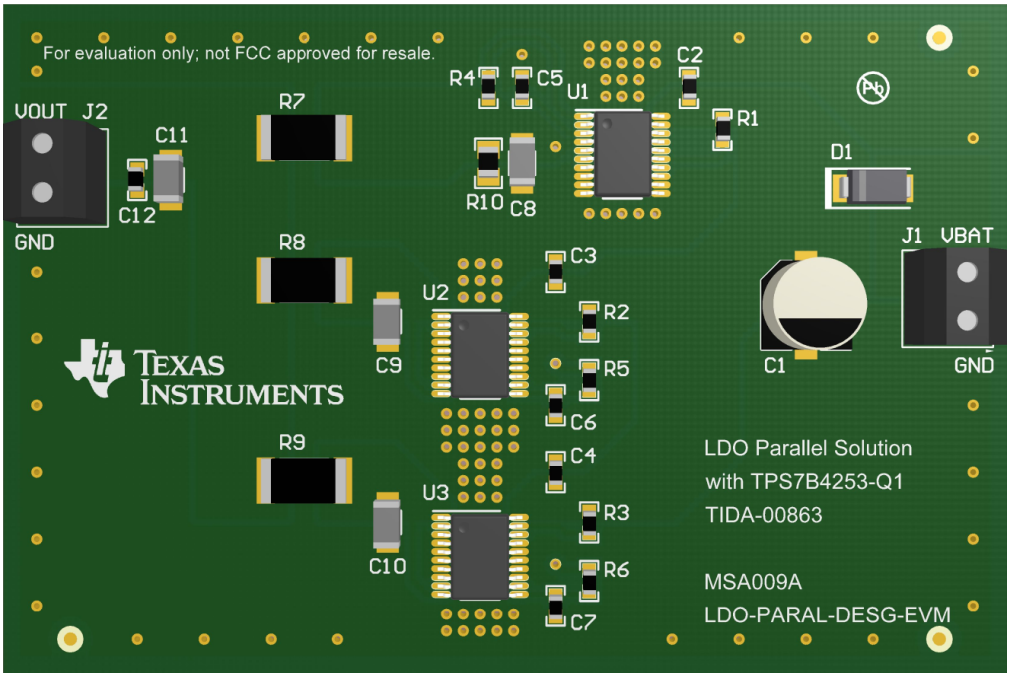

Figure 1. LDO Parallel Design EVM Component Placement (Assembly Top View)

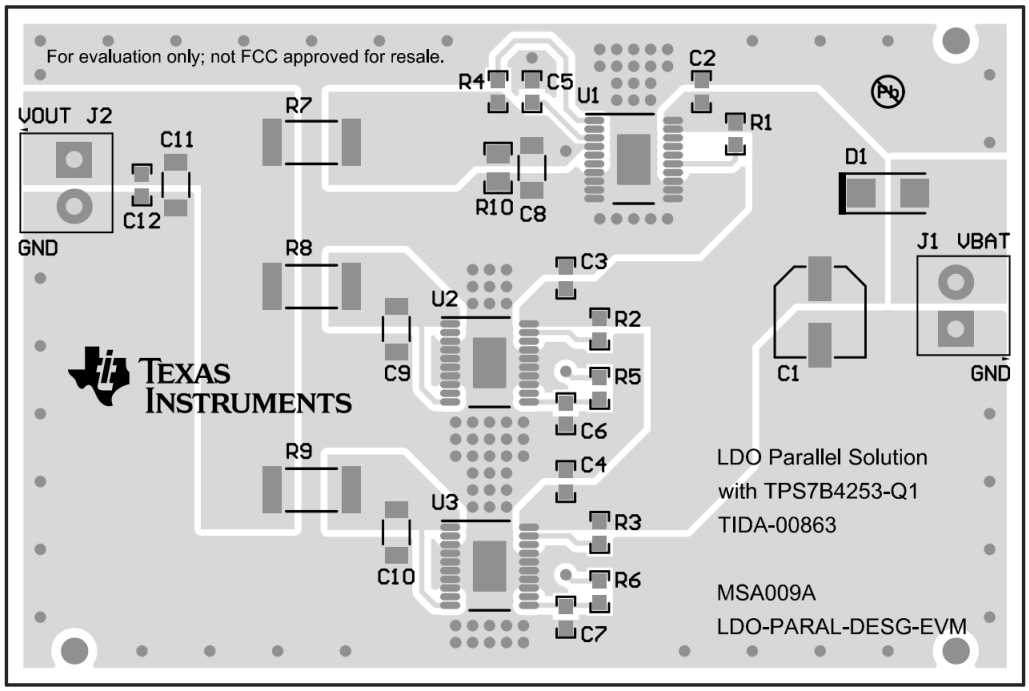

Figure 2. LDO Parallel Design EVM Top Layer Routing

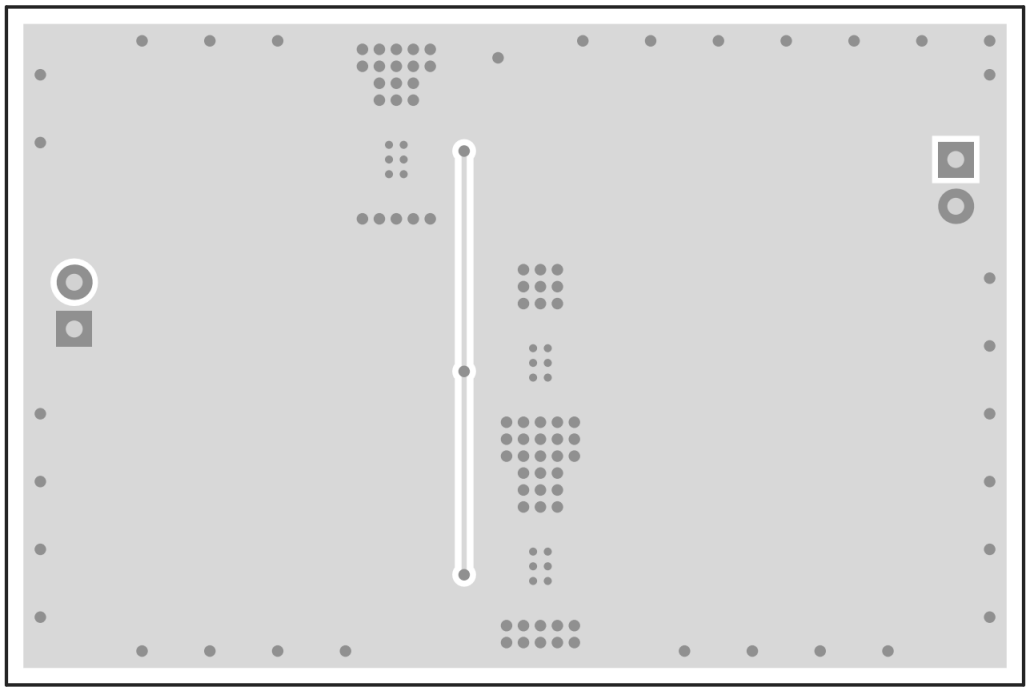

Figure 3. LDO Parallel Design EVM Bottom Layer Routing

4 Schematic and Bill of Materials

4.1 Schematic

Figure 4 illustrates the EVM schematic.

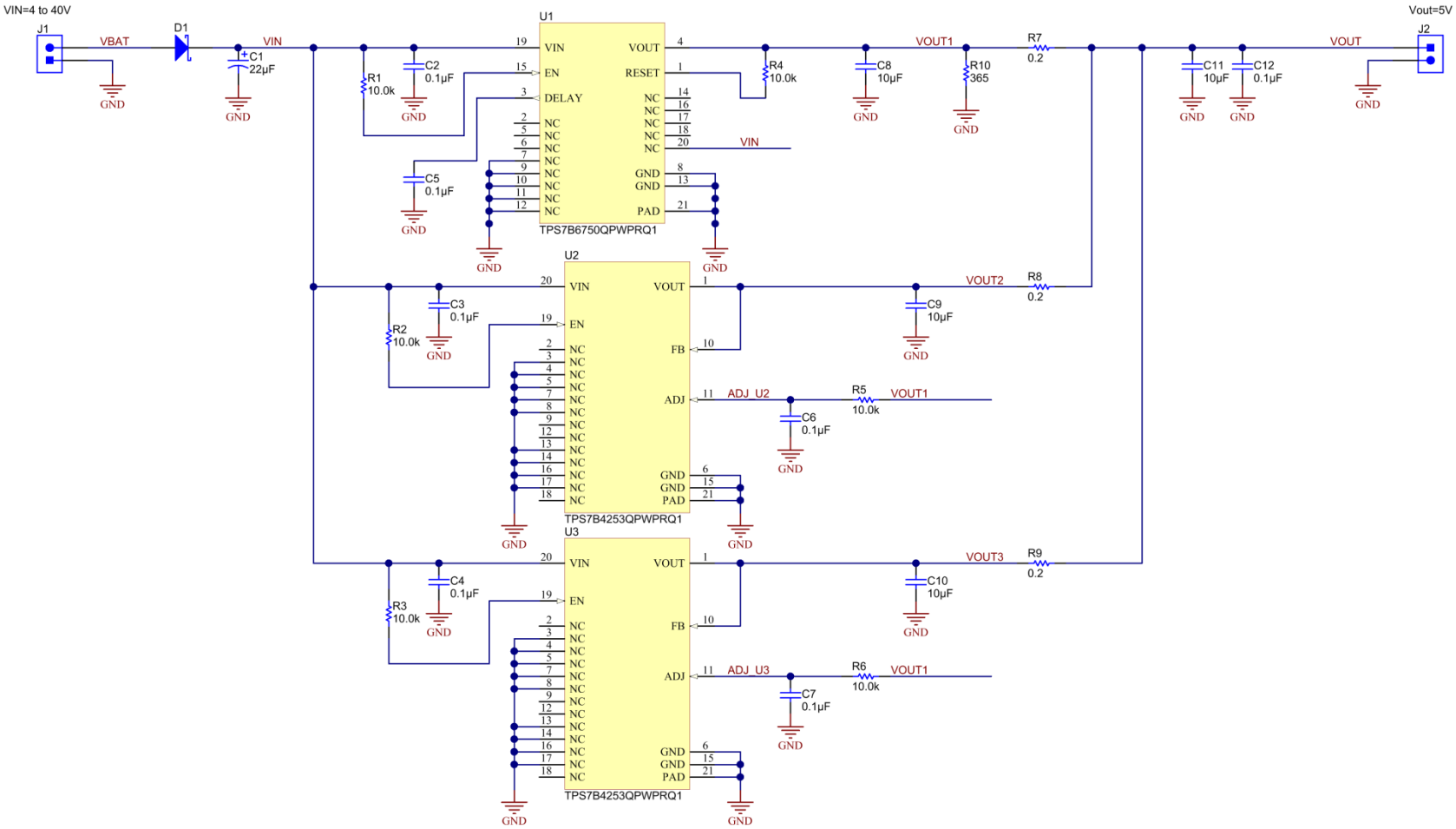

Figure 4. LDO Parallel Design EVM Schematic

4.2 Bill of Materials

Table 2 lists the EVM BOM.

Table 2. LDO Parallel Design EVM Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		MSA009	Any
C1	1	22uF	CAP, AL, 22 µF, 50 V, +/- 20%, 0.88 ohm, SMD	SMT Radial D	EEE-FK1H220P	Panasonic
C2, C3, C4, C5, C6, C7, C12	7	0.1uF	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0603	0603	GCM188R71H104KA57D	Murata
C8, C9, C10, C11	4	10uF	CAP, CERM, 10 µF, 16 V, +/- 10%, X7R, AEC-Q200 Grade 1, 1206_190	1206_190	GCM31CR71C106KA64L	Murata
D1	1	60V	Diode, Schottky, 60 V, 2 A, SMA	SMA	B260A-13-F	Diodes Inc.
J1, J2	2		Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	7.0x8.2x6.5mm	ED555/2DS	On-Shore Technology
R1, R2, R3, R4, R5, R6	6	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	CRCW060310K0FKEA	Vishay-Dale
R7, R8, R9	3	0.2	RES, 0.2, 1%, 1 W, 2512	2512	WSL2512R2000FEA	Vishay-Dale
R10	1	365	RES, 365, 1%, 0.125 W, 0805	0805	CRCW0805365RFKEA	Vishay-Dale
U1	1		450-mA High-Voltage Ultra-Low IQ Low-Dropout Regulator, PWP0020D	PWP0020D	TPS7B6750QPWPRQ1	Texas Instruments
U2, U3	2		300mA Low Dropout Voltage Tracking LDO, PWP0020D	PWP0020D	TPS7B4253QPWPRQ1	Texas Instruments
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A

5 References

LDO Parallel Solution Reference Design with TPS7B4253-Q1 TIDA-00863.

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

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Concernant les EVMs avec antennes détachables

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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