SAF1508BET

ULPI Hi-Speed Universal Serial Bus On-The-Go transceiver

Rev. 2 — 23 July 2012 Product data sheet

1. General description

The SAF1508BET is a UTMI+ Low Pin Interface (ULPI) Universal Serial Bus (USB) transceiver that is fully compliant with *Universal Serial Bus Specification Rev. 2.0*, *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3* and *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

The SAF1508BET can transmit and receive USB data at high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s), and provides a pin-optimized, physical layer front-end attachment to the USB host, peripheral or On-The-Go (OTG) controller with Single Data Rate (SDR) or Dual Data Rate (DDR) ULPI interface. The SAF1508BET can transparently transmit and receive UART signaling.

It allows USB Application-Specific Integrated Circuits (ASICs), Programmable Logic Devices (PLDs) or any system chip set to interface with the physical layer of the USB through an 8-pin (DDR) or 12-pin (SDR) synchronous digital interface.

The SAF1508BET can interface to devices with digital I/O voltages in the range of 1.4 V to 1.95 V.

The SAF1508BET is available in TFBGA36 package.

2. Features and benefits

- Fully complies with:
  - USB: *Universal Serial Bus Specification Rev. 2.0*
  - OTG: *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3*
  - ULPI: *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*
- Interfaces to USB host, peripheral or OTG cores; optimized for system ASICs with built-in ULPI link
- Complete Hi-Speed USB physical front-end solution that supports high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s)
  - Integrated 45 Ω high-speed termination resistors, 1.5 kΩ full-speed device pull-up resistor, and 15 kΩ host termination resistors
  - Integrated parallel-to-serial and serial-to-parallel converters to transmit and receive
  - USB clock and data recovery to receive USB data up to ±500 ppm
  - Insertion of stuff bits during transmit and discarding of stuff bits during receive
  - Non-Return-to-Zero Inverted (NRZI) encoding and decoding
  - Supports bus reset, suspend, resume and high-speed detection handshake (chirp)

- Complete USB OTG physical front-end that supports Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
  - Supports external charge pump or external V_{BUS} power switch
  - Complete control over USB termination resistors
  - Data line and V_{BUS} pulsing session request methods
  - Integrated V_{BUS} voltage comparators
  - Integrated cable (ID) detector
- Flexible system integration and very low power consumption
  - 3.0 V to 4.5 V power supply input range
  - Internal voltage regulator supplies 2.7 V or 3.3 V and 1.8 V
  - Supports interfacing I/O voltage of 1.4 V to 1.95 V; separate I/O voltage supply pins minimize crosstalk
  - Power-down internal regulators in power-down mode when $V_{CC(I/O)}$ is not present or the CHIP_SEL pin is not active
  - Typical operating current of 13 mA to 32 mA, depending on the USB speed and bus utilization
  - Typical V_{CC} power consumption in suspend mode is 70 μA and in power-down mode is 0.5 μA
  - 3-state ULPI interface by the CHIP_SEL pin, allowing bus reuse by other applications
- Highly optimized ULPI-compliant interface
  - 60 MHz, 8-pin or 12-pin interface between the core and the transceiver, including a 4-bit DDR bus or an 8-bit SDR bus
  - DDR or SDR interface selectable by pin
  - Supports 60 MHz output clock configuration
  - Integrated Phase-Locked Loop (PLL) supporting crystal or clock frequencies of 13 MHz, 19.2 MHz, 24 MHz or 26 MHz
  - Crystal or clock frequency selectable by pin
  - Fully programmable ULPI-compliant register set
  - 3-pin or 6-pin full-speed or low-speed serial mode
  - Internal Power-On Reset (POR) circuit
- UART interface:
  - Supports transparent UART signaling on pins DP and DM for the UART accessory application
  - 2.7 V UART signaling on pins DP and DM
  - Entering UART mode by register setting
  - Exiting UART mode by asserting STP or by toggling the CHIP_SEL pin
- Full industrial grade operating temperature range from −40 °C to +85 °C
- ESD compliance:
  - *JESD22-A114D*, 2 kV contact Human Body Model (HBM)
  - *JESD22-A115-A,* 200 V Machine Model (MM)
  - *JESD22-C101C*, 500 V Charge Device Model (CDM)
- Available in small TFBGA36 (3.5 mm × 3.5 mm) Restriction of Hazardous Substances (RoHS) compliant, halogen-free and lead-free package

3. Applications

This NXP USB product can only be used in automotive applications. Inclusion or use of the NXP USB products in other than automotive applications is not permitted and for your company's own risk. Your company agrees to full indemnify NXP for any damages resulting from such inclusion or use.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SAF1508BET	TFBGA36	plastic thin fine-pitch ball grid array package; 36 balls; body 3.5 × 3.5 × 0.8 mm	SOT912-1

5. Block diagram

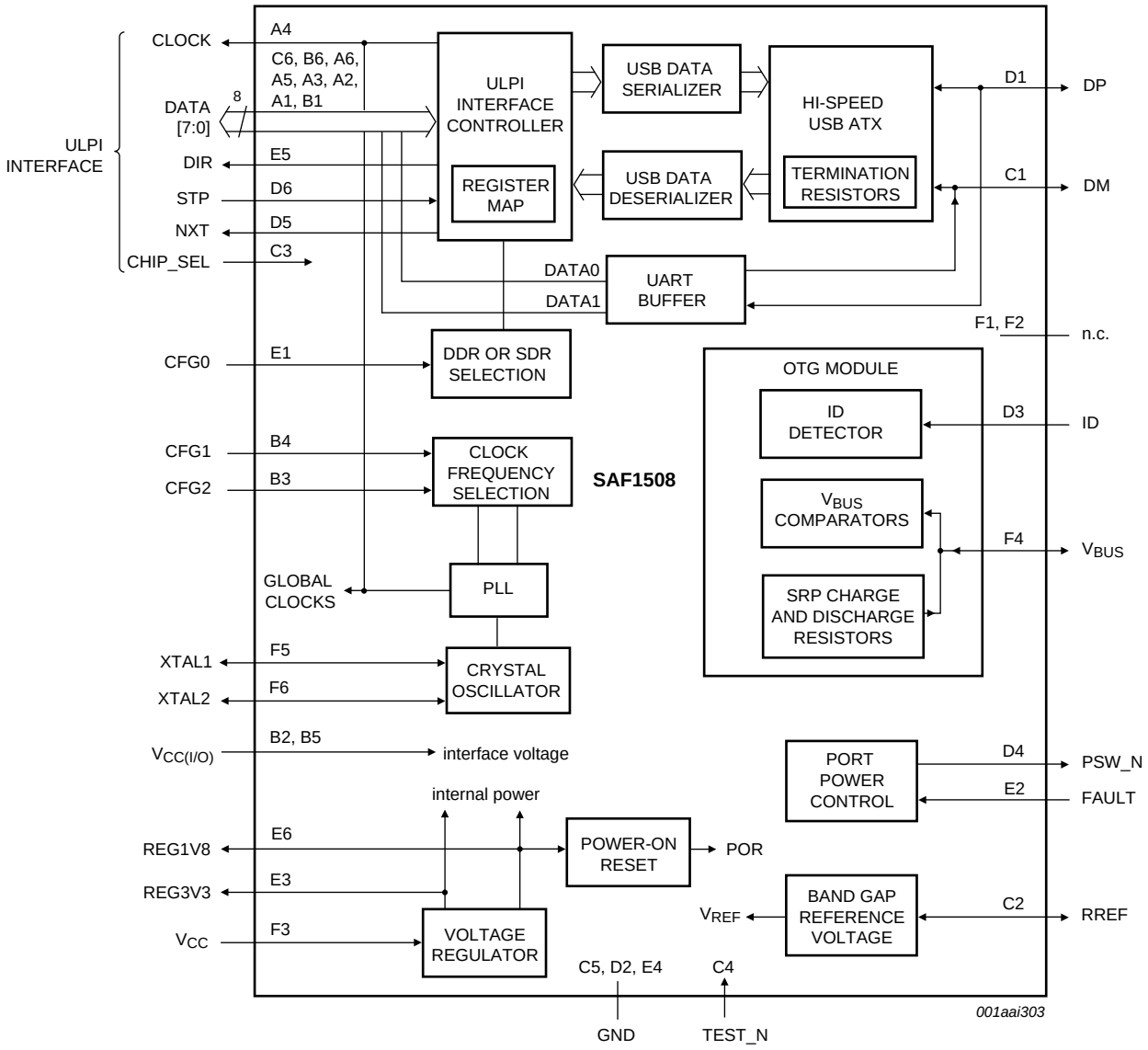
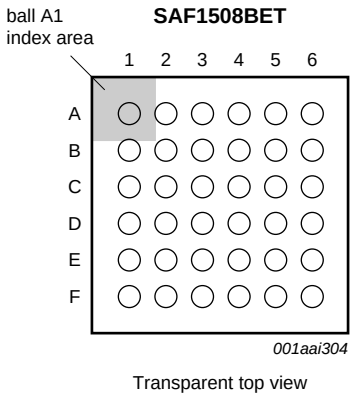


Fig 1. Block diagram

6. Pinning information

6.1 Pinning



Transparent top view

Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol[1]	Pin	Type[2]	Description[3]
DATA1	A1	I/O	ULPI data pin 1 3-state output; plain input
DATA2	A2	I/O	ULPI data pin 2 3-state output; plain input
DATA3	A3	I/O	ULPI data pin 3 3-state output; plain input
CLOCK	A4	O	60 MHz clock output 3-state output
DATA4	A5	I/O	ULPI data pin 4; when DDR mode is selected, this pin can be left open 3-state output; plain input
DATA5	A6	I/O	ULPI data pin 5; when DDR mode is selected, this pin can be left open 3-state output; plain input
DATA0	B1	I/O	ULPI data pin 0 3-state output; plain input
$V_{CC(I/O)}$	B2, B5	P	input I/O supply voltage; 1.4 V to 1.95 V; a 0.1 μF decoupling capacitor is recommended for each pin
CFG2	B3	I	select crystal or clock frequency with CFG1; see Table 5 plain input
CFG1	B4	I	select crystal or clock frequency with CFG2; see Table 5 plain input
DATA6	B6	I/O	ULPI data pin 6; when DDR mode is selected, this pin can be left open 3-state output; plain input

Table 2. Pin description *...continued*

Symbol[1]	Pin	Type[2]	Description[3]
DM	C1	AI/O	connect to the D− pin of the USB connector • USB mode: D− input or output • UART mode: TXD output
RREF	C2	AI/O	resistor reference; connect through a 12 kΩ ± 1 % resistor to GND
CHIP_SEL	C3	I	• When this pin is not active, ULPI pins will be in 3-state and the SAF1508BET is in power-down mode. • When this pin is active, ULPI pins will operate normally. active LOW chip select input; if this pin is not in use, connect it to GND plain input
TEST_N	C4	I	directly connect to $V_{CC(I/O)}$ for normal operation plain input (active LOW)
DATA7	C6	I/O	ULPI data pin 7; when DDR mode is selected, this pin can be left open 3-state output; plain input
DP	D1	AI/O	connect to the D+ pin of the USB connector • USB mode: D+ input or output • UART mode: RXD input
ID	D3	I	IDentification (ID) pin of the micro-USB connector; if this pin is not in use, leave it open (an internal 400 kΩ pull-up resistor is present on this pin) plain input; TTL
PSW_N	D4	OD	active LOW external V_{BUS} power switch or external charge pump enable open-drain output; 4 mA current sinking capability; 5 V tolerant
NXT	D5	O	ULPI next signal 3-state output
STP	D6	I	ULPI stop signal plain input
CFG0	E1	I	Select SDR or DDR ULPI interface • SDR: connect this pin to GND • DDR: connect this pin to REG3V3 plain input; TTL
FAULT	E2	I	input for the V_{BUS} digital overcurrent or fault detector signal; if this pin is not in use, connect it to GND plain input; 5 V tolerant
REG3V3	E3	P	3.3 V regulator output for USB mode or 2.7 V regulator output for UART mode; requires parallel 0.1 μF and 4.7 μF capacitors; internally powers ATX and other analog circuits; must not be used to power external circuits
GND	C5, D2, E4	P	ground supply
DIR	E5	O	ULPI direction signal 3-state output
REG1V8	E6	P	1.8 V regulator output; requires parallel 0.1 μF and 4.7 μF capacitors; internally powers the digital core; must not be used to power external circuits
n.c.	F1, F2	-	not connected; leave this pin open
V_{CC}	F3	P	input supply voltage or battery source; 3.0 V to 4.5 V **Remark:** Below 3.0 V, USB full-speed and low-speed transactions are not guaranteed, though some devices may work with the SAF1508BET at these voltages.

Table 2. Pin description *...continued*

Symbol[1]	Pin	Type[2]	Description[3]
V_{BUS}	F4	AI/O	connect to the V_{BUS} pin of the USB connector; if this pin is not in use, leave it open (an internal 70 kΩ pull-down resistor is present on this pin)
XTAL1	F5	AI/O	crystal oscillator or clock input; 1.8 V peak input allowed; frequency depends on status on the CFG1 and CFG2 pins
XTAL2	F6	AI/O	crystal oscillator output; when a clock is driven into the XTAL1 pin, leave this pin open

[1] Symbol names ending with underscore N (for example, NAME_N) indicate active LOW signals.

[2] I = input; O = output; I/O = digital input/output; OD = open-drain output; AI/O = analog input/output; P = power or ground pin.

[3] A detailed description of these pins can be found in Section 7.

7. Detailed description of pins

7.1 DATA[7:0] pins

Bidirectional data bus pins. In SDR mode, these pins are synchronized to the rising edge of CLOCK. In DDR mode, DATA[3:0] are synchronized to both the rising and falling edges of CLOCK, and DATA[7:4] can be left unconnected.

The USB link must drive these pins to LOW when the ULPI bus is idle. When the link has data to transmit to the PHY, it drives a nonzero value. Weak pull-down resistors are incorporated on these pins as part of the interface protect feature. For details, see Section 8.11.1.

These pins can also be 3-stated when pin CHIP_SEL is not active.

These pins are reconfigured to carry various data types when the chip is not in synchronous mode. For details, see Section 9.2.

7.2 $V_{CC(I/O)}$ pin

The input power pin that sets the I/O voltage level. A 0.1 μF decoupling capacitor is recommended on each $V_{CC(I/O)}$ pin. $V_{CC(I/O)}$ powers the on-chip pads of the following pins:

- CFG1
- CFG2
- CHIP_SEL
- CLOCK
- DATA[7:0]
- DIR
- NXT
- STP
- TEST_N

7.3 RREF pin

Resistor reference analog I/O pin. A 12 kΩ ± 1 % resistor must be connected between the RREF pin and GND. This provides an accurate voltage reference that biases internal analog circuitry. Less accurate resistors cannot be used. It will affect the biasing current for analog circuits, thus the USB signal quality.

7.4 DP and DM pins

When the SAF1508BET is in USB mode, the DP pin functions as the USB data plus line, and the DM pin functions as the USB data minus line.

When the SAF1508BET is in transparent UART mode, the DP pin functions as the UART RXD input pin, and the DM pin functions as the UART TXD output pin.

The DP and DM pins must be connected to the D+ and D− pins of the USB receptacle.

7.5 FAULT pin

This pin is used to detect the V_{BUS} fault condition. If the function is not used, this pin must be connected to ground to avoid floating input.

If an external V_{BUS} overcurrent or fault detection circuit is used, the output fault indicator of that circuit can be connected to the FAULT input pin. The USE_EXT_VBUS_IND bit in the OTG Control register and the IND_PASSTHRU bit in the Interface Control register must be set to logic 1. The SAF1508BET will inform the link of V_{BUS} fault events by sending RXCMDs on the ULPI bus.

The FAULT input pin is mapped to the A_VBUS_VLD bit in RXCMD. Any changes to the FAULT input will trigger RXCMD carrying the FAULT condition with A_VBUS_VLD.

For details, see Section 10.2.2.2 and Section 10.2.2.3.

7.6 PSW_N pin

The PSW_N pin is an active-LOW open-drain output pin. It is used to control external charge pumps or V_{BUS} power switches to supply V_{BUS}. When in use, an external pull-up resistor is required. This allows for per-port or ganged power control.

To enable the external power source by driving PSW_N to LOW, the link must set the DRV_VBUS_EXT bit in the OTG Control register to logic 1.

Table 3 summarizes settings to drive 5 V on V_{BUS}.

Table 3. OTG Control register power control bits

DRV_VBUS_EXT	Power source used
0	external 5 V V_{BUS} power source disabled (PSW_N = HIGH)
1	external 5 V V_{BUS} power source enabled (PSW_N = LOW)

7.7 ID pin

For OTG applications, the ID (identification) pin is connected to the ID pin of the micro-AB receptacle. As defined in *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3*, the ID pin dictates the initial role of the link. If ID is detected as HIGH, the link must assume the role of a peripheral. If ID is detected as LOW, the link must assume a host role. Roles can be swapped at a later time by using HNP.

The SAF1508BET provides an internal pull-up resistor ($R_{UP(ID)}$) to sense the value of the ID pin. The pull-up resistor must first be enabled by setting the ID_PULLUP register bit to logic 1. If the value on ID has changed, the SAF1508BET will send an RXCMD or interrupt to the link. If the link does not receive any RXCMD or interrupt by time t_{ID}, then the ID value has not changed.

The SAF1508BET also provides an internal weak pull-up resistor ($R_{weakPU(ID)}$). This weak pull-up resistor is always enabled to avoid the possible floating condition on the ID pin. The ID pin can be left open when not in use.

7.8 V_{CC} pin

Main input supply voltage for the SAF1508BET. The SAF1508BET operates correctly when V_{CC} is between 3.0 V and 4.5 V. A 0.1 μF decoupling capacitor is recommended.

7.9 V_{BUS} pin

This I/O pin acts as an input to V_{BUS} comparators, and also as a power pin for SRP charge and discharge resistors. For details, see Figure 3.

The V_{BUS} pin requires a capacitive load. Table 4 provides the recommended capacitor values for various applications.

Table 4. Recommended V_{BUS} capacitor value

Application	V_{BUS} capacitor (C_{VBUS})
OTG	1 μF to 6.5 μF; 10 V
Standard host	120 μF ± 20 %; 10 V
Standard peripheral	1 μF to 10 μF; 10 V

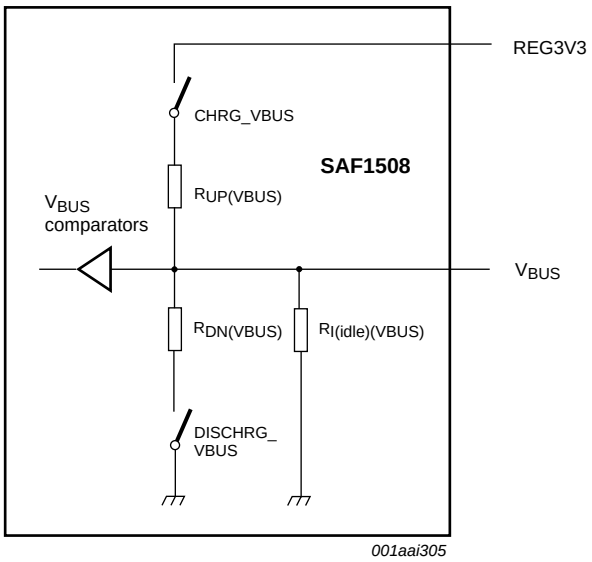


Fig 3. V_{BUS} pin internal pull-up and pull-down scheme

7.10 REG3V3 and REG1V8 pins

These are output voltage pins from the internal regulator. These supplies are used internally to power digital and analog circuits.

For proper operation of the regulator, REG3V3 and REG1V8 must each be connected to a 0.1 μF capacitor in parallel with a 4.7 μF low ESR capacitor.

REG3V3 powers on-chip pads of the following pins:

- CFG0
- DM
- DP
- FAULT
- ID
- PSW_N
- RREF

7.11 XTAL1 and XTAL2 pins

XTAL1 is the crystal oscillator input, and XTAL2 is the crystal oscillator output. The allowed crystal or clock frequency on the XTAL1 pin is selectable by the CFG1 and CFG2 pins, as shown in Table 5.

Table 5. Allowed crystal or clock frequency on the XTAL1 pin

CFG1	CFG2	Allowed crystal or clock frequency on the XTAL1 pin
0	0	19.2 MHz

Table 5. Allowed crystal or clock frequency on the XTAL1 pin *...continued*

CFG1	CFG2	Allowed crystal or clock frequency on the XTAL1 pin
0	1	26 MHz
1	0	24 MHz
1	1	13 MHz

XTAL2 must be left open when a clock is driven into XTAL1.

If a crystal is attached, it requires a capacitor on each terminal of the crystal to GND. The recommended crystal specification and required external capacitors are given in Table 6 and Table 7.

Table 6. External capacitor values for 13 MHz or 19.2 MHz clock frequency

Load capacitance C_L of the crystal[1]	Maximum series resistance R_S of the crystal[1]	External capacitor C_{XTAL} value
10 pF	< 180 Ω	18 pF
20 pF	< 100 Ω	39 pF

[1] Specified by the crystal manufacturer.

Table 7. External capacitor values for 24 MHz or 26 MHz clock frequency

Load capacitance C_L of the crystal[1]	Maximum series resistance R_S of the crystal[1]	External capacitor C_{XTAL} value
10 pF	< 140 Ω	18 pF
20 pF	< 60 Ω	39 pF

[1] Specified by the crystal manufacturer.

7.12 CHIP_SEL pin

When CHIP_SEL is inactive, ULPI pins DATA[7:0], CLOCK, DIR and NXT are 3-stated. In addition the STP input is ignored; internal circuits are powered-down as well.

When CHIP_SEL is active, the SAF1508BET will operate normally.

7.13 DIR pin

ULPI direction output pin. Synchronous to the rising edge of CLOCK. Controls the direction of the data bus. By default, the SAF1508BET holds DIR at LOW, causing the data bus to be an input. When DIR is LOW, the SAF1508BET listens for data from the link. The SAF1508BET pulls DIR to HIGH only when it has data to send to the link, which is for one of the two reasons:

- To send the USB receive data, RXCMD status updates and register reads data to the link.
- To block the link from driving the data bus during power-up, reset and low power (suspend) mode.

This pin can be 3-stated when the CHIP_SEL pin is not active.

7.14 STP pin

ULPI stop input pin. Synchronous to the rising edge of CLOCK. The link must assert STP to signal the end of a USB transmit packet or a register write operation. When DIR is asserted, the link can optionally assert STP for one cycle to abort the SAF1508BET, causing it to deassert DIR in the next clock cycle.

7.15 NXT pin

ULPI next data output pin. Synchronous to the rising edge of CLOCK. The SAF1508BET holds NXT at LOW, by default. When DIR is LOW and the link is sending data to the SAF1508BET, NXT will be asserted to notify the link to provide the next data byte. When DIR is HIGH and the SAF1508BET is sending data to the link, NXT will be asserted to notify the link that another valid byte is on the bus. NXT is not used for register read data or the RXCMD status update.

This pin can be 3-stated when the CHIP_SEL pin is not active.

7.16 CLOCK pin

A 60 MHz interface clock to synchronize the ULPI bus. In SDR mode, all ULPI pins are synchronous to the rising edge of CLOCK. In DDR mode, DATA[3:0] are the only interface pins that are synchronous to both the rising and falling edges of CLOCK. All other pins are synchronous to the rising edge of CLOCK only, including DIR, NXT and STP.

The SAF1508BET outputs 60 MHz clock when:

- A crystal is attached between the XTAL1 and XTAL2 pins.
- A clock is driven into the XTAL1 pin, with the XTAL2 pin left unconnected.

7.17 GND pin

Global ground signal. To ensure the correct operation of the SAF1508BET, GND must be soldered to the cleanest available ground.

8. Functional description

8.1 ULPI interface controller

The SAF1508BET provides an 8-pin or 12-pin interface that is compliant with *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*. This interface must be connected to a USB link.

The ULPI interface controller provides the following functions:

- ULPI-compliant interface and register set
- Allows full control over the USB peripheral, host or OTG functionality
- Parses the USB transmit and receive data
- Prioritizes the USB receive data, USB transmit data, interrupts and register operations
- Low-power mode
- Transparent UART mode
- 3-pin serial mode
- 6-pin serial mode
- Generates RXCMDs (status updates)
- Maskable interrupts

For more information on the ULPI protocol, see Section 10.

8.2 USB serializer and deserializer

The USB data serializer prepares data to transmit on the USB bus. To transmit data, the USB link sends a transmit command and data on the ULPI bus. The serializer performs parallel-to-serial conversion, bit stuffing and NRZI encoding. For packets with a Package IDentifier (PID), the serializer adds a SYNC pattern to the start of the packet, and an EOP pattern to the end of the packet. When the serializer is busy and cannot accept any more data, the ULPI interface controller deasserts NXT.

The USB data deserializer decodes data received from the USB bus. When data is received, the deserializer strips the SYNC and EOP patterns, and then performs serial-to-parallel conversion, NRZI decoding and discarding of stuff bits on the data payload. The ULPI interface controller sends data to the USB link by asserting DIR, and then asserting NXT whenever a byte is ready. The deserializer also detects various receive errors, including bit stuff errors, elasticity buffer underrun or overrun, and byte-alignment errors.

8.3 Hi-Speed USB (USB 2.0) ATX

The Hi-Speed USB ATX block is an analog front-end containing the circuitry needed to transmit, receive and terminate the USB bus in high-speed, full-speed and low-speed, for USB peripheral, host or OTG implementations. The following circuitry is included:

- Differential drivers to transmit data at high-speed, full-speed and low-speed
- Differential and single-ended receivers to receive data at high-speed, full-speed and low-speed

- Squelch circuit to detect high-speed bus activity
- High-speed disconnect detector
- 45 Ω high-speed bus terminations on DP and DM
- 1.5 kΩ pull-up resistor on DP
- 15 kΩ bus terminations on DP and DM

For details on controlling resistor settings, see Table 14.

8.4 Voltage regulator

The SAF1508BET contains a built-in voltage regulator that conditions the V_{CC} supply for use inside the SAF1508BET. The voltage regulator:

- Supports input supply range 3.0 V < V_{CC} < 4.5 V.
- Can be supplied from a battery with the preceding voltage range.
- Supplies internal digital circuitry with 1.8 V and analog circuitry with 3.3 V or 2.7 V.
- In USB mode, automatically bypasses the internal 3.3 V regulator when V_{CC} < 3.5 V, the internal analog circuitry directly draws power from the V_{CC} pin. In UART mode, the bypass switch will be disabled.
- Will be shut down when $V_{CC(I/O)}$ is not present or when the CHIP_SEL pin is not active.

8.5 Crystal oscillator and PLL

The SAF1508BET has a built-in crystal oscillator and a Phase-Locked Loop (PLL) for clock generation. When a crystal is in use, the built-in crystal oscillator generates a square wave clock for internal use. A square wave clock of the same frequency can also be driven directly into the XTAL1 pin. Using an existing square wave clock can save the cost of the crystal and also reduce the board space. The crystal or clock frequencies supported are 13 MHz, 19.2 MHz, 24 MHz and 26 MHz.

The PLL takes the square wave clock from the crystal oscillator, and multiplies or divides it into various frequencies for internal use.

The PLL produces the following frequencies, irrespective of the clock source:

- 1.5 MHz for low-speed USB data
- 12 MHz for full-speed USB data
- 60 MHz clock for the ULPI interface controller
- 480 MHz for high-speed USB data
- Other internal frequencies for data conversion and data recovery

8.6 UART buffer

The UART buffer includes circuits to support the transparent UART signaling between the DATA0 or DATA1 pin and the DM or DP pin.

When the SAF1508BET is put into UART mode, it acts as a voltage level shifter between the following pins:

- From DATA0 ($V_{CC(I/O)}$ level) to DM (2.7 V level) for the UART TXD signaling path.
- From DP (2.7 V level) to DATA1 ($V_{CC(I/O)}$ level) for the UART RXD signaling path.

8.7 OTG module

This module contains several sub-blocks that provide all the functionality required by the USB OTG specification. Specifically, it provides the following circuits:

- The ID detector to sense the ID pin of the micro-USB cable. The ID pin dictates which device is initially configured as a host and which as a peripheral.
- V_{BUS} comparators to determine the V_{BUS} voltage level. This is required for the V_{BUS} detection, SRP and HNP.
- Resistors to temporarily charge and discharge V_{BUS}. This is required for SRP.

8.7.1 ID detector

The ID detector detects which end of the micro-USB cable is plugged in. The ID detector must first be enabled by setting the ID_PULLUP register bit to logic 1. If the SAF1508BET senses a value on the ID pin that is different from the previously reported value, an RXCMD status update will be sent to the USB link, or an interrupt will be asserted.

- If the micro-B end of the cable is plugged in (or nothing is plugged in), the SAF1508BET will report that ID_GND is logic 1. The USB link must be in the B-device state.
- If the micro-A end of the cable is plugged in, the SAF1508BET will report that ID_GND is logic 0. The USB link must be in the A-device state.

The ID pin has a weak pull-up resistor ($R_{weakPU(ID)}$) permanently enabled to avoid the floating condition.

8.7.2 V_{BUS} comparators

The SAF1508BET provides three comparators to detect the V_{BUS} voltage level. The comparators are explained in the following subsections.

8.7.2.1 V_{BUS} valid comparator

This comparator is used only by hosts and A-devices to determine whether the voltage on V_{BUS} is at a valid level for operation. The SAF1508BET minimum threshold for the V_{BUS} valid comparator is 4.4 V. Any voltage on V_{BUS} below this threshold is considered invalid. During power-up, it is expected that the comparator output will be ignored.

8.7.2.2 Session valid comparator

The session valid comparator is a TTL-level input that determines when V_{BUS} is high enough for a session to start. Peripherals, A-devices and B-devices use this comparator to detect when a session is started. The A-device also uses this comparator to determine when a session is completed. The session valid threshold of the SAF1508BET is between 0.8 V to 2.0 V.

8.7.2.3 Session end comparator

The session end comparator determines when V_{BUS} is below the B-device session end threshold of 0.2 V to 0.8 V. The B-device uses this threshold to determine when a session has ended.

8.7.3 SRP charge and discharge resistors

The SAF1508BET provides on-chip resistors for short-term charging and discharging of V_{BUS}. These are used by the B-device to request a session, prompting the A-device to restore the V_{BUS} power. First, the B-device makes sure that V_{BUS} is fully discharged from the previous session by setting the DISCHRG_VBUS register bit to logic 1 and waiting for SESS_END to be logic 1. Then the B-device charges V_{BUS} by setting the CHRG_VBUS register bit to logic 1. The A-device sees that V_{BUS} is charged above the session valid threshold and starts a session by turning on the V_{BUS} power.

8.8 Port power control

For an OTG or host application, the SAF1508BET uses the PSW_N pin to control the external power switch for the V_{BUS} 5 V supply. The overcurrent detector output of the external power switch can be connected to the FAULT pin of the SAF1508BET to indicate to the ULPI link the V_{BUS} overcurrent status. For the connection scheme, see Figure 4.

When the FAULT pin is not used, connect it to GND.

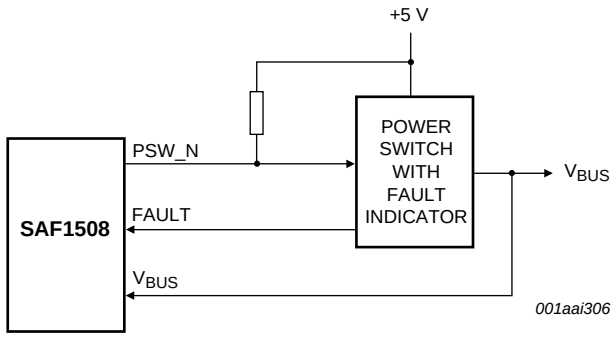


Fig 4. Digital overcurrent detection scheme

8.9 Band gap reference voltage

The band gap circuit provides a stable internal voltage reference to bias the analog circuitry. This band gap circuit requires an accurate external reference resistor. Connect a 12 kΩ ± 1 % resistor between the RREF pin and GND.

8.10 Power-On Reset (POR)

An internal POR is generated when REG1V8 rises above $V_{POR(trip)}$. The internal POR pulse will be generated whenever REG1V8 drops below $V_{POR(trip)}$ for more than $t_{w(REG1V8\_L)}$.

To give a better view of the functionality, Figure 5 shows a possible curve of REG1V8. The internal POR starts with logic 0 at t0. At t1, the detector will see the passing of the trip level so that POR pulse is generated to reset all internal circuits. If REG1V8 dips from t2 to t3 for greater than $t_{w(REG1V8\_L)}$, another POR pulse is generated. If the dip from t4 to t5 is less than $t_{w(REG1V8\_L)}$, the internal POR pulse will not be generated and will remain LOW.

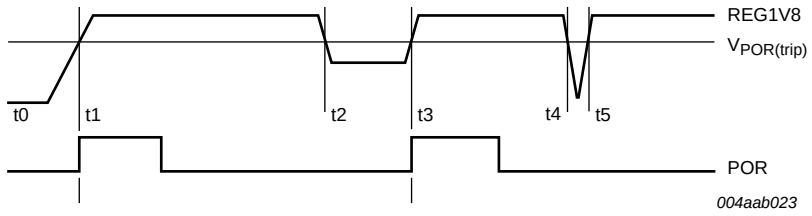


Fig 5. Internal power-on reset timing

8.11 Power-up, reset and bus idle sequence

Figure 6 shows a typical start-up sequence.

On power-up, the SAF1508BET performs an internal power-on reset and asserts DIR to indicate to the link that the ULPI bus cannot be used. When the internal PLL is stable, the SAF1508BET deasserts DIR and drives 60 MHz clock out from the CLOCK pin. The power-up time depends on the V_{CC} supply rise time, the crystal start-up time, and PLL start-up time $t_{startup(PLL)}$. When DIR is deasserted, the link must drive the data bus to a valid level. By default, the link must drive data to LOW. Before beginning USB packets, the link must set the RESET bit in the Function Control register to reset the SAF1508BET. After the RESET bit is set, the SAF1508BET will assert DIR until the internal reset completes. The SAF1508BET will automatically deassert DIR and clear the RESET bit when the reset has completed. After every reset, an RXCMD is sent to the link to update USB status information. After this sequence, the ULPI bus is ready for use and the link can start USB operations.

If $V_{CC(I/O)}$ is not present or the CHIP_SEL pin is non-active, the SAF1508BET will be kept in power-down mode. In power-down mode, all ULPI interface pins will be put in 3-state, the internal regulator will be shut down (see Table 8), and the total power current from V_{CC} will be less than I_{CC} in power-down mode.

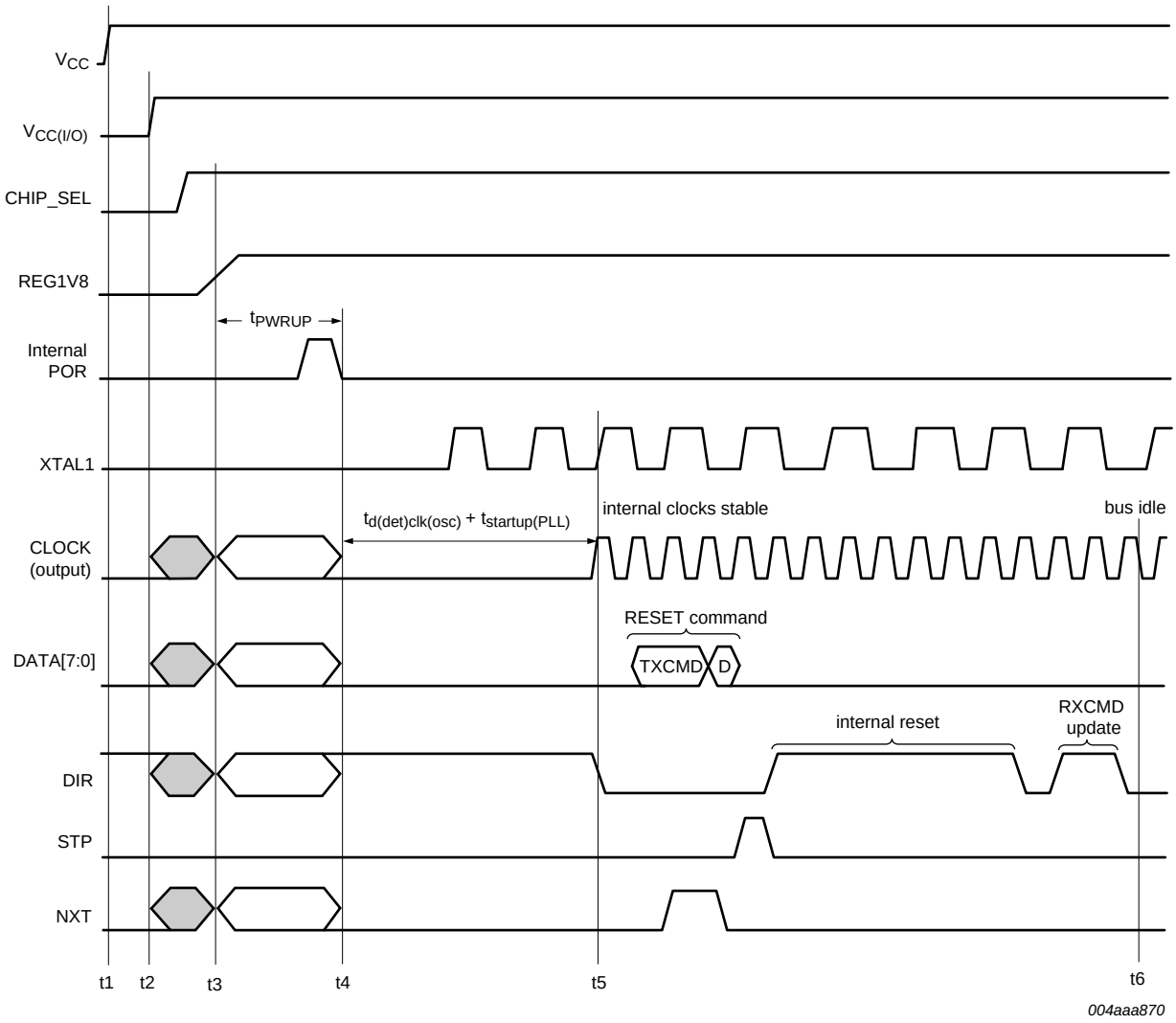
The link can do a hardware reset to the SAF1508BET by toggling the CHIP_SEL pin. The recommended sequence is:

1. Deactivate the CHIP_SEL pin.
2. Wait for at least t_{PWRDN}.
3. Activate the CHIP_SEL pin.

The recommended power-up sequence for the link is:

1. Apply the V_{CC} and $V_{CC(I/O)}$ power.
2. Activate the CHIP_SEL pin.
3. The link waits for at least t_{PWRUP}, ignoring all the ULPI pin status.
4. The link may start to detect the DIR status level. If DIR is detected LOW, the link may send a RESET command.

The ULPI interface is ready for use.



t1 = V_{CC} is applied to the SAF1508BET.

t2 = $V_{CC(I/O)}$ is turned on. ULPI interface pins CLOCK, DATA[7:0], DIR and NXT are in 3-state as long as CHIP_SEL is non-active.

t3 = CHIP_SEL turns from non-active to active. The SAF1508BET regulator starts to turn on. ULPI pads are not in 3-state and may drive to either LOW or HIGH. It is recommended that the link ignores ULPI pins status during t_{PWRUP}.

t4 = Power-on reset threshold is reached and the POR pulse is generated. After the POR pulse, ULPI pins are driven to a defined level. DIR is driven to HIGH and the other pins are driven to LOW.

t5 = The PLL is stabilized after $t_{d(det)clk(osc)} + t_{startup(PLL)}$. The CLOCK pin starts to output 60 MHz. The DIR pin will transition from HIGH to LOW. The link must drive DATA[7:0] and STP to LOW as the idle state. The link will then issue a reset command to initialize the SAF1508BET.

t6 = The power-up sequence is completed and the ULPI bus interface is ready for use.

Fig 6. Power-up and reset sequence required before the ULPI bus is ready for use

8.11.1 Interface protection

By default, the SAF1508BET enables a weak pull-up resistor on STP. If the STP pin is unexpectedly HIGH at any time, the SAF1508BET will protect the ULPI interface by enabling weak pull-down resistors on DATA[7:0].

The interface protect feature prevents unwanted activity of the SAF1508BET whenever the ULPI interface is not correctly driven by the link. For example, when the link powers up more slowly than the SAF1508BET.

The interface protect feature can be disabled by setting the INTF_PROT_DIS bit to logic 1.

8.11.2 Interface behavior with respect to the CHIP_SEL pin

The use of the CHIP_SEL pin is optional. When not active, ULPI pins will be 3-stated and the internal circuitry is powered down. If the CHIP_SEL pin is not used, it must be connected to GND in the SAF1508BET. Figure 7 shows the ULPI interface behavior when the CHIP_SEL pin is asserted and subsequently deasserted.

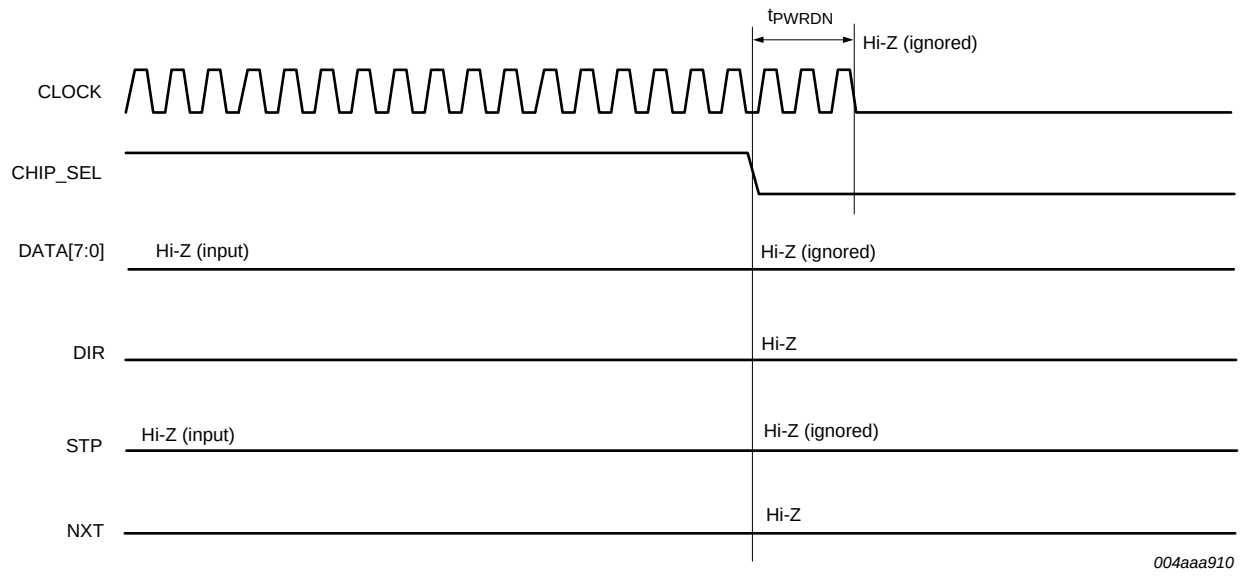


Fig 7. Interface behavior with respect to the CHIP_SEL pin

9. Modes of operation

9.1 Power modes

When both $V_{CC(I/O)}$ and V_{CC} are not powered, there will be no leakage from the V_{BUS} pin to all the remaining pins, including V_{CC} and $V_{CC(I/O)}$. Applying V_{BUS} within the normal range will not damage the SAF1508BET chip.

When both V_{CC} and $V_{CC(I/O)}$ are powered and are within the operating voltage range, the SAF1508BET will be fully functional as in normal mode.

When $V_{CC(I/O)}$ is powered and the V_{CC} voltage is below the operating voltage range of the SAF1508BET, the application system must detect the low voltage condition and set the CHIP_SEL pin to non-active state to put the SAF1508BET in power-down mode. This is to protect the ULPI and USB interfaces from driving wrong levels. Under this condition, the $V_{CC(I/O)}$ voltage will not leak to USB pins (V_{BUS}, DP, DM and ID) and the V_{CC} pin. All the digital pins (see Section 7.2) powered by $V_{CC(I/O)}$ are configured as high-impedance inputs. These pins must be driven to defined states or terminated by using pull-up or pull-down resistors to avoid floating input condition. Other pins (see Section 7.10) are not powered.

9.1.1 Normal mode

In normal mode, both V_{CC} and $V_{CC(I/O)}$ are powered. The CHIP_SEL pin is active. The SAF1508BET is fully functional.

9.1.2 Power-down mode

When $V_{CC(I/O)}$ is not present or when the CHIP_SEL pin is not active, the SAF1508BET is put into power-down mode. In this mode, internal regulators are powered down to keep the V_{CC} current to a minimum. The voltage on the V_{CC} pin will not leak to the $V_{CC(I/O)}$ and/or V_{BUS} pins. In this mode, the SAF1508BET pin states are given in Table 8.

Table 8. Pin states in power-down mode

Pin name	Pin state when $V_{CC(I/O)}$ is not present	Pin state when $V_{CC(I/O)}$ is present and CHIP_SEL is HIGH
V_{CC}	3.0 V to 4.5 V	3.0 V to 4.5 V
$V_{CC(I/O)}$	not powered[1]	1.4 V to 1.95 V
REG3V3, REG1V8, DP, DM, V_{BUS}, ID, CFG0, XTAL1, XTAL2, RREF, PSW_N, FAULT	not powered[1]	not powered[1]
CHIP_SEL, CFG1, CFG2, TEST_N, STP, NXT, DIR, DATA[7:0], CLOCK	not powered[1]	high-Z

[1] These pins must not be externally driven to HIGH. Otherwise, the SAF1508BET behavior is undefined and leakage current will occur.

When $V_{CC(I/O)}$ is not present, all digital pins (see Section 7.2) that are powered by $V_{CC(I/O)}$ are not powered. These pins must not be externally driven to HIGH, otherwise the SAF1508BET behavior is undefined and leakage current will occur. Other pins (see Section 7.10) are not powered.

When the SAF1508BET is put into power-down mode by disabling the CHIP_SEL pin, all the digital pins (see Section 7.2) that are powered by $V_{CC(I/O)}$ are configured as high-impedance inputs. These pins must be driven to defined states or terminated by

using pull-up or pull-down resistors to avoid floating input condition. Other pins (see Section 7.10) are not powered. In this mode, minimum current will be drawn by $V_{CC(I/O)}$ to detect the CHIP_SEL pin status.

9.2 ULPI modes

The SAF1508BET ULPI interface can be programmed to operate in five modes. In each mode, the signals on the data bus are reconfigured as described in the following subsections. Setting more than one mode will lead to undefined behavior.

9.2.1 Synchronous mode

This is default mode. On power-up and when CLOCK is stable, the SAF1508BET will enter synchronous mode.

In synchronous mode, the link must synchronize all ULPI signals to CLOCK, meeting the set-up time and the hold time as defined in Section 15.

This mode is used by the link to perform the following tasks:

- High-speed detection handshake (chirp)
- Transmit and receive USB packets
- Read and write to registers
- Receive USB status updates (RXCMDs) from the SAF1508BET

For more information on various synchronous mode protocols, see Section 10.

Table 9. ULPI signal description

Signal name	Direction on the SAF1508BET	Signal description
CLOCK	O	**60 MHz interface clock**: When a crystal is attached or a clock is driven into the XTAL1 pin, the SAF1508BET will drive a 60 MHz output clock. During low-power, serial and UART modes, the clock is turned off to save power.
DATA[7:0]	I/O	**8-bit data bus**: In synchronous mode, the link drives DATA[7:0] to LOW by default. The link initiates transfers by sending a nonzero data pattern called a TXCMD (transmit command). In synchronous mode, the direction of DATA[7:0] is controlled by DIR. Contents of DATA[7:0] lines must be ignored for exactly one clock cycle whenever DIR changes value. This is called a turnaround cycle. Data lines have fixed directions and different meanings in low-power, 3-pin serial and UART modes.

Table 9. ULPI signal description *...continued*

Signal name	Direction on the SAF1508BET	Signal description
DIR	O	**Direction**: Controls the direction of data bus DATA[7:0]. In synchronous mode, the SAF1508BET drives DIR to LOW by default, making the data bus an input so that the SAF1508BET can listen for TXCMD from the link. The SAF1508BET drives DIR to HIGH only when it has data for the link. When DIR and NXT are HIGH, the byte on the data bus contains decoded USB data. When DIR is HIGH and NXT is LOW, the byte contains status information called an RXCMD (receive command). The only exception to this rule is when the PHY returns register read data, where NXT is also LOW, replacing the usual RXCMD byte. Every change in DIR causes a turnaround cycle on the data bus, during which DATA[7:0] are not valid and must be ignored by the link. DIR is always asserted during low-power, serial and UART modes.
STP	I	**Stop**: In synchronous mode, the link drives STP to HIGH for one cycle after the last byte of data is sent to the SAF1508BET. The link can optionally assert STP to force DIR to be deasserted. In low-power, serial and UART modes, the link holds STP at HIGH to wake up the SAF1508BET, causing the ULPI bus to return to synchronous mode.
NXT	O	**Next**: In synchronous mode, the SAF1508BET drives NXT to HIGH to throttle data. If DIR is LOW, the SAF1508BET asserts NXT to notify the link to place the next data byte on DATA[7:0] in the following clock cycle. If DIR is HIGH, the SAF1508BET asserts NXT to notify the link that a valid USB data byte is on DATA[7:0] in the current cycle. The SAF1508BET always drives an RXCMD when DIR is HIGH and NXT is LOW, unless register read data is to be returned to the link in the current cycle. NXT is not used in low-power, serial and UART modes.

9.2.2 Low-power mode

When the USB bus is idle, the link can place the SAF1508BET into low-power mode (also called suspend mode). In low-power mode, the data bus definition changes to that shown in Table 10. To enter low-power mode, the link sets the SUSPENDM bit in the Function Control register to logic 0. To exit low-power mode, the link asserts the STP signal. After exiting low-power mode, the SAF1508BET will send an RXCMD to the link if a change was detected in any interrupt source, and the change still exists. An RXCMD may not be sent if the interrupt condition is removed before exiting.

The SAF1508BET will draw only suspend current from the V_{CC} supply. See Table 52.

During low-power mode, the clock on XTAL1 can be stopped. The clock must be started again before asserting STP to exit low-power mode.

For more information on low-power mode enter and exit protocols, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

Table 10. Signal mapping during low-power mode

Signal	Maps to	Direction	Description
LINESTATE0	DATA0	O	combinatorial LINESTATE0 directly driven by the analog receiver
LINESTATE1	DATA1	O	combinatorial LINESTATE1 directly driven by the analog receiver

Table 10. Signal mapping during low-power mode *...continued*

Signal	Maps to	Direction	Description
reserved	DATA2	O	reserved; the SAF1508BET will drive this pin to LOW
INT	DATA3	O	active HIGH interrupt indication; will be asserted and latched whenever any unmasked interrupt occurs
reserved	DATA[7:4]	O	reserved; the SAF1508BET will drive these pins to LOW

9.2.3 6-pin full-speed or low-speed serial mode

If the link requires a 6-pin serial interface to transmit and receive full-speed or low-speed USB data, it can set the SAF1508BET to 6-pin serial mode. In 6-pin serial mode, the data bus definition changes to that shown in Table 11. To enter 6-pin serial mode, the link sets the 6PIN_FSLS_SERIAL bit in the Interface Control register to logic 1. To exit 6-pin serial mode, the link asserts the STP signal. This is provided primarily for links that contain legacy full-speed or low-speed functionality, providing a more cost-effective upgrade path to high-speed. An interrupt pin is also provided to inform the link of USB events. If the link requires CLOCK to be running during 6-pin serial mode, the CLOCK_SUSPENDM register bit must be set to logic 1 before entering 6-pin serial mode.

For more information on 6-pin serial mode enter and exit protocols, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

The 6-pin serial mode is not applicable if the SAF1508BET functions as a 4-bit DDR.

Table 11. Signal mapping for 6-pin serial mode

Signal	Maps to	Direction	Description
TX_ENABLE	DATA0	I	active HIGH transmit enable
TX_DAT	DATA1	I	transmit differential data on DP and DM
TX_SE0	DATA2	I	transmit single-ended zero on DP and DM
INT	DATA3	O	active HIGH interrupt indication; will be asserted and latched whenever any unmasked interrupt occurs
RX_DP	DATA4	O	single-ended receive data from DP
RX_DM	DATA5	O	single-ended receive data from DM
RX_RCV	DATA6	O	differential receive data from DP and DM
reserved	DATA7	O	reserved; the SAF1508BET will drive this pin to LOW

9.2.4 3-pin full-speed or low-speed serial mode

If the link requires a 3-pin serial interface to transmit and receive full-speed or low-speed USB data, it can set the SAF1508BET to 3-pin serial mode. In 3-pin serial mode, the data bus definition changes to that shown in Table 12. To enter 3-pin serial mode, the link sets the 3PIN_FSLS_SERIAL bit in the Interface Control register to logic 1. To exit 3-pin serial mode, the link asserts the STP signal. This is provided primarily for links that contain legacy full-speed or low-speed functionality, providing a more cost-effective upgrade path to high-speed. An interrupt pin is also provided to inform the link of USB events. If the link requires CLOCK to be running during 3-pin serial mode, the CLOCK_SUSPENDM register bit must be set to logic 1 before entering 3-pin serial mode.

For more information on 3-pin serial mode enter and exit protocols, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

Table 12. Signal mapping for 3-pin serial mode

Signal	Maps to	Direction	Description
TX_ENABLE	DATA0	I	active HIGH transmit enable
DAT	DATA1	I/O	transmit differential data on DP and DM when TX_ENABLE is HIGH receive differential data from DP and DM when TX_ENABLE is LOW
SE0	DATA2	I/O	transmit single-ended zero on DP and DM when TX_ENABLE is HIGH receive single-ended zero from DP and DM when TX_ENABLE is LOW
INT	DATA3	O	active HIGH interrupt indication; will be asserted and latched whenever any unmasked interrupt occurs
reserved	DATA[7:4]	O	reserved; the SAF1508BET will drive these pins to LOW

9.2.5 Transparent UART mode

In transparent UART mode, the SAF1508BET functions as a voltage level shifter between the following pins:

- From pin DATA0 ($V_{CC(I/O)}$ level) to pin DM (2.7 V level).
- From pin DP (2.7 V level) to pin DATA1 ($V_{CC(I/O)}$ level).

The USB transceiver is used to drive the UART transmitting signal on the DM line. The rise time and the fall time of the transmitting signal is determined by whether a full-speed or low-speed transceiver is in use. It is recommended to use a low-speed transceiver if the UART bit rate is below 921 kbit/s for better ElectroMagnetic Interference (EMI) performance. If the UART bit rate is equal to or above 921 kbit/s, a full-speed transceiver can be used.

In transparent UART mode, data bus definitions change to that shown in Table 13.

Table 13. UART signal mapping

Signal	Maps to	Direction	Description
TXD	DATA0	I	UART TXD signal that is routed to the DM pin
RXD	DATA1	O	UART RXD signal that is routed from the DP pin
reserved	DATA2	O	reserved; the SAF1508BET will drive this pin to LOW in UART mode
INT	DATA3	O	active HIGH interrupt indication; will be asserted and latched whenever any unmasked interrupt occurs
reserved	DATA[7:4]	O	reserved; the SAF1508BET will drive these pins to LOW

Transparent UART mode is entered by setting some register bits in ULPI registers. The recommended sequence is:

1. Set the XCVRSELECT[1:0] bits in the Function Control register to 10b (low-speed) or 01b (full-speed). This setting affects the rise time and the fall time of the UART transmitting signal on the DM line.
2. Set the DP_PULLDOWN and DM_PULLDOWN bits in the OTG Control register to logic 0.
3. Set the TERMSELECT bit in the Function Control register to logic 0 (power-on default value).

   Remark: Mandatory when a full-speed driver is used and optional for a low-speed driver.

4. Set the TXD_EN and RXD_EN bits in the carkit Control register to logic 1. These two bits must be set together in one TXCMD.
5. Set the CARKIT_MODE bit in the Interface Control register to logic 1.

   Remark: The CARKIT_MODE, TXD_EN and RXD_EN bits must be set to logic 1. The sequence of setting these register bits is ignored.

After the register configuration is complete:

1. A weak pull-up resistor will be enabled on the DP and DATA0 pins. This is to avoid the possible floating condition on these input pins when UART mode is enabled.
2. The 39 Ω serial termination resistors on the DP and DM pins will be enabled.
3. One clock cycle after DIR goes from LOW to HIGH, the SAF1508BET will drive the data bus for five clock cycles. This is to charge the DATA0 pin to a HIGH level for a slow link. The link, however, can start driving DATA0 to HIGH immediately after the turnaround cycle.
4. UART buffers between DATA0 or DATA1 and DM or DP are enabled. Transparent UART mode is entered.

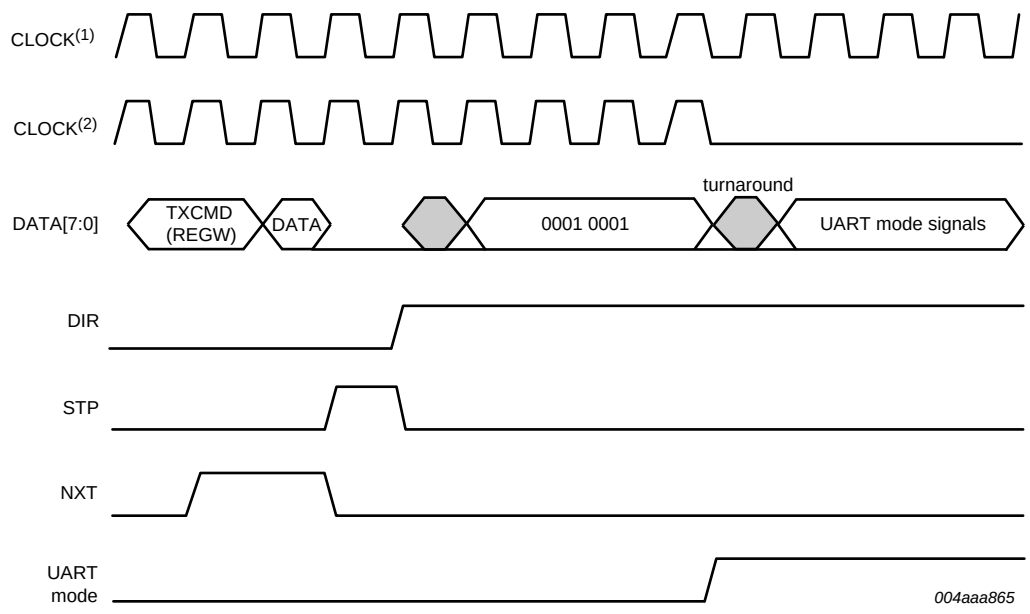
   Remark: The DP pin will be slowly charged up to HIGH by the weak pull-up resistor. The time needed depends on the capacitive loading on DP.

By default, the clock is powered down when the SAF1508BET enters UART mode. If the link requires CLOCK to be running in UART mode, it can set the CLOCK_SUSPENDM bit in the Interface Control register to logic 1 before entering UART mode.

Transparent UART mode is exited by asserting the STP pin to HIGH or by toggling the CHIP_SEL pin.

The INT pin is asserted and latched whenever an unmasked interrupt event occurs. When the link detects INT as HIGH, it must wake-up the PHY from transparent UART mode by asserting STP. When the PHY is in synchronous mode, the link can read the USB Interrupt Latch register to determine the source of the interrupt. Note that the SAF1508BET does not implement the optional carkit interrupt registers.

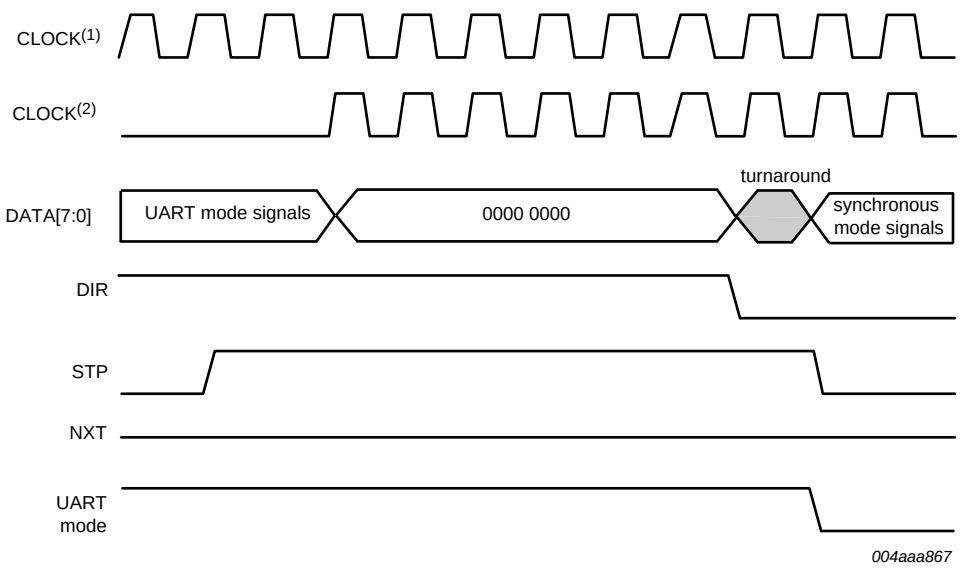
An alternative way to exit UART mode is to set the CHIP_SEL pin to non-active for more than t_{PWRDN} and then set it to active. A power-on reset will be generated and the ULPI bus will be put in default synchronous mode.



(1) Clock remains powered when the CLOCK_SUSPENDM register bit is logic 1.

(2) Clock is powered down when the CLOCK_SUSPENDM register bit is logic 0 (default).

Fig 8. Interface behavior when entering UART mode



(1) Clock remains powered when the CLOCK_SUSPENDM register bit is logic 1.

(2) Clock is powered down when the CLOCK_SUSPENDM register bit is logic 0 (default).

Fig 9. Interface behavior when exiting UART mode

9.3 USB state transitions

A Hi-Speed USB peripheral, host or OTG device handles more than one electrical state as defined in *Universal Serial Bus Specification Rev. 2.0* and *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3*. The SAF1508BET accommodates various states through register settings of the XCVRSELECT[1:0], TERMSELECT, OPMODE[1:0], DP_PULLDOWN and DM_PULLDOWN bits.

Table 14 summarizes operating states. The values of register settings in Table 14 will force resistor settings as also given in Table 14. Resistor setting signals are defined as follows:

- RPU_DP_EN enables the 1.5 kΩ pull-up resistor on DP
- RPD_DP_EN enables the 15 kΩ pull-down resistor on DP
- RPD_DM_EN enables the 15 kΩ pull-down resistor on DM
- HSTERM_EN enables the 45 Ω termination resistors on DP and DM

It is up to the link to set the desired register settings.

Table 14. Operating states and their corresponding resistor settings

Signaling mode	Register settings					Internal resistor settings			
	XCVR SELECT [1:0]	TERM SELECT	OPMODE [1:0]	DP_ PULL DOWN	DM_ PULL DOWN	RPU_DP _EN	RPD_DP _EN	RPD_ DM_EN	HSTERM_ EN
General settings									
3-state drivers	XXb	Xb	01b	Xb	Xb	0b	0b	0b	0b
Power-up or V_{BUS} < $V_{B\_SESS\_END}$	01b	0b	00b	1b	1b	0b	1b	1b	0b
Host settings									
Host chirp	00b	0b	10b	1b	1b	0b	1b	1b	1b
Host high-speed	00b	0b	00b	1b	1b	0b	1b	1b	1b
Host full-speed	X1b	1b	00b	1b	1b	0b	1b	1b	0b
Host high-speed or full-speed suspend	01b	1b	00b	1b	1b	0b	1b	1b	0b
Host high-speed or full-speed resume	01b	1b	10b	1b	1b	0b	1b	1b	0b
Host low-speed	10b	1b	00b	1b	1b	0b	1b	1b	0b
Host low-speed suspend	10b	1b	00b	1b	1b	0b	1b	1b	0b
Host low-speed resume	10b	1b	10b	1b	1b	0b	1b	1b	0b
Host Test J or Test K	00b	0b	10b	1b	1b	0b	1b	1b	1b
Peripheral settings									
Peripheral chirp	00b	1b	10b	0b	0b	1b	0b	0b	0b
Peripheral high-speed	00b	0b	00b	0b	0b	0b	0b	0b	1b
Peripheral full-speed	01b	1b	00b	0b	0b	1b	0b	0b	0b

Table 14. Operating states and their corresponding resistor settings *...continued*

Signaling mode	Register settings					Internal resistor settings			
	XCVR SELECT [1:0]	TERM SELECT	OPMODE [1:0]	DP_ PULL DOWN	DM_ PULL DOWN	RPU_DP _EN	RPD_DP _EN	RPD_ DM_EN	HSTERM_ EN
Peripheral high-speed or full-speed suspend	01b	1b	00b	0b	0b	1b	0b	0b	0b
Peripheral high-speed or full-speed resume	01b	1b	10b	0b	0b	1b	0b	0b	0b
Peripheral Test J or Test K	00b	0b	10b	0b	0b	0b	0b	0b	1b
OTG settings									
OTG device peripheral chirp	00b	1b	10b	0b	1b	1b	0b	1b	0b
OTG device peripheral high-speed	00b	0b	00b	0b	1b	0b	0b	1b	1b
OTG device peripheral full-speed	01b	1b	00b	0b	1b	1b	0b	1b	0b
OTG device peripheral high-speed and full-speed suspend	01b	1b	00b	0b	1b	1b	0b	1b	0b
OTG device peripheral high-speed and full-speed resume	01b	1b	10b	0b	1b	1b	0b	1b	0b
OTG device peripheral Test J or Test K	00b	0b	10b	0b	1b	0b	0b	1b	1b

10. Protocol description

10.1 ULPI references

The SAF1508BET provides an 8-pin or 12-pin ULPI interface to communicate with the link. It is highly recommended that users of the SAF1508BET read *UTMI+ Specification Rev. 1.0* and *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

10.2 TXCMD and RXCMD

Commands between the SAF1508BET and the link are described in the following subsections.

10.2.1 TXCMD

By default, the link must drive the ULPI bus to its idle state of 00h. To send commands and USB packets, the link drives a nonzero value on DATA[7:0] to the SAF1508BET by sending a byte called TXCMD. Commands include USB packet transmissions, and register reads and writes. Once the TXCMD is interpreted and accepted by the SAF1508BET, the NXT signal is asserted and the link can follow up with the required number of data bytes. The TXCMD byte format is given in Table 15. Any values other than those in Table 15 are illegal and will result in undefined behavior.

Various TXCMD packet and register sequences are given in later sections.

Table 15. TXCMD byte format

Command type name	Command code DATA[7:6]	Command payload DATA[5:0]	Command name	Command description
Idle	00b	00 0000b	NOOP	No operation. 00h is the idle value of the data bus. The link must drive NOOP by default.
Packet transmit	01b	00 0000b	NOPID	Transmit USB data that does not have a PID, such as chirp and resume signaling. The SAF1508BET starts transmitting only after accepting the next data byte.
		00 XXXXb	PID	Transmit USB packet. DATA[3:0] indicates USB packet identifier PID[3:0].
Register write	10b	10 1111b	EXTW	Extended register write command (optional). The 8-bit address must be provided after the command is accepted.
		XX XXXXb	REGW	Register write command with 6-bit immediate address.
Register read	11b	10 1111b	EXTR	Extended register read command (optional). The 8-bit address must be provided after the command is accepted.
		XX XXXXb	REGR	Register read command with 6-bit immediate address.

10.2.2 RXCMD

The SAF1508BET communicates status information to the link by asserting DIR and sending an RXCMD byte on the data bus. The RXCMD data byte format follows *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1* and is given in Table 16.

The SAF1508BET will automatically send an RXCMD whenever there is a change in any of the RXCMD data fields. The link must be able to accept an RXCMD at any time; including single RXCMDs, back-to-back RXCMDs, and RXCMDs at any time during USB receive packets when NXT is LOW. An example is shown in Figure 10. For details and diagrams, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

Table 16. RXCMD byte format

DATA	Name	Description and value
1 to 0	LINESTATE	**LINESTATE signals**: For a definition of LINESTATE, see Section 10.2.2.1. **DATA0 —** LINESTATE0 **DATA1 —** LINESTATE1
3 to 2	V_{BUS} state	**Encoded V_{BUS} voltage state**: For an explanation of the V_{BUS} state, see Section 10.2.2.2.
5 to 4	RxEvent	**Encoded USB event signals**: For an explanation of RxEvent, see Section 10.2.2.4.
6	ID	Reflects the value of the ID pin. Valid 50 ms after ID_PULLUP is set to logic 1.
7	ALT_INT	By default, this signal is not used and is not needed in typical designs. Optionally, the link can enable the BVALID_RISE and/or BVALID_FALL bits in the Power Control register. Corresponding changes in BVALID will cause an RXCMD to be sent to the link with the ALT_INT bit asserted.

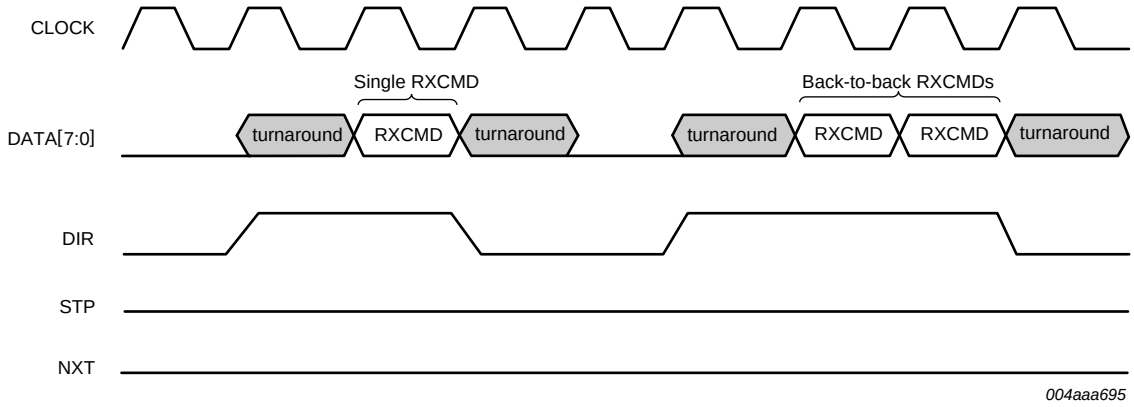


Fig 10. Single and back-to-back RXCMDs from the SAF1508BET to the link

10.2.2.1 Linestate encoding

LINESTATE[1:0] reflects the current state of DP and DM. Whenever the SAF1508BET detects a change in DP or DM, an RXCMD will be sent to the link with the new LINESTATE[1:0] value. The value given on LINESTATE[1:0] depends on the setting of various registers.

Table 17 shows the LINESTATE[1:0] encoding for upstream facing ports, which applies to peripherals. Table 18 shows the LINESTATE[1:0] encoding for downstream facing ports, which applies to host controllers. Dual-role devices must choose the correct table, depending on whether it is in peripheral or host mode.

Table 17. LINESTATE[1:0] encoding for upstream facing ports: peripheral
DP_PULLDOWN = 0.[1]

Mode		Full-speed	High-speed	Chirp
XCVRSELECT[1:0]		01, 11	00	00
TERMSELECT		1	0	1
LINESTATE[1:0]	00	SE0	squelch	squelch
	01	FS-J	!squelch	!squelch and HS_Differential_Receiver_Output
	10	FS-K	invalid	!squelch and !HS_Differential_Receiver_Output
	11	SE1	invalid	invalid

[1] !squelch indicates inactive squelch. !HS_Differential_Receiver_Output indicates inactive HS_Differential_Receiver_Output.

Table 18. LINESTATE[1:0] encoding for downstream facing ports: host
DP_PULLDOWN and DM_PULLDOWN = 1.[1]

Mode		Low-speed	Full-speed	High-speed	Chirp
XCVRSELECT[1:0]		10	01, 11	00	00
TERMSELECT		1	1	0	0
OPMODE[1:0]		X	X	00, 01 or 11	10
LINESTATE[1:0]	00	SE0	SE0	squelch	squelch
	01	LS-K	FS-J	!squelch	!squelch and HS_Differential_Receiver_Output
	10	LS-J	FS-K	invalid	!squelch and !HS_Differential_Receiver_Output
	11	SE1	SE1	invalid	invalid

[1] !squelch indicates inactive squelch. !HS_Differential_Receiver_Output indicates inactive HS_Differential_Receiver_Output.

10.2.2.2 V_{BUS} state encoding

USB devices must monitor the V_{BUS} voltage for purposes such as overcurrent detection, starting a session and SRP. The V_{BUS} state field in the RXCMD is an encoding of the voltage level on V_{BUS}.

The SESS_END and SESS_VLD indicators in the V_{BUS} state are directly taken from internal comparators built-in to the SAF1508BET, and encoded as shown in Table 16 and Table 19.

Table 19. Encoded V_{BUS} voltage state

Value	V_{BUS} voltage	SESS_END	SESS_VLD	A_VBUS_VLD
00	$V_{BUS} < V_{B\_SESS\_END}$	1	0	0
01	$V_{B\_SESS\_END} \leq V_{BUS} < V_{A\_SESS\_VLD}$	0	0	0
10	$V_{A\_SESS\_VLD} \leq V_{BUS} < V_{A\_VBUS\_VLD}$	X	1	0
11	$V_{BUS} \geq V_{A\_VBUS\_VLD}$	X	X	1

The A_VBUS_VLD indicator in the V_{BUS} state provides several options and must be configured based on current draw requirements. A_VBUS_VLD can input from one or more V_{BUS} voltage indicators, as shown in Figure 11.

A description on how to use and select the V_{BUS} state encoding is given in Section 10.2.2.3.

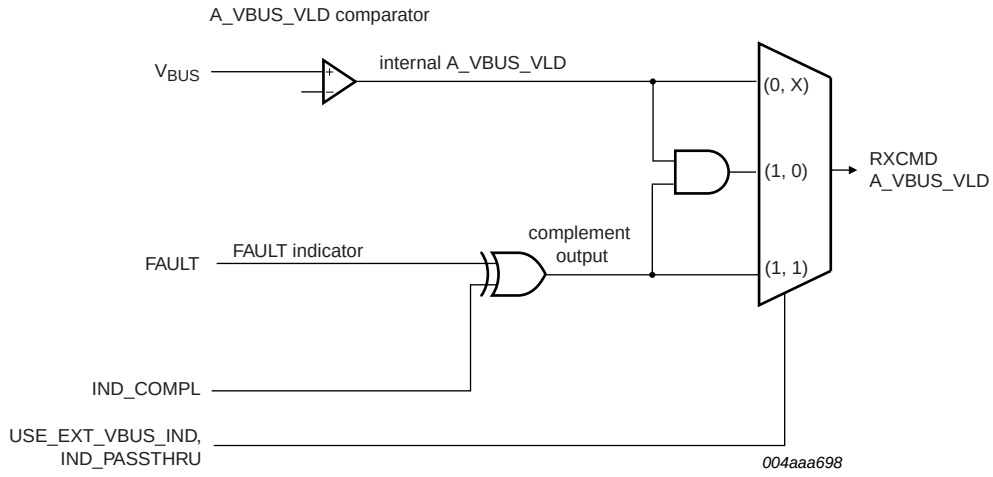


Fig 11. RXCMD A_VBUS_VLD indicator source

10.2.2.3 Using and selecting the V_{BUS} state encoding

The V_{BUS} state encoding is shown in Table 16. The SAF1508BET will send an RXCMD to the link whenever there is a change in the V_{BUS} state. To receive V_{BUS} state updates, the link must first enable the corresponding interrupts in the USB Interrupt Enable Rising and USB Interrupt Enable Falling registers.

The link can use the V_{BUS} state to monitor V_{BUS} and take appropriate action. Table 20 shows the recommended usage for typical applications.

Table 20. V_{BUS} indicators in RXCMD required for typical applications

Application	A_VBUS_VLD	SESS_VLD	SESS_END
Standard host	yes	no	no
Standard peripheral	no	yes	no
OTG A-device	yes	yes	no
OTG B-device	no	yes	yes

Standard USB host controllers: For standard hosts, the system must be able to provide 500 mA on V_{BUS} in the range of 4.75 V to 5.25 V. An external circuit must be used to detect overcurrent conditions. If the external overcurrent detector provides a digital fault signal, then the fault signal must be connected to the SAF1508BET FAULT input pin, and the link must do the following:

1. Set the IND_COMPL bit in the Interface Control register to logic 0 or logic 1, depending on the polarity of the external fault signal.
2. Set the USE_EXT_VBUS_IND bit in the OTG Control register to logic 1.
3. If it is not necessary to qualify the fault indicator with the internal A_VBUS_VLD comparator, set the IND_PASSTHRU bit in the Interface Control register to logic 1.

Standard USB peripheral controllers: Standard peripherals must be able to detect when V_{BUS} is at a sufficient level for operation. SESS_VLD must be enabled to detect the start and end of USB peripheral operations. Detection of A_VBUS_VLD and SESS_END thresholds is not needed for standard peripherals.

OTG devices: When an OTG device is configured as an OTG A-device, it must be able to provide a minimum of 8 mA on V_{BUS}. If the OTG A-device provides less than 100 mA, then there is no need for an overcurrent detection circuit because the internal A_VBUS_VLD comparator is sufficient. If the OTG A-device provides more than 100 mA on V_{BUS}, an overcurrent detector must be used and Section "Standard USB host controllers" applies. The OTG A-device also uses SESS_VLD to detect when an OTG A-device is initiating V_{BUS} pulsing SRP.

When an OTG device is configured as an OTG B-device, SESS_VLD must be used to detect when V_{BUS} is at a sufficient level for operation. SESS_END must be used to detect when V_{BUS} has dropped to a LOW level, allowing the B-device to safely initiate V_{BUS} pulsing SRP.

10.2.2.4 RxEvent encoding

The RxEvent field (see Table 21) of the RXCMD informs the link of information related packets received on the USB bus. RxActive and RxError are defined in *USB 2.0 Transceiver Macrocell Interface (UTMI) Specification Ver. 1.05*. HostDisconnect is defined in *UTMI+ Specification Rev. 1.0*. A short definition is also given in the following subsections.

Table 21. Encoded USB event signals

Value	RxActive	RxError	HostDisconnect
00	0	0	0
01	1	0	0
11	1	1	0
10	X	X	1

RxActive: When the SAF1508BET has detected a SYNC pattern on the USB bus, it signals an RxActive event to the link. An RxActive event can be communicated using two methods. The first method is for the SAF1508BET to simultaneously assert DIR and NXT. The second method is for the SAF1508BET to send an RXCMD to the link with the RxActive field in the RxEvent bits set to logic 1. The link must be capable of detecting both methods. RxActive frames the receive packet from the first byte to the last byte.

The link must assume that RxActive is set to logic 0 when indicated in an RXCMD or when DIR is deasserted, whichever occurs first.

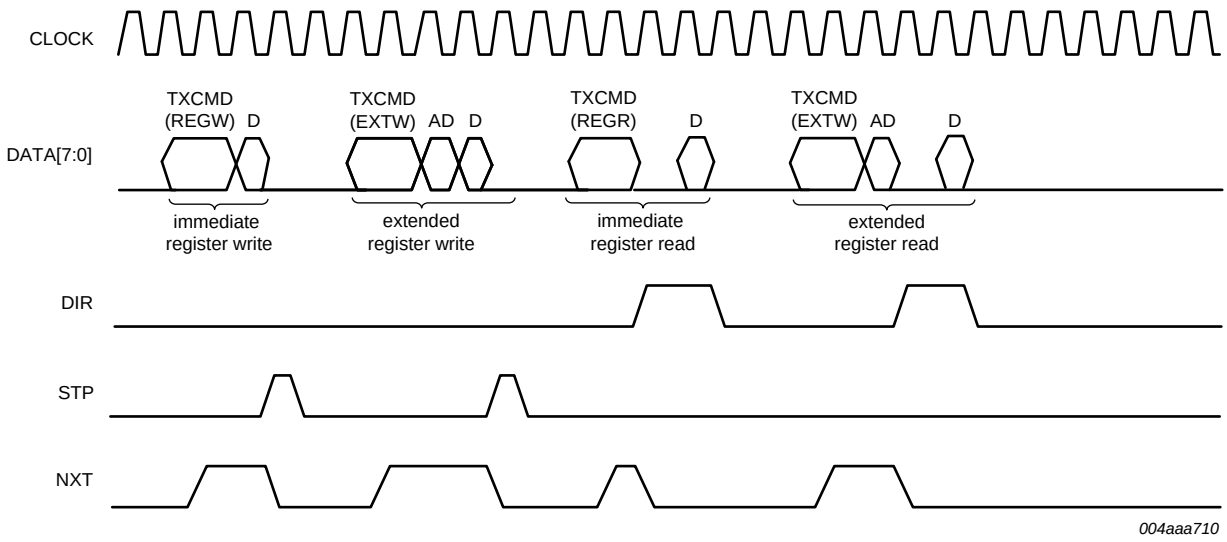
The link uses RxActive to time high-speed packets and ensure that bus turnaround times are met. For more information on the USB packet timing, see Section 10.5.1.

RxError: When the SAF1508BET has detected an error while receiving a USB packet, it deasserts NXT and sends an RXCMD with the RxError field set to logic 1. The received packet is no longer valid and must be dropped by the link.

HostDisconnect: HostDisconnect is encoded into the RxEvent field of the RXCMD. HostDisconnect is valid only when the SAF1508BET is configured as a host (both DP_PULLDOWN and DM_PULLDOWN are set to logic 1), and indicates to the host controller when a peripheral is connected (0b) or disconnected (1b). The host controller must enable HostDisconnect by setting the HOST_DISCON_R and HOST_DISCON_F bits in the USB Interrupt Enable Rising and USB Interrupt Enable Falling registers, respectively. Changes in HostDisconnect will cause the PHY to send an RXCMD to the link with the updated value.

10.3 Register read and write operations

Figure 12 shows register read and write sequences. The SAF1508BET supports immediate addressing and extended addressing register operations. Extended register addressing is optional for links. Note that register operations will be aborted if the SAF1508BET asserts DIR during the operation. When a register operation is aborted, the link must retry until successful. For more information on register operations, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.



AD indicates the address byte, and D indicates the data byte.

Fig 12. Example of register write, register read, extended register write and extended register read

10.4 USB reset and high-speed detection handshake (chirp)

Figure 13 shows the sequence of events for USB reset and high-speed detection handshake (chirp). The sequence is shown for hosts and peripherals. Figure 13 does not show all RXCMD updates, and timing is not to scale. The sequence is as follows:

1. USB reset: The host detects a peripheral attachment as low-speed if DM is HIGH and as full-speed if DP is HIGH. If a host detects a low-speed peripheral, it does not follow the remainder of this protocol. If a host detects a full-speed peripheral, it resets the peripheral by writing to the Function Control register and setting XCVRSELECT[1:0] = 00b (high-speed) and TERMSELECT = 0b that drives SE0 on the bus (DP and DM connected to ground through 45 Ω). The host also sets OPMODE[1:0] = 10b for correct chirp transmit and receive. The start of SE0 is labeled T_0.

   Remark: To receive chirp signaling, the host must also consider the high-speed differential receiver output. The host controller must interpret LINESTATE as shown in Table 18.

2. High-speed detection handshake (chirp)

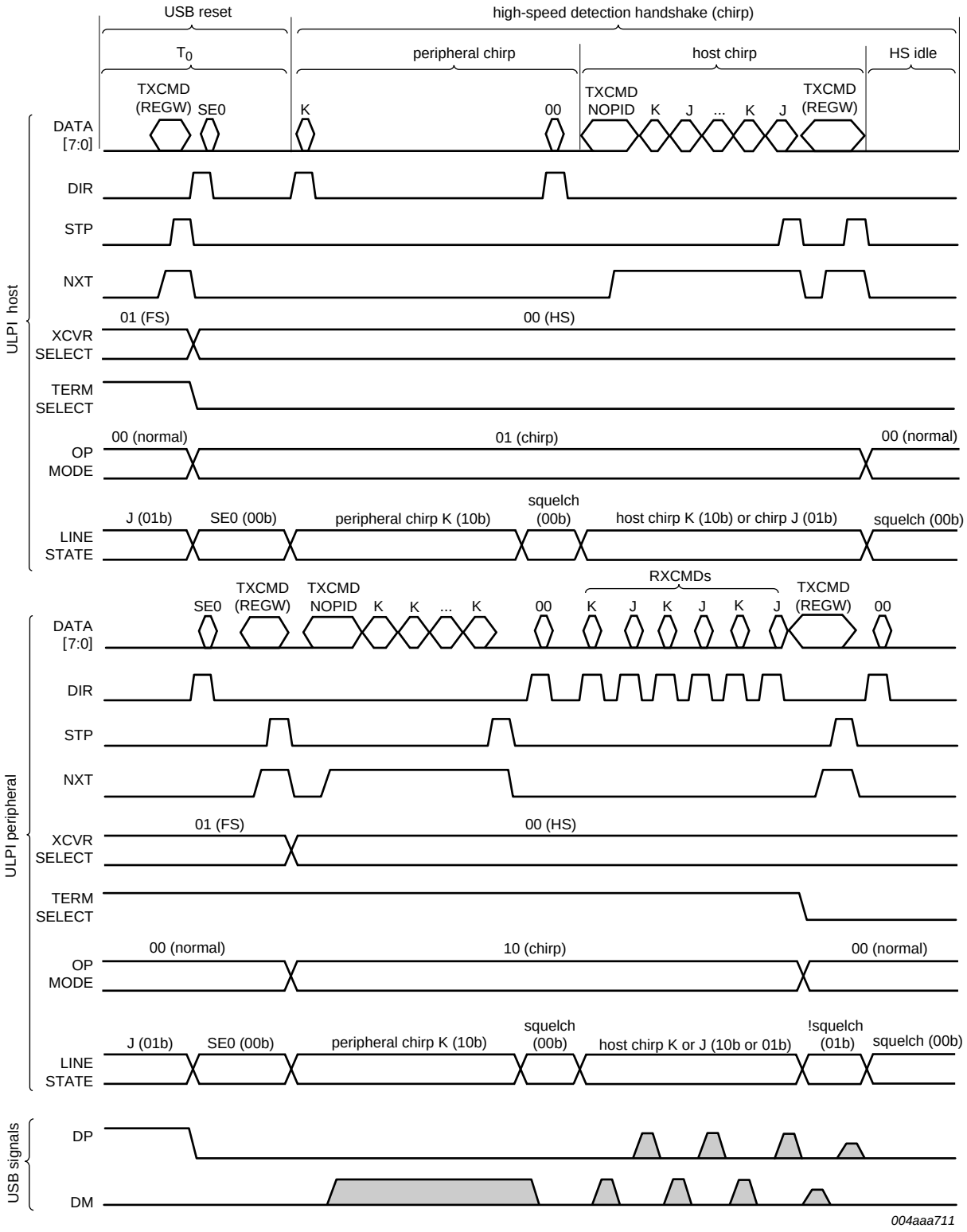
   a. Peripheral chirp: After detecting SE0 for no less than 2.5 μs, if the peripheral is capable of high-speed, it sets XCVRSELECT[1:0] to 00b (high-speed) and OPMODE[1:0] to 10b (chirp). The peripheral immediately follows this with a TXCMD (NOPID), transmitting a Chirp K for no less than 1 ms and ending no more

than 7 ms after reset time T_0. If the peripheral is in low-power mode, it must wake up its clock within 5.6 ms, leaving 200 μs for the link to start transmitting the Chirp K, and 1.2 ms for the Chirp K to complete (worst case with 10 % slow clock).

b. Host chirp: If the host does not detect the peripheral chirp, it must continue asserting SE0 until the end of reset. If the host detects the peripheral Chirp K for no less than 2.5 μs, then no more than 100 μs after the bus leaves the Chirp K state, the host sends a TXCMD (NOPID) with an alternating sequence of Chirp Ks and Js. Each Chirp K or Chirp J must last no less than 40 μs and no longer than 60 μs.

c. High-speed idle: The peripheral must detect a minimum of Chirp K-J-K-J-K-J. Each Chirp K and Chirp J must be detected for at least 2.5 μs. After seeing that minimum sequence, the peripheral sets TERMSELECT = 0b and OPMODE[1:0] = 00b. The peripheral is now in high-speed mode and sees !squelch (01b on LINESTATE). When the peripheral sees squelch (10b on LINESTATE), it knows that the host has completed chirp and waits for Hi-Speed USB traffic to begin. After transmitting the chirp sequence, the host changes OPMODE[1:0] to 00b and begins sending USB packets.

For more information, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.



Timing is not to scale.

Fig 13. USB reset and high-speed detection handshake (chirp) sequence

10.5 USB packet transmit and receive

An example of a packet transmit and receive is shown in Figure 14. For details on USB packets, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

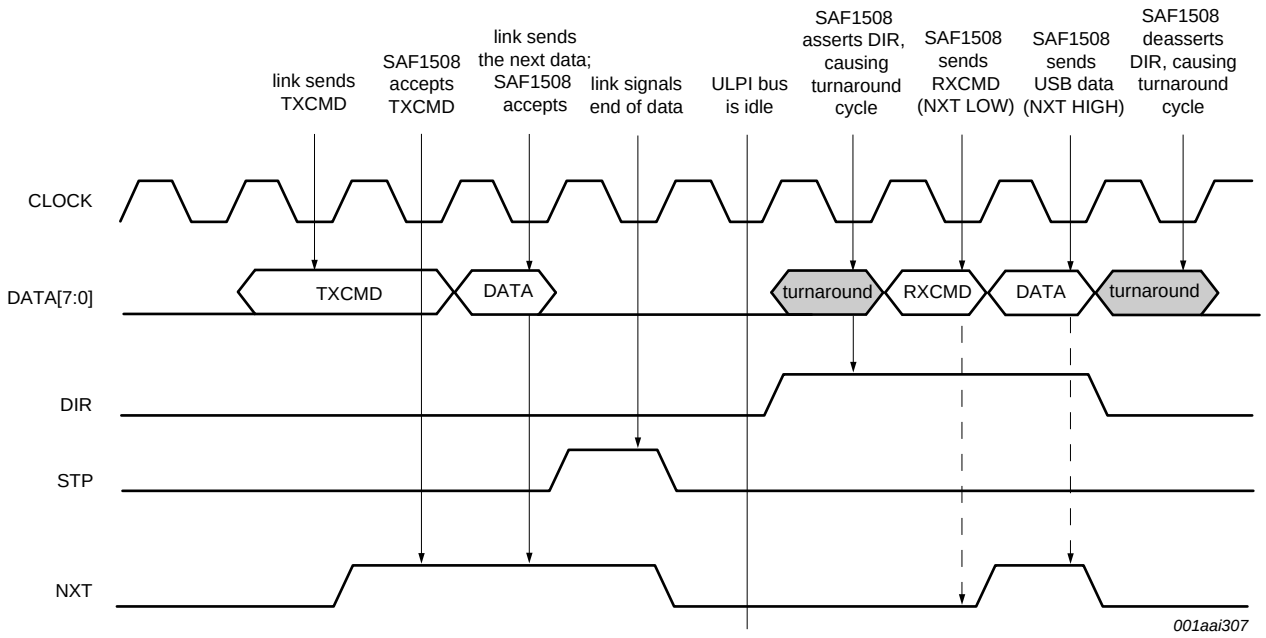


Fig 14. Example of using the SAF1508BET to transmit and receive USB data

10.5.1 USB packet timing

10.5.1.1 SAF1508BET pipeline delays

The SAF1508BET delays are shown in Table 22. For detailed description, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1, Section 3.8.2.6.2*.

Table 22. PHY pipeline delays

Parameter name	High-speed PHY delay	Full-speed PHY delay	Low-speed PHY delay
RXCMD delay (J and K)	4	4	4
RXCMD delay (SE0)	4	4 to 6	16 to 18
TX start delay	1 to 2	6 to 10	74 to 75
TX end delay (packets)	3 to 4	not applicable	not applicable
TX end delay (SOF)	6 to 9	not applicable	not applicable
RX start delay	5 to 6	not applicable	not applicable
RX end delay	5 to 6	17 to 18	122 to 123

10.5.1.2 Allowed link decision time

The amount of clock cycles allocated to the link to respond to a received packet and correctly receive back-to-back packets is given in Table 23. Link designs must follow the values given in Table 23 for correct USB system operation. Examples of high-speed packet sequences and timing are shown in Figure 15 and Figure 16. For details, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1, Section 3.8.2.6.3*.

Table 23. Link decision times

Packet sequence	High-speed link delay	Full-speed link delay	Low-speed link delay	Definition
Transmit-Transmit (host only)	15 to 24	7 to 18	77 to 247	Number of clock cycles a host link must wait before driving the TXCMD for the second packet. In high-speed, the link starts counting from the assertion of STP for the first packet. In full-speed, the link starts counting from the RXCMD, indicating LINESTATE has changed from SE0 to J for the first packet. The timing given ensures inter-packet delays of 2 bit times to 6.5 bit times.
Receive-Transmit (host or peripheral)	1 to 14	7 to 18	77 to 247	Number of clock cycles the link must wait before driving the TXCMD for the transmit packet. In high-speed, the link starts counting from the end of the receive packet; deassertion of DIR or an RXCMD, indicating RxActive is LOW. In full-speed or low-speed, the link starts counting from the RXCMD, indicating LINESTATE has changed from SE0 to J for the receive packet. The timing given ensures inter-packet delays of 2 bit times to 6.5 bit times.
Receive-Receive (peripheral only)	1	1	1	Minimum number of clock cycles between consecutive receive packets. The link must be capable of receiving both packets.
Transmit-Receive (host or peripheral)	92	80	718	Host or peripheral transmits a packet and will time-out after this amount of clock cycles if a response is not received. Any subsequent transmission can occur after this time.

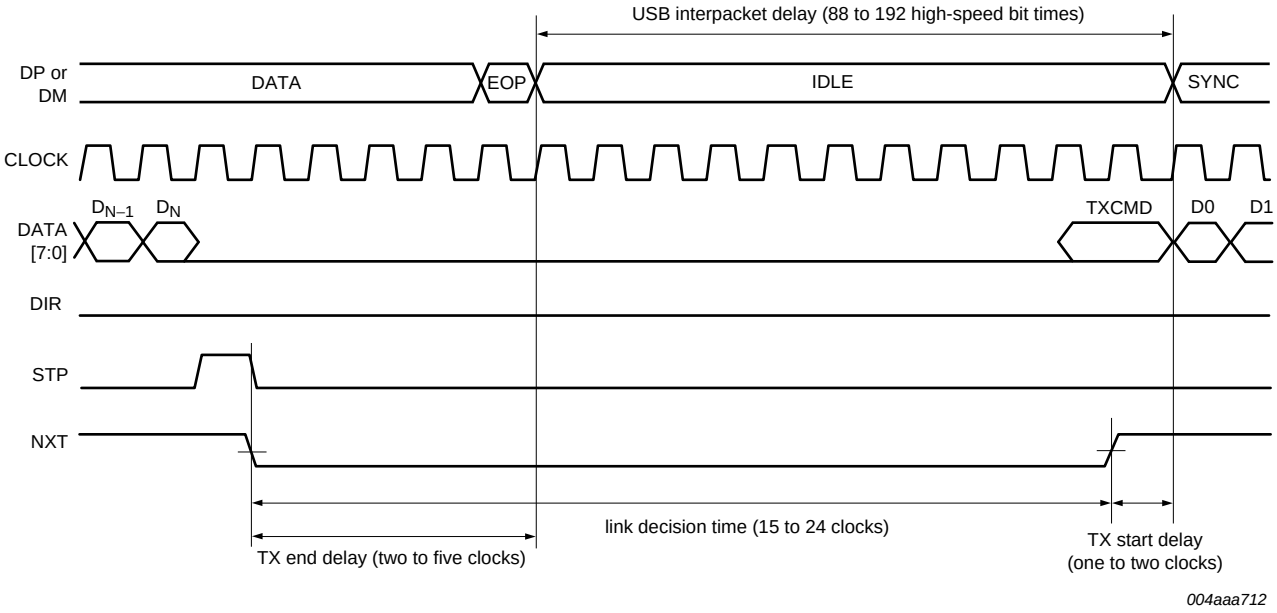


Fig 15. High-speed transmit-to-transmit packet timing

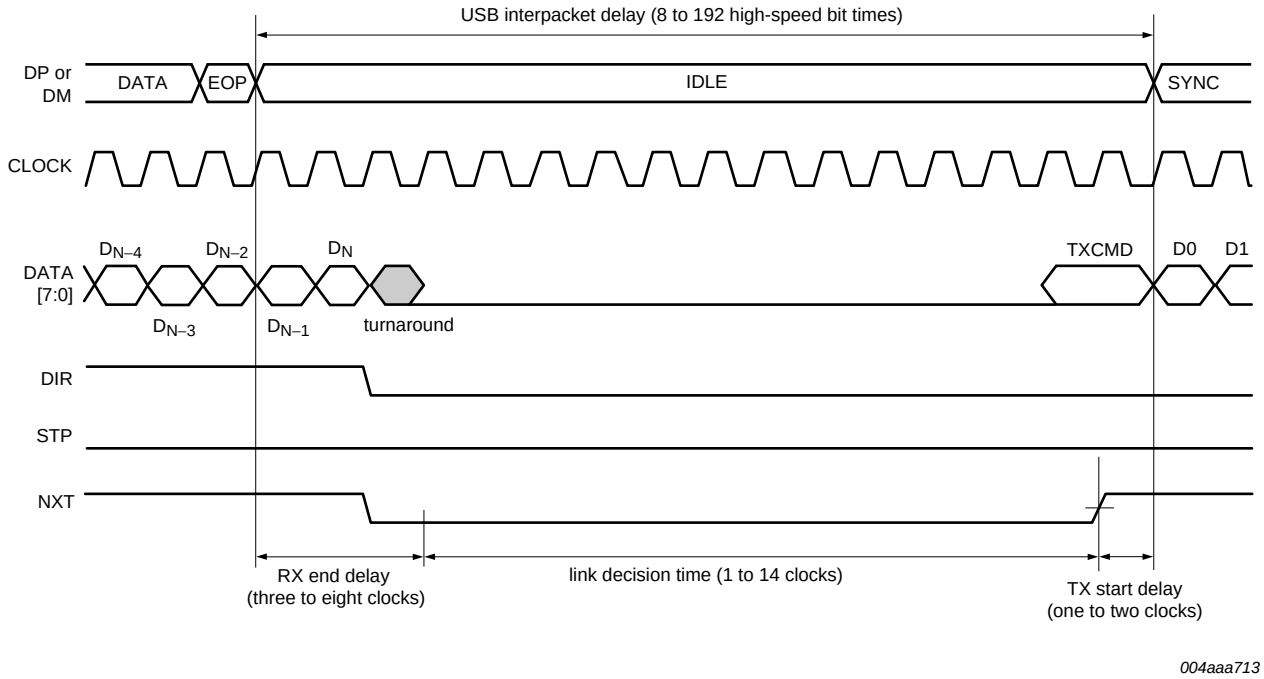
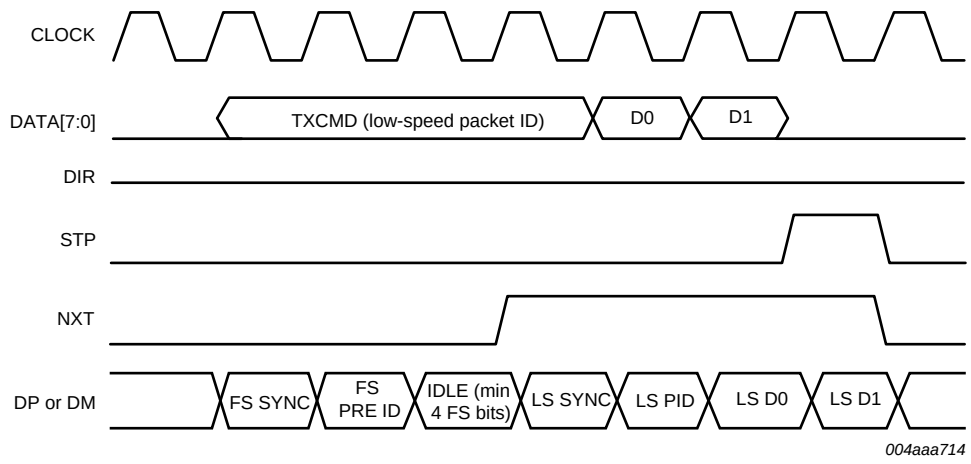


Fig 16. High-speed receive-to-transmit packet timing

10.6 Preamble

Preamble packets are headers to low-speed packets that must travel over a full-speed bus, between a host and a hub. To enter preamble mode, the link sets XCVRSELECT[1:0] = 11b in the Function Control register. When in preamble mode, the SAF1508BET operates just as in full-speed mode, and sends all data with the full-speed rise time and fall time. Whenever the link transmits a USB packet in preamble mode, the SAF1508BET will automatically send a preamble header at full-speed bit rate before sending the link packet at low-speed bit rate. The SAF1508BET will ensure a minimum gap of four full-speed bit times between the last bit of the full-speed PRE PID and the first bit of the low-speed packet SYNC. The SAF1508BET will drive a J for at least one full-speed bit time after sending the PRE PID, after which the pull-up resistor can hold the J state on the bus. An example transmit packet is shown in Figure 17.

In preamble mode, the SAF1508BET can also receive low-speed packets from the full-speed bus.



DP and DM timing is not to scale.

Fig 17. Preamble sequence

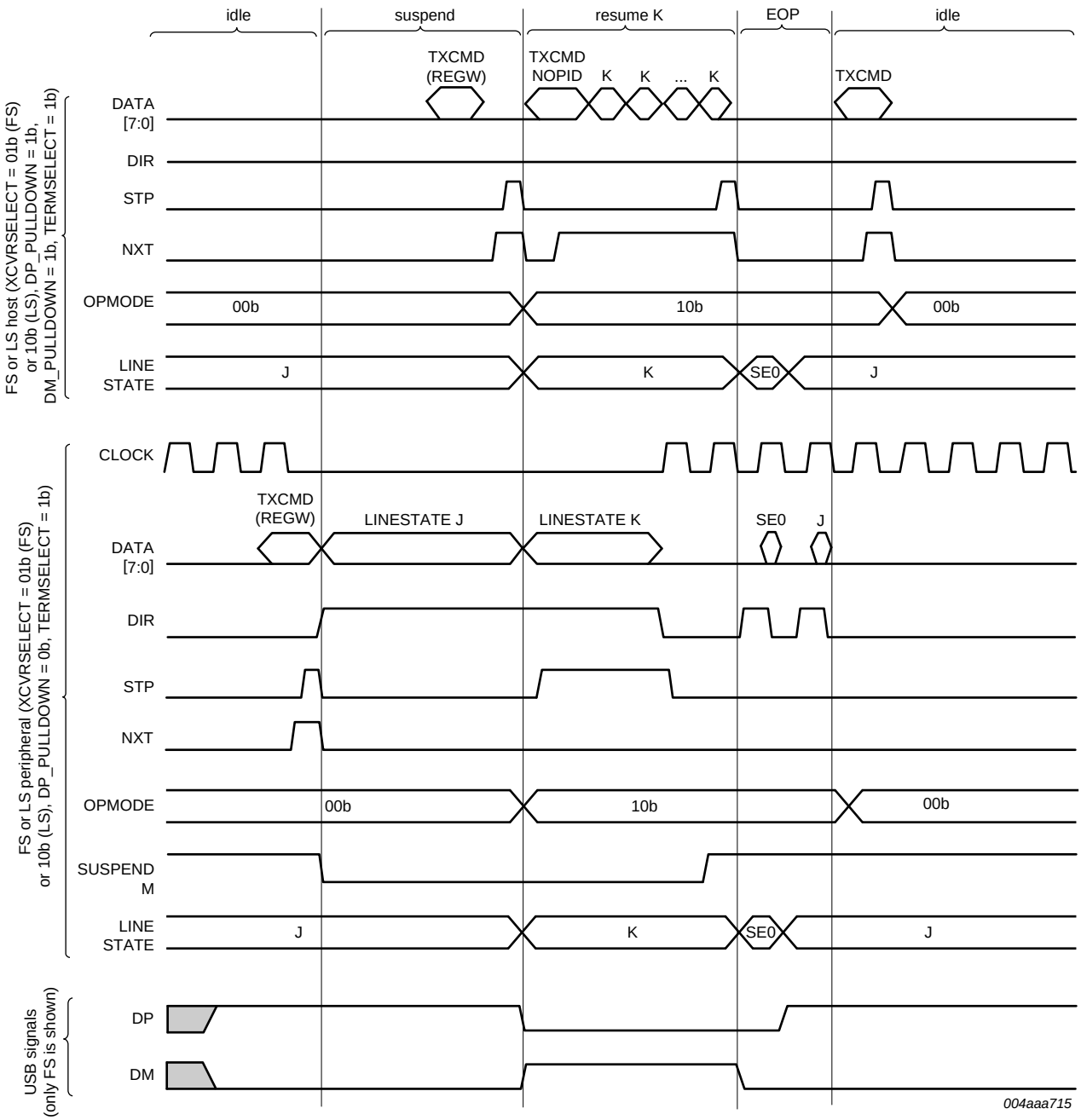
10.7 USB suspend and resume

10.7.1 Full-speed or low-speed host-initiated suspend and resume

Figure 18 illustrates how a host or a hub places a full-speed or low-speed peripheral into suspend and sometime later initiates resume signaling to wake-up the downstream peripheral. Note that Figure 18 timing is not to scale, and does not show all RXCMD LINESTATE updates.

The sequence of events for a host and a peripheral, both with SAF1508BET, is as follows:

1. Idle: Initially, the host and the peripheral are idle. The host has its 15 kΩ pull-down resistors enabled (DP_PULLDOWN and DM_PULLDOWN are set to 1b) and 45 Ω terminations disabled (TERMSELECT is set to 1b). The peripheral has the 1.5 kΩ pull-up resistor connected to DP for full-speed or DM for low-speed (TERMSELECT is set to 1b).
2. Suspend: When the peripheral sees no bus activity for 3 ms, it enters the suspend state. The peripheral link places the PHY into low-power mode by clearing the SUSPENDM bit in the Function Control register, causing the PHY to draw only suspend current. The host may or may not be powered down.
3. Resume K: When the host wants to wake up the peripheral, it sets OPMODE[1:0] to 10b and transmits a K for at least 20 ms. The peripheral link sees the resume K on LINESTATE, and asserts STP to wake up the PHY.
4. EOP: When STP is asserted, the SAF1508BET on the host side automatically appends an EOP of two bits of SE0 at low-speed bit rate followed by one bit of J. The SAF1508BET on the host side knows to add the EOP because DP_PULLDOWN and DM_PULLDOWN are set to 1b for a host. After the EOP is completed, the host link sets OPMODE[1:0] to 00b for normal operation. The peripheral link sees the EOP and also resumes normal operation.



Timing is not to scale.

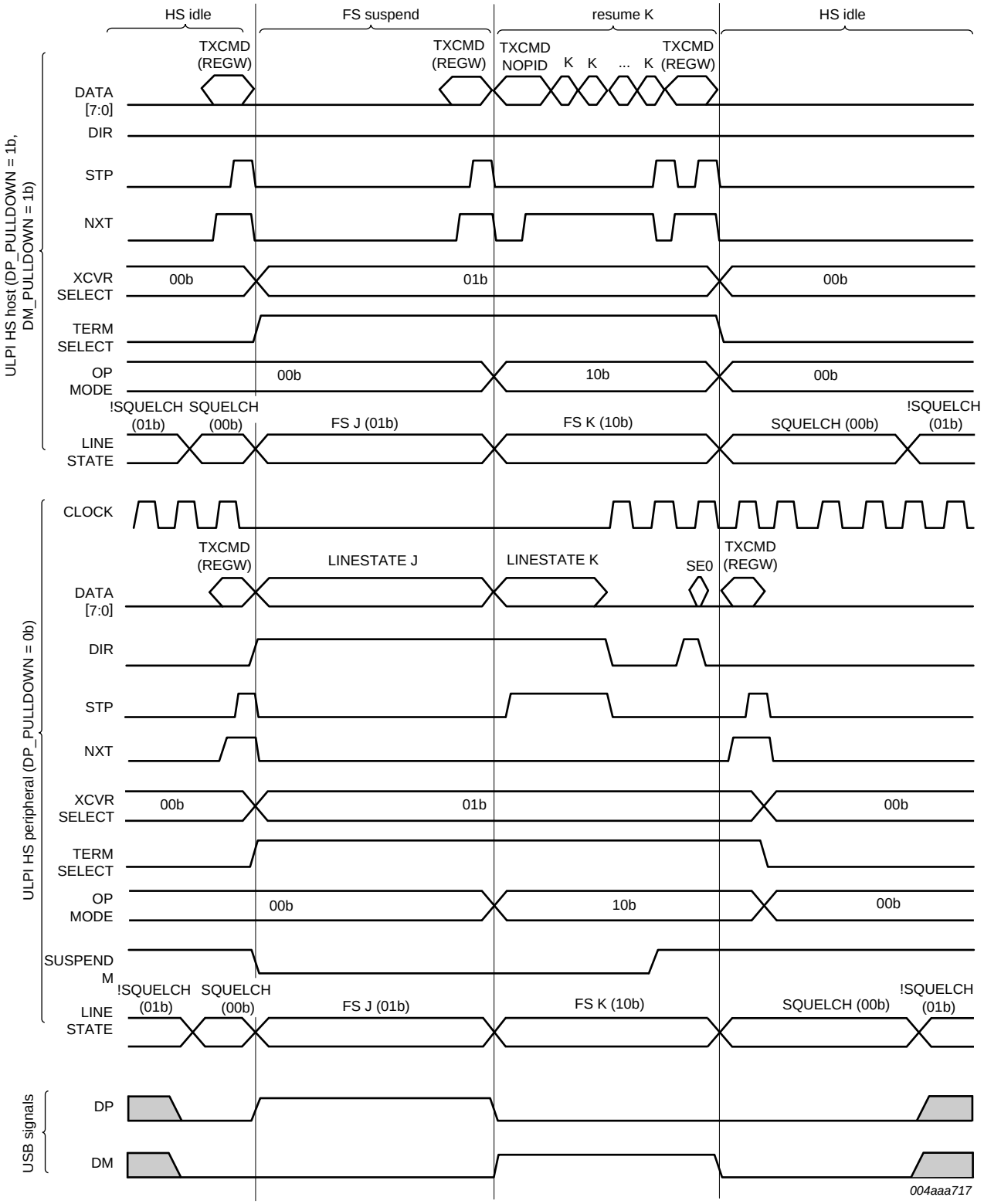
Fig 18. Full-speed suspend and resume

10.7.2 High-speed suspend and resume

Figure 19 illustrates how a host or a hub places a high-speed enabled peripheral into suspend and then initiates resume signaling. The high-speed peripheral will wake up and return to high-speed operations. Note that Figure 19 timing is not to scale, and does not show all RXCMD LINESTATE updates.

The sequence of events related to a host and a peripheral, both with SAF1508BET, is as follows.

1. High-speed idle: Initially, the host and the peripheral are idle. The host has its 15 kΩ pull-down resistors enabled (DP_PULLDOWN and DM_PULLDOWN are set to 1b) and 45 Ω terminations enabled (TERMSELECT is set to 0b). The peripheral has its 45 Ω terminations enabled (TERMSELECT is set to 0b).
2. Full-speed suspend: When the peripheral sees no bus activity for 3 ms, it enters the suspend state. The peripheral link places the SAF1508BET into full-speed mode (XCVRSELECT is set to 01b), removes 45 Ω terminations, and enables the 1.5 kΩ pull-up resistor on DP (TERMSELECT is set to 1b). The peripheral link then places the SAF1508BET into low-power mode by setting SUSPENDM, causing the SAF1508BET to draw only suspend current. The host also changes the SAF1508BET to full-speed (XCVRSELECT is set to 01b), removes 45 Ω terminations (TERMSELECT is set to 1b), and then may or may not be powered down.
3. Resume K: When the host wants to wake up the peripheral, it sets OPMODE to 10b and transmits a full-speed K for at least 20 ms. The peripheral link sees the resume K (10b) on LINESTATE, and asserts STP to wake up the SAF1508BET.
4. High-speed traffic: The host link sets high-speed (XCVRSELECT is set to 00b), and enables its 45 Ω terminations (TERMSELECT is set to 0b). The peripheral link sees SE0 on LINESTATE and also sets high-speed (XCVRSELECT is set to 00b), and enables its 45 Ω terminations (TERMSELECT is set to 0b). The host link sets OPMODE to 00b for normal high-speed operation.



Timing is not to scale.

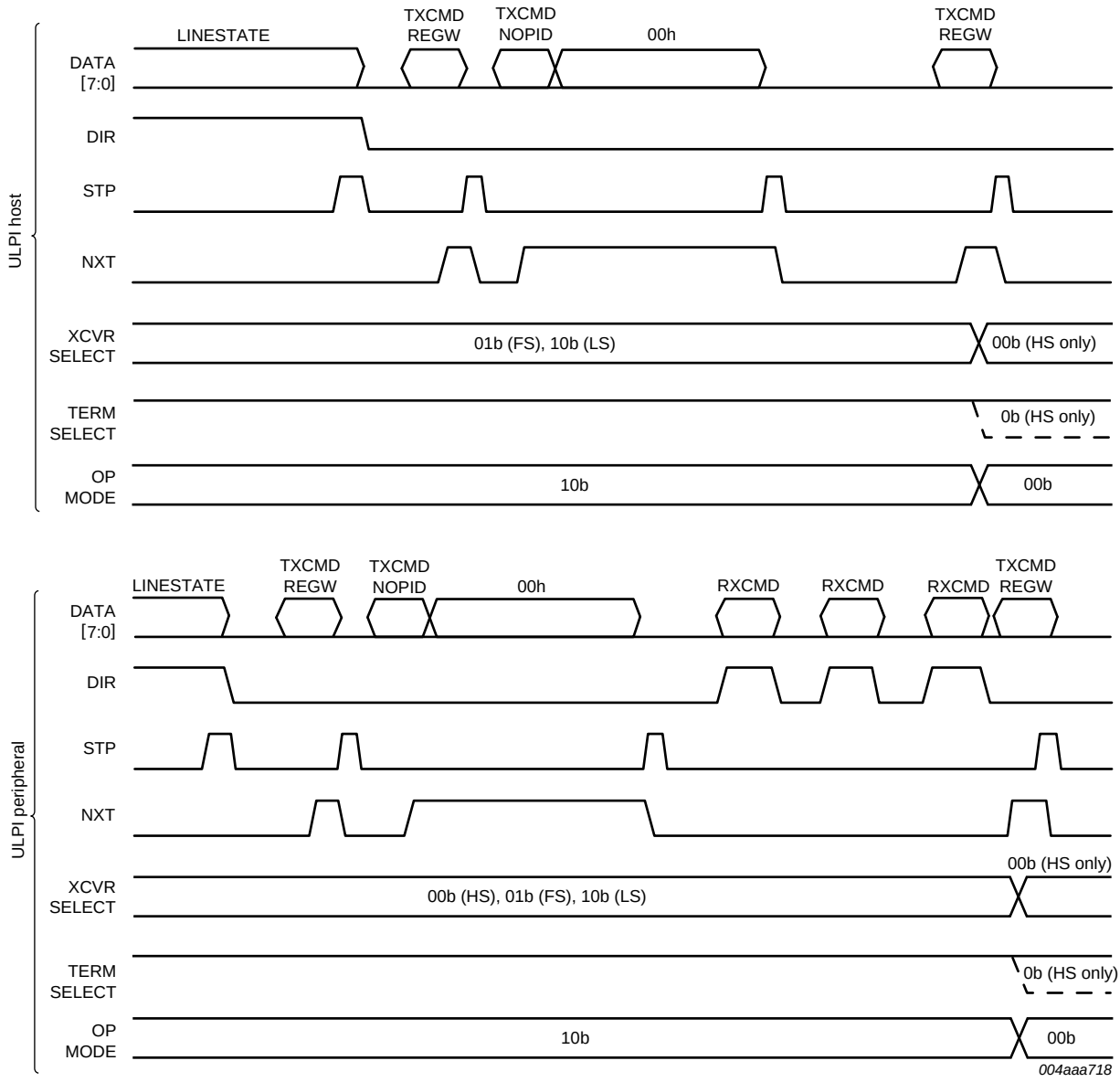
Fig 19. High-speed suspend and resume

10.7.3 Remote wake-up

The SAF1508BET supports peripherals that initiate remote wake-up resume. When placed into USB suspend, the peripheral link remembers at what speed it was originally operating. Depending on the original speed, the link follows one of the protocols detailed here. In Figure 20, timing is not to scale, and not all RXCMD LINESTATE updates are shown.

The sequence of events related to a host and a peripheral, both with SAF1508BET, is as follows:

1. Both the host and the peripheral are assumed to be in low-power mode.
2. The peripheral begins remote wake-up by re-enabling its clock and setting its SUSPENDM bit to 1b.
3. The peripheral begins driving K on the bus to signal resume. Note that the peripheral link must assume that LINESTATE is K (01b) while transmitting because it will not receive any RXCMDs.
4. The host recognizes the resume, re-enables its clock and sets its SUSPENDM bit.
5. The host takes over resume driving within 1 ms of detecting the remote wake-up.
6. The peripheral stops driving resume.
7. The peripheral sees the host continuing to drive the resume.
8. The host stops driving resume and the SAF1508BET automatically adds the EOP to the end of the resume. The peripheral recognizes the EOP as the end of resume.
9. Both the host and the peripheral revert to normal operation by writing 00b to OPMODE. If the host or the peripheral was previously in high-speed mode, it must revert to high-speed before the SE0 of the EOP is completed. This can be achieved by writing XCVRSELECT[1:0] = 00b and TERMSELECT = 0b after LINESTATE indicates SE0.



Timing is not to scale.

Fig 20. Remote wake-up from low-power mode

10.8 No automatic SYNC and EOP generation (optional)

This setting allows the link to turn off the automatic SYNC and EOP generation, and must be used for high-speed packets only. It is provided for backward compatibility with legacy controllers that include SYNC and EOP bytes in the data payload when transmitting packets. The SAF1508BET will not automatically generate SYNC and EOP patterns when OPMODE[1:0] is set to 11b. The SAF1508BET will still NRZI encode data and perform bit stuffing. An example of a sequence is shown in Figure 21. The link must always send packets using the TXCMD (NOPID) type. The SAF1508BET does not provide a mechanism to control bit stuffing in individual bytes, but will automatically turn off bit stuffing for EOP when STP is asserted with data set to FEh. If data is set to 00h when STP

is asserted, the PHY will not transmit any EOP. The SAF1508BET will also detect if the PID byte is A5h, indicating an SOF packet, and automatically send a long EOP when STP is asserted. To transmit chirp and resume signaling, the link must set OPMODE to 10b.

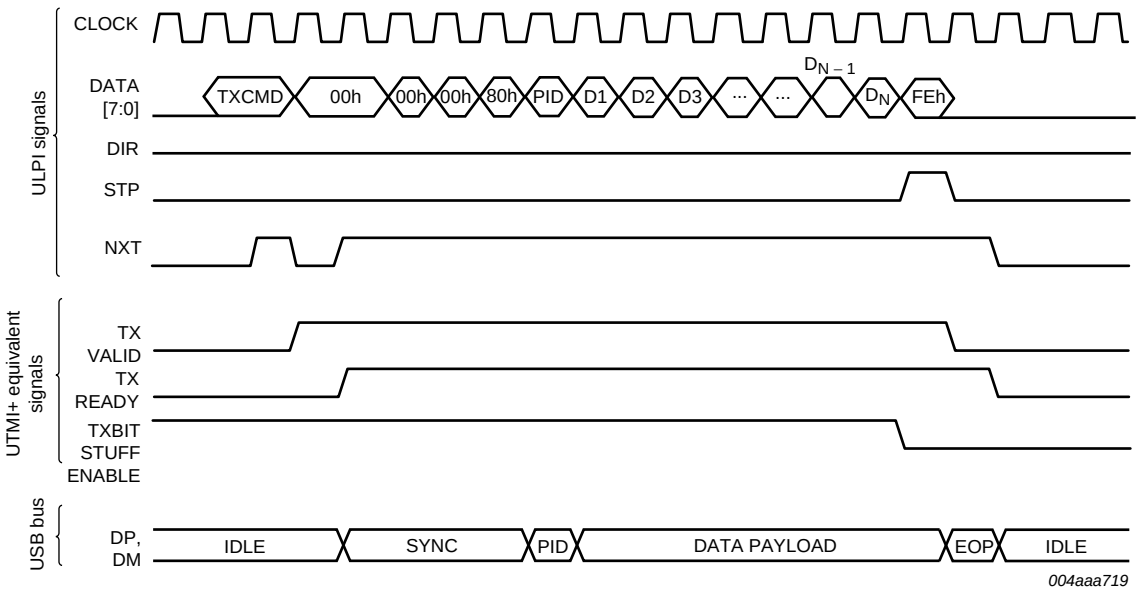


Fig 21. Transmitting USB packets without automatic SYNC and EOP generation

10.9 On-The-Go operations

On-The-Go (OTG) is a supplement to *Universal Serial Bus Specification Rev. 2.0* that allows a portable USB device to assume the role of a limited USB host by defining improvements, such as a small connector and low power. Non-portable devices, such as standard hosts and embedded hosts, can also benefit from OTG features.

The SAF1508BET OTG PHY is designed to support all the tasks specified in the OTG supplement. The SAF1508BET provides the front end analog support for Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for dual-role devices. The supporting components include:

- Voltage comparators
  - A_VBUS_VLD
  - SESS_VLD (session valid, can be used for both A-session and B-session valid)
  - SESS_END (session end)
- Pull-up and pull-down resistors on DP and DM
- ID detector indicates if micro-A or micro-B plug is inserted
- Charge and discharge resistors on V_{BUS}

The following subsections describe how to use the SAF1508BET OTG components.

10.9.1 OTG comparators

The SAF1508BET provides comparators that conform to *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3* requirements of $V_{A\_VBUS\_VLD}$, $V_{A\_SESS\_VLD}$, $V_{B\_SESS\_VLD}$ and $V_{B\_SESS\_END}$. In this data sheet, $V_{A\_SESS\_VLD}$ and $V_{B\_SESS\_VLD}$ are combined into $V_{A\_SESS\_VLD}$. Comparators are described in Section 8.7.2. Changes in comparator values are communicated to the link by RXCMDs as described in Section 10.2.2.2. Control over comparators is described in Section 11.5 to Section 11.8.

10.9.2 Pull-up and pull-down resistors

The USB resistors on DP and DM can be used to initiate data-line pulsing SRP. The link must set the required bus state using the mode settings in Table 14.

10.9.3 ID detection

The SAF1508BET provides an internal pull-up resistor to sense the value of the ID pin. The pull-up resistor must first be enabled by setting the ID_PULLUP register bit to logic 1. If the value on ID has changed, the SAF1508BET will send an RXCMD or interrupt to the link by time t_{ID}. If the link does not receive any RXCMD or interrupt by t_{ID}, then the ID value has not changed.

10.9.4 V_{BUS} charge and discharge resistors

A pull-up resistor, $R_{UP(VBUS)}$, is provided to perform V_{BUS} pulsing SRP. A B-device is allowed to charge V_{BUS} above the session valid threshold to request the host to turn on the V_{BUS} power.

A pull-down resistor, $R_{DN(VBUS)}$, is provided for a B-device to discharge V_{BUS}. This is done whenever the A-device turns off the V_{BUS} power; the B-device can use the pull-down resistor to ensure V_{BUS} is below $V_{B\_SESS\_END}$ before starting a session.

For details, refer to *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3*.

10.10 Serial modes

The SAF1508BET supports both 6-pin serial mode and 3-pin serial mode, controlled by bits 6PIN_FSLS_SERIAL and 3PIN_FSLS_SERIAL of the Interface Control register. For details, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1, Section 3.10*.

Figure 22 and Figure 23 provide example of 6-pin serial mode and 3-pin serial mode, respectively.

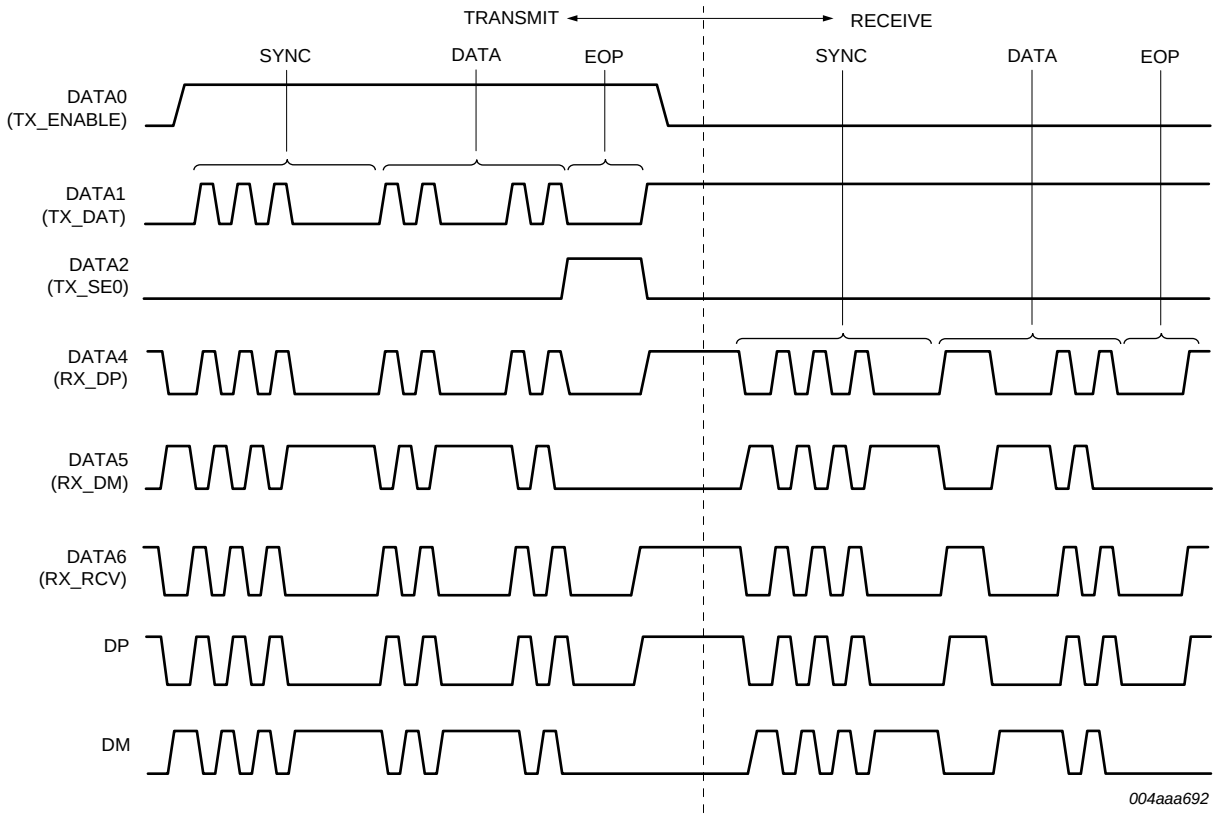


Fig 22. Example of transmit followed by receive in 6-pin serial mode

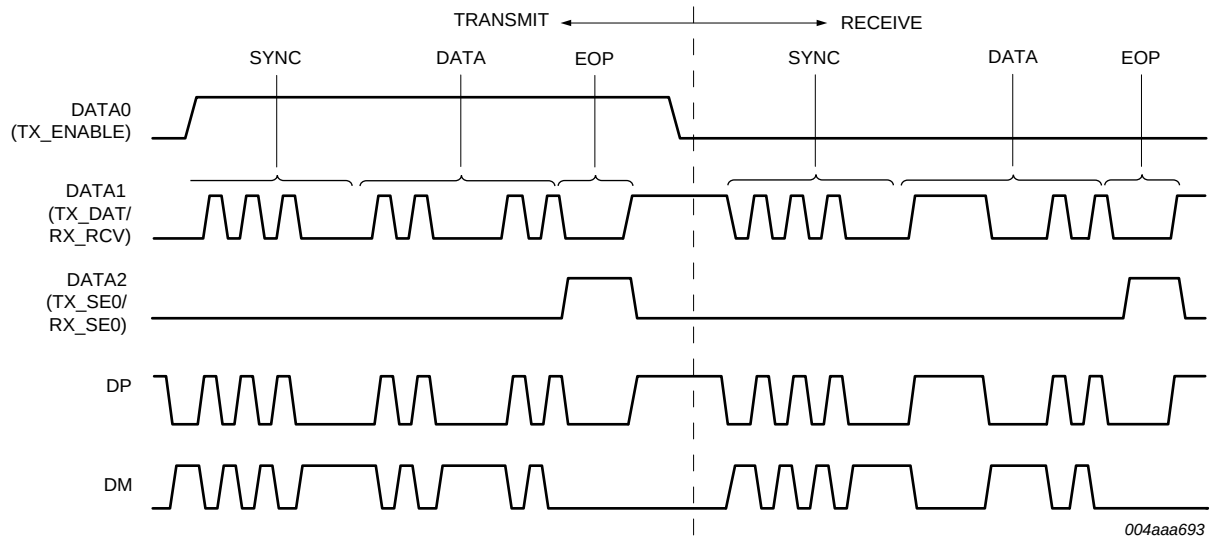


Fig 23. Example of transmit followed by receive in 3-pin serial mode

10.11 Aborting transfers

The SAF1508BET supports aborting transfers on the ULPI bus. For details, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1, Section 3.8.4.*

10.12 Avoiding contention on the ULPI data bus

Because the ULPI data bus is bidirectional, avoid situations in which both the link and the PHY simultaneously drive the data bus.

The following points must be considered while implementing the data bus drive control on the link.

After power-up and clock stabilization, default states are as follows:

- The SAF1508BET drives DIR to LOW.
- The data bus is input to the SAF1508BET.
- The ULPI link data bus is output, with all data bus lines driven to LOW.

When the SAF1508BET wants to take control of the data bus to initiate a data transfer, it changes the DIR value from LOW to HIGH.

At this point, the link must disable its output buffers. This must be as fast as possible so the link must use a combinational path from DIR.

The SAF1508BET will not immediately enable its output buffers, but will delay the enabling of its buffers until the next clock edge, avoiding bus contention.

When the data transfer is no longer required by the SAF1508BET, it changes DIR from HIGH to LOW and starts to immediately turn off its output drivers. The link senses the change of DIR from HIGH to LOW, but delays enabling its output buffers for one CLOCK cycle, avoiding data bus contention.

11. Register map

Table 24. Register map

Field name	Size (bit)	Address (6 bit)				References
		R[1]	W[2]	S[3]	C[4]	
Vendor ID Low	8	00h	-	-	-	Section 11.1.1
Vendor ID High	8	01h	-	-	-	Section 11.1.2
Product ID Low	8	02h	-	-	-	Section 11.1.3
Product ID High	8	03h	-	-	-	Section 11.1.4
Function Control	8	04h to 06h	04h	05h	06h	Section 11.2
Interface Control	8	07h to 09h	07h	08h	09h	Section 11.3
OTG Control	8	0Ah to 0Ch	0Ah	0Bh	0Ch	Section 11.4
USB Interrupt Enable Rising	8	0Dh to 0Fh	0Dh	0Eh	0Fh	Section 11.5
USB Interrupt Enable Falling	8	10h to 12h	10h	11h	12h	Section 11.6
USB Interrupt Status	8	13h	-	-	-	Section 11.7
USB Interrupt Latch	8	14h	-	-	-	Section 11.8
Debug	8	15h	-	-	-	Section 11.9
Scratch	8	16h to 18h	16h	17h	18h	Section 11.10
Carkit Control	8	19h to 1Bh	19h	1Ah	1Bh	Section 11.11
reserved	8	1Ch to 3Ch				-
Power Control	8	3Dh to 3Fh	3Dh	3Eh	3Fh	Section 11.12

[1] Read (R): A register can be read. Read-only if this is the only mode given.

[2] Write (W): The pattern on the data bus will be written over all bits of a register.

[3] Set (S): The pattern on the data bus is OR-ed with and written to a register.

[4] Clear (C): The pattern on the data bus is a mask. If a bit in the mask is set, then the corresponding register bit will be set to zero (cleared).

11.1 Vendor ID and Product ID registers

11.1.1 Vendor ID Low register

Table 25 shows the bit description of the register.

Table 25. Vendor ID Low register (address R = 00h) bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	VENDOR_ID_LOW[7:0]	R	CCh*	**Vendor ID Low**: Lower byte of the NXP vendor ID supplied by USB-IF; fixed value of CCh

11.1.2 Vendor ID High register

Table 26 shows the bit description of the register.

Table 26. Vendor ID High register (address R = 01h) bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	VENDOR_ID_HIGH[7:0]	R	04h*	**Vendor ID High**: Upper byte of the NXP vendor ID supplied by USB-IF; fixed value of 04h

11.1.3 Product ID Low register

The bit description of the Product ID Low register is given in Table 27.

Table 27. Product ID Low register (address R = 02h) bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	PRODUCT_ID_LOW[7:0]	R	08h*	**Product ID Low**: Lower byte of the NXP product ID number; fixed value of 08h

11.1.4 Product ID High register

The bit description of the register is given in Table 28.

Table 28. Product ID High register (address R = 03h) bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	PRODUCT_ID_HIGH[7:0]	R	15h*	**Product ID High**: Upper byte of the NXP product ID number; fixed value of 15h

11.2 Function Control register

This register controls UTMI function settings of the PHY. The bit allocation of the register is given in Table 29.

Table 29. Function Control register (address R = 04h to 06h, W = 04h, S = 05h, C = 06h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	SUSPENDM	RESET	OPMODE[1:0]		TERM SELECT	XCVRSELECT[1:0]	
Reset	0	1	0	0	0	0	0	1
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 30. Function Control register (address R = 04h to 06h, W = 04h, S = 05h, C = 06h) bit description

Bit	Symbol	Description
7	-	reserved
6	SUSPENDM	**Suspend LOW**: Active LOW PHY suspend. Places the PHY into low-power mode. The PHY will power-down all blocks, except the full-speed receiver, OTG comparators and ULPI interface pins. To come out of low-power mode, the link must assert STP. The PHY will automatically clear this bit when it exits low-power mode. **0b —** Low-power mode **1b —** Powered
5	RESET	**Reset**: Active HIGH transceiver reset. After the link sets this bit, the PHY will assert DIR and reset the digital core. This does not reset the ULPI interface or the ULPI register set. When the reset is completed, the PHY will deassert DIR and automatically clear this bit, followed by an RXCMD update to the link. The link must wait for DIR to deassert before using the ULPI bus **0b —** Do not reset **1b —** Reset

Table 30. Function Control register (address R = 04h to 06h, W = 04h, S = 05h, C = 06h) bit description *...continued*

Bit	Symbol	Description
4 to 3	OPMODE[1:0]	**Operation Mode**: Selects the required bit-encoding style during transmit. **00b —** Normal operation **01b —** Non-driving **10b —** Disable bit-stuffing and NRZI encoding **11b —** Do not automatically add SYNC and EOP when transmitting; must be used only for high-speed packets
2	TERMSELECT	**Termination Select**: Controls the internal 1.5 kΩ full-speed pull-up resistor and 45 Ω high-speed terminations. Control over bus resistors changes, depending on XCVRSELECT[1:0], OPMODE[1:0], DP_PULLDOWN and DM_PULLDOWN, as shown in Table 14.
1 to 0	XCVRSELECT [1:0]	**Transceiver Select**: Selects the required transceiver speed. **00b —** Enable the high-speed transceiver **01b —** Enable the full-speed transceiver **10b —** Enable the low-speed transceiver **11b —** Enable the full-speed transceiver for low-speed packets (full-speed preamble is automatically prefixed)

11.3 Interface Control register

The Interface Control register enables alternative interfaces. All of these modes are optional features provided for legacy link cores. Setting more than one of these fields results in undefined behavior. Table 31 provides the bit allocation of the register.

Table 31. Interface Control register (address R = 07h to 09h, W = 07h, S = 08h, C = 09h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	INTF_ PROT_DIS	IND_PASS THRU	IND_ COMPL	reserved	CLOCK_ SUSPENDM	CARKIT_ MODE	3PIN_FSLS _SERIAL	6PIN_FSLS _SERIAL
Reset	0	0	0	0	0	0	0	0
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 32. Interface Control register (address R = 07h to 09h, W = 07h, S = 08h, C = 09h) bit description

Bit	Symbol	Description
7	INTF_PROT_DIS	**Interface Protect Disable**: Controls circuitry built into the SAF1508BET to protect the ULPI interface when the link 3-states STP and DATA[7:0]. When this bit is enabled, the SAF1508BET will automatically detect when the link stops driving STP. **0b —** Enables the interface protect circuit. The SAF1508BET attaches a weak pull-up resistor on STP. If STP is unexpectedly HIGH, the SAF1508BET attaches weak pull-down resistors on DATA[7:0], protecting data inputs. **1b —** Disables the interface protect circuit, detaches weak pull-down resistors on DATA[7:0], and a weak pull-up resistor on STP.
6	IND_PASSTHRU	**Indicator Pass-through**: Controls whether the complement output is qualified with the internal A_VBUS_VLD comparator before being used in the V_{BUS} state in RXCMD. **0b —** The complement output signal is qualified with the internal A_VBUS_VLD comparator. **1b —** The complement output signal is not qualified with the internal A_VBUS_VLD comparator.
5	IND_COMPL	**Indicator Complement**: Informs the PHY to invert the FAULT input signal, generating the complement output. **0b —** The SAF1508BET will not invert the FAULT signal. **1b —** The SAF1508BET will invert the FAULT signal.
4	-	reserved
3	CLOCK_SUSPENDM	**Clock Suspend LOW**: Active LOW clock suspend. Powers down the internal clock circuitry only. By default, the clock will not be powered in 6-pin serial mode or 3-pin serial mode. Valid only in 6-pin serial mode and 3-pin serial mode. Valid only when SUSPENDM is set to logic 1, otherwise this bit is ignored. **0b —** Clock will not be powered in 3-pin or 6-pin serial mode, or UART mode. **1b —** Clock will be powered in 3-pin and 6-pin serial mode, or UART mode.
2	CARKIT_MODE	**Carkit Mode**: Changes the ULPI interface to the carkit interface (UART mode). Bits TXD_EN and RXD_EN in the Carkit Control register must change as well. The PHY must automatically clear this bit when carkit mode is exited. **0b —** Disable carkit mode. **1b —** Enable carkit mode.
1	3PIN_FSLS_SERIAL	**3-Pin Full-Speed Low-Speed Serial Mode**: Changes the ULPI interface to a 3-bit serial interface. The SAF1508BET will automatically clear this bit when 3-pin serial mode is exited. **0b —** Full-speed or low-speed packets are sent using the parallel interface. **1b —** Full-speed or low-speed packets are sent using the 3-pin serial interface.
0	6PIN_FSLS_SERIAL	**6-Pin Full-Speed Low-Speed Serial Mode**: Changes the ULPI interface to a 6-bit serial interface. The SAF1508BET will automatically clear this bit when 6-pin serial mode is exited. **0b —** Full-speed or low-speed packets are sent using the parallel interface. **1b —** Full-speed or low-speed packets are sent using the 6-pin serial interface.

11.4 OTG Control register

This register controls various OTG functions of the SAF1508BET. The bit allocation of the OTG Control register is given in Table 33.

Table 33. OTG Control register (address R = 0Ah to 0Ch, W = 0Ah, S = 0Bh, C = 0Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	USE_EXT_ VBUS_IND	DRV_ VBUS_EXT	reserved	CHRG_ VBUS	DISCHRG_ VBUS	DM_PULL DOWN	DP_PULL DOWN	ID_PULL UP
Reset	0	0	0	0	0	1	1	0
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 34. OTG Control register (address R = 0Ah to 0Ch, W = 0Ah, S = 0Bh, C = 0Ch) bit description

Bit	Symbol	Description
7	USE_EXT_ VBUS_IND	**Use External V_{BUS} Indicator**: Informs the PHY to use an external V_{BUS} overcurrent indicator. **0b —** Use the internal OTG comparator. **1b —** Use the external V_{BUS} valid indicator signal input from the FAULT pin.
6	DRV_VBUS_EXT	**Drive V_{BUS} External**: Controls the external charge pump or 5 V supply by the PSW_N pin. **0b —** PSW_N is HIGH. **1b —** PSW_N to LOW.
5	-	reserved
4	CHRG_VBUS	**Charge V_{BUS}**: Charges V_{BUS} through a resistor. Used for the V_{BUS} pulsing of SRP. The link must first check that V_{BUS} is discharged (see bit DISCHRG_VBUS), and that both the DP and DM data lines have been LOW (SE0) for 2 ms. **0b —** Do not charge V_{BUS}. **1b —** Charge V_{BUS}.
3	DISCHRG_VBUS	**Discharge V_{BUS}**: Discharges V_{BUS} through a resistor. If the link sets this bit to logic 1, it waits for an RXCMD indicating that SESS_END has changed from 0 to 1, and then resets this bit to 0 to stop the discharge. **0b —** Do not discharge V_{BUS}. **1b —** Discharge V_{BUS}.
2	DM_PULLDOWN	**DM Pull Down**: Enables the 15 kΩ pull-down resistor on DM. **0b —** Pull-down resistor is not connected to DM. **1b —** Pull-down resistor is connected to DM.
1	DP_PULLDOWN	**DP Pull Down**: Enables the 15 kΩ pull-down resistor on DP. **0b —** Pull-down resistor is not connected to DP. **1b —** Pull-down resistor is connected to DP.
0	ID_PULLUP	**ID Pull Up**: Connects a pull-up to the ID line and enables sampling of the ID level. Disabling the ID line sampler will reduce the PHY power consumption. **0b —** Disable sampling of the ID line. **1b —** Enable sampling of the ID line.

11.5 USB Interrupt Enable Rising register

The bits in this register enable interrupts and RXCMDs to be sent when the corresponding bits in the USB Interrupt Status register change from logic 0 to logic 1. By default, all transitions are enabled. Table 35 shows the bit allocation of the register.

Table 35. USB Interrupt Enable Rising register (address R = 0Dh to 0Fh, W = 0Dh, S = 0Eh, C = 0Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			ID_GND_R	SESS_END_R	SESS_VALID_R	VBUS_VALID_R	HOST_DISCON_R
Reset	0	0	0	1	1	1	1	1
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 36. USB Interrupt Enable Rising register (address R = 0Dh to 0Fh, W = 0Dh, S = 0Eh, C = 0Fh) bit description

Bit	Symbol	Description
7 to 5	-	reserved
4	ID_GND_R	**ID Ground Rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on ID_GND.
3	SESS_END_R	**Session End Rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on SESS_END.
2	SESS_VALID_R	**Session Valid Rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on SESS_VLD.
1	VBUS_VALID_R	**V_{BUS} Valid Rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on A_VBUS_VLD.
0	HOST_DISCON_R	**Host Disconnect Rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on HOST_DISCON.

11.6 USB Interrupt Enable Falling register

The bits in this register enable interrupts and RXCMDs to be sent when the corresponding bits in the USB Interrupt Status register change from logic 1 to logic 0. By default, all transitions are enabled. See Table 37.

Table 37. USB Interrupt Enable Falling register (address R = 10h to 12h, W = 10h, S = 11h, C = 12h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			ID_GND_F	SESS_END_F	SESS_VALID_F	VBUS_VALID_F	HOST_DISCON_F
Reset	0	0	0	1	1	1	1	1
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 38. USB Interrupt Enable Falling register (address R = 10h to 12h, W = 10h, S = 11h, C = 12h) bit description

Bit	Symbol	Description
7 to 5	-	reserved
4	ID_GND_F	**ID Ground Fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on ID_GND.
3	SESS_END_F	**Session End Fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on SESS_END.

Table 38. USB Interrupt Enable Falling register (address R = 10h to 12h, W = 10h, S = 11h, C = 12h) bit description

Bit	Symbol	Description
2	SESS_VALID_F	**Session Valid Fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on SESS_VLD.
1	VBUS_VALID_F	**V_{BUS} Valid Fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on A_VBUS_VLD.
0	HOST_DISCON_F	**Host Disconnect Fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on HOST_DISCON.

11.7 USB Interrupt Status register

This register (see Table 39) indicates the current value of the interrupt source signal.

Table 39. USB Interrupt Status register (address R = 13h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			ID_GND	SESS_END	SESS_VALID	VBUS_VALID	HOST_DISCON
Reset	X	X	X	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 40. USB Interrupt Status register (address R = 13h) bit description

Bit	Symbol	Description
7 to 5	-	reserved
4	ID_GND	**ID Ground**: Reflects the current value of the ID detector circuit.
3	SESS_END	**Session End**: Reflects the current value of the session end voltage comparator.
2	SESS_VALID	**Session Valid**: Reflects the current value of the session valid voltage comparator.
1	VBUS_VALID	**V_{BUS} Valid**: Reflects the current value of the V_{BUS} valid voltage comparator.
0	HOST_DISCON	**Host Disconnect**: Reflects the current value of the host disconnect detector.

11.8 USB Interrupt Latch register

The bits of the USB Interrupt Latch register are automatically set by the SAF1508BET when an unmasked change occurs on the corresponding interrupt source signal. The SAF1508BET will automatically clear all bits when the link reads this register, or when the PHY enters low-power mode.

Remark: It is optional for the link to read this register when the clock is running because all signal information will automatically be sent to the link through the RXCMD byte.

The bit allocation of this register is given in Table 41.

Table 41. USB Interrupt Latch register (address R = 14h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			ID_GND_L	SESS_END_L	SESS_VALID_L	VBUS_VALID_L	HOST_DISCON_L
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 42. USB Interrupt Latch register (address R = 14h) bit description

Bit	Symbol	Description
7 to 5	-	reserved
4	ID_GND_L	**ID Ground Latch**: Automatically set when an unmasked event occurs on ID_GND. Cleared when this register is read.
3	SESS_END_L	**Session End Latch**: Automatically set when an unmasked event occurs on SESS_END. Cleared when this register is read.
2	SESS_VALID_L	**Session Valid Latch**: Automatically set when an unmasked event occurs on SESS_VLD. Cleared when this register is read.
1	VBUS_VALID_L	**V_{BUS} Valid Latch**: Automatically set when an unmasked event occurs on A_VBUS_VLD. Cleared when this register is read.
0	HOST_DISCON_L	**Host Disconnect Latch**: Automatically set when an unmasked event occurs on HOST_DISCON. Cleared when this register is read.

11.9 Debug register

The bit allocation of the Debug register is given in Table 43. This register indicates the current value of signals useful for debugging.

Table 43. Debug register (address R = 15h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved						LINE STATE1	LINE STATE0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 44. Debug register (address R = 15h) bit description

Bit	Symbol	Description
7 to 2	-	reserved
1	LINESTATE1	**Line State 1**: Contains the current value of LINESTATE 1.
0	LINESTATE0	**Line State 0**: Contains the current value of LINESTATE 0.

11.10 Scratch register

This is a 1-byte empty register for testing purposes, see Table 45.

Table 45. Scratch register (address R = 16h to 18h, W = 16h, S = 17h, C = 18h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	SCRATCH[7:0]	R/W/S/C	00h	**Scratch**: This is an empty register byte for testing purposes. Software can read, write, set and clear this register, and the functionality of the PHY will not be affected.

11.11 Carkit Control register

This register controls transparent UART mode. This register is only valid when the CARKIT_MODE register bit in the Interface Control register is set. When entering UART mode, set the CARKIT_MODE bit, and then set the TXD_EN and RXD_EN bits. After entering UART mode, the ULPI interface is not available. When exiting UART mode, assert the STP pin or perform a hardware reset using the CHIP_SEL pin. For bit allocation, see Table 46.

Table 46. Carkit Control register (address R = 19h to 1Bh, W = 19h, S = 1Ah, C = 1Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved				RXD_EN	TXD_EN	reserved	
Reset	0	0	0	0	0	0	0	0
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 47. Carkit Control register (address R = 19h to 1Bh, W = 19h, S = 1Ah, C = 1Bh) bit description

Bit	Symbol	Description
7 to 4	-	reserved; the link must never write logic 1 to these bits
3	RXD_EN	**RXD Enable**: Routes the UART RXD signal from the DP pin to the DATA1 pin. This bit will automatically be cleared when UART mode is exited.
2	TXD_EN	**TXD Enable**: Routes the UART TXD signal from the DATA0 pin to the DM pin. This bit will automatically be cleared when UART mode is exited.
1 to 0	-	reserved; the link must never write logic 1 to these bits

11.12 Power Control register

This vendor-specific register controls the power feature of the SAF1508BET. The bit allocation of the register is given in Table 48.

Table 48. Power Control register (address R = 3Dh to 3Fh, W = 3Dh, S = 3Eh, C = 3Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			DP_WKPU_EN	BVALID_FALL	BVALID_RISE	reserved	
Reset	0	0	0	0	0	0	0	0
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 49. Power Control register (address R = 3Dh to 3Fh, W = 3Dh, S = 3Eh, C = 3Fh) bit description

Bit	Symbol	Description
7 to 5	-	reserved; the link must never write logic 1 to these bits
4	DP_WKPU_EN	**DP Weak Pull-Up Enable**: Enable the weak pull-up resistor on the DP pin ($R_{weakUP(DP)}$) in synchronous mode when V_{BUS} is above the $V_{A\_SESS\_VLD}$ threshold. Note that when the SAF1508BET is in UART mode, the DP weak pull-up will be enabled, regardless of the value of this register bit. **0 —** DP weak pull-up is disabled. **1 —** DP weak pull-up is enabled when $V_{BUS} > V_{A\_SESS\_VLD}$.
3	BVALID_FALL	**BValid Fall**: Enables RXCMDs for HIGH-to-LOW transitions on BVALID. When BVALID changes from HIGH to LOW, the SAF1508BET will send an RXCMD to the link with the ALT_INT bit set to logic 1. This bit is optional and is not necessary for OTG devices. This bit is provided for debugging purposes. Disabled by default.
2	BVALID_RISE	**BValid Rise**: Enables RXCMDs for LOW-to-HIGH transitions on BVALID. When BVALID changes from LOW to HIGH, the SAF1508BET will send an RXCMD to the link with the ALT_INT bit set to logic 1. This bit is optional and is not necessary for OTG devices. This bit is provided for debugging purposes. Disabled by default.
1 to 0	-	reserved; the link must never write logic 1 to these bits

12. Limiting values

Table 50. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+5.5	V
$V_{CC(I/O)}$	input/output supply voltage			–0.5	+2.5	V
V_I	input voltage	on pins PSW_N and FAULT		–0.5	+5.5	V
		on pins CLOCK, STP, DATA[7:0], CFG1, CFG2, TEST_N and CHIP_SEL		–0.5	+2.5	V
		on pins ID and CFG0		–0.5	+4.6	V
		on pins DP and DM	[1]	–0.5	+4.6	V
		on pin XTAL1		–0.5	+2.5	V
		on pin V_{BUS}	[2]	–0.5	+5.5	V
V_{ESD}	electrostatic discharge voltage	human body model (*JESD22-A114D*)		–2	+2	kV
		machine model (*JESD22-A115-A*)		–200	+200	V
		charge device model (*JESD22-C101C*)		–500	+500	V
		IEC 61000-4-2 contact on pins DP and DM	[3]	–8	+8	kV
I_{lu}	latch-up current			-	100	mA
T_{stg}	storage temperature			–60	+125	°C

[1] The SAF1508BET has been tested according to the additional requirements listed in *Universal Serial Bus Specification Rev. 2.0, Section 7.1.1*. The short circuit withstand test and the AC stress test were performed for 24 hours, and the SAF1508BET was found to be fully operational after the test completed.

[2] When an external series resistor is added to the V_{BUS} pin, it can withstand higher voltages for longer periods of time because the resistor limits the current flowing into the V_{BUS} pad. For example, with an external 1 kΩ resistor, V_{BUS} can tolerate 10 V for at least 5 seconds. Actual performance may vary depending on the resistor used and whether other components are connected to V_{BUS}.

[3] The SAF1508BET has been tested in-house according to the *IEC 61000-4-2* standard on the DP and DM pins. It is recommended that customers perform their own ESD tests, depending on application requirements.

13. Recommended operating conditions

Table 51. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		3.0	3.6	4.5	V
$V_{CC(I/O)}$	input/output supply voltage		1.4	1.8	1.95	V
V_I	input voltage	on pins PSW_N, FAULT and V_{BUS}	0	-	5.25	V
		on pins CLOCK, STP, DATA[7:0], CFG1, CFG2, TEST_N and CHIP_SEL	0	-	$V_{CC(I/O)}$	V
		on pins DP, DM, ID and CFG0	0	-	3.6	V
		on pin XTAL1	0	-	1.95	V
T_{amb}	ambient temperature		–40	+25	+85	°C

14. Static characteristics

Table 52. Static characteristics: supply pins

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR(trip)}$	power-on reset trip voltage	on REG1V8 pin	0.95	-	1.5	V
I_{CC}	supply current	power-down mode ($V_{CC(I/O)}$ is lost or CHIP_SEL is non-active)	-	0.5	10	µA
		full-speed transceiver; bus idle; no USB activity	-	13	-	mA
		full-speed transceiver; continuous transmission	-	14	-	mA
		high-speed transceiver; continuous transmission	-	32	-	mA
		low-power mode (bit SUSPENDM is logic 0); V_{BUS} valid detector disabled (bits VBUS_VALID_R and VBUS_VALID_F are cleared)				
		$V_{CC(I/O)}$ = 1.4 V	-	70	300	µA
		$V_{CC(I/O)}$ = 1.5 V	-	70	200	µA
		$V_{CC(I/O)}$ = 1.8 V	-	70	200	µA
		UART mode; low-speed transceiver; idle	-	750	-	µA
		UART mode; full-speed transceiver; idle	-	600	-	µA
$I_{CC(I/O)(stat)}$	static supply current on pin $V_{CC(I/O)}$	power-down mode (CHIP_SEL is non-active)	-	-	10	µA
$I_{CC(I/O)}$	supply current on pin $V_{CC(I/O)}$	ULPI bus idle; 15 pF load on pin CLOCK [1]	-	1.7	-	mA

[1] The actual value of $I_{CC(I/O)}$ varies depending on the capacitance loading, interface voltage and bus activity. Use the value provided here only for reference.

Table 53. Static characteristics: digital pins

Digital pins: CLOCK, DIR, STP, NXT, DATA[7:0], CHIP_SEL, CFG2, CFG1 and TEST_N.
V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input levels						
V_{IL}	LOW-level input voltage		-	-	$0.3 \times V_{CC(I/O)}$	V
V_{IH}	HIGH-level input voltage		$0.7 \times V_{CC(I/O)}$	-	-	V
I_{LI}	input leakage current		−1	-	+1	µA
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = −2 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = +2 mA	$V_{CC(I/O)} - 0.4$	-	-	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{CC(I/O)} - 0.4$ V	−4.8	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	4.2	-	-	mA

Table 53. Static characteristics: digital pins *...continued*

Digital pins: CLOCK, DIR, STP, NXT, DATA[7:0], CHIP_SEL, CFG2, CFG1 and TEST_N.
V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Impedance						
Z_L	load impedance		-	50	-	Ω
Pull-up and pull-down						
I_{pd}	pull-down current	interface protect enabled; DATA[7:0] pins only; $V_I = V_{CC(I/O)}$	18	55	93	μA
I_{pu}	pull-up current	interface protect enabled; STP pin only; V_I = 0 V	−17	−55	−82	μA
		UART mode; DATA0 pin only	−17	−55	−82	μA
Capacitance						
C_{in}	input capacitance		1.0	3.0	3.3	pF

Table 54. Static characteristics: digital pin FAULT

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input levels						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
I_{IL}	LOW-level input current	V_I = 0 V	−1	-	-	μA
I_{IH}	HIGH-level input current	V_I = 5.25 V	-	-	1	μA

Table 55. Static characteristics: digital pin PSW_N

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output levels						
V_{OH}	HIGH-level output voltage	external pull-up resistor connected	3.0[1]	-	5.25	V
V_{OL}	LOW-level output voltage	I_{OL} = −4 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	external pull-up resistor connected	-	-	10	μA
I_{OL}	LOW-level output current	V_O = 0.4 V	4	-	-	mA

[1] When V_{OH} is less than REG3V3, I_{CC} may increase because of the cross current.

Table 56. Static characteristics: analog pins (DP and DM)

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Original USB transceiver (full-speed and low-speed)						
Input levels (differential data receiver)						
V_{DI}	differential input sensitivity voltage	$\|V_{DP} - V_{DM}\|$	0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range	0.8	-	2.5	V
Input levels (single-ended receivers)						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	pull-up on DP; R_L = 1.5 kΩ to 3.6 V	0.0	-	0.3	V
V_{OH}	HIGH-level output voltage	pull-down on DP and DM; R_L = 15 kΩ to GND	2.8	-	3.6	V
V_{CRS}	output signal crossover voltage	excluding the first transition from the idle state	1.3	-	2.0	V
Termination						
V_{TERM}	termination voltage for upstream facing port pull-up	for 1.5 kΩ pull-up resistor	3.0	-	3.6	V
Resistance						
$R_{UP(DP)}$	pull-up resistance on pin DP		1425	1500	1575	Ω
$R_{weakUP(DP)}$	weak pull-up resistance on pin DP	bit DP_WKPU_EN = 1 and $V_{BUS} > V_{A\_SESS\_VLD}$	94	118	144	kΩ
High-speed USB transceiver (HS)						
Input levels						
V_{HSSQ}	high-speed squelch detection threshold voltage (differential signal amplitude)		100	-	150	mV
V_{HSDSC}	high-speed disconnect detection threshold voltage (differential signal amplitude)		525	-	625	mV
V_{HSDI}	high-speed differential input sensitivity	$\|V_{DP} - V_{DM}\|$	300	-	-	mV
V_{HSCM}	high-speed data signaling common mode voltage range (guideline for receiver)	includes V_{DI} range	−50	-	+500	mV
Output levels						
V_{HSOI}	high-speed idle level voltage		−10	-	+10	mV
V_{HSOL}	high-speed data signaling LOW-level voltage		−10	-	+10	mV
V_{HSOH}	high-speed data signaling HIGH-level voltage		360	-	440	mV

Table 56. Static characteristics: analog pins (DP and DM) *…continued*

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CHIRPJ}	Chirp J level (differential voltage)		700	-	1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)		−900	-	−500	mV
Leakage current						
I_{LZ}	off-state leakage current		−1.0	-	+1.0	μA
Capacitance						
C_{in}	input capacitance	pin to GND	-	-	5	pF
Resistance						
$R_{DN(DP)}$	pull-down resistance on pin DP		14.25	15	24.8	kΩ
$R_{DN(DM)}$	pull-down resistance on pin DM		14.25	15	24.8	kΩ
Termination						
$Z_{O(drv)(DP)}$	driver output impedance on pin DP	steady-state drive	40.5	45	49.5	Ω
$Z_{O(drv)(DM)}$	driver output impedance on pin DM	steady-state drive	40.5	45	49.5	Ω
Z_{INP}	input impedance exclusive of pull-up/pull-down (for low-/full-speed)		1	-	-	MΩ
UART mode						
Input levels						
V_{IL}	LOW-level input voltage	pin DP	-	-	0.8	V
V_{IH}	HIGH-level input voltage	pin DP	2.35	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	pin DM; I_{OL} = −4 mA	-	-	0.3	V
V_{OH}	HIGH-level output voltage	pin DM; I_{OH} = 4 mA	2.4	-	-	V

Table 57. Static characteristics: analog pin V_{BUS}

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Comparators						
$V_{A\_VBUS\_VLD}$	A-device V_{BUS} valid voltage		4.4	-	4.75	V
$V_{A\_SESS\_VLD}$	A-device session valid voltage	for A-device and B-device	0.8	1.6	2.0	V
$V_{hys(A\_SESS\_VLD)}$	A-device session valid hysteresis voltage	for A-device and B-device	-	100	-	mV
$V_{B\_SESS\_END}$	B-device session end voltage		0.2	-	0.8	V

Table 57. Static characteristics: analog pin V_{BUS} *…continued*

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Resistance						
$R_{UP(VBUS)}$	pull-up resistance on pin V_{BUS}	connect to REG3V3 when CHRG_VBUS = 1	281	680	-	Ω
$R_{DN(VBUS)}$	pull-down resistance on pin V_{BUS}	connect to GND when DISCHRG_VBUS = 1	656	1200	-	Ω
$R_{I(idle)(VBUS)}$	idle input resistance on pin V_{BUS}		40	60	100	kΩ

Table 58. Static characteristics: ID detection circuit

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{ID}	ID detection time		50	-	-	ms
$V_{th(ID)}$	ID detector threshold voltage		0.8	-	2.0	V
$R_{UP(ID)}$	ID pull-up resistance	bit ID_PULLUP = 1	40	50	60	kΩ
$R_{weakPU(ID)}$	weak pull-up resistance on pin ID	bit ID_PULLUP = 0	320	400	480	kΩ
$V_{PU(ID)}$	pull-up voltage on pin ID		3.0	3.3	3.6	V

Table 59. Static characteristics: resistor reference

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{O(RREF)}$	output voltage on pin RREF	SUSPENDM = HIGH	-	1.22	-	V

Table 60. Static characteristics: regulator

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{O(REG1V8)}$	output voltage from internal 1.8 V regulator	SUSPENDM = HIGH	1.65	1.8	1.95	V
$V_{O(REG3V3)}$	output voltage from internal 3.3 V regulator	SUSPENDM = HIGH; not in UART mode	3.0	3.3	3.6	V
		SUSPENDM = HIGH; in UART mode	2.5	2.77	2.9	V

Table 61. Static characteristics: pin XTAL1

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	LOW-level input voltage		-	-	0.37	V
V_{IH}	HIGH-level input voltage		1.32	-	-	V

15. Dynamic characteristics

Table 62. Dynamic characteristics: reset and power

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{W(POR)}$	internal power-on reset pulse width		0.2	-	-	µs
$t_{w(REG1V8\_H)}$	REG1V8 HIGH pulse width		-	-	2	µs
$t_{w(REG1V8\_L)}$	REG1V8 LOW pulse width		-	-	11	µs
$t_{startup(PLL)}$	PLL start-up time	measured after $t_{d(det)clk(osc)}$	-	-	640	µs
$t_{d(det)clk(osc)}$	oscillator clock detector delay	measured from regulator start-up time	-	-	640	µs
t_{PWRUP}	regulator start-up time	4.7 µF ± 20 % capacitor each on the REG1V8 and REG3V3 pins	-	-	1	ms
t_{PWRDN}	regulator power-down time	4.7 µF ± 20 % capacitor each on the REG1V8 and REG3V3 pins	-	-	100	ms

Table 63. Dynamic characteristics: clock applied to XTAL1

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{i(XTAL1)}$	input frequency on pin XTAL1	see Table 5	-	13.000	-	MHz
		see Table 5	-	24.000	-	MHz
		see Table 5	-	26.000	-	MHz
		see Table 5	-	19.200	-	MHz
$t_{jit(i)(XTAL1)RMS}$	RMS input jitter on pin XTAL1	26 MHz	-	-	300	ps
		other frequencies	-	-	200	ps
$\Delta f_{i(XTAL1)}$	input frequency tolerance on pin XTAL1		-	-	200	ppm
$\delta_{i(XTAL1)}$	input duty cycle on pin XTAL1	[1]	-	50	-	%
$t_{r(XTAL1)}$	rise time on pin XTAL1	only for square wave input	-	-	5	ns
$t_{f(XTAL1)}$	fall time on pin XTAL1	only for square wave input	-	-	5	ns

[1] The internal PLL is triggered only on the positive edge from the crystal oscillator. Therefore, the duty cycle is not critical.

Table 64. Dynamic characteristics: CLOCK output

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{o(CLOCK)}$	output frequency on pin CLOCK		59.970	60.000	60.030	MHz
$t_{jit(o)(CLOCK)RMS}$	RMS output jitter on pin CLOCK		-	-	500	ps
$\delta_{o(CLOCK)}$	output clock duty cycle on pin CLOCK		40	50	60	%

Table 65. Dynamic characteristics: digital I/O pins (SDR)

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{su}	set-up time	set-up time with respect to the positive edge of CLOCK; input-only pin (STP) and bidirectional pins (DATA[7:0]) as inputs		6.0	-	-	ns
t_h	hold time	hold time with respect to the positive edge of CLOCK; input-only pin (STP) and bidirectional pins (DATA[7:0]) as inputs		0.0	-	-	ns
$t_{d(o)}$	output delay time	output delay with respect to the positive edge of CLOCK; output-only pins (DIR and NXT)		-	-	9.0	ns
		output delay with respect to the positive edge of CLOCK; bidirectional pins as output (DATA[7:0])		-	-	9.0	ns
C_L	load capacitance	DATA[7:0], CLOCK, DIR, NXT and STP; $V_{CC(I/O)}$ = 1.4 V to 1.65 V	[1]	-	-	10	pF
		DATA[7:0], CLOCK, DIR, NXT and STP; $V_{CC(I/O)}$ = 1.65 V to 1.95 V	[1]	-	-	20	pF

[1] Load capacitance on each ULPI pin.

Table 66. Dynamic characteristics: digital I/O pins (DDR)

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{su}	set-up time	set-up time with respect to the positive edge of CLOCK; input-only pin (STP)		6.0	-	-	ns
		set-up time with respect to the positive and negative edges of CLOCK; bidirectional pins (DATA[3:0]) as inputs	[1]	4.4	-	-	ns
t_h	hold time	hold time with respect to the positive edge of CLOCK; input-only pin (STP)		0.0	-	-	ns
		hold time with respect to the positive and negative edges of CLOCK; bidirectional pins (DATA[7:0]) as inputs		0.0	-	-	ns
$t_{d(o)}$	output delay time	output delay with respect to the positive edge of CLOCK; output-only pins (DIR and NXT)		-	-	9.0	ns
		output delay with respect to the positive and negative edges of CLOCK; bidirectional pins as output (DATA[3:0])		-	-	4.0	ns
C_L	load capacitance	DATA[3:0], CLOCK, DIR, NXT and STP	[2]	-	-	15	pF

[1] Note that the value exceeds that specified in *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

[2] Load capacitance on each ULPI pin.

Table 67. Dynamic characteristics: analog I/O pins (DP and DM) in USB mode

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
High-speed driver characteristics						
t_{HSR}	rise time (10 % to 90 %)	drive 45 Ω to GND on DP and DM	500	-	-	ps
t_{HSF}	fall time (10 % to 90 %)	drive 45 Ω to GND on DP and DM	500	-	-	ps

Table 67. Dynamic characteristics: analog I/O pins (DP and DM) in USB mode *…continued*

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Full-speed driver characteristics						
t_{FR}	rise time	C_L = 50 pF; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FF}	fall time	C_L = 50 pF; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FRFM}	differential rise and fall time matching	t_{FR}/t_{FF}; excluding the first transition from the idle state	90	-	111.1	%
Low-speed driver characteristics						
t_{LR}	transition time: rise time	C_L = 200 pF to 600 pF; 1.5 kΩ pull-up on DM enabled; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$	75	-	300	ns
t_{LF}	transition time: fall time	C_L = 200 pF to 600 pF; 1.5 kΩ pull-up on DM enabled; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$	75	-	300	ns
t_{LRFM}	rise and fall time matching	t_{LR}/t_{LF}; excluding the first transition from the idle state	80	-	125	%

Table 68. Dynamic characteristics: analog I/O pins (DP and DM) in transparent UART mode

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Full-speed driver characteristics (DM only)						
$t_{r(UART)}$	rise time for UART TXD	C_L = 185 pF; 0.37 V to 2.16 V	25	-	75	ns
$t_{f(UART)}$	fall time for UART TXD	C_L = 185 pF; 2.16 V to 0.37 V	25	-	75	ns
$t_{PLH(drv)}$	driver propagation delay (LOW to HIGH)	C_L = 185 pF; DATA0 to DM	-	-	39	ns
$t_{PHL(drv)}$	driver propagation delay (HIGH to LOW)	C_L = 185 pF; DATA0 to DM	-	-	34	ns
Low-speed driver characteristics (DM only)						
$t_{r(UART)}$	rise time for UART TXD	C_L = 185 pF; 0.37 V to 2.16 V	100	-	400	ns
$t_{f(UART)}$	fall time for UART TXD	C_L = 185 pF; 2.16 V to 0.37 V	100	-	400	ns
$t_{PLH(drv)}$	driver propagation delay (LOW to HIGH)	C_L = 185 pF; DATA0 to DM	-	-	614	ns
$t_{PHL(drv)}$	driver propagation delay (HIGH to LOW)	C_L = 185 pF; DATA0 to DM	-	-	614	ns
Full-speed receiver characteristics (DP only)						
$t_{PLH(rcv)}$	receiver propagation delay (LOW to HIGH)	DP to DATA1	-	-	7	ns
$t_{PHL(rcv)}$	receiver propagation delay (HIGH to LOW)	DP to DATA1	-	-	7	ns
Low-speed receiver characteristics (DP only)						
$t_{PLH(rcv)}$	receiver propagation delay (LOW to HIGH)	DP to DATA1	-	-	7	ns
$t_{PHL(rcv)}$	receiver propagation delay (HIGH to LOW)	DP to DATA1	-	-	7	ns

Table 69. Dynamic characteristics: analog I/O pins (DP and DM) in serial mode

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.4 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver timing						
$t_{PLH(drv)}$	driver propagation delay (LOW to HIGH)	TX_DAT, TX_SE0 to DP and DM; see Figure 25	-	-	11	ns
$t_{PHL(drv)}$	driver propagation delay (HIGH to LOW)	TX_DAT, TX_SE0 to DP and DM; see Figure 25	-	-	11	ns
t_{PHZ}	HIGH to OFF-state propagation delay	TX_ENABLE to DP and DM; see Figure 26	-	-	12	ns
t_{PLZ}	LOW to OFF-state propagation delay	TX_ENABLE to DP and DM; see Figure 26	-	-	12	ns
t_{PZH}	OFF-state to HIGH propagation delay	TX_ENABLE to DP and DM; see Figure 26	-	-	20	ns
t_{PZL}	OFF-state to LOW propagation delay	TX_ENABLE to DP and DM; see Figure 26	-	-	20	ns
Receiver timing						
Differential receiver						
$t_{PLH(rcv)}$	receiver propagation delay (LOW to HIGH)	DP, DM to RX_RCV, RX_DP and RX_DM; see Figure 27	-	-	17	ns
$t_{PHL(rcv)}$	receiver propagation delay (HIGH to LOW)	DP, DM to RX_RCV, RX_DP and RX_DM; see Figure 27	-	-	17	ns
Single-ended receiver						
$t_{PLH(se)}$	single-ended propagation delay (LOW to HIGH)	DP, DM to RX_RCV, RX_DP and RX_DM; see Figure 27	-	-	17	ns
$t_{PHL(se)}$	single-ended propagation delay (HIGH to LOW)	DP, DM to RX_RCV, RX_DP and RX_DM; see Figure 27	-	-	17	ns

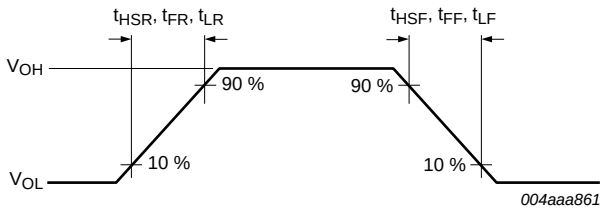


Fig 24. Rise time and fall time

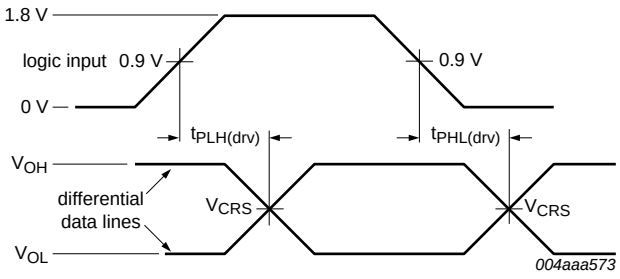


Fig 25. Timing of TX_DAT and TX_SE0 to DP and DM

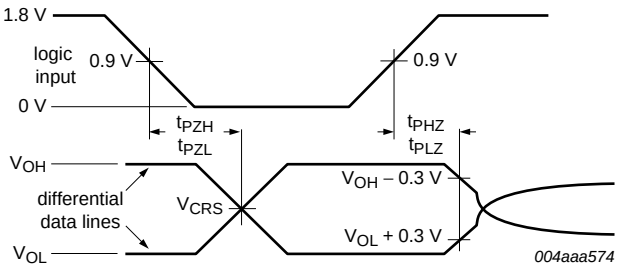


Fig 26. Timing of TX_ENABLE to DP and DM

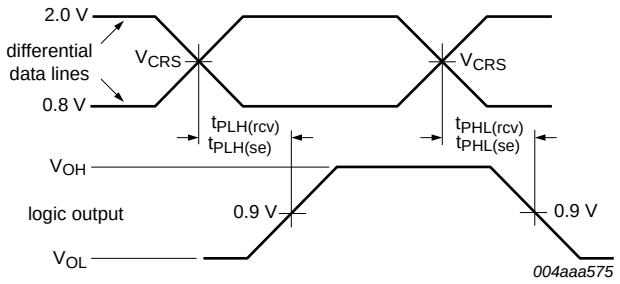


Fig 27. Timing of DP and DM to RX_RCV, RX_DP and RX_DM

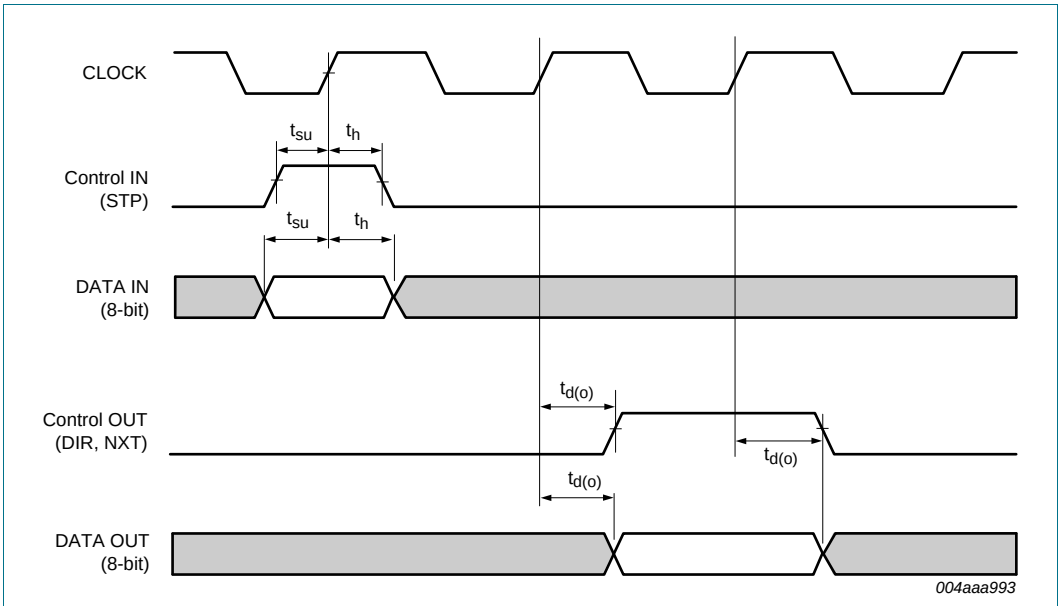


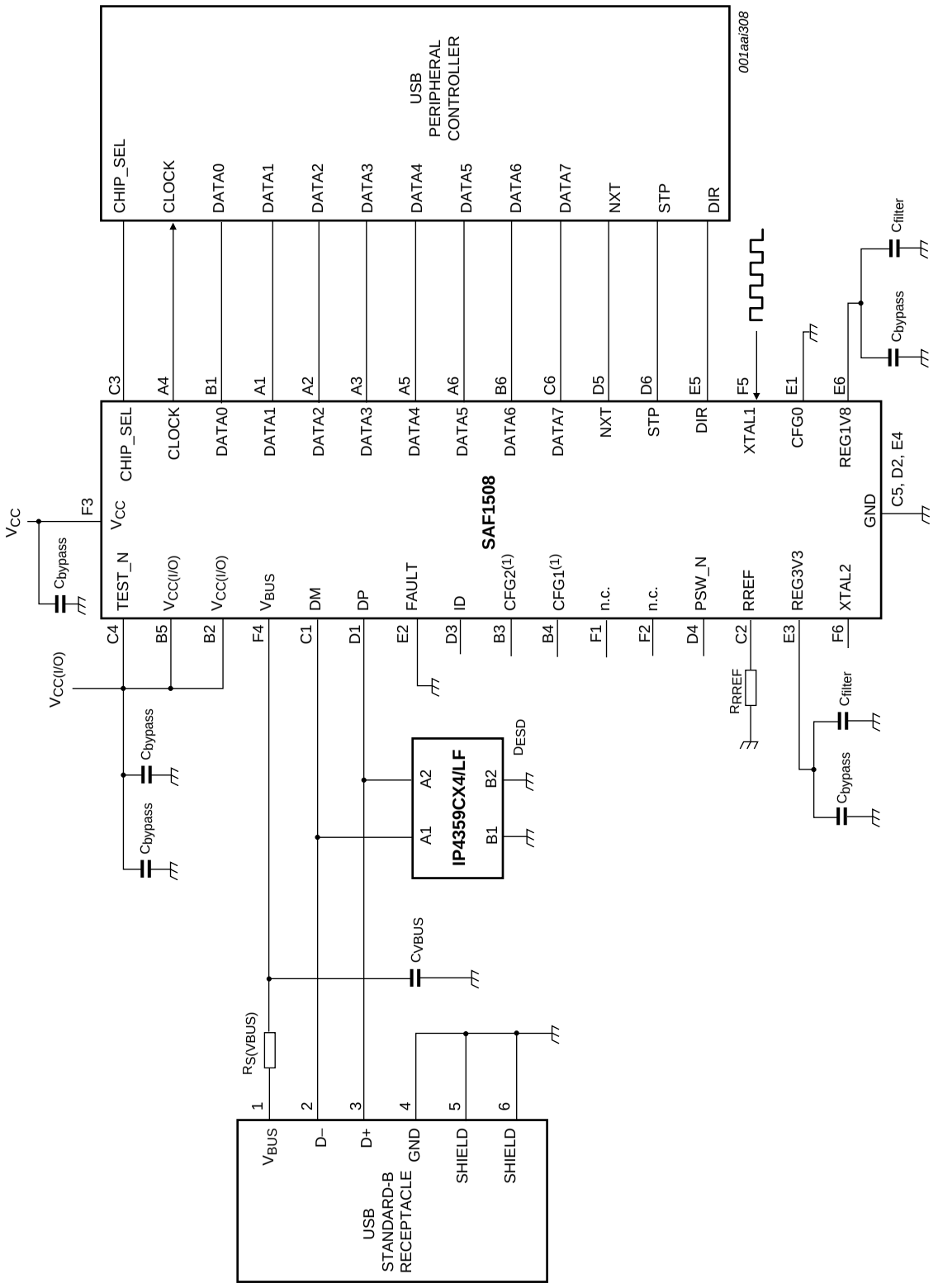
Fig 28. ULPI timing interface

16. Application information

Table 70. Recommended bill of materials

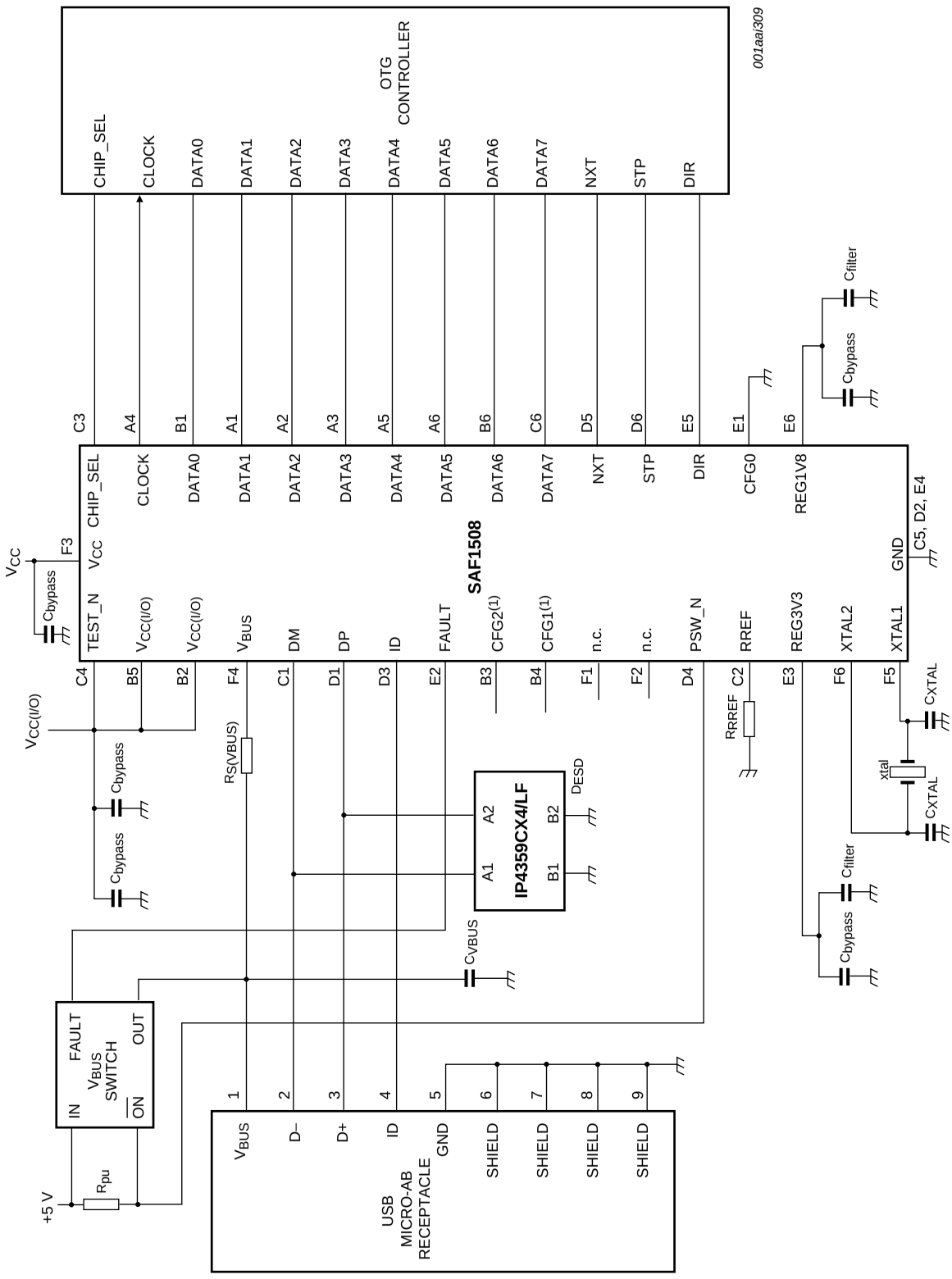
Designator	Application	Part type	Remark
R_{RREF}	mandatory in all applications	12 kΩ ± 1 %	-
$R_{S(VBUS)}$	recommended for peripherals or external 5 V applications	1 kΩ ± 5 %	-
C_{XTAL}	in all applications	18 pF ± 20 %	-
C_{VBUS}	mandatory for peripherals	1 μF to 10 μF	use low ESR capacitor
	mandatory for host	120 μF (min)	use low ESR capacitor
	mandatory for OTG	1 μF to 6.5 μF	use low ESR capacitor
C_{bypass}	highly recommended for all applications	0.1 μF ± 20 %	-
C_{filter}	highly recommended for all applications	4.7 μF ± 20 %	use ESR = 300 Ω type capacitor for best performance
R_{pullup}	recommended; for applications with an external V_{BUS} supply controlled by PSW_N	10 kΩ	-
D_{ESD}	recommended to prevent damages from ESD		IP4359CX4/LF; Wafer-Level Chip-Scale Package (WLCSP); ESD *IEC 61000-4-2* level 4; ±15 kV contact; ±15 kV air discharge compliant protection
xtal	mandatory in all applications	13 MHz	50 ppm; C_L = 10 pF; R_S < 300 Ω; C_{XTAL} = 18 pF
		19.2 MHz	50 ppm; C_L = 10 pF; R_S < 220 Ω; C_{XTAL} = 18 pF
		24 MHz	50 ppm; C_L = 10 pF; R_S < 160 Ω; C_{XTAL} = 18 pF
		26 MHz	50 ppm; C_L = 10 pF; R_S < 130 Ω; C_{XTAL} = 18 pF
		-	CSTCE26M0XK2***-R0[1]; C_{XTAL} is not required

[1] For more information, contact Murata.



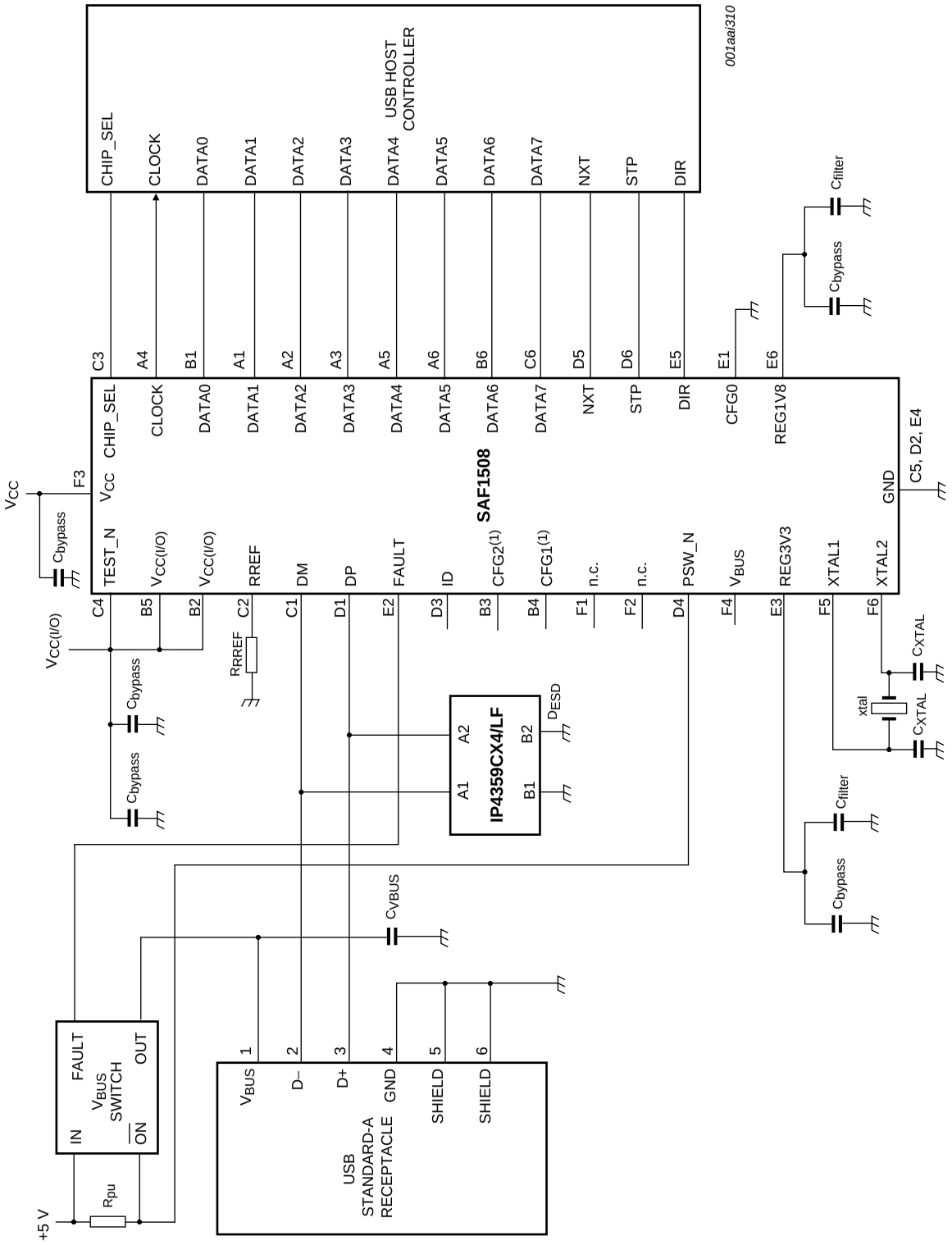
(1) Connect to either GND or $V_{CC(I/O)}$, depending on the clock frequency used. See Table 5.

Fig 29. SAF1508BET in peripheral only application



(1) Connect to either GND or $V_{CC(I/O)}$, depending on the crystal frequency used. See Table 5.

Fig 30. SAF1508BET in OTG application

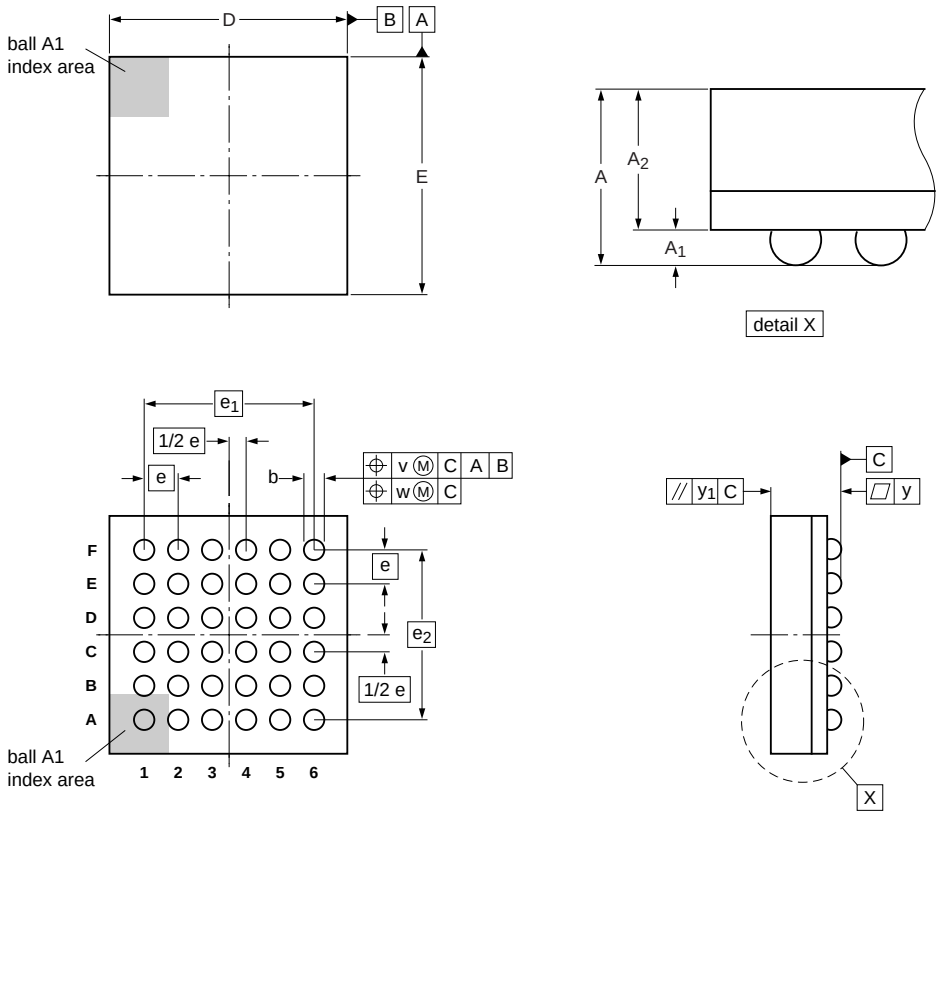


(1) Connect to either GND or $V_{CC(I/O)}$, depending on the crystal frequency used. See Table 5.

Fig 31. SAF1508BET in host application

17. Package outline

TFBGA36: plastic thin fine-pitch ball grid array package; 36 balls; body 3.5 x 3.5 x 0.8 mm **SOT912-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.15	0.25 0.15	0.90 0.75	0.35 0.25	3.6 3.4	3.6 3.4	0.5	2.5	2.5	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT912-1	- - -	- - -	- - -			~~05-08-09~~ 05-09-01

Fig 32. Package outline SOT912-1 (TFBGA36)

18. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 33) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 71 and 72

Table 71. SnPb eutectic process (from J-STD-020C)

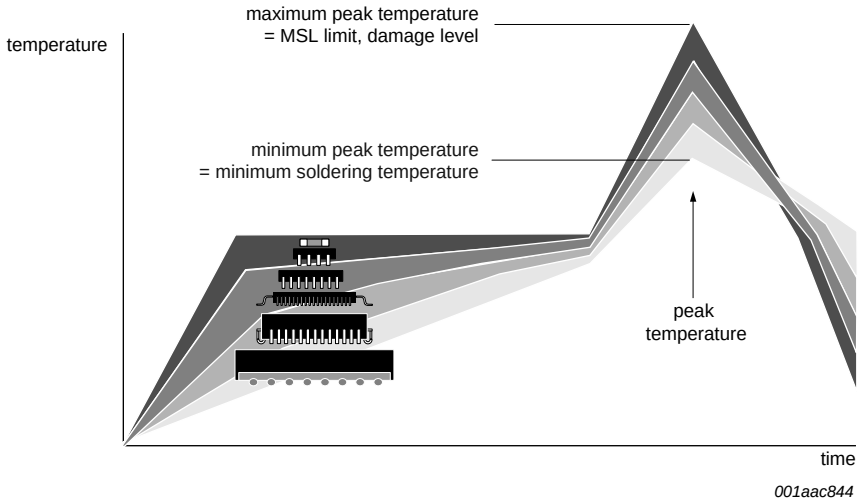
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 72. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 33.



MSL: Moisture Sensitivity Level

Fig 33. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

19. Abbreviations

Table 73. Abbreviations

Acronym	Description
AD	ADdress
ASIC	Application-Specific Integrated Circuit
ATX	Analog USB Transceiver
CD	Compact Disc
CDM	Charge Device Model
CD-RW	Compact Disc-ReWritable
D	Data
DDR	Dual Data Rate
DVD	Digital Video Disc
EMI	ElectroMagnetic Interference
EOP	End-Of-Packet
ESD	ElectroStatic Discharge
ESR	Effective Series Resistance
FPGA	Field Programmable Gate-Array
FS	Full-Speed
HBM	Human Body Model
HNP	Host Negotiation Protocol
HS	High-Speed
ID	IDentification

Table 73. Abbreviations *...continued*

Acronym	Description
IEC	International Electrotechnical Commission
I/O	Input/Output
LS	Low-Speed
MM	Machine Model
MO	Magneto-Optical
MPEG	Motion Picture Experts Group
NOOP	NO OPeration
NOPID	NO Packet IDentifier
NRZI	Non-Return-to-Zero Inverted
NXT	NeXT signal
OTG	On-The-Go
PCB	Printed-Circuit Board
PDA	Personal Digital Assistant
PHY	PHYsical; see also Section 20
PID	Packet IDentifier
PLD	Programmable Logic Device
PLL	Phase-Locked Loop
POR	Power-On Reset
RoHS	Restriction of Hazardous Substances
ROM	Read-Only Memory
RXCMD	Receive CoMmanD
RXD	Receive Data
SDR	Single Data Rate
SE0	Single-Ended Zero
SMD	Surface Mount Device
SOC	System-On-Chip
SOF	Start-Of-Frame
SRP	Session Request Protocol
STB	Set-Top Box
STP	SToP signal
SYNC	SYNChronous
TTL	Transistor-Transistor Logic
TV	TeleVision
TXCMD	Transmit CoMmanD
TXD	Transmit Data
UART	Universal Asynchronous Receiver-Transmitter
ULPI	UTMI+ Low Pin Interface
USB	Universal Serial Bus
USB-IF	USB Implementers Forum
UTMI	USB Transceiver Macrocell Interface

Table 73. Abbreviations *...continued*

Acronym	Description
UTMI+	USB Transceiver Macrocell Interface Plus
WLCSP	Wafer-Level Chip-Scale Package
XTAL	CrysTAL

20. Glossary

A-device — An OTG device with an attached micro-A plug.

B-device — An OTG device with an attached micro-B plug.

Link — ASIC, SOC or FPGA that contains the USB host or peripheral core.

PHY — Physical layer containing the USB transceiver.

Chirp — A signal with increasing or decreasing frequency.

MP3 — Shorthand notation the audio encoding format MPEG-1 audio layer 3.

On-chip pad — On-chip contact, which many times includes some circuitry as well.

RX — A common abbreviation from telegraphy for receive.

Squelch — Complete suppression of an unwanted signal.

Transceiver — A device which can both transmit and receive data.

TX — An abbreviation in communications for transmit or transmission, sometimes for transceiver.

21. References

[1] Universal Serial Bus Specification Rev. 2.0

[2] On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3

[3] ECN_27%_Resistor

[4] UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1

[5] UTMI+ Specification Rev. 1.0

[6] USB 2.0 Transceiver Macrocell Interface (UTMI) Specification Ver. 1.05

[7] Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) (JESD22-A114D)

[8] Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM) (JESD22-A115-A)

[9] Field-Induced Charged-Device Model Test Method for Electrostatic Discharge-Withstand Thresholds of Microelectronic Components (JESD22-C101C)

[10] Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test (IEC 61000-4-2)

22. Revision history

Table 74. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SAF1508 v.2	20120723	Product data sheet	-	SAF1508 v.1
Modifications:	• Limit application to automotive use			
SAF1508BET_1	20090611	Product data sheet	-	-

23. Legal information

23.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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25. Tables

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