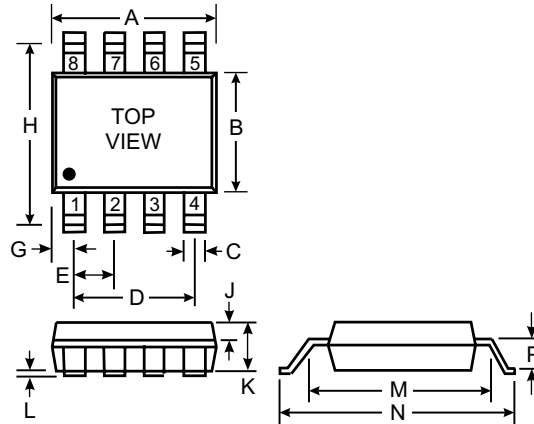


**SINGLE P-CHANNEL ENHANCEMENT MODE
FIELD EFFECT TRANSISTOR**

Features

- High Cell Density DMOS Technology
- Lower On-State Resistance
- High Power and Current Capability
- Fast Switching Speed
- High Transient Tolerance



SO-8		
Dim	Min	Max
A	3.94	4.19
B	3.20	3.40
C	0.381	0.495
D	2.67	3.05
E	0.89	1.02
G	0.527	0.679
J	0.41 Nominal	
K	0.94	1.09
L	0.025	0.152
M	4.37	4.62
N	4.39	4.70
P	0.939 Nominal	
All Dimensions in mm		

Mechanical Data

- SO-8 Plastic Case
- Terminal Connections: See Outline Drawing and Internal Circuit Diagram above

Maximum Ratings 25°C unless otherwise specified

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V_{bss}	-30	V
Gate-Source Voltage	V_{gss}	± 20	V
Drain Current	I_D	± 3.4 ± 10	A
Maximum Power Dissipation	P_d	2.5 1.2 1.0	W
Operating and Storage Temperature Range	T_j, T_{STG}	-55 to +150	°C

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	°C/W
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	25	°C/W

Notes: 1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance ($R_{\theta JC} + R_{\theta CA}$) where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ in this instance is 25°C/W but is dependent on the specific circuit board thermal design.

- 1a. With 1 in² of 2 oz. copper mounting pad $R_{\theta JA} = 50^\circ\text{C/W}$.
- 1b. With 0.04 in² of 2 oz. copper mounting pad $R_{\theta JA} = 105^\circ\text{C/W}$.
- 1c. With 0.006 in² of 2 oz. copper mounting pad $R_{\theta JA} = 125^\circ\text{C/W}$.

Electrical Characteristics

25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	-30	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
Zero Gate Voltage Drain Current $T_j = 55^\circ C$	I_{DSS}	—	—	-2.0 -25	μA	$V_{DS} = -24V, V_{GS} = 0V$
Gate-Body Leakage, Forward	I_{GSSF}	—	—	100	nA	$V_{GS} = 20V, V_{DS} = 0V$
Gate-Body Leakage, Reverse	I_{GSSR}	—	—	-100	nA	$V_{GS} = -20V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage $T_j = 125^\circ C$	$V_{GS(th)}$	-1.0 -0.85	-1.60 -1.25	-2.8 -2.5	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
Static Drain-Source On-Resistance $T_j = 125^\circ C$	$R_{DS(ON)}$	—	0.11 0.15 0.17 0.24	0.13 0.21 0.20 0.32	Ω	$V_{GS} = -10V, I_D = -1.0A$ $V_{GS} = -10V, I_D = -1.0A$ $V_{GS} = -4.5V, I_D = -0.5A$ $V_{GS} = -4.5V, I_D = -0.5A$
On-State Drain Current	$I_{D(ON)}$	-10	—	—	A	$V_{GS} = -10V, V_{DS} = -5V$
Forward Transconductance	g_{FS}	—	4.0	—	m	$V_{DS} = -15V, I_D = -3.4A$
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	—	350	—	pF	$V_{DS} = -10V, V_{GS} = 0V$ $f = 1.0MHz$
Output Capacitance	C_{OSS}	—	260	—	pF	
Reverse Transfer Capacitance	C_{RSS}	—	100	—	pF	
SWITCHING CHARACTERISTICS (Note 2)						
Turn-On Delay Time	$t_{D(ON)}$	—	9.0	40	ns	$V_{DD} = -10V, I_D = -1.0A$ $V_{GEN} = -10V, R_{GEN} = 6.0\Omega$
Turn-On Rise Time	t_r	—	21	40	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	21	90	ns	
Turn-Off Fall Time	t_f	—	8.0	50	ns	
Total Gate Charge	Q_g	—	10	25	nC	$V_{DS} = -10V, I_D = -3.4A$ $V_{GS} = -10V$
Gate-Source Charge	Q_{gs}	—	1.6	—	nC	
Gate-Drain Charge	Q_{gd}	—	3.4	—	nC	
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Max Continuous Drain-Source Diode Forward Current	I_S	—	—	-1.9	A	
Drain-Source Diode Forward Voltage	V_{SD}	—	-0.8	-1.3	V	$V_{GS} = 0V, I_S = -1.25A$ (Note 2)
Reverse Recovery Time	t_{rr}	—	—	100	ns	$V_{GS} = 0V, I_F = -2.0A$ $di_F/dt = 100A/\mu s$
Reverse Recovery Current	I_{rr}	—	1.9	—	A	

Notes: 2. Pulse Test: Pulse width $\geq 300\mu s$, duty cycle $\leq 2.0\%$.

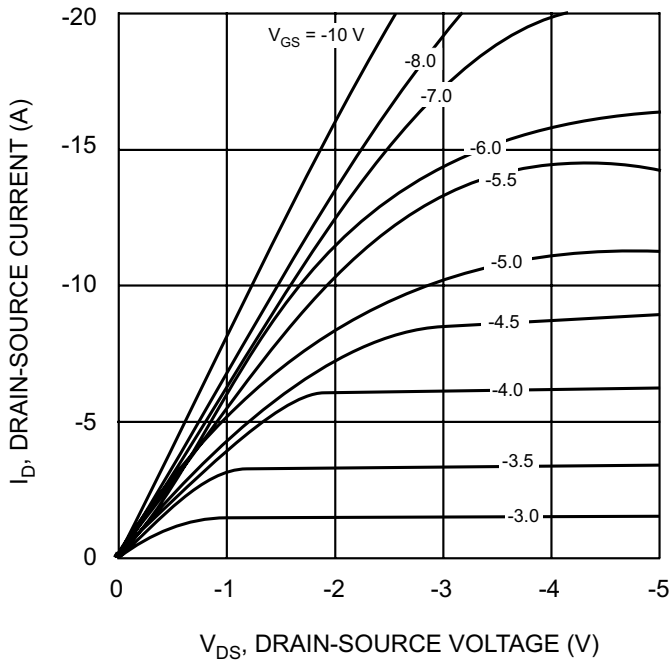


Fig. 1 On-Region Characteristics

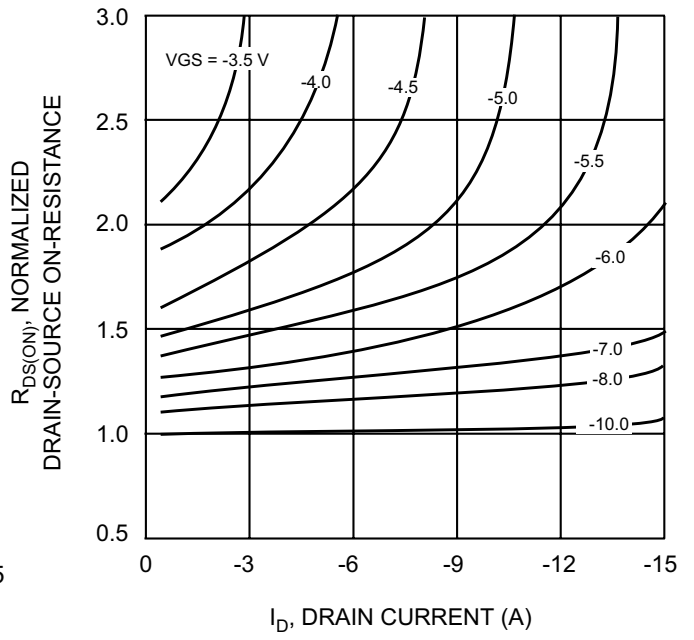


Fig. 2 On-Resistance vs Gate Voltage & Drain Current

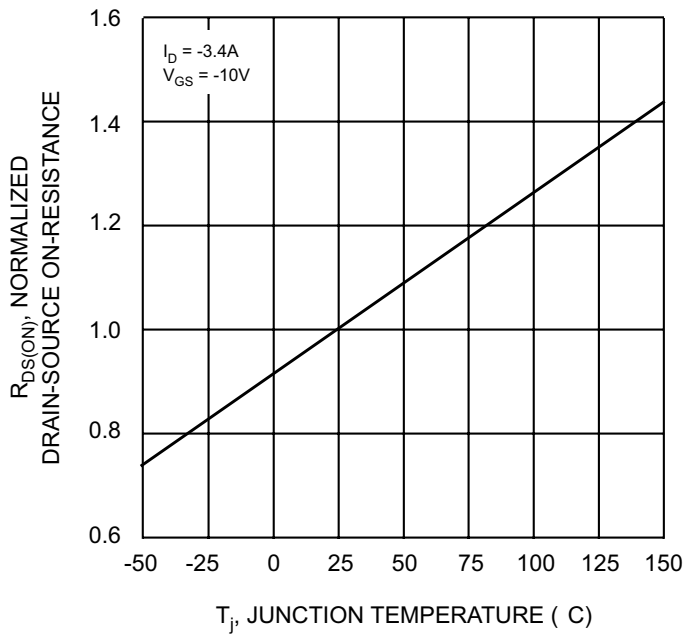


Fig. 3 On-Resistance vs Junction Temperature

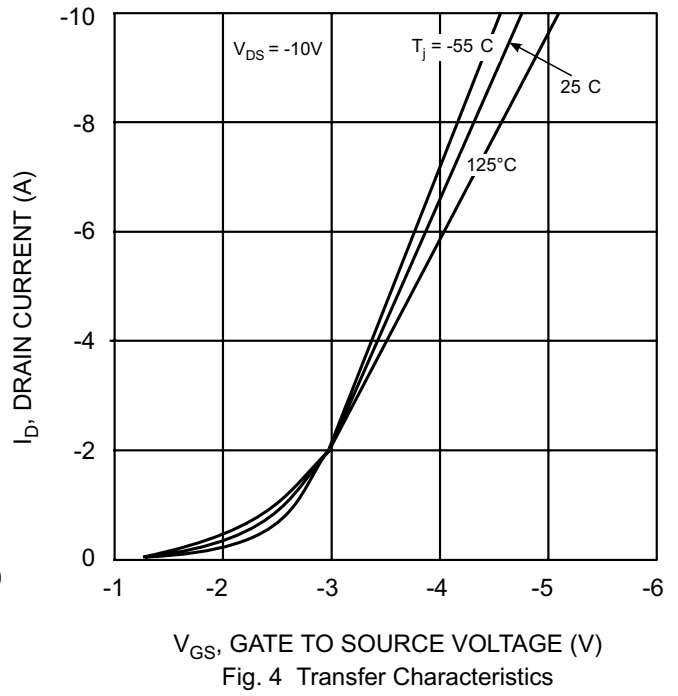
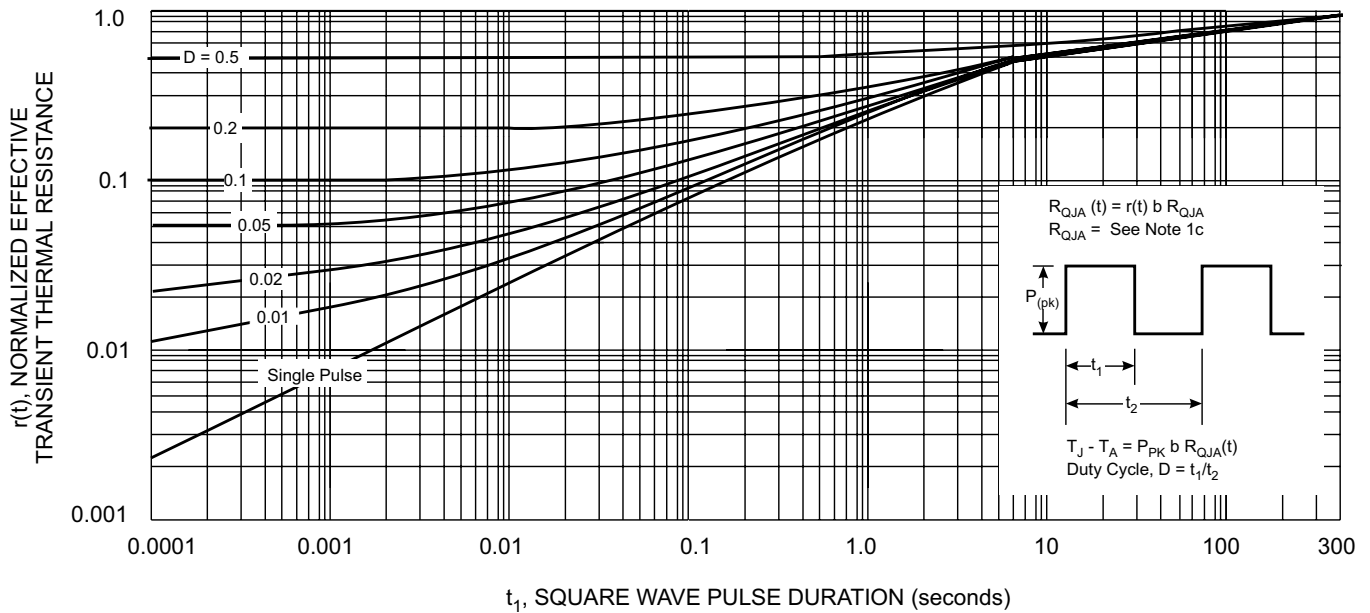
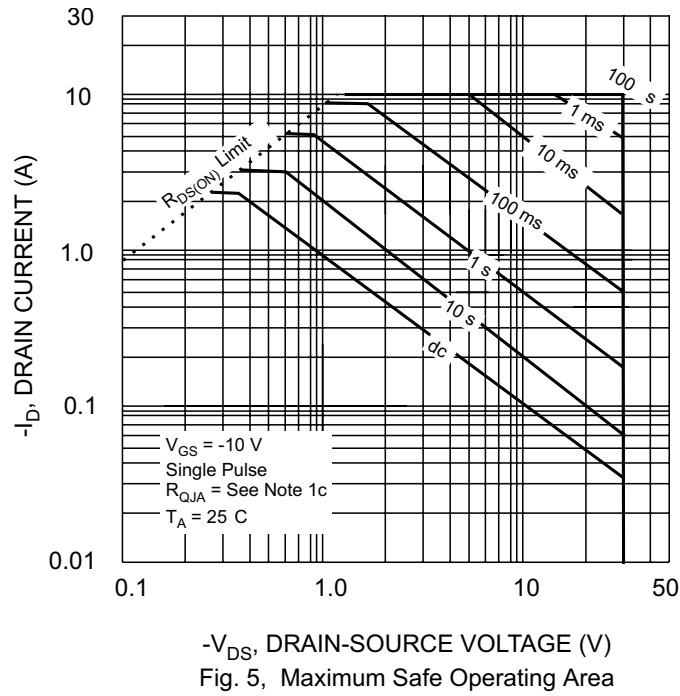


Fig. 4 Transfer Characteristics



Remark: Thermal characterization performed under conditions of Note 1c. Better thermal design such as shown in Notes 1a and 1b or 1d will offer lower R_{QJA} values and allow junction to reach thermal equilibrium sooner.