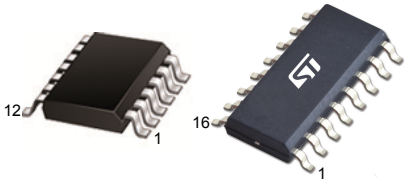
# VND5T100LAJ-E, VND5T100LAS-E

Datasheet

## Double channel high-side driver with analog current sense for 24 V automotive applications




**PowerSSO-12** **SO-16N**

| Product status links |
|---|
| VND5T100LAJ-E |
| VND5T100LAS-E |

## Features

| Description | Parameter | Value |
|---|---|---|
| Max. transient supply voltage | $V_{CC}$ | 58 V |
| Operating voltage range | $V_{CC}$ | 8 to 36 V |
| Typ. on-state resistance (per channel) | $R_{ON}$ | 100 mΩ |
| Current limitation (typ.) | $I_{LIM}$ | 22 A |
| Off-state supply current | $I_S$ | 2 µA(1) |

1. *Typical value with all loads connected.*

- AEC-Q100 qualified
- General
  - Very low standby current
  - 3.0 V CMOS compatible input
  - Optimized electromagnetic emission
  - Very low electromagnetic susceptibility
  - Compliant with European directive 2002/95/EC
  - Fault reset standby pin (FR_Stby)
  - Optimized for LED application
- Diagnostic functions
  - Proportional load current sense
  - High current sense precision for wide range currents
  - Off-state openload detection
  - Output short to $V_{CC}$ detection
  - Overload and short to ground latch-off
  - Thermal shutdown latch-off
  - Very low current sense leakage
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of $V_{CC}$
  - Thermal shutdown
  - Electrostatic discharge protection

## Applications

- All types of resistive, inductive and capacitive loads

## Description

The VND5T100LAJ-E and VND5T100LAS-E are monolithic devices made using STMicroelectronics VIPower technology, intended for driving resistive or inductive loads with one side connected to the ground. Active $V_{CC}$ pin voltage clamp protects the device against low energy spikes.

These devices integrate an analog current sense, which delivers a current proportional to the load current.

Fault conditions such as overload, overtemperature, or short to $V_{CC}$ are reported via the current sense pin.

Output current limitation protects the devices in overload conditions. The device latches off in case of overload or thermal shutdown.

The devices are reset by a low level pass on the fault reset standby pin.

A permanent low level on the inputs and on the fault reset standby pin disables all outputs and sets the device in standby mode.

# 1 Block diagram and pin description

**Figure 1. Block diagram**

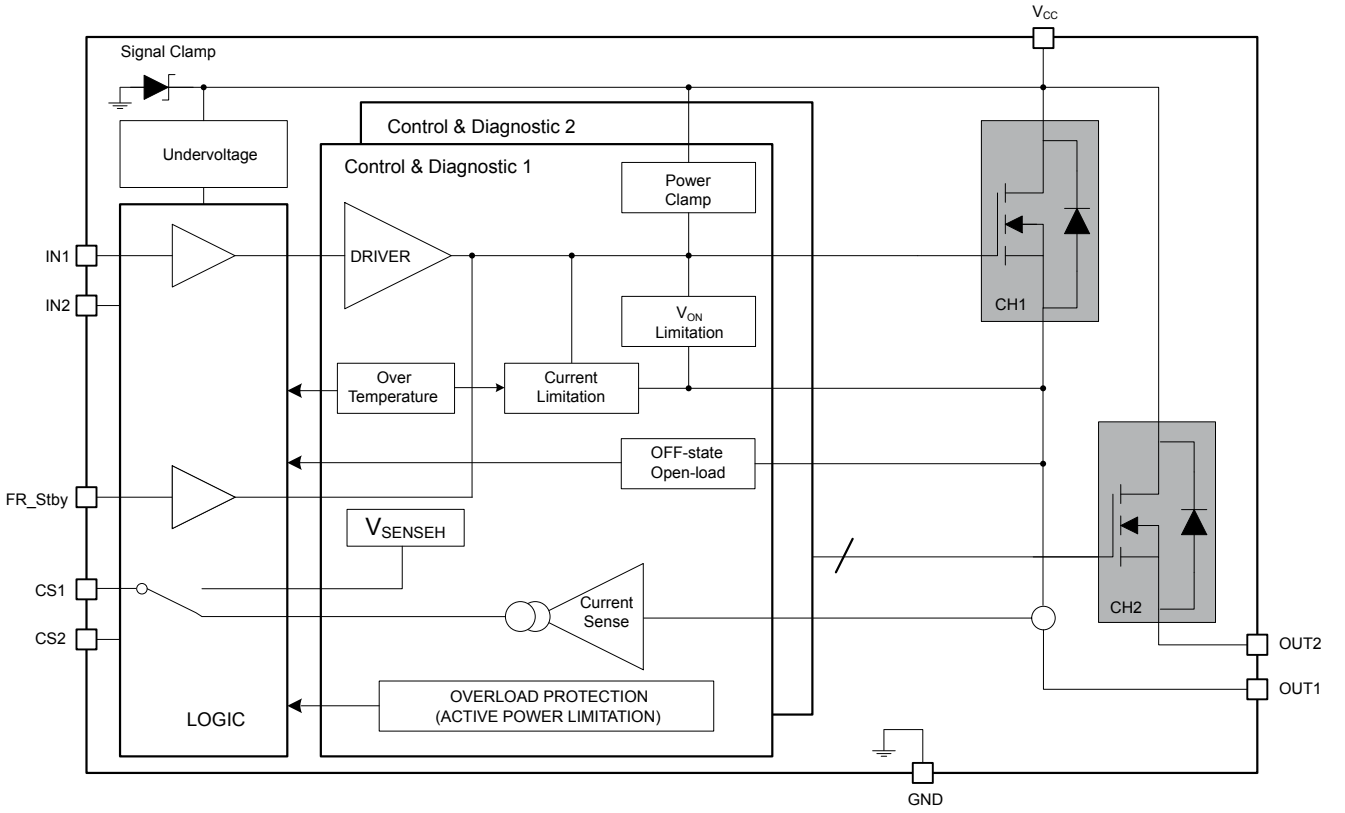



**Table 1. Pin function**

| Name | Function |
|---|---|
| $V_{CC}$ | Battery connection. |
| OUT1, 2 | Power outputs. |
| GND | Ground connection. |
| IN1, 2 | Voltage controlled input pins with hysteresis, CMOS compatible. They control output switch state. |
| CS1, 2 | Analog current sense pins, they deliver a current proportional to the load current. |
| FR_Stby | In case of latch-off for overtemperature/overcurrent condition, a low pulse on the FR_Stby pin is needed to reset the channel.<br>The device enters in standby mode if all inputs and the FR_Stby pin are low. |

**Figure 2. Configuration diagram PowerSSO-12 (top view)**

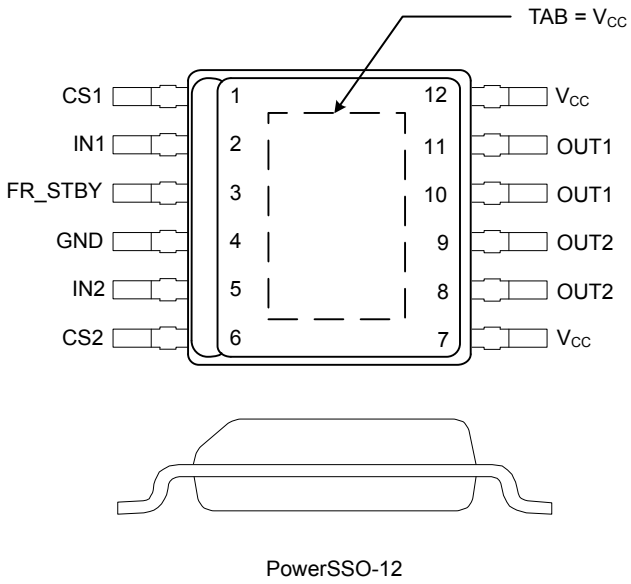



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**Figure 3. Configuration diagram SO-16N (top view)**

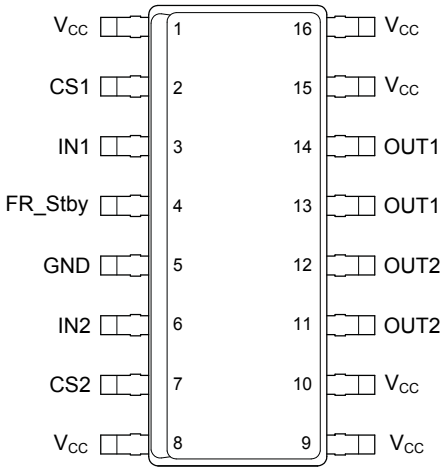


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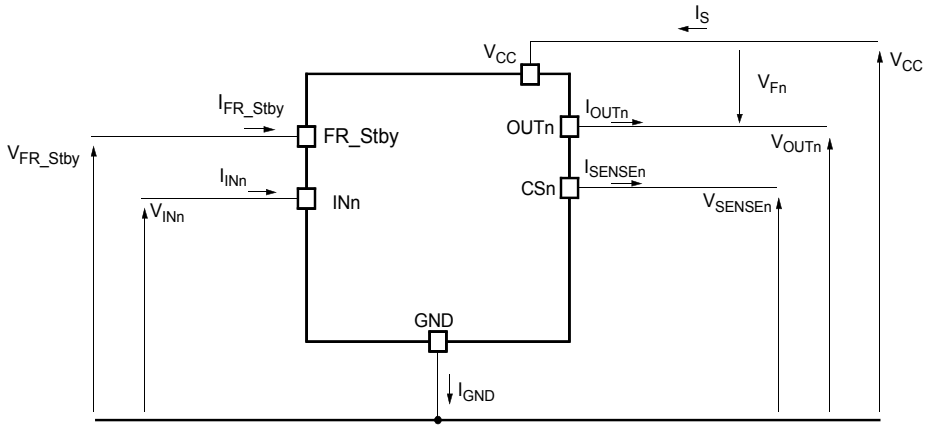
**Table 2. Suggested connections for unused and not connected pins**

| Connection/pin | CurrentSense | NC | Output | Input | FR_Stby |
|---|---|---|---|---|---|
| Floating | Not allowed | X(1) | X | X | X |
| To ground | Through 10 kΩ resistor | X | Not allowed | Through 10 kΩ resistor | Through 10 kΩ resistor |

1. *X: do not care.*

# 2 Electrical specification

Figure 4. **Current and voltage conventions**

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## 2.1 Absolute maximum ratings

Stressing the device above the ratings listed in the Table 3 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions reported in this section for extended periods may affect device reliability.

Table 3. **Absolute maximum ratings**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage | | 58 | V |
| $-V_{CC}$ | Reverse DC supply voltage | | 0.3 | V |
| $-I_{GND}$ | DC reverse ground pin current | | 200 | mA |
| $I_{OUT}$ | DC output current | | Internally limited | A |
| $-I_{OUT}$ | Reverse DC output current | | 20 | A |
| $I_{IN}$ | DC input current | | -1 to 10 | mA |
| $I_{FR\_Stby}$ | Fault reset standby DC input current | | -1 to 1.5 | mA |
| $-I_{CSENSE}$ | DC reverse CS pin current | | 200 | mA |
| $V_{CSENSE}$ | Current sense maximum voltage | | ($V_{CC}$ - 58) to $V_{CC}$ | V |
| $E_{MAX}$ | Maximum switching energy ($L$ = 1.9 mH; $V_{BAT}$ = 32 V; $T_{Jstart}$ = 150 °C; $I_{OUT}$ = $I_{limL\ (typ.)}$) | | 70 | mJ |
| $L_{smax}$ | Maximum stray inductance in short circuit condition $R_L$ = 300 mΩ, $V_{BAT}$ = 32 V, $T_{Jstart}$ = 150 °C, $I_{OUT}$ = $I_{limH\ (max.)}$ | | 40 | µH |
| $V_{ESD}$ | Electrostatic discharge (human body model: R = 1.5 kΩ, C = 100 pF) | IN1, 2 | 4000 | V |
| | | CS1, 2 | 2000 | |
| | | FR_Stby | 4000 | |
| | | OUT1, 2 | 5000 | |
| | | $V_{CC}$ | 5000 | |
| $V_{ESD}$ | Charge device model (CDM-AEC-Q100-011) | | 750 | V |
| $T_J$ | Junction operating temperature | | -40 to 150 | °C |

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $T_{stg}$ | Storage temperature | -55 to 150 | °C |

## 2.2 Thermal data

**Table 4. Thermal data**

| Symbol | Parameter | Maximum value | | Unit |
|---|---|---|---|---|
| | | PowerSSO-12 | SO-16N | |
| $R_{thJC}$ | Thermal resistance, junction-to-case (with one channel ON) | 6 | | °C/W |
| $R_{thJP}$ | Thermal resistance junction-pin (with one channel ON) | | 26 | °C/W |
| $R_{thJA}$ | Thermal resistance, junction-to-ambient | See Figure 28 | See Figure 32 | °C/W |

## 2.3 Electrical characteristics

8 V < $V_{CC}$ < 36 V, -40 °C < $T_J$ < 150 °C, unless otherwise specified.

**Table 5. Power section**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Operating supply voltage | | 8 | 24 | 36 | V |
| $V_{USD}$ | Undervoltage shutdown | | | 3.5 | 5 | V |
| $V_{USDhyst}$ | Undervoltage shutdown hysteresis | | | 0.5 | | V |
| $R_{ON}$ | On-state resistance(1) | $I_{OUT}$ = 1.5 A, $T_J$ = 25 °C | | 100 | | mΩ |
| | | $I_{OUT}$ = 1.5 A, $T_J$ = 150 °C | | | 200 | |
| $V_{clamp}$ | Clamp voltage | $I_S$ = 20 mA | 58 | 64 | 70 | V |
| $I_S$ | Supply current | Off-state, $V_{CC}$ = 24 V, $T_J$ = 25 °C, $V_{IN}$ = $V_{OUT}$ = $V_{SENSE}$ = 0 V, $V_{FR\_Stby}$ = 0 V | | 2(2) | 5(2) | µA |
| | | On-state, $V_{CC}$ = 24 V, $V_{IN}$ = 5 V, $I_{OUT}$ = 0 A | | 4.2 | 6 | mA |
| $I_{L(off)}$ | Off-state output current | $V_{IN}$ = $V_{OUT}$ = 0 V, $V_{CC}$ = 24 V, $T_J$ = 25 °C | 0 | 0.01 | 3 | µA |
| | | $V_{IN}$ = $V_{OUT}$ = 0 V, $V_{CC}$ = 24 V, $T_J$ = 125 °C | 0 | | 5 | |
| $V_F$ | Output - $V_{CC}$ diode voltage | -$I_{OUT}$ = 1.5 A, $T_J$ = 150 °C | | | 0.7 | V |

1. *For each channel.*
2. *Power MOSFET leakage included.*

**Table 6. Switching ($V_{CC}$ = 24 V, $T_J$ = 25 °C)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $R_L$ = 16 Ω | | 27 | | µs |
| $t_{d(off)}$ | Turn-off delay time | $R_L$ = 16 Ω | | 38 | | µs |
| $(dV_{OUT}/dt)_{(on)}$ | Turn-on voltage slope | $R_L$ = 16 Ω | | 1 | | V/µs |
| $(dV_{OUT}/dt)_{(off)}$ | Turn-off voltage slope | $R_L$ = 16 Ω | | 0.65 | | V/µs |
| $W_{ON}$ | Switching energy losses during $t_{won}$ | $R_L$ = 16 Ω | | 0.23 | | mJ |
| $W_{OFF}$ | Switching energy losses during $t_{woff}$ | $R_L$ = 16 Ω | | 0.26 | | mJ |

**Table 7. Logic inputs**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low level voltage | | | | 0.9 | V |
| $I_{IL}$ | Low level input current | $V_{IN}$ = 0.9 V | 1 | | | µA |
| $V_{IH}$ | Input high level voltage | | 2.1 | | | V |
| $I_{IH}$ | High level input current | $V_{IN}$ = 2.1 V | | | 10 | µA |
| $V_{I(hyst)}$ | Input hysteresis voltage | | 0.25 | | | V |

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{ICL}$ | Input clamp voltage | $I_{IN}$ = 1 mA | 5.5 | | 7 | V |
| | | $I_{IN}$ = -1 mA | | -0.7 | | |
| $V_{FR\_Stby\_L}$ | Fault_reset_standby low level voltage | | | | 0.9 | V |
| $I_{FR\_Stby\_L}$ | Low level fault_reset_standby current | $V_{FR\_Stby}$ = 0.9 V | 1 | | | µA |
| $V_{FR\_Stby\_H}$ | Fault_reset_standby high level voltage | | 2.1 | | | V |
| $I_{FR\_Stby\_H}$ | High level fault_reset_standby current | $V_{FR\_Stby}$ = 2.1 V | | | 10 | µA |
| $V_{FR\_Stby(hyst)}$ | Fault_reset_standby hysteresis voltage | | 0.25 | | | V |
| $V_{FR\_Stby\_CL}$ | Fault_reset_standby clamp voltage | $I_{FR\_Stby}$ = 15 mA (t < 10 ms) | 11 | | 15 | V |
| | | $I_{FR\_Stby}$ = -1 mA | | -0.7 | | V |
| $t_{reset}$ | Overload latch-off reset time | See Figure 5 | 2 | | 24 | µs |
| $t_{stby}$ | Standby delay | See Figure 6 | 120 | | 1200 | µs |

**Figure 5. $t_{reset}$ definition**

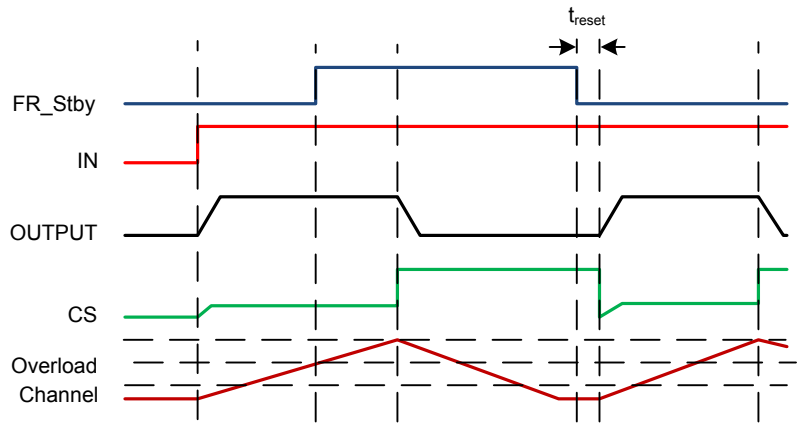


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**Figure 6. $t_{stby}$ definition**

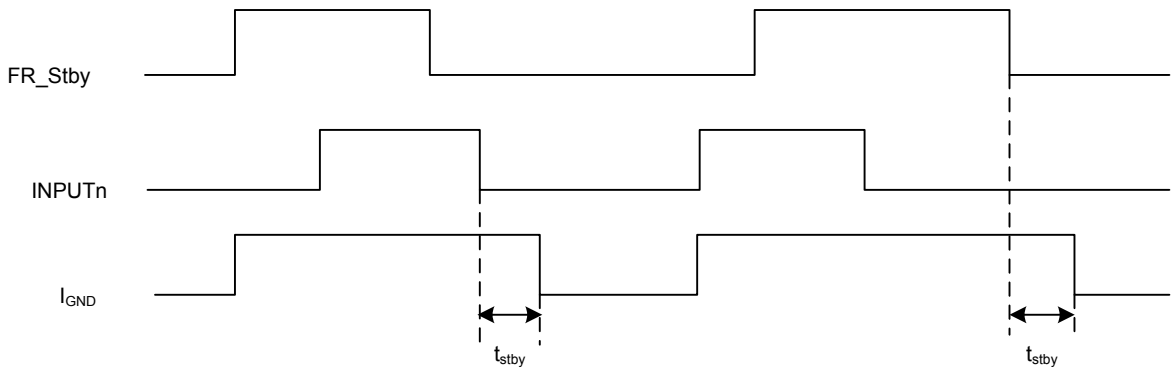


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**Table 8. Protections and diagnostics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{limH}$ | DC short circuit current | $V_{CC}$ = 24 V | 16 | 22 | 30 | A |
| | | 5 V < $V_{CC}$ < 36 V | | | 30 | |
| $I_{limL}$ | Short circuit current during thermal cycling | $V_{CC}$ = 24 V, $T_R$ < $T_J$ < $T_{TSD}$ | | 6 | | A |
| $T_{TSD}$ | Shutdown temperature | | 150 | 175 | 200 | °C |
| $T_R$ | Reset temperature | | $T_{RS}$ + 1 | $T_{RS}$ + 5 | | °C |
| $T_{RS}$ | Thermal reset of status | | 135 | | | °C |
| $T_{HYST}$ | Thermal hysteresis ($T_{TSD}$ - $T_R$) | | | 7 | | °C |
| $V_{DEMAG}$ | Turn-off output voltage clamp | $I_{OUT}$ = 1.5 A, $V_{IN}$ = 0 V, L = 6 mH | $V_{CC}$ - 58 | $V_{CC}$ - 64 | $V_{CC}$ - 70 | V |
| $V_{ON}$ | Output voltage drop limitation | $I_{OUT}$ = 50 A, $T_J$ = -40 °C to 150 °C | | 25 | | mV |

**Table 9. Current sense (8 V < $V_{CC}$ < 36 V)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $K_{OL}$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 12 mA, $V_{SENSE}$ = 0.5 V, $T_J$ = -40 °C to 150 °C | 833 | | | |
| $K_{LED}$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 50 mA, $V_{SENSE}$ = 0.5 V, $T_J$ = -40 °C to 150 °C | 1328 | 2190 | 3332 | |
| $dK_{LED}/K_{LEDTOT}$ (1) | Current sense ratio drift | $I_{OUT}$ = 12 mA to 25 mA, $I_{CAL}$ = 18 mA, $V_{SENSE}$ = 0.5 V, $T_J$ = -40 °C to 150 °C | -30 | | 30 | % |
| $K_0$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 100 mA, $V_{SENSE}$ = 0.5 V, $T_J$ = -40 °C to 150 °C | 1170 | 1950 | 2730 | |
| $dK_0/K_0$ (1) | Current sense ratio drift | $I_{OUT}$ = 100 mA, $V_{SENSE}$ = 0.5 V, $T_J$ = -40 °C to 150 °C | -18 | | 18 | % |
| $K_1$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 0.4 A, $V_{SENSE}$ = 1 V, $T_J$ = -40 °C to 150 °C | 1259 | 1740 | 2191 | |
| $dK_1/K_1$ (1) | Current sense ratio drift | $I_{OUT}$ = 0.4 A, $V_{SENSE}$ = 1 V, $T_J$ = -40 °C to 150 °C | -15 | | 15 | % |
| $K_2$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 0.8 A, $V_{SENSE}$ = 2 V, $T_J$ = -40 °C to 150 °C | 1372 | 1730 | 2058 | |
| $dK_2/K_2$ (1) | Current sense ratio drift | $I_{OUT}$ = 0.8 A, $V_{SENSE}$ = 2 V, $T_J$ = -40 °C to 150 °C | -12 | | 12 | % |
| $K_3$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 1.6 A, $V_{SENSE}$ = 2 V, $T_J$ = -40 °C to 150 °C | 1509 | 1720 | 1921 | |
| $dK_3/K_3$ (1) | Current sense ratio drift | $I_{OUT}$ = 1.6 A, $V_{SENSE}$ = 2 V, $T_J$ = -40 °C to 150 °C | -8 | | 8 | % |
| $K_4$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 6 A, $V_{SENSE}$ = 4 V, $T_J$ = -40 °C to 150 °C | 1646 | 1720 | 1784 | |
| $dK_4/K_4$ (1) | Current sense ratio drift | $I_{OUT}$ = 6 A, $V_{SENSE}$ = 4 V, $T_J$ = -40 °C to 150 °C | -4 | | 4 | % |
| $I_{SENSE0}$ | Analog sense leakage current | $I_{OUT}$ = 0 A, $V_{SENSE}$ = 0 V, $V_{IN}$ = 0 V, $T_J$ = -40 °C to 150 °C | 0 | | 1 | µA |
| | | $I_{OUT}$ = 0 A, $V_{SENSE}$ = 0 V, $V_{IN}$ = 5 V, $T_J$ = -40 °C to 150 °C | 0 | | 2 | |

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{SENSE}$ | Max analog sense output voltage | $I_{OUT}$ = 6 A, $R_{SENSE}$ = 3.9 kΩ | 5 | | | V |
| $V_{SENSEH}$ | Analog sense output voltage in fault condition(2) | $V_{CC}$ = 24 V, $R_{SENSE}$ = 3.9 kΩ | 7.5 | 8.5 | 9.5 | V |
| $I_{SENSEH}$ | Analog sense output current in fault condition(2) | $V_{CC}$ = 24 V, $V_{SENSE}$ = 5 V | 4.9 | 9 | 12 | mA |
| $t_{DSENSE2H}$ | Delay response time from rising edge of INPUT pins | $V_{SENSE}$ < 4 V, 0.07 A < $I_{OUT}$ < 6 A, $I_{SENSE}$ = 90% of $I_{SENSEMAX}$, (see Figure 7) | | 100 | 200 | µs |
| $\Delta t_{DSENSE2H}$ | Delay response time between rising edge of output current and rising edge of current sense | $V_{SENSE}$ < 4 V, $I_{SENSE}$ = 90 % of $I_{SENSEMAX}$, $I_{OUT}$ = 90 % of $I_{OUTMAX}$, $I_{OUTMAX}$ = 1.5 A (see Figure 11) | | | 150 | µs |
| $t_{DSENSE2L}$ | Delay response time from falling edge of INPUT pins | $V_{SENSE}$ < 4 V, 0.07 A < $I_{OUT}$ < 6 A, $I_{SENSE}$ = 10% of $I_{SENSEMAX}$, (see Figure 7) | | 5 | 20 | µs |

1. *Specified by design, not tested in production.*
2. *Fault condition includes: power limitation, overtemperature and openload in off-state condition.*

**Table 10. Openload detection ($V_{FR\_Stby}$ = 5 V)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OL}$ | Openload off-state voltage detection threshold | $V_{IN}$ = 0 V, 8 V < $V_{CC}$ < 36 V, $V_{FR\_Stby}$ = 5 V | 2 | - | 4 | V |
| $t_{DSTKON}$ | Output short circuit to $V_{CC}$ detection delay at turn off | $V_{FR\_Stby}$ = 5 V (see Figure 8) | 180 | - | 1800 | µs |
| $I_{L(off2)}$ | Off-state output current at $V_{OUT}$ = 4 V | $V_{IN}$ = 0 V, $V_{SENSE}$ = 0 V, $V_{OUT}$ rising from 0 V to 4 V, $V_{FR\_Stby}$ = 5 V | -120 | - | 0 | µA |
| $t_{d\_vol}$ | Delay response from output rising edge to $V_{SENSE}$ rising edge in openload | $V_{OUT}$ = 4 V, $V_{IN}$ = 0 V, $V_{SENSE}$ = 90 % of $V_{SENSEH}$, $R_{SENSE}$ = 3.9 kΩ, $V_{FR\_Stby}$ = 5 V | | - | 20 | µs |
| $t_{DFRSTK\_ON}$ | Output short circuit to $V_{CC}$ detection delay at FR_Stby activation | Input1, 2 = low (see Figure 10) | | - | 50 | µs |

**Figure 7. Current sense delay characteristics**

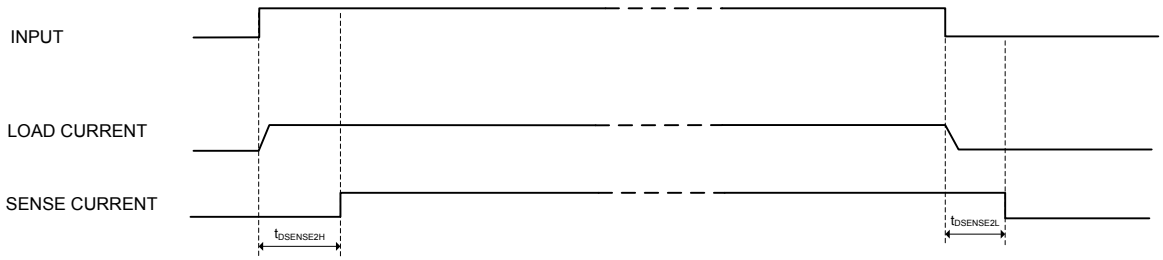


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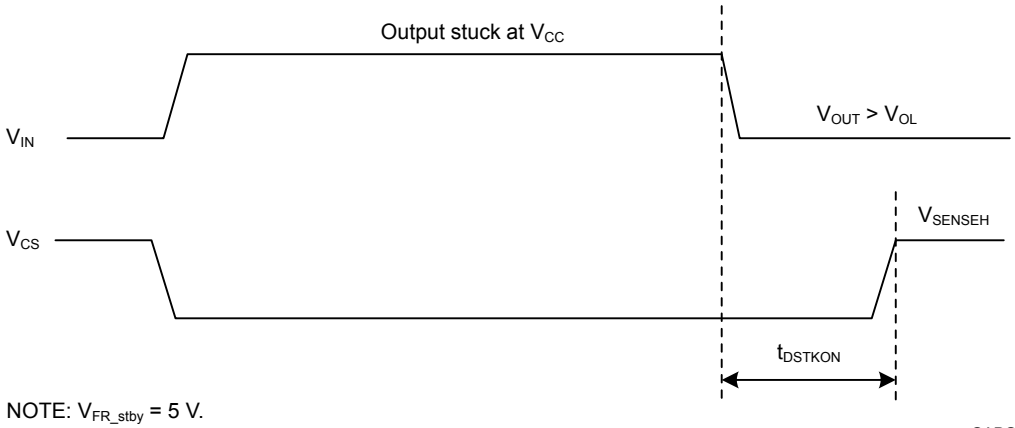
**Figure 8. Openload off-state delay timing**




NOTE: $V_{FR\_stby}$ = 5 V.

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Figure 9. **Switching characteristics**

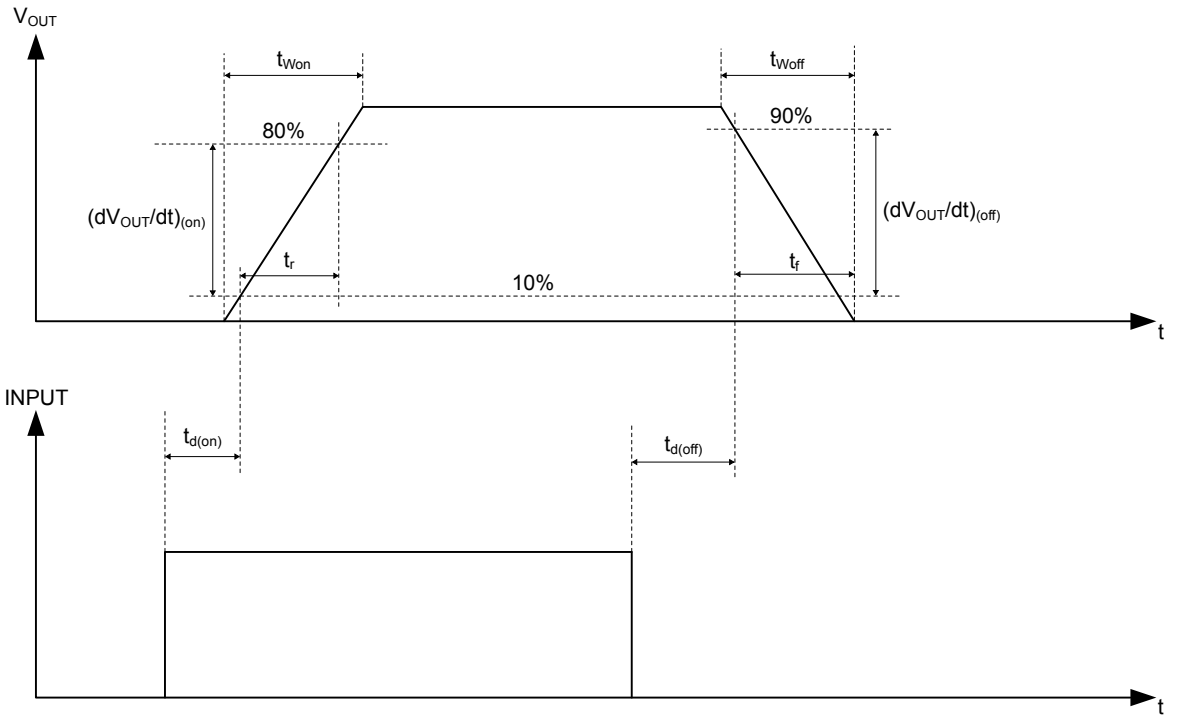


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Figure 10. **Output stuck to $V_{CC}$ detection delay time at FR_Stby activation**

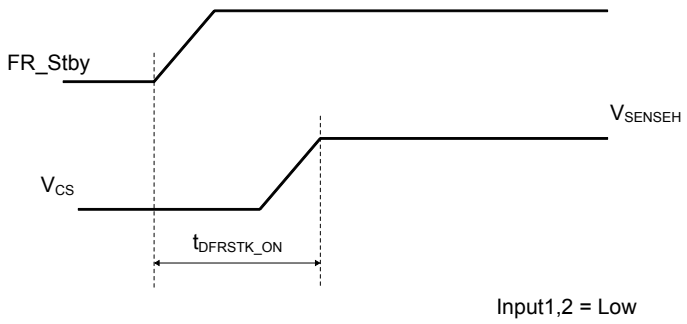


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**Figure 11. Delay response time between rising edge of ouput current and rising edge of current sense**

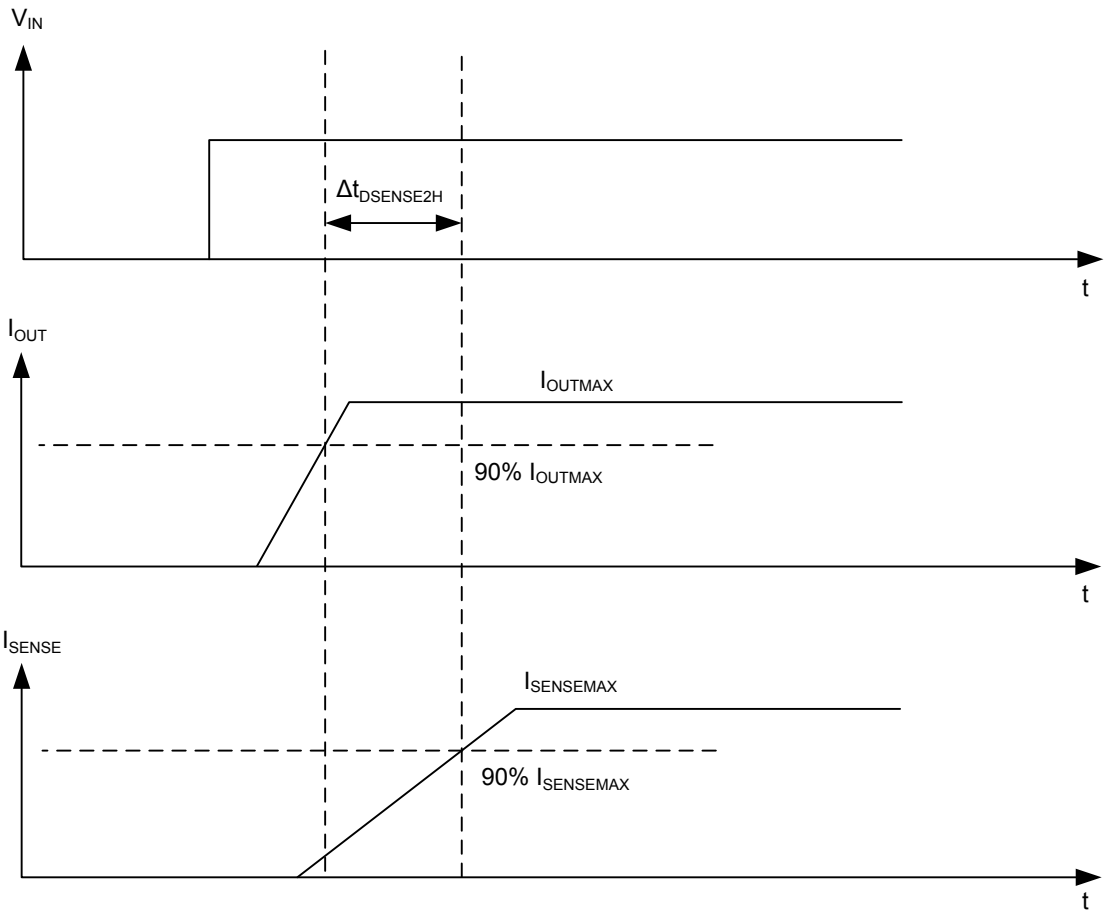


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**Figure 12. Output voltage drop limitation**

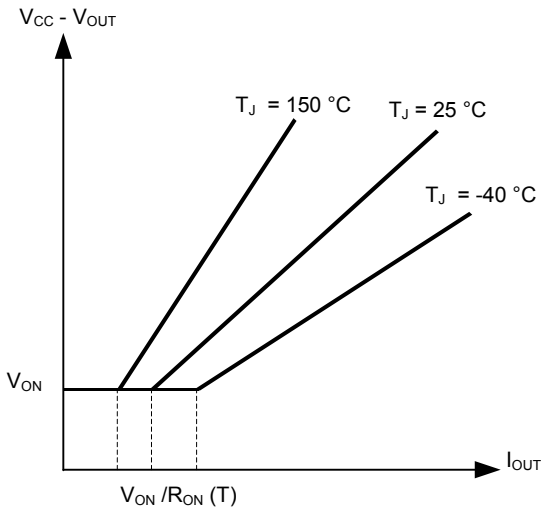


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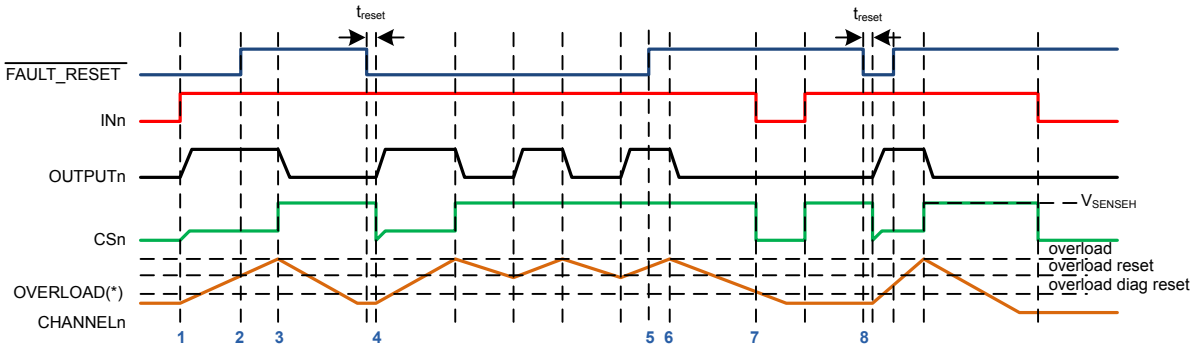
**Figure 13. Device behavior in overload condition**




1: OUTPUTn and CSn controlled by INn
2: FAULT_RESET from '0' to '1' → no action on CSn pin
3: overload latch-off. INn high → CSn high
4: FAULT_RESET low AND Temp channeln < overload_reset → overload latch reset after t_reset
4 to 5: FAULT_RESET low AND INn high → thermal cycling, CSn high
5: FAULT_RESET high → latch-off reset disabled
6 to 7: overload event and FAULT_RESET high → latch-off, no thermal cycling
7 to 8: overload diagnostic disabled/enabled by the input
8: overload latch-off reset by FAULT_RESET

(*) OVERLOAD = thermal shutdown OR power limitation

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**Table 11. Truth table**

| Conditions | Fault reset standby | Input | Output | Sense |
|---|---|---|---|---|
| Standby | L | L | L | 0 |
| Normal operation | X | L | L | 0 |
| | X | H | H | Nominal |
| Overload | X | L | L | 0 |
| | X | H | H | > Nominal |
| Overtemperature/short to ground | X | L | L | 0 |
| | L | H | Cycling | $V_{SENSEH}$ |
| | H | H | Latched | $V_{SENSEH}$ |
| Undervoltage | X | X | L | 0 |
| Short to $V_{BAT}$ | L | L | H | 0 |
| | H | L | H | $V_{SENSEH}$ |
| | X | H | H | < Nominal |
| Openload off-state (with pull-up) | L | L | H | 0 |
| | H | L | H | $V_{SENSEH}$ |
| | X | H | H | 0 |
| Negative output voltage clamp | X | L | Negative | 0 |

**Table 12. Electrical transient requirements (part 1)**

| ISO 7637-2: 2004 (E) Test pulse | Test levels(1) | | Number of pulses or test times | Burst cycle/pulse repetition time | | Delays and impedence |
|---|---|---|---|---|---|---|
| | III | IV | | | | |
| 1 | -450 V | -600 V | 5000 pulses | 0.5 s | 5 s | 1 ms, 50 Ω |
| 2a | 37 V | 50 V | 5000 pulses | 0.2 s | 5 s | 50 µs, 2 Ω |
| 3a | - 150 V | - 200 V | 1 h | 90 ms | 100 ms | 0.1 µs, 50 Ω |
| 3b | + 150 V | + 200 V | 1 h | 90 ms | 100 ms | 0.1 µs, 50 Ω |
| 4 | - 12 V | - 16 V | 1 pulse | | | 100 ms, 0.01 Ω |
| 5b(2) | + 123 V | + 174 V | 1 pulse | | | 350 ms, 1 Ω |

1. *The above test levels must be considered referred to $V_{CC}$ = 24.5 V except for pulse 5b.*
2. *Valid in case of external load dump clamp: 58 V maximum referred to ground.*

**Table 13. Electrical transient requirements (part 2)**

| ISO 7637-2: 2004 (E) Test pulse | Test level results | |
|---|---|---|
| | III | IV |
| 1 | C | C |
| 2a | C | C |
| 3a | C | C |
| 3b(1) | E | E |
| 3b(2) | C | C |
| 4 | C | C |
| 5b(3) | C | C |

1. *Without capacitor between $V_{CC}$ and GND.*
2. *With 10 nF between $V_{CC}$ and GND.*
3. *External load dump clamp, 58 V maximum, referred to ground.*

**Table 14. Electrical transient requirements (part 3)**

| Class | Contents |
|---|---|
| C | All functions of the device are performed as designed after exposure to disturbance. |
| E | One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device. |

## 2.4 Electrical characteristics (curves)

**Figure 14. Off-state output current**

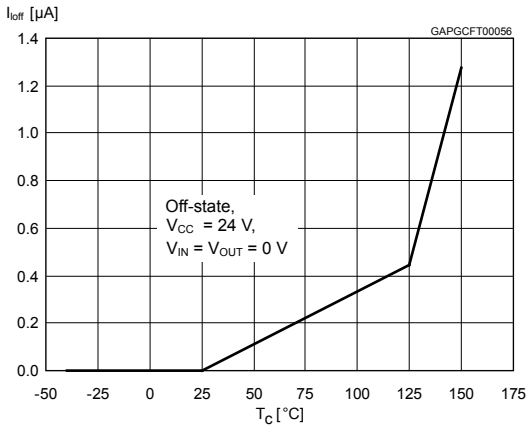



**Figure 15. High level input current**

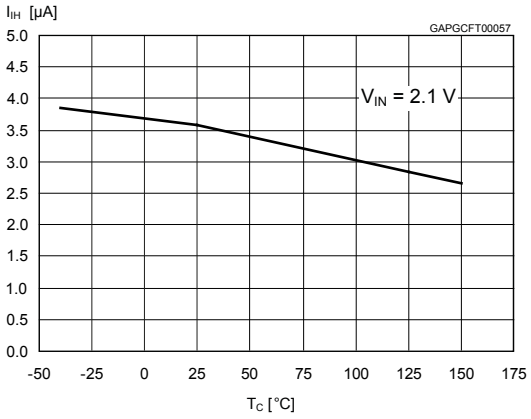



**Figure 16. Input clamp voltage**

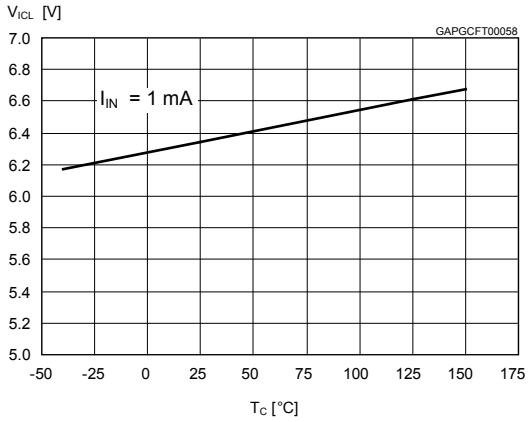



**Figure 17. Low level input voltage**

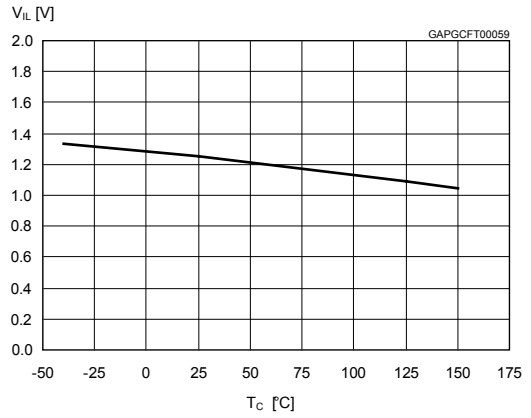



**Figure 18. High level input voltage**

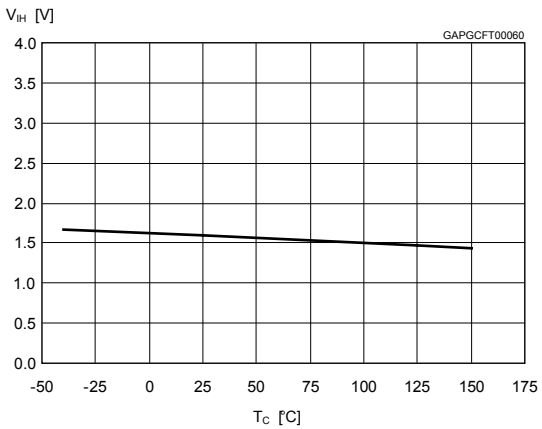



**Figure 19. Input hysteresis voltage**

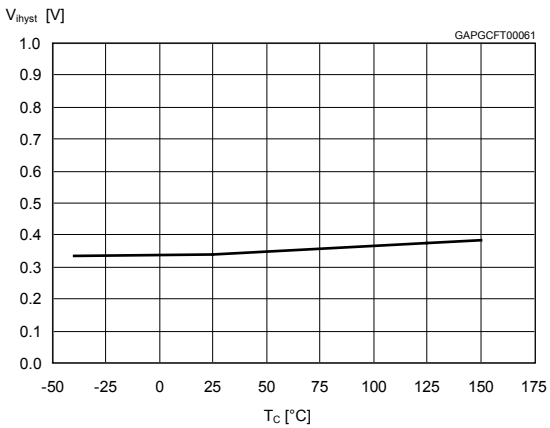


**Figure 20. On-state resistance vs $T_C$**

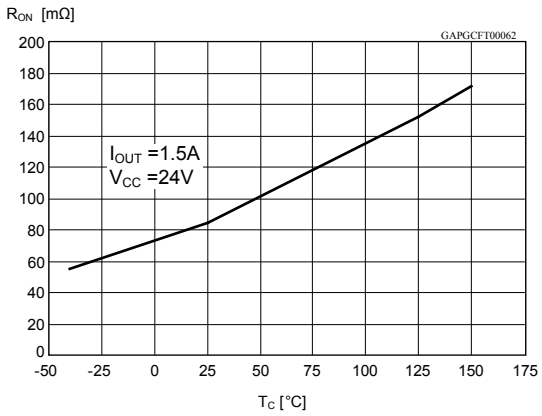



**Figure 21. On-state resistance vs $V_{CC}$**

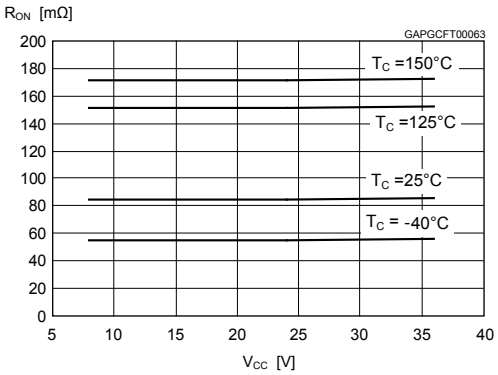



**Figure 22. Turn-on voltage slope**

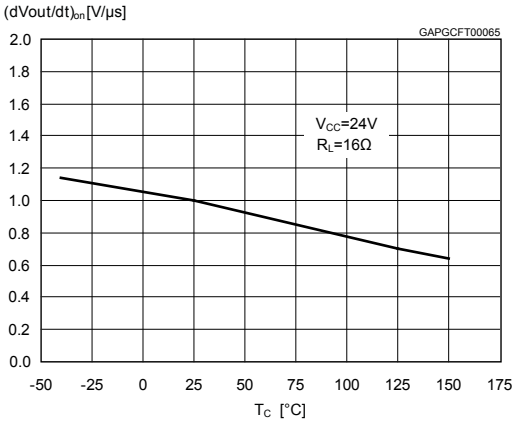



**Figure 23. Turn-off voltage slope**

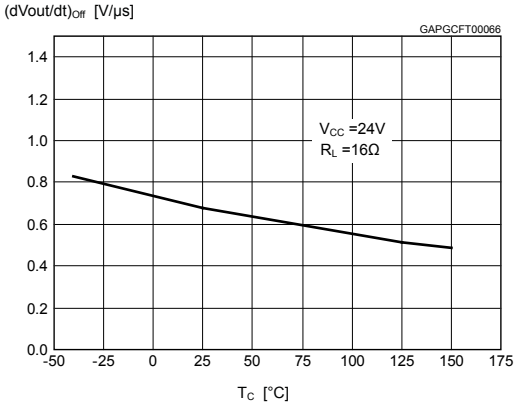
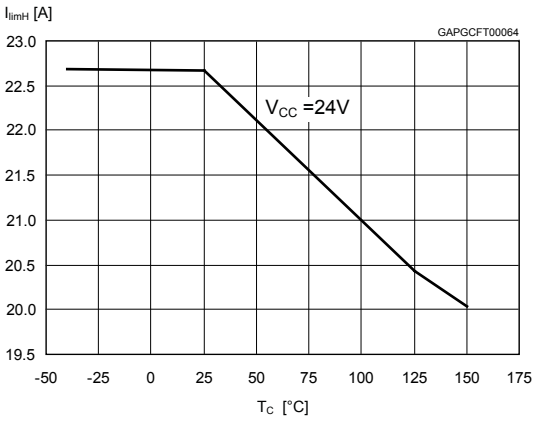
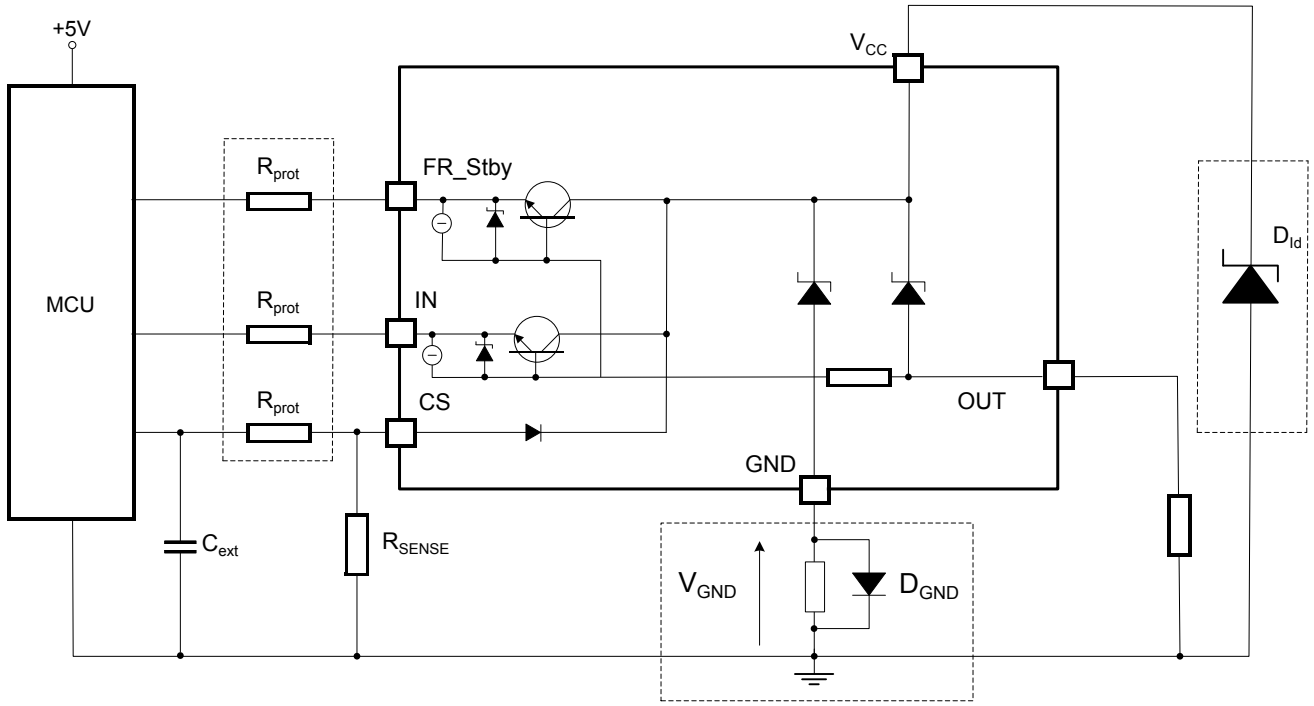



**Figure 24. $I_{LIMH}$ vs $T_C$**



# 3 Application information

Figure 25. **Application schematic**

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## 3.1 GND protection network against reverse battery

### 3.1.1 Solution 1: resistor in the ground line ($R_{GND}$ only)

This solution can be used with any load type.

The following is an indication on how to dimension the $R_{GND}$ resistor.

1. $R_{GND} \leq 600\ mV / (I_{S(on)max.})$
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

Where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in $R_{GND}$ (when $V_{CC} < 0$ V: during reverse battery situations) is:

$P_D = (-V_{CC})^2 / R_{GND}$

This resistor can be shared among several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max.}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the $R_{GND}$ produces a shift ($I_{S(on)max.} * R_{GND}$) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in the case of several high side drivers sharing the same $R_{GND}$.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor, then ST suggests solution 2 is used (see below).

### 3.1.2 Solution 2: diode ($D_{GND}$) in the ground line

A resistor ($R_{GND}$ = 4.7 kΩ) should be inserted in parallel to $D_{GND}$ if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift (≈600 mV) in the input threshold and in the status output values, if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

## 3.2 Load dump protection

$D_{ld}$ is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the $V_{CC}$ maximum DC rating. The same applies if the device is subject to transients on the $V_{CC}$ line that are greater than the ones shown in the ISO 7637-2 2004 (E) Table 12, Table 13 and Table 14.

## 3.3 MCU I/Os protection

If a ground protection network is used and negative transient is present on the $V_{CC}$ line, the control pins are pulled negative. ST suggests that a resistor ($R_{prot}$) has to be inserted in line to prevent the microcontroller I/Os pins from latching-up.

The value of these resistors is a compromise between the leakage current of the microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

**Equation: $R_{prot}$ range calculation**

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$

**Calculation example:**

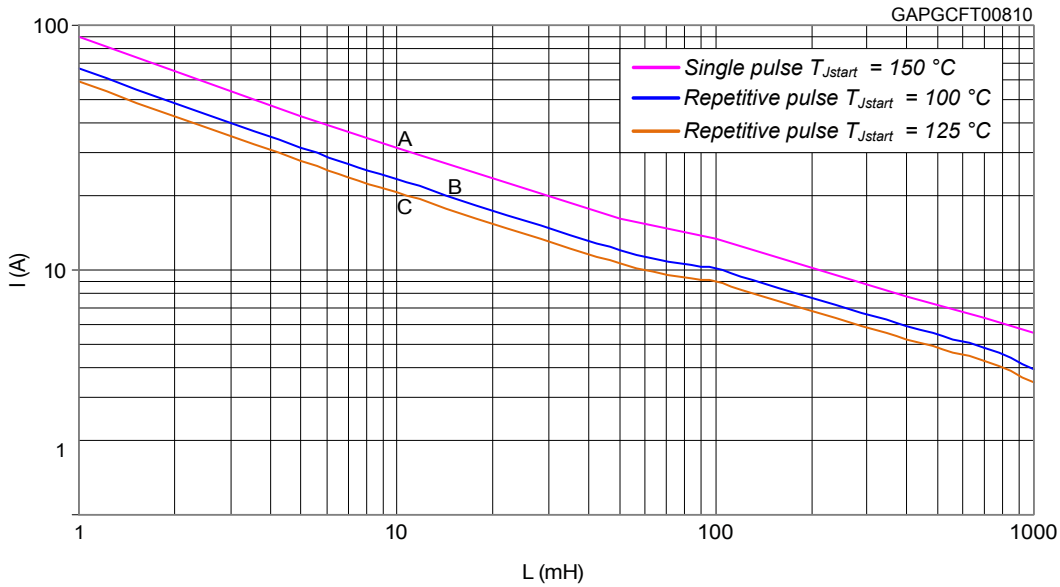
For $V_{CCpeak}$ = -600 V and $I_{latchup} \geq$ 20 mA; $V_{OH\mu C} \geq$ 4.5 V

30 kΩ ≤ $R_{prot}$ ≤ 180 kΩ.

Recommended value: $R_{prot}$ = 60 kΩ.

# 4 Maximum demagnetization energy ($V_{CC}$ = 24 V)

**Figure 26. Maximum turn off current versus inductance**




*Note: Values are generated with $R_L$ = 0 Ω. In case of repetitive pulses, $T_{Jstart}$ (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.*

# 5 Package and PCB thermal data

## 5.1 PowerSSO-12 thermal data

Figure 27. **PowerSSO-12 PCB**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Layout condition of $R_{th}$ and $Z_{th}$ measurements (board finish thickness 1.6 mm ±10%; board double layer; board dimension 77 mm x 86 mm; board material FR4; Cu thickness 0.070 mm (front and back side); thermal vias separation 1.2 mm; thermal via diameter 0.3 mm ±0.08 mm; Cu thickness on vias 0.025 mm; footprint dimension 4.1 mm x 6.5 mm).

Figure 28. **$R_{thJA}$ vs PCB copper area in open box free air condition (one channel ON)**

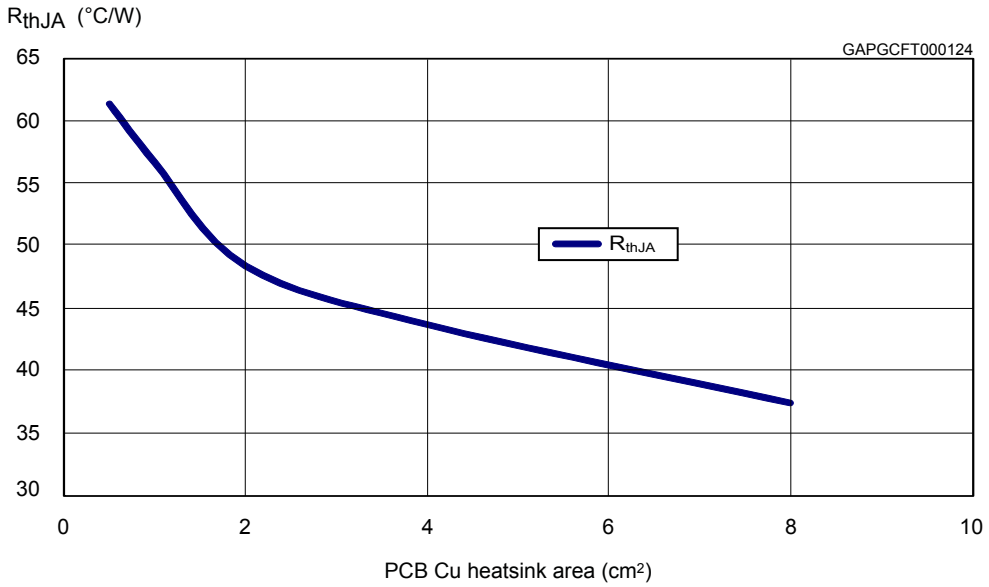


**Figure 29. PowerSSO-12 thermal impedance junction ambient single pulse (one channel ON)**

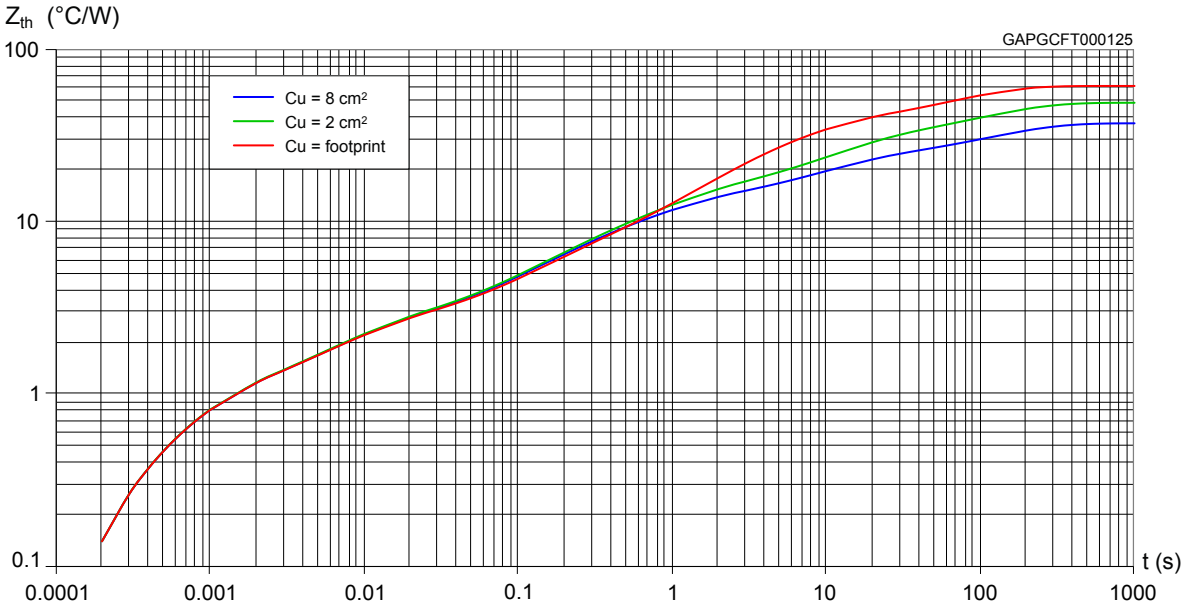
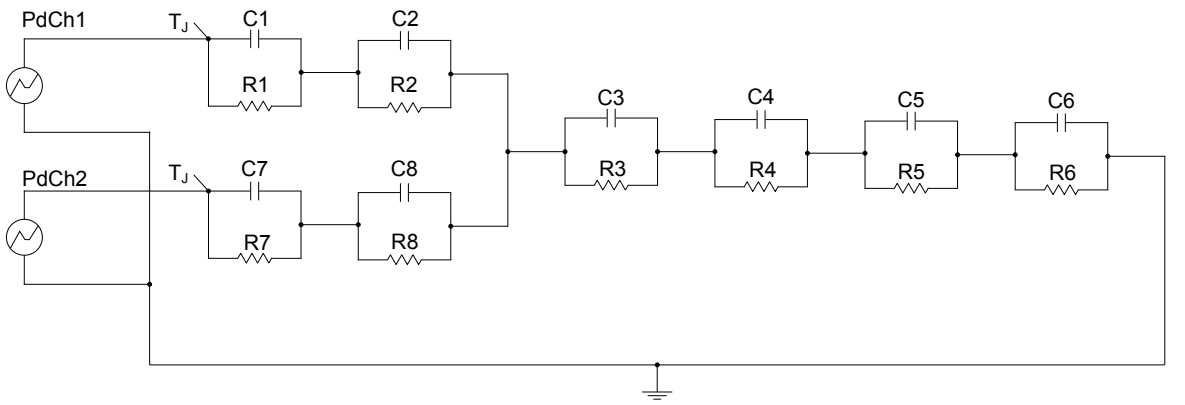



**Figure 30. Thermal fitting model of a double channel HSD in PowerSSO-12**




The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

**Equation: pulse calculation formula**

$Z_{th\delta} = R_{th} \cdot \delta + Z_{thtp} (1 - \delta)$

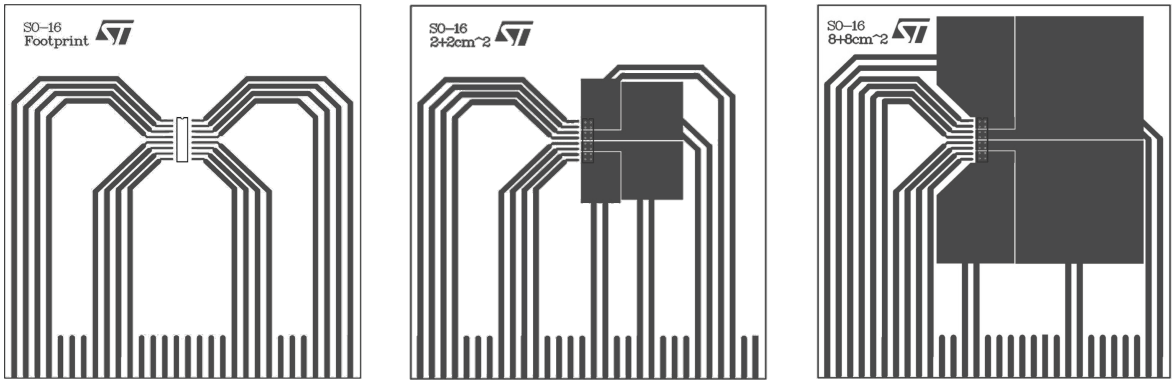
Where $\delta = t_P/T$

Table 15. **Thermal parameters**

| Area/island ($cm^2$) | Footprint | 2 | 8 |
|---|---|---|---|
| R1 = R7 (°C/W) | 0.8 | | |
| R2 = R8 (°C/W) | 1.5 | | |
| R3 (°C/W) | 3 | | |
| R4 (°C/W) | 8 | 8 | 7 |
| R5 (°C/W) | 22 | 15 | 10 |
| R6 (°C/W) | 26 | 20 | 15 |
| C1 = C7 (W.s/°C) | 0.0008 | | |
| C2 = C8 (W.s/°C) | 0.005 | | |
| C3 (W.s/°C) | 0.05 | | |
| C4 (W.s/°C) | 0.2 | 0.1 | 0.1 |
| C5 (W.s/°C) | 0.27 | 0.8 | 1 |
| C6 (W.s/°C) | 3 | 6 | 9 |

## 5.2 SO-16N thermal data

Figure 31. **SO-16N PCB**

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Layout condition of $R_{th}$ and $Z_{th}$ measurements (board finish thickness 1.6 mm ±10%; board double layer; board dimension 129 mm x 60 mm; board material FR4; Cu thickness 0.070 mm (front and back side); thermal vias separation 1.2 mm; thermal via diameter 0.3 mm ±0.08 mm; Cu thickness on vias 0.025 mm).

Figure 32. **$R_{thJA}$ vs PCB copper area in open box free air condition (one channel ON)**

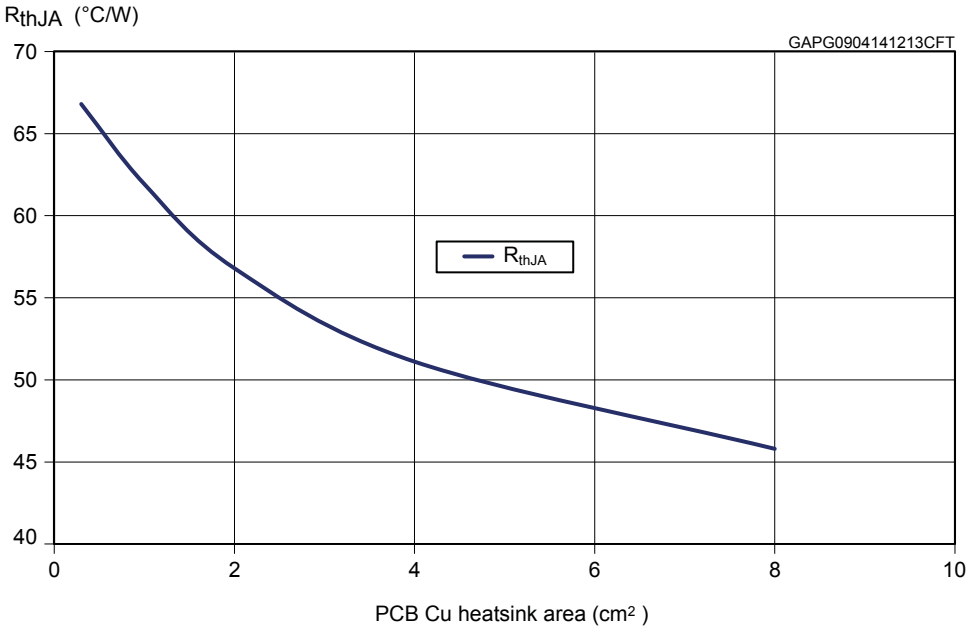


**Figure 33. SO-16N thermal impedance junction ambient single pulse (one channel ON)**

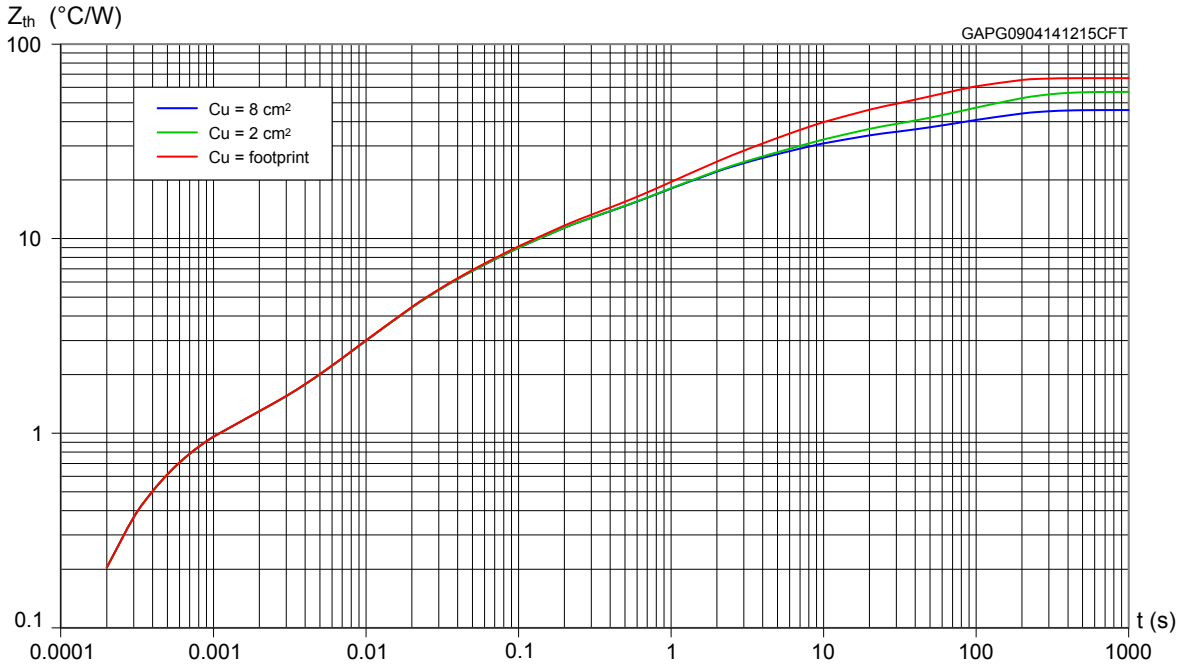
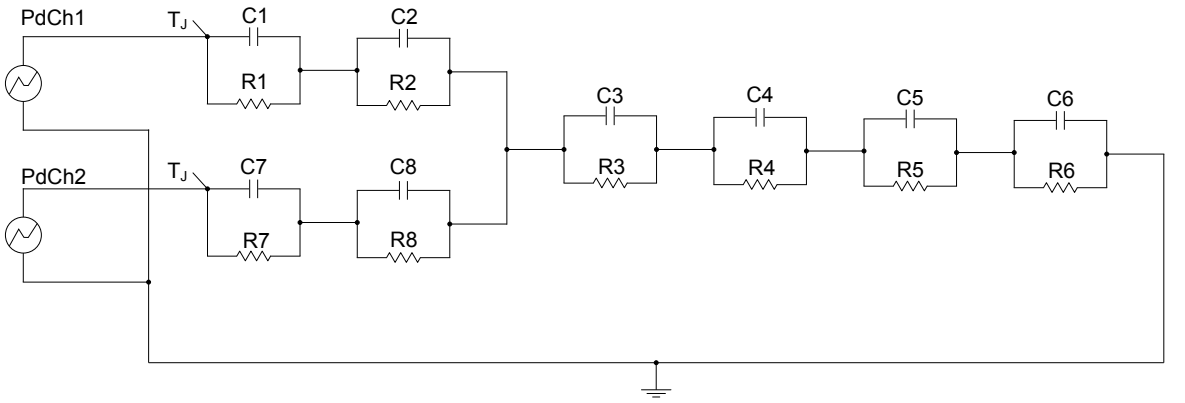



**Figure 34. Thermal fitting model of a double channel HSD in SO-16N**




The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

**Equation: pulse calculation formula**

$Z_{th\delta} = R_{th} \cdot \delta + Z_{thtp} (1 - \delta)$

Where $\delta = t_P/T$

Table 16. **Thermal parameters**

| Area/island ($cm^2$) | Footprint | 2 | 8 |
|---|---|---|---|
| R1 = R7 (°C/W) | 0.8 | | |
| R2 = R8 (°C/W) | 3 | | |
| R3 (°C/W) | 6 | | |
| R4 (°C/W) | 10 | | |
| R5 (°C/W) | 20 | 14 | 12 |
| R6 (°C/W) | 27 | 23 | 14 |
| C1 = C7 (W.s/°C) | 0.0005 | | |
| C2 = C8 (W.s/°C) | 0.005 | | |
| C3 (W.s/°C) | 0.015 | | |
| C4 (W.s/°C) | 0.1 | | |
| C5 (W.s/°C) | 0.3 | 0.5 | 0.5 |
| C6 (W.s/°C) | 2.5 | 5 | 7 |

# 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 6.1 PowerSSO-12 package information

**Figure 35. PowerSSO-12 package dimensions**

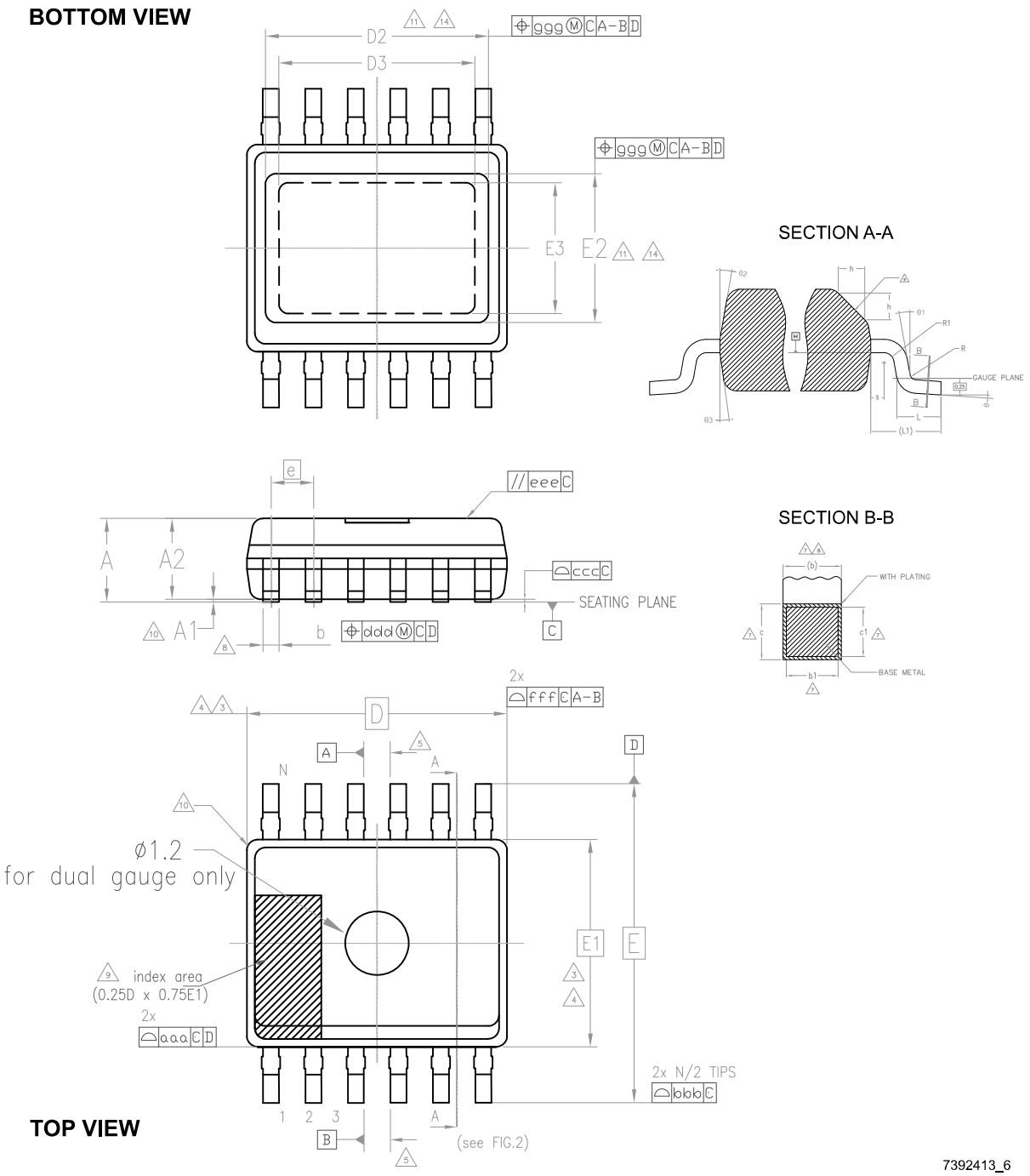


**Table 17. PowerSSO-12 mechanical data**

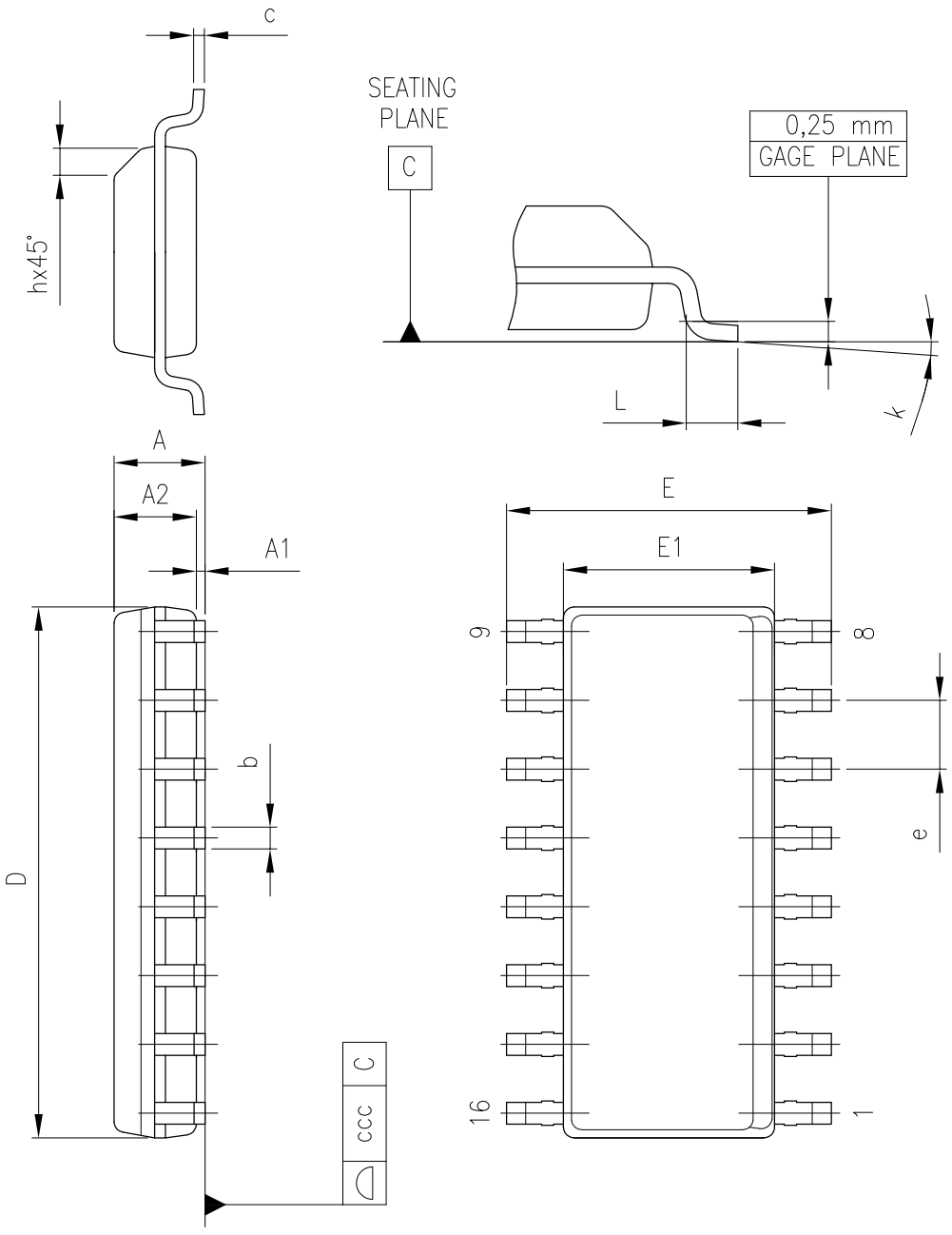
| Symbol | Millimeters | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| θ | 0° | | 8° |
| θ1 | 0° | | |
| θ2 | 5° | | 15° |
| θ3 | 5° | | 15° |
| A | 1.25 | | 1.70 |
| A1 | 0.00 | | 0.10 |
| A2 | 1.10 | | 1.60 |
| b | 0.23 | | 0.41 |
| b1 | 0.20 | 0.25 | 0.39 |
| c | 0.19 | | 0.25 |
| c1 | 0.19 | 0.20 | 0.23 |
| D | 4.90 BSC | | |
| D2 | 3.60 | | 4.20 |
| D3 | 2.90 | | |
| e | 0.80 BSC | | |
| E | 6.00 BSC | | |
| E1 | 3.90 BSC | | |
| E2 | 1.90 | | 2.50 |
| E3 | 1.20 | | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| L1 | 1.00 REF | | |
| N | 12 | | |
| R | 0.07 | | |
| R1 | 0.07 | | |
| S | 0.20 | | |

**Table 18. PowerSSO-12 tolerance of form and position**

| Symbol | Millimeters |
|---|---|
| aaa | 0.10 |
| bbb | 0.10 |
| ccc | 0.10 |
| ddd | 0.08 |
| eee | 0.10 |
| fff | 0.10 |
| ggg | 0.15 |

## 6.2 SO-16N package information

Figure 36. **SO-16N package dimensions**



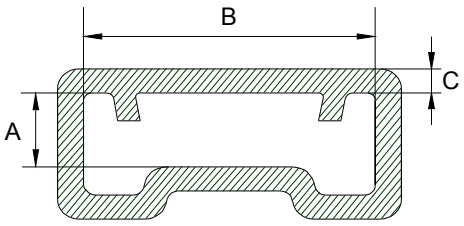

0016020_10

Table 19. **SO-16N mechanical data**

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | | | 1.75 |
| A1 | 0.10 | | 0.25 |
| A2 | 1.25 | | 1.60 |
| b | 0.31 | | 0.51 |
| c | 0.17 | | 0.25 |
| D | 9.80 | 9.90 | 10.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | | 1.27 | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| k | 0° | | 8° |
| ccc | | | 0.10 |

## 6.3 PowerSSO-12 packing information

**Figure 37. PowerSSO-12 tube shipment (no suffix)**




All dimensions are in mm.

| | |
|---|---|
| Base q.ty | 100 |
| Bulk q.ty | 2000 |
| Tube length ( ±0.5) | 532 |
| A | 1.85 |
| B | 6.75 |
| C ( ±0.1) | 0.6 |

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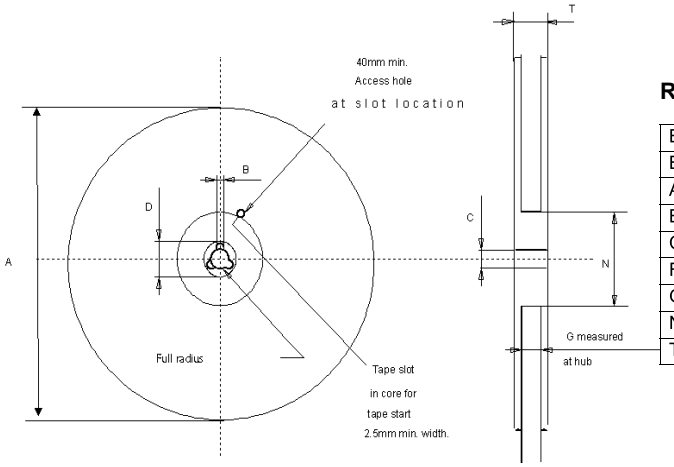
**Figure 38. PowerSSO-12 tape and reel shipment (suffix "TR")**




**Reel dimensions**

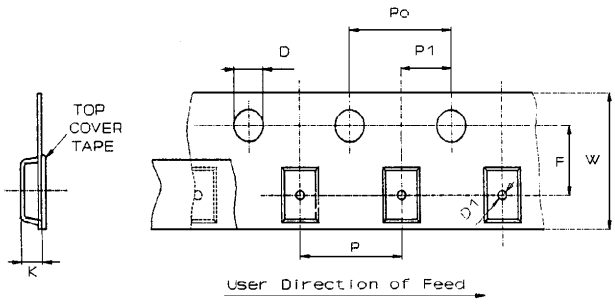
| | |
|---|---|
| Base q.ty | 2500 |
| Bulk q.ty | 2500 |
| A (max) | 330 |
| B (min) | 1.5 |
| C ( ±0.2) | 13 |
| F | 20.2 |
| G (+ 2 / -0) | 12.4 |
| N (min) | 60 |
| T (max) | 18.4 |

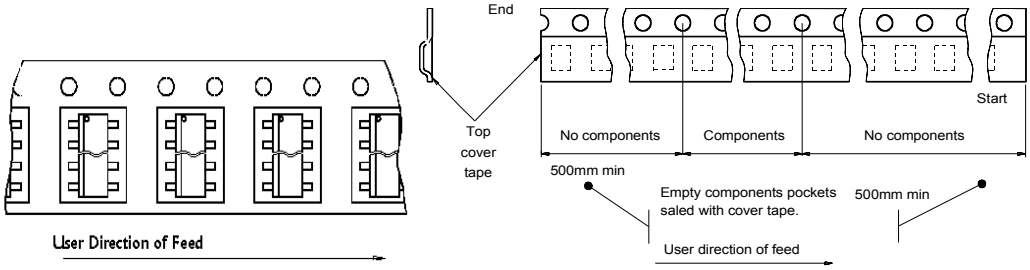
**Tape dimensions**

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

| | | |
|---|---|---|
| Tape width | W | 12 |
| Tape hole spacing | P0 (± 0.1) | 4 |
| Component spacing | P | 8 |
| Hole diameter | D ( ±0.05) | 1.5 |
| Hole diameter | D1 (min) | 1.5 |
| Hole position | F ( ±0.1) | 5.5 |
| Compartment depth | K (max) | 4.5 |
| Hole spacing | P1 ( ±0.1) | 2 |

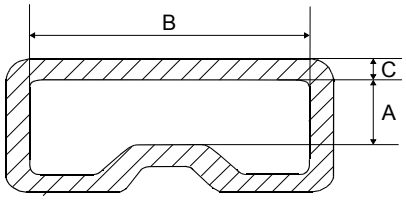
All dimensions are in mm.



## 6.4 SO-16N packing information

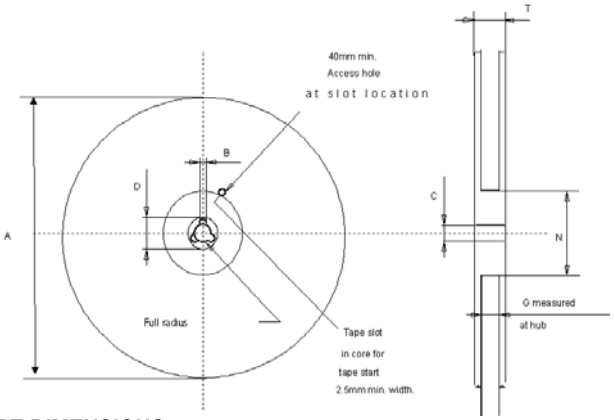
**Figure 39. SO-16N tube shipment (no suffix)**




| | |
|---|---|
| Base q.ty | 50 |
| Bulk q.ty | 1000 |
| Tube length (±0.5) | 532 |
| A | 3.2 |
| B | 6 |
| C (±0.1) | 0.6 |

All dimensions are in mm.

**Figure 40. SO-16N tape and reel shipment (suffix "TR")**




**REEL DIMENSIONS**

| | |
|---|---|
| Base q.ty | 1000 |
| Bulk q.ty | 1000 |
| A (max.) | 330 |
| B (min.) | 1.5 |
| C (±0.2) | 13 |
| F | 20.2 |
| G (+2 / -0) | 16.4 |
| N (min.) | 60 |
| T (max.) | 22.4 |

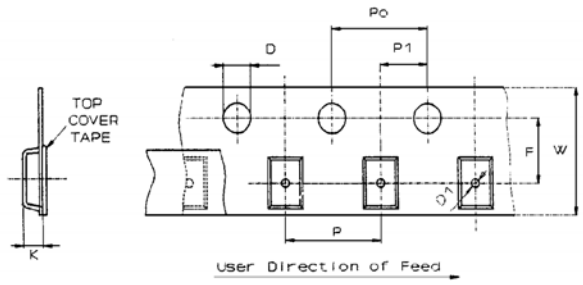
All dimensions are in mm.

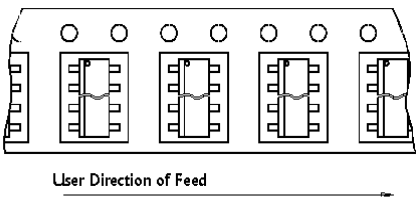
**TAPE DIMENSIONS**

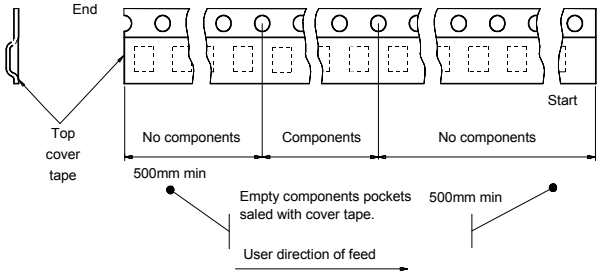
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

| | | |
|---|---|---|
| Tape width | W | 16 |
| Tape hole spacing | P0 (±0.1) | 4 |
| Component spacing | P | 8 |
| Hole diameter | D (±0.1/-0) | 1.5 |
| Hole diameter | D1 (min.) | 1.5 |
| Hole position | F (±0.05) | 7.5 |
| Compartment depth | K (max.) | 6.5 |
| Hole spacing | P1 (±0.1) | 2 |

All dimensions are in mm.



# 7 Order codes

Table 20. **Device summary**

| Package | Order codes | |
|---|---|---|
| | Tube | Tape and reel |
| PowerSSO-12 | VND5T100LAJ-E | VND5T100LAJTR-E |
| SO-16N | VND5T100LAS-E | VND5T100LASTR-E |

## Revision history

Table 21. **Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 25-Jun-2012 | 1 | Initial release. |
| 18-Sep-2013 | 2 | Disclaimer updated. |
| 30-Apr-2014 | 3 | Added SO-16N package and related details. |
| 08-Feb-2016 | 4 | *Table 4: Thermal data*:<br>– Rthj-case: updated values<br>– Rthj-pin: added row<br>Updated *Section 5.2: PowerSSO-12 mechanical data* and *Section 5.3: SO-16N package information* |
| 23-Aug-2016 | 5 | Added indication of AEC-Q100 qualification in *Features*.<br>Updated *Figure 3: Configuration diagram SO-16N (top view)*. |
| 16-Jun-2022 | 6 | Updated PowerSSO-12 and SO-16N cover image.<br>Updated Table 5. Power section.<br>Added notes in Table 12. Electrical transient requirements (part 1)<br>Updated Figure 25. Application schematic.<br>Moved *Section 3.4: Maximum demagnetization energy ($V_{CC}$ = 24 V)* to Section 4 Maximum demagnetization energy (VCC = 24 V)<br>Updated Section 6.1 PowerSSO-12 package information.<br>Removed *Packing information* chapter and moved related sections under Section 6 Package information.<br>Minor text changes. |

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