LM96551 Ultrasound Transmit Pulser

Check for Samples: LM96551

FEATURES

- **8-Channel High-Voltage CMOS Pulse Generator**
- **Output Pulses with ±50V and 2A Peak Current**
- **Active Damper with Built-In Blocking Diodes**
- **Built-In Floating Supply Voltages for Output Stage**
- **Up to 15 MHz Operating Frequency**
- **Matched Delays for Rising and Falling Edges**
- **Low Second Harmonic Distortion Allows and Improves Harmonic Imaging**
- **Continuous-Wave (CW) Operation Down to ±3.3V**
- **Low Phase Noise Enables Doppler Measurements**
  - **-145 dBc/Hz Phase Noise at 10 MHz (1 kHz offset)**
- **Output State Over-Temperature Protection**
- **Blocking Diodes for Direct Interface to Transducer**
- **2.5V to 5.0V CMOS Logic Interface**
- **Low-Power Consumption per Channel**
- **Over Temperature Protection**

KEY SPECIFICATIONS

- **Output voltage ±50 V**
- **Output peak current ±2.0 A**
- **Output pulse rate Up to 15 MHz**
- **Rise/fall delay matching (max) < 3.7 ns**
- **Pulser HD2 (5 MHz) -40 dB**
- **Operating Temp. 0 to +70 °C**

APPLICATIONS

- **Ultrasound Imaging**

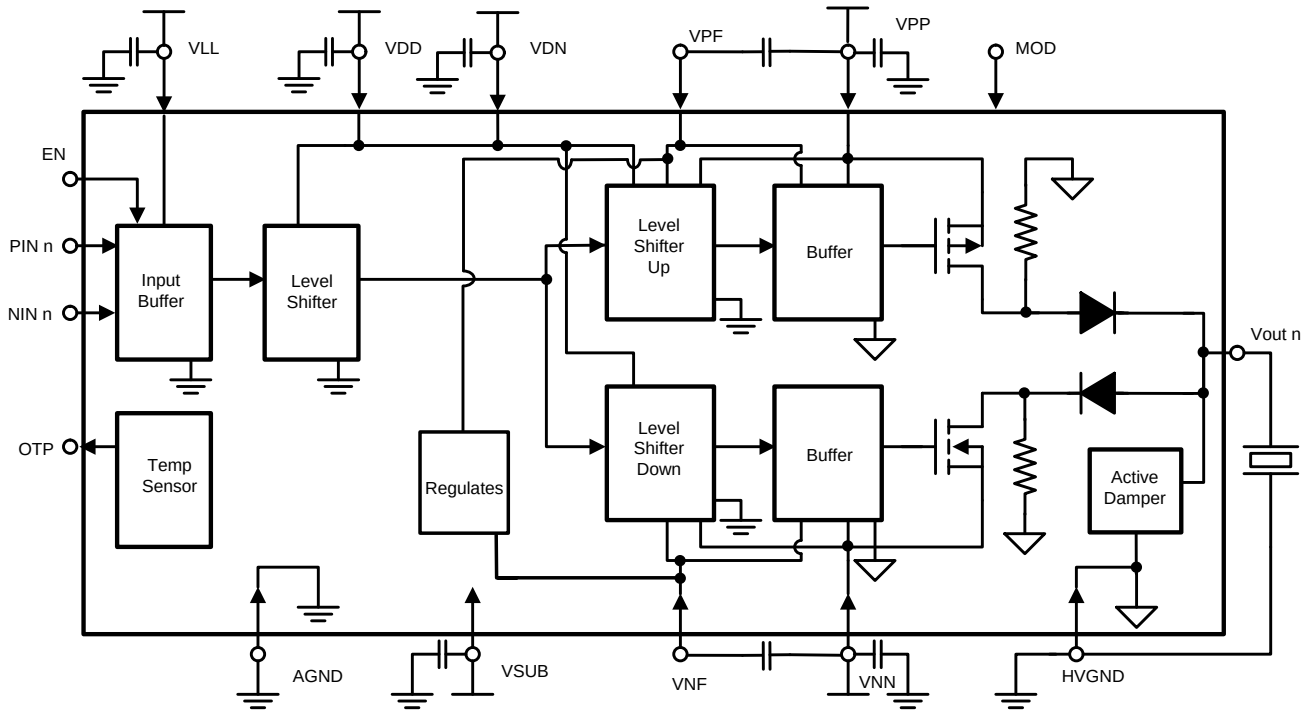
DESCRIPTION

The LM96551 is an eight-channel monolithic high-voltage, high-speed pulse generator for multi-channel medical ultrasound applications. It is well-suited for use with Texas Instrument's LM965XX series chipset which offers a complete medical ultrasound solution targeted towards low-power, portable systems.

The LM96551 contains eight high-voltage pulsers with integrated diodes generating ±50V bipolar pulses with peak currents of up to 2A and pulse rates of up to 15 MHz. Advanced features include low-jitter and low-phase-noise output pulses ideal for continuous-wave (CW) modes of operation. Active clamp circuitry is integrated for ensuring low harmonic distortion of the output signal waveform.

The LM96551 also featuers a low-power operation mode and over-temperature protection (OTP) which are enabled by on-chip temperature sensing and power-down logic.

Block Diagram



Typical Application

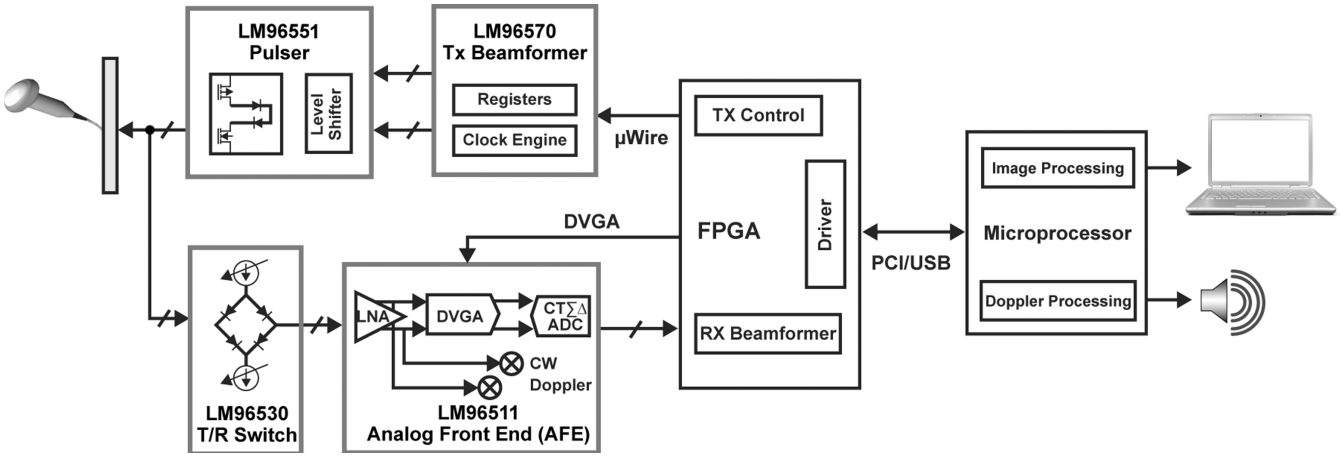


Figure 1. 8-Channel Transmit/Receive Chipset

Pin Diagram

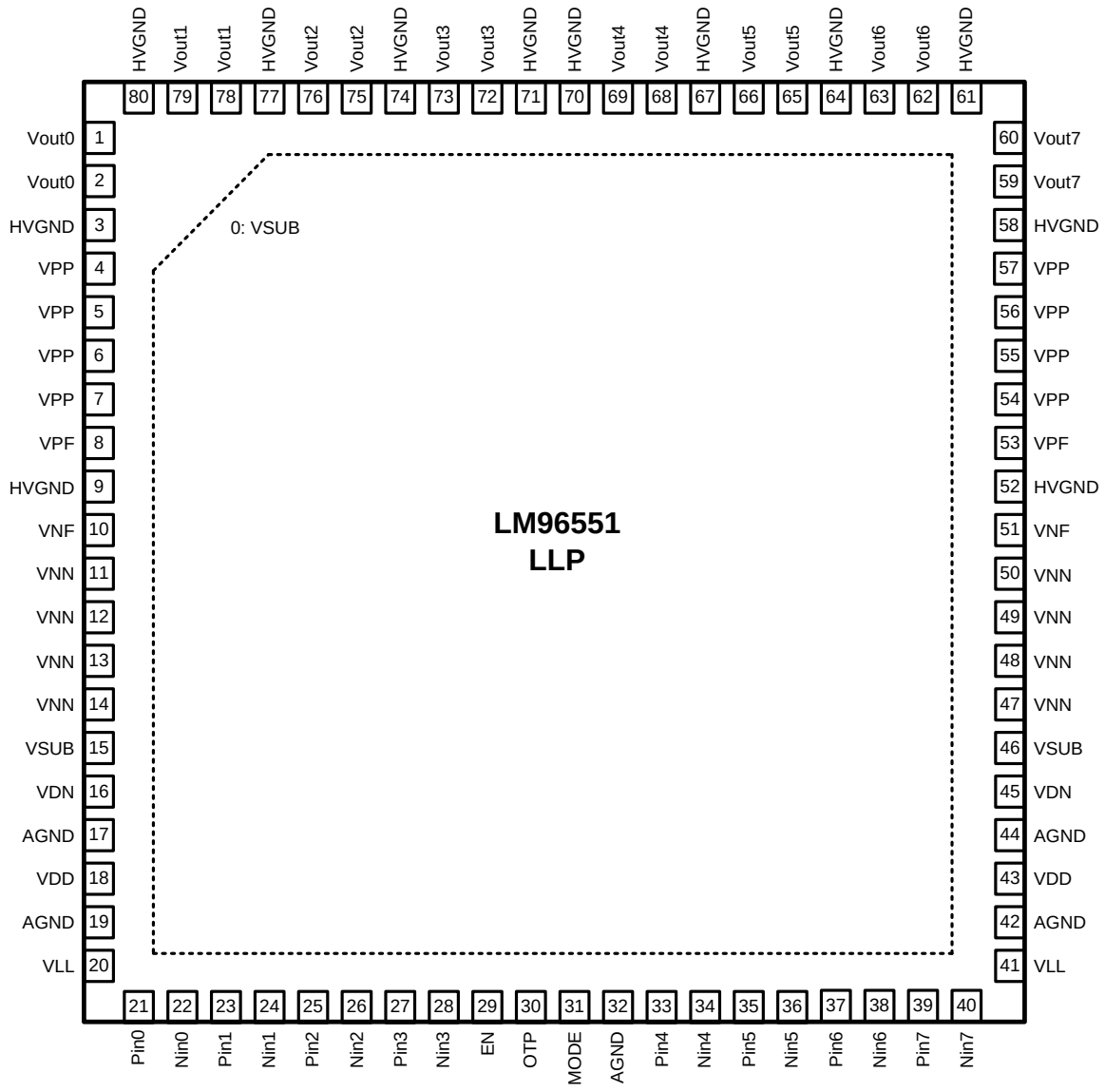


Figure 2. WQFN Package
See Package Number NKF0080A

PIN DESCRIPTIONS

Pin No.	Name	Type	Function and Connection
21, 23, 25, 27, 33, 35, 37, 39	PIN n=0...7	Input	Logic control positive output channel P 1 = ON 0 = OFF
22, 24, 26, 28, 34, 36, 38, 40	NIN n=0...7	Input	Logic control negative output channel N 1 = ON 0 = OFF
59, 60	V_{OUT7}	Output	High voltage output of channels 0 to 7
62, 63	V_{OUT6}		
65, 66	V_{OUT5}		
68, 69	V_{OUT4}		
72, 73	V_{OUT3}		
75, 76	V_{OUT2}		
78, 79	V_{OUT1}		
1, 2	V_{OUT0}		
29	EN	Input	Chip power enable 1 = ON 0 = OFF
31	MODE	Input	Output current mode control 1 = Max Current 0 = Low Current
30	OTP	Output	Over-temperature indicating IC temp > 125°C 0 = Over-temperature 1 = Normal temperature This pin is open-drain.
4, 5, 6, 7, 54, 55, 56, 57	VPP	Power	Positive high voltage power supply (+3.3V to +50V)
11, 12, 13, 14, 47, 48, 49, 50	VNN	Power	Negative high voltage power supply (-3.3V to -50V)
8, 53	VPF	Power	Positive internal floating power supply (VPP -10V)
10, 51	VNF	Power	Negative internal floating power supply (VNN +10V)
18, 43	VDD	Power	Positive level-shifter supply voltage (+10V)
16, 45	VDN	Power	Negative level-shifter supply voltage (-10V)
20, 41	VLL	Power	Logic supply voltage. Hi voltage reference input (+2.5 to +5V)
0, 15, 46	VSUB	Power	All VSUB pins must be connected to most negative potential of the IC. NOTE: The exposed thermal pad is connected to VSUB.
3, 9, 52, 58, 61, 64, 67, 70, 71, 74, 77, 80	HVGND	Ground	High voltage reference potential (0V)
17, 19, 32, 42, 44	AGND	Ground	Analog and Logic voltage reference input, logic ground (0V)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Maximum Junction Temperature (T_{JMAX})	+150°C
Storage Temperature Range	−40°C to +125°C
Supply Voltage (VDD)	–0.3V to +12V
Supply Voltage (VDN)	+0.3V and −12V
Supply Voltage (VPP)	–0.3V and +55V
Supply Voltage (VNN)	+0.3V and −55V
Supply Voltage (VSUB)	−65V
IO Supply Voltage (VLL)	−0.3V to +5.5V
Voltage at Logic Inputs	−0.3V to VLL +0.3V

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is specified to be functional, but do not specify specific performance limits. For specifications and test conditions, see the Electrical Characteristics.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Operating Ratings

Operation Junction Temperature		0°C to + 70°C
VPP, −VNN; High-voltage supply		+3.3V to +50V
VDD, −VDN; Level-shift supply		+9V to 11V
VLL, Logic Supply		+2.4V to +5.3V
VSUB, Substrate bias supply		must be most negative supply
Package Thermal Resistance (θ_{JA})		19.7 °C/W
ESD Tolerance	Human Body Model	2KV
	Machine Model	150V
	Charge Device Model	750V

Analog Characteristics

Unless otherwise stated, the following conditions apply
VLL = +3.3V, VPP = −VNN = 50V, VSUB = −55V, VDD = −VDN = 10V, R_L = 2KΩ, T_A = 25°C, Fin=5MHz, Mode = LO, EN = HI.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
F_{OUT}	Output Frequency Range	R_L = 100Ω		1		15	MHz
	Output Voltage Range			-48.5		+48.5	V
	Output Current	2% Duty Cycle			2		A
	Output Current	100% Duty Cycle, Mode=HI			0.6		
HD2	Second harmonic distortion	R_L = 100Ω, C_L = 330pF			-40		dBc
R_{ON}	Output ON Resistance	100 mA			7	11	Ω
	Output clamp	Positive or Negative pulse			2		A
	Power Supply Current	Pin = Nin = LO	VPP		3.2	7	mA
			VNN		3.4	8	
			VDD		12	18	
			VDN		8	13	
			VLL		25	50	µA
			VSUB		0.7	6	mA
		En = LO	VPP		3.2	7	mA
			VNN		3.4	8	
			VDD		4	7	
			VDN		3	6.5	
			VLL		25	50	µA
			VSUB		0.7	6	mA
OTP	Over Temperature Protection				125		°C
σ_{OTP}	OTP sigma				3.0		°C
$Hsys_{OTP}$	OTP hysteresis				5.5		°C

AC and Timing Characteristics

Unless otherwise stated, the following conditions apply
VLL = +3.3V, VDD = −VDN = 10V, VSUB = −55V, VPP = −VNN = 50V, R_L = 100Ω, C_L = 330pF, Fin=5MHz, T_A = 25°C. Mode = LO, EN = HI.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	Output rise time			19	29	ns
t_f	Output fall time			19	29	
t_E	Enable time			1		µs
t_{dr}	Delay time on inputs rise			32	39	ns
t_{df}	Delay time on inputs fall			32	39	
$\lvert t_{dr} - t_{dr} \rvert$	Delay time mismatch	P-to-N (1)			3.7	
t_{dm}	Delay on mode change			1		µs

(1) The delay time mismatch can be adjust to be less than 0.8ns with the LM96570 duty cycle control function.

DC Characteristics

Unless otherwise stated, the following conditions apply.
VLL = +3.3V, VDD = −VDN = 10V, VSUB = −55V, VPP = −VNN = 50V, T_A = 25°C,

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low Input “LO” threshold				1	V
V_{IH}	High Input “HI” threshold		2.3			V
I_{IN}	input current			1		µA

Overview

The LM96551 pulser provides an 8-channel transmit side solution for medical ultrasound applications suitable for integration into multi-channel (128/256 channel) systems. Its flexible, integrated ±50V pulser architecture enables low-power designs targeting portable systems. A complete system can be designed using Texas Instrument’s companion LM965XX chipset.

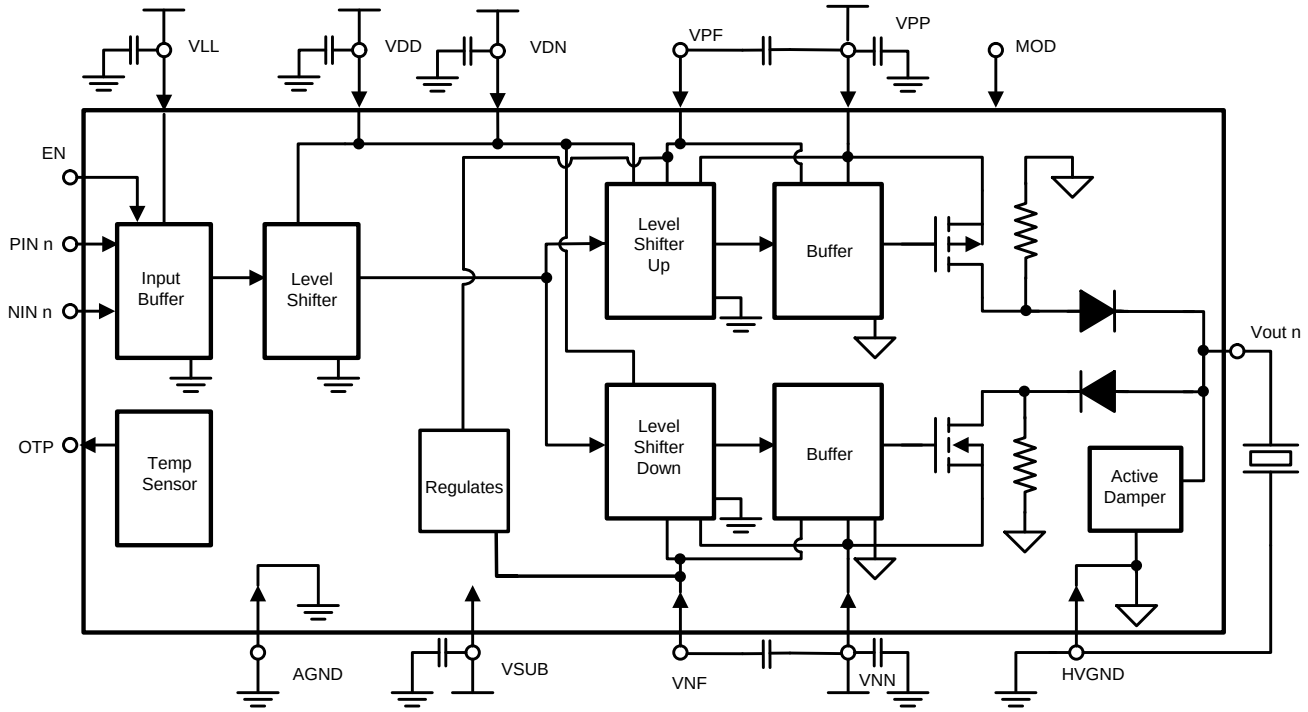


Figure 3. Block Diagram of High-Voltage Pulser Channel

A functional block diagram of the LM96551 is shown in Figure 3. It has an input buffer at its CMOS logic interface, which is powered by VLL (2.5 to 5.0V). When EN=HI, driving a channel’s inputs (PIN n or NIN n) HI will result in a positive or negative pulse at the channel’s output pin (V_{OUT} n), respectively. The output pins V_{OUT} are pulled to either the positive or negative supplies, VPP or VNN by power MOSFETs.

When PIN and NIN are both LO, Vout is actively clamped to GNDHI at 0V. This clamping reduces harmonic distortions compared to competing architectures that use bleeding resistors for implementing the return to zero of the output. **The user must avoid the condition in which PIN and NIN are both HI simultaneously, as this will damage the output stage!**

The impedance of the output stage can be controlled via the Mode-pin. When the Mode = HI as shown, only one output transistor pair drives the output resulting in a peak current of 600 mA at VPP = -VNN = 50V. When Mode=LO, a peak-current of 2A is achievable resulting in faster transients at the output. However, faster output transients can lead to significant overshoot of the output signal. This can be avoided using the lower drive current option.

Continuous-wave (CW) applications are supported for low power consumption down to VPP = -VNN = 3.3V with Mode =HI.

Internally, the CMOS logic input signals are level shifted to VDD = 10V and VDN = -10V for pulse transmission. The outputs of the level shifter drive the high-voltage P and N drivers that control the output power MOSFETs, which are supplied from the positive and negative rails VPP and VNN, respectively. The high-voltage rails are designed for a maximum of 50V; however, they can be operated down to 3.3V. The necessary gate-overdrive voltage levels for the output drivers are internally generated from the high-voltage rails.

Over-Temperature Protection (OTP) is implemented by continuously monitoring the on-chip temperature. The OTP output (open drain) pin goes LO when the chip temperature exceeds a critical level. Prior to this event, the user must ensure that the chip is powered down before fatal damage occurs. In addition to a primary software controlled safety shutdown, the OTP pin can be also be hard-wired to the EN pin as a secondary safety measure.

Timing Diagrams

RISE AND FALL TIME

The timing diagram shown in Figure 4 defines the rise and fall times tr and tf.

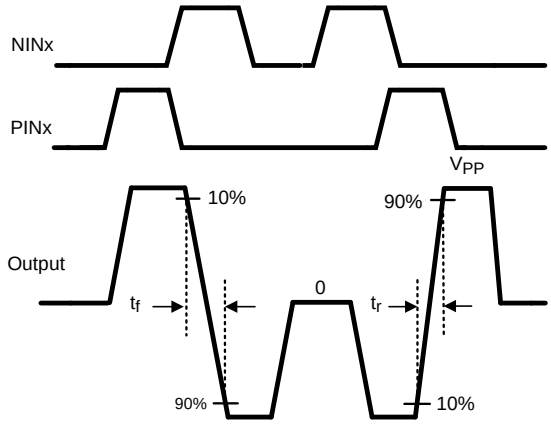


Figure 4. Timing Diagram Defining Rise and Fall Times tr and tf, respectively

INPUT TO OUTPUT DELAY

The timing diagram shown in Figure 5 defines the delays between the input and output signals.

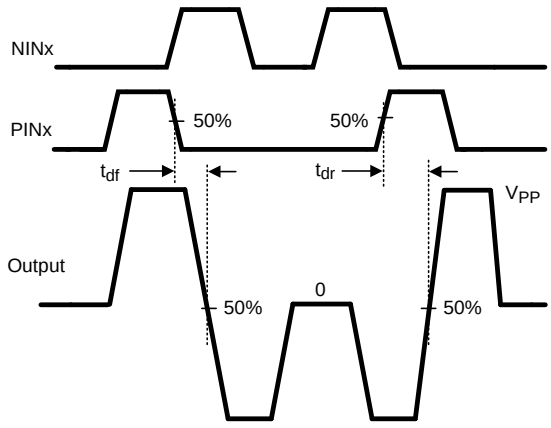


Figure 5. Timing Diagram Defining Input-to-Output Delays Times

Typical Performance Characteristics

Unless otherwise stated, the following conditions apply
VLL = +3.3V, VDD = −VDN = 10V, VSUB = −55V, VPP = −VNN = 50V, R_L = 100Ω, C_L = 330pF, Fin=5MHz, T_A = 25°C. Mode = LO, EN = HI

Return-to-Zero Rise Time (R_L=2KΩ)

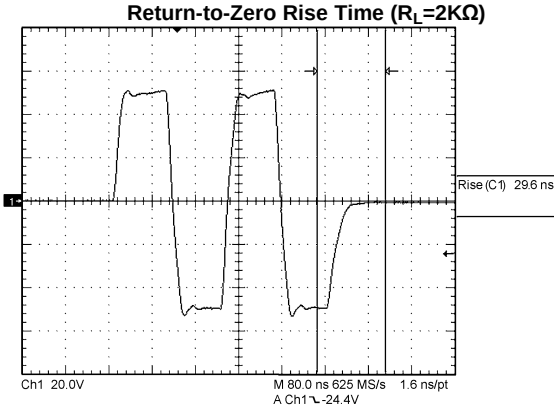


Figure 6.

Return-to-Zero Fall Time (R_L=2KΩ)

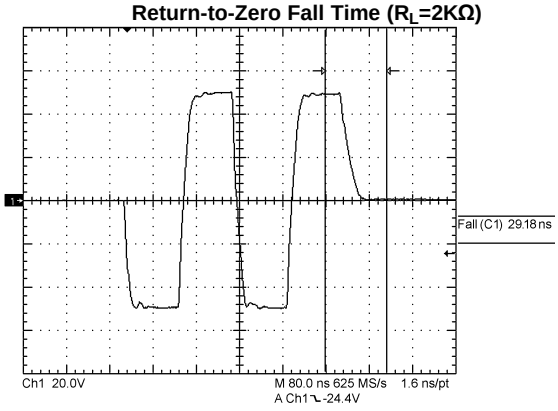


Figure 7.

Harmonic Distortion (8 pulses)

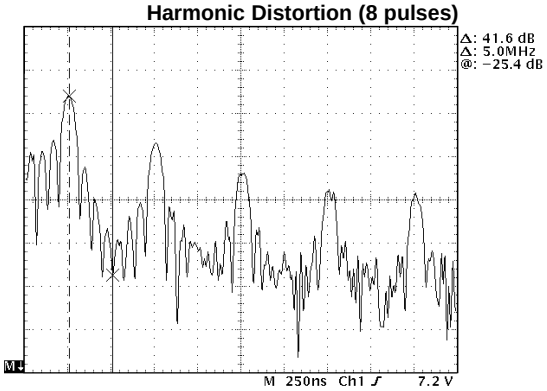


Figure 8.

Differential Input vs. Pulser Output Phase Noise(1)

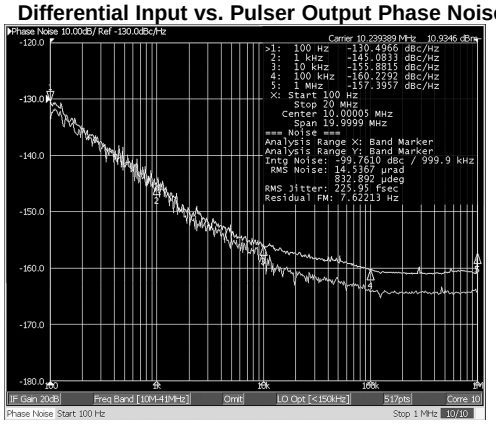


Figure 9.

Constant 5W Total Power R_L=300Ω
100% CW mode, Mode=HI, VSUB=-10V

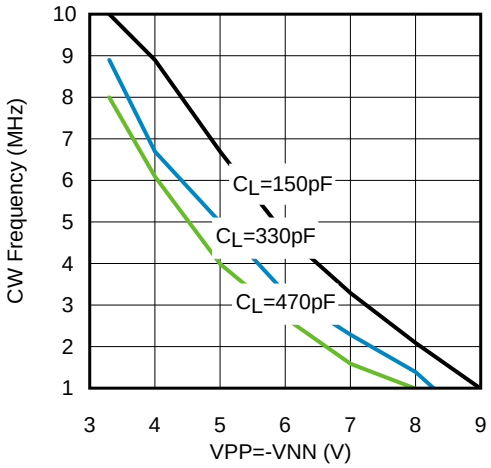


Figure 10.

Over Temperature Protection

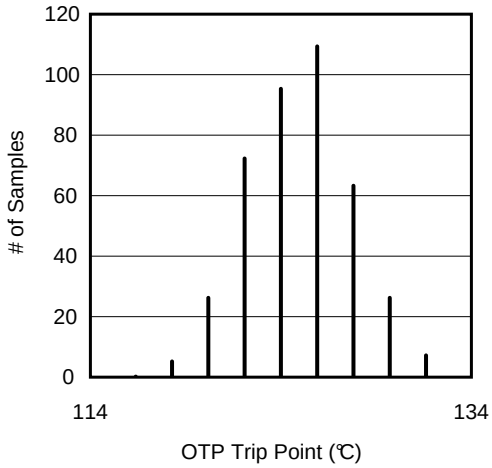


Figure 11.

(1) 10.24 MHz Differential Input signal from LMK04800 Evaluation board with 122.88 MHz Crystek CVHD-950 VCXO clock source. The LMK04800 clock output channel was configured with a divide value of 12 and LVCMOS outputs with opposite polarity.

FUNCTIONAL DESCRIPTION

Note that the case, PINn = NNn = HI is not allowed as it will damage the output transistors.

Logic inputs			Output
EN	PINn	NINn	Voutn
1	0	0	0V
1	1	0	VPP - 0.7V
1	0	1	VNN + 0.7V
1	1	1	**not allowed**
0	X	X	0V

APPLICATIONS INFORMATION

POWER-UP AND POWER-DOWN SEQUENCES

VSUB must always be the most negative supply, i.e., it must be equal to or more negative than the most negative supply, VNN or VDN.

Power UP Sequence:

1. Turn ON VSUB, hold EN pin LO
2. Turn On VLL
3. Turn ON VDD, VDN, VPP, and VNN

Power DOWN Sequence:

1. Turn OFF VDD, VDN, VPP & VNN
2. Turn OFF VLL
3. Turn OFF VSUB

REVISION HISTORY

Changes from Revision A (May 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM96551SQE/NOPB	LIFEBUY	WQFN	NKF	80	250	Green (RoHS & no Sb/Br)	CU SN | Call TI	Level-3-260C-168 HR		LM96551SQ	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

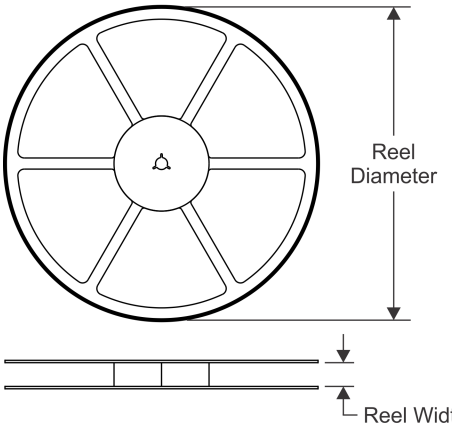
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

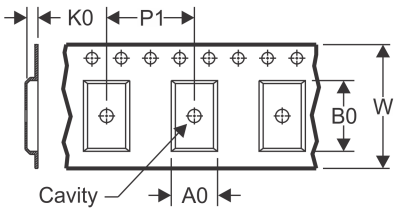
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

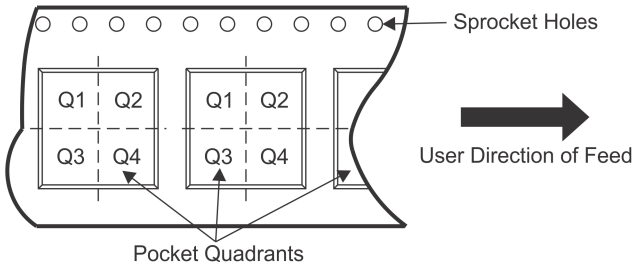


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

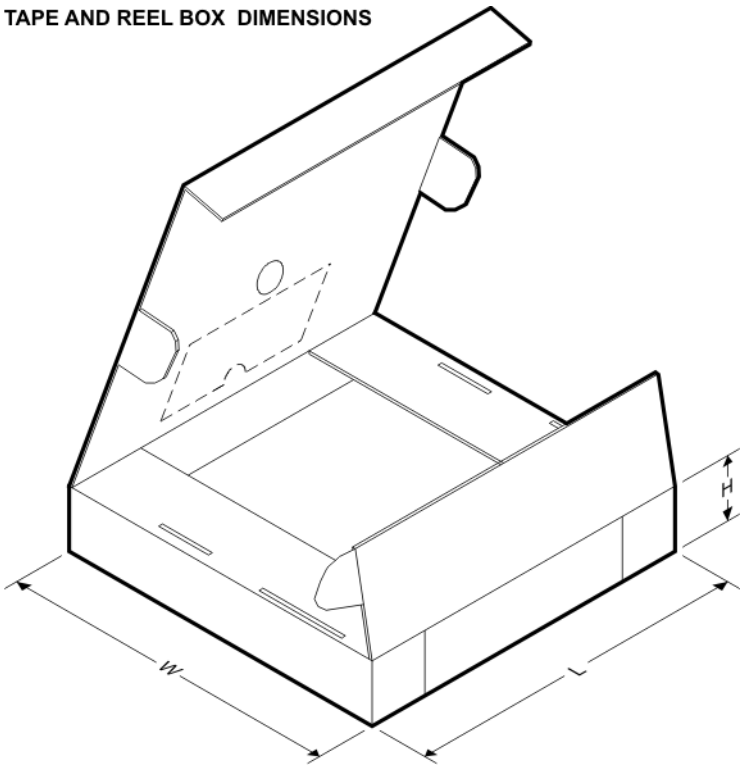
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM96551SQE/NOPB	WQFN	NKF	80	250	178.0	24.4	12.3	12.3	1.0	16.0	24.0	Q1

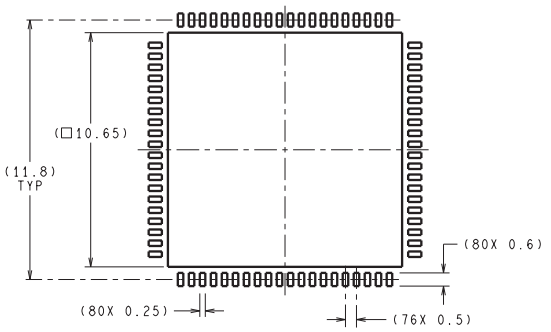
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

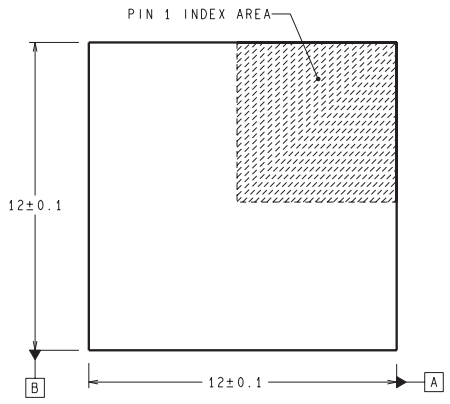
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM96551SQE/NOPB	WQFN	NKF	80	250	213.0	191.0	55.0

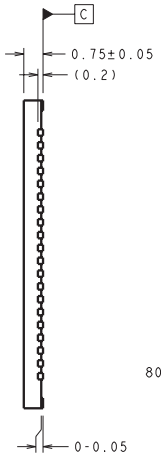
NKF0080A

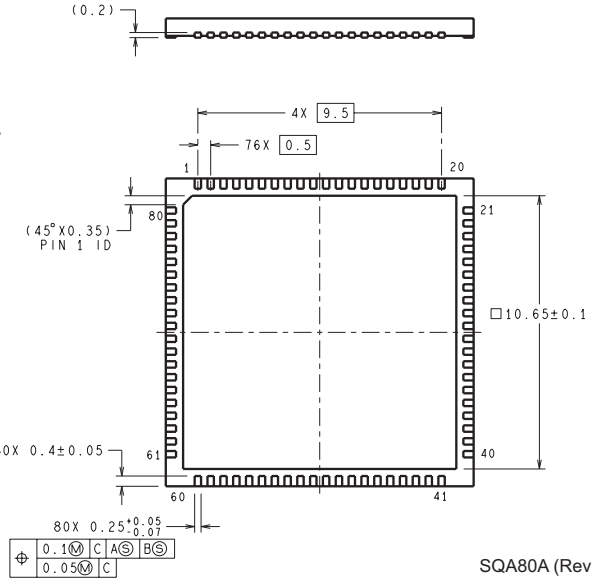


RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY







SQA80A (Rev A)

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