



CY8CPROTO-062-4343W

# PSoC 6 Wi-Fi BT Prototyping Kit Guide

Doc. # 002-25200 Rev. \*A

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# Safety and Regulatory Compliance Information



The CY8CPROTO-062-4343W PSoC<sup>®</sup> 6 Wi-Fi BT Prototyping Kit is intended for development purposes only. Users are advised to test and evaluate this kit in an RF development environment.

Safety evaluation for this kit is done in factory default settings using default accessories shipped with the kit. All evaluations for safety are carried out using a 5-V (USB 2.0, @500 mA) supply. Attaching additional wiring to this product or modifying the product operation from the factory default may affect its performance and cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required authorizations are first obtained. Contact [support@cypress.com](mailto:support@cypress.com) for details.



PSoC 6 Wi-Fi BT Prototyping Boards contain electrostatic discharge (ESD)- sensitive devices. Electrostatic charges readily accumulate on the human body and any equipment, which can cause a discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused PSoC 6 Wi-Fi BT Prototyping Boards in the protective shipping package.



## End-of-Life/Product Recycling

The end-of-life cycle for this kit is five years from the date of manufacture mentioned on the back of the box. Contact your nearest recycler to discard the kit.

## General Safety Instructions

### ESD Protection

ESD can damage boards and associated components. Cypress recommends that you perform procedures only at an ESD workstation. If an ESD workstation is unavailable, use appropriate ESD protection by wearing an anti-static wrist strap attached to a grounded metal object.

### Handling Boards

The CY8CPROTO-062-4343W PSoC 6 Wi-Fi BT Prototyping Kit is sensitive to ESD. Hold the board only by its edges. After removing the board from its box, place it on a grounded, static-free surface. Use a conductive foam pad, if available. Do not slide the board over any surface.

## Regulatory Compliance Information

The CY8CPROTO-062-4343W PSoC 6 Wi-Fi BT Prototyping Kit contains devices that transmit and receive radio signals in accordance with the spectrum regulations for the 2.4-GHz unlicensed frequency range.

The CY8CPROTO-062-4343W PSoC 6 Wi-Fi BT Prototyping Kit as shipped from the factory has been verified to meet with requirements for the following compliances:

- As a Class A compliant product meeting requirement for CE

# 1. Introduction



Thank you for your interest in the CY8CPROTO-062-4343W PSoC 6 Wi-Fi BT Prototyping Kit. The PSoC 6 Wi-Fi BT Prototyping Kit enables you to evaluate and develop your applications using the [PSoC 6 MCU](#) and CYW4343W WICED Wi-Fi/BT combo device.

PSoC 6 MCU is Cypress' latest, ultra-low-power PSoC specifically designed for wearables and IoT products. PSoC 6 MCU is a true programmable embedded system-on-chip, integrating a 150-MHz Arm® Cortex®-M4 as the primary application processor, a 100-MHz Arm Cortex®-M0+ that supports low-power operations, up to 2 MB Flash and 1 MB SRAM, Secure Digital Host Controller (SDHC) supporting SD/SDIO/eMMC interfaces, CapSense® touch-sensing, and programmable analog and digital peripherals that allow higher flexibility, in-field tuning of the design, and faster time-to-market.

You can use ModusToolbox™ to develop and debug your PSoC 6 MCU and CYW4343W applications. ModusToolbox software is a set of tools that enable you to integrate Cypress devices into your existing development methodology. One of the tools is a multi-platform, Eclipse-based Integrated Development Environment (IDE) that supports configuration and application development, called ModusToolbox IDE.

If you are new to PSoC 6 MCU and ModusToolbox IDE, you can find introductions in the application note [AN221774 - Getting Started with PSoC 6 MCU](#).

## 1.1 Kit Contents

The PSoC 6 Wi-Fi BT Prototyping Kit has the following contents.

- PSoC 6 Wi-Fi BT Prototyping Board
- USB Type-A to Micro-B cable
- Quick Start Guide (printed on the kit package)

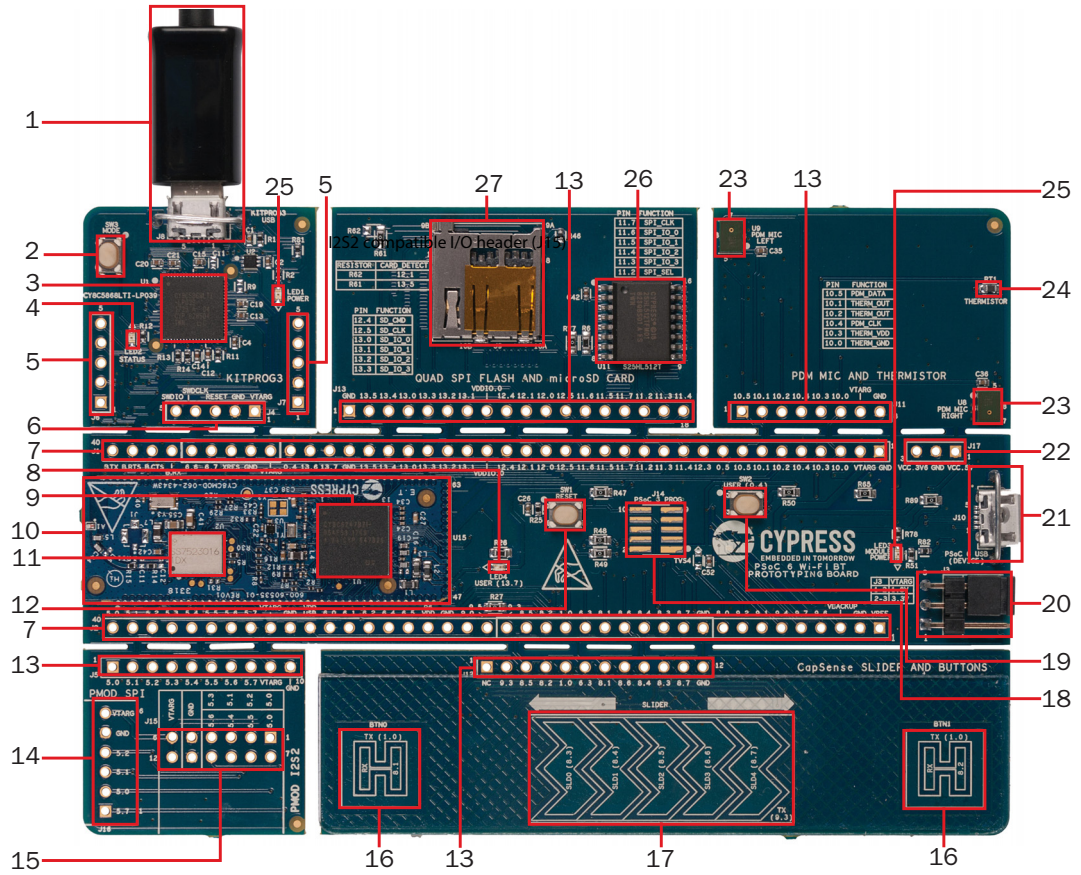
Inspect the contents of the kit; if you find any part missing, contact your nearest Cypress sales office for help: [www.cypress.com/support](http://www.cypress.com/support).

## 1.2 Board Details

Figure 1-1 shows the PSoC 6 Wi-Fi BT Prototyping Board, that has the following features:

- CY8CMOD-062-4343W PSoC 6 MCU with CYW4343W Wi-Fi BT module that contains
  - PSoC 6 MCU with SDHC
  - Murata Type 1DX ultra-small 2.4-GHz WLAN and Bluetooth functionality module based on CYW4343W
- microSD card slot
- 512-Mbit external Quad SPI NOR Flash that provides a fast, expandable memory for data and code
- A thermistor to measure ambient temperature and two PDM microphones for voice input
- KitProg3 onboard SWD programmer/debugger with USB-UART and USB-I2C bridge functionality
- CapSense touch-sensing slider (5 elements) and two CapSense buttons, all of which are capable of both self- capacitance (CSD) and mutual-capacitance (CSX) operation
- A Micro-B connector for USB device interface and a separate Micro-B connector for programming/debug using the KitProg3
- Expansion headers that are compatible with Digilent® Pmod™ modules
- 1.8 V and 3.3 V operation of PSoC 6 MCU is supported
- One user LED, a user button, and a reset button for PSoC 6 MCU
- One Mode selection button and one Mode LED for KitProg3

Figure 1-1. Board Components



- |  |   |
|--|---|
| 1. KitProg3 USB connector (J8)   | 14. Digilent® Pmod™ SPI compatible I/O header (J16)           |
| 2. KitProg3 programming mode selection button (SW3)                    | 15. Digilent® Pmod™ I2S2 compatible I/O header (J15)          |
| 3. KitProg3 (PSoC 5LP) programmer and debugger (CY8C5868LTI-LP039, U1) | 16. CapSense buttons  |
| 4. KitProg3 status LED (LED2)  | 17. CapSense slider   |
| 5. KitProg3 I/O headers (J6, J7)                                       | 18. PSoC 6 MCU program and debug header (J14)                 |
| 6. KitProg3 5-pin programming header (J4)                              | 19. PSoC 6 MCU user button (SW2)                              |
| 7. PSoC 6 MCU I/O headers (J1, J2)                                     | 20. Power selection jumper (J3)                               |
| 8. PSoC 6 MCU user LED (LED4)  | 21. PSoC 6 USB device Connector (J10)                         |
| 9. PSoC 6 MCU (CY8C624ABZI-D44)  | 22. External power supply connector (J17)                     |
| 10. Cypress PSoC 6 Wi-Fi-BT Module (CY8CM0D-062-4343W, U15)            | 23. PDM microphones (U8, U9)                                  |
| 11. CYW4343W based Murata Type 1DX Module (LBEE5KL1DX)                 | 24. Thermistor (RT1)  |
| 12. Reset button (SW1)   | 25. Power LEDs (LED1, LED3)                                   |
| 13. On-board peripheral headers (J5, J11, J12 and J13)                 | 26. Cypress 512-Mbit serial NOR flash memory (S25HL512T, U11) |
|  | 27. microSD Card holder (J9)                                  |



Figure 1-2. Prototyping Board Pinout

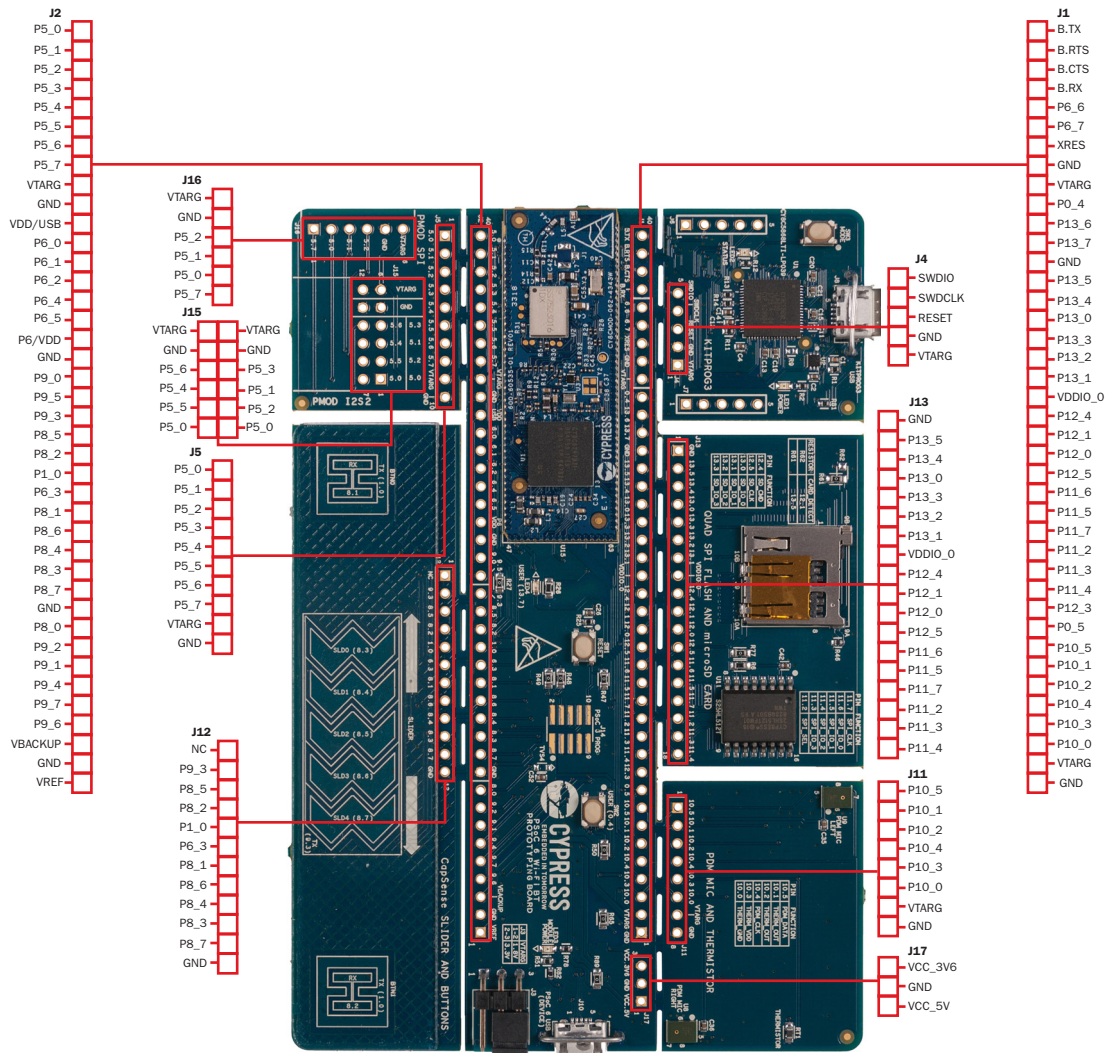


Table 1-1. Board Pinout

PSoC 6 MCU Pin	Primary On-board Function	Secondary On-board Function	Connection details
XRES	Hardware Reset	–	Remove R47 to disconnect it from KitProg3 reset
P0.4	User Button with Hibernate wakeup capability	–	Connected to ground as active low logic by default. Remove R24, R22 and populate R21, R23 to change the switch to active high logic.
P0.5	GPIO	–	–
P1.0	CapSense Button TX	GPIO	Connected to CapSense by default. Remove R35 to disconnect CapSense.
P5.0	UART RX	MCLK	To use PMOD, Remove R72 to disconnect from KitProg3 UART TX
P5.1	UART TX	TX_SCK	To use PMOD, Remove R73 to disconnect from KitProg3 UART RX
P5.2	UART RTS	TX_WS	To use PMOD, Remove R75 to disconnect from KitProg3 UART CTS
P5.3	UART CTS	TX_SDO	To use PMOD, Remove R74 to disconnect from KitProg3 UART RTS
P5.4	GPIO	RX_SCK	–
P5.5	GPIO	RX_WS	–
P5.6	GPIO	RX_SDO	–
P5.7	GPIO	–	–
P6.0	I2C_SCL	–	EEPROM (U16) can be accessed by this line.
P6.1	I2C_SDA	–	EEPROM (U16) can be accessed by this line.
P6.2	GPIO	–	–
P6.3	GPIO	CAP_SH	Remove R76 and populate R55 to connect Hatch to CapSense Shield pin
P6.4	GPIO	TDO_SWO	–
P6.5	GPIO	TDI	–
P6.6	SWDIO	GPIO	Remove R49 to disconnect from KitProg3 SWDIO
P6.7	SWDCLK	GPIO	Remove R48 to disconnect from KitProg3 SWDCLK
P8.0	GPIO	–	–
P8.1	CapSense Button0 Rx	GPIO	Connected to CapSense by default. Remove R34 to disconnect CapSense.
P8.2	CapSense Button1 Rx	GPIO	Connected to CapSense by default. Remove R45 to disconnect CapSense.
P8.3	CapSense Slider0 Rx	GPIO	Connected to CapSense by default. Remove R40 to disconnect CapSense.

Table 1-1. Board Pinout (*continued*)

PSoC 6 MCU Pin	Primary On-board Function	Secondary On-board Function	Connection details
P8.4	CapSense Silder1 Rx	GPIO	Connected to CapSense by default. Remove R41 to disconnect CapSense.
P8.5	CapSense Silder2 Rx	GPIO	Connected to CapSense by default. Remove R42 to disconnect CapSense.
P8.6	CapSense Silder3 Rx	GPIO	Connected to CapSense by default. Remove R43 to disconnect CapSense.
P8.7	CapSense Silder4 Rx	GPIO	Connected to CapSense by default. Remove R44 to disconnect CapSense.
P9.0	GPIO	–	–
P9.1	GPIO	–	–
P9.2	GPIO	–	–
P9.3	CapSense Slider Tx	GPIO	Connected to CapSense by default. Remove R79 to disconnect CapSense.
P9.4	GPIO	–	–
P9.5	GPIO	–	–
P9.6	GPIO	–	–
P9.7	GPIO	–	–
P10.0	Thermistor VDD	–	–
P10.1	Thermistor Output	–	To disconnect from thermistor, remove R36
P10.2	Thermistor Output	–	To disconnect from thermistor, remove R37
P10.3	Thermistor GND	–	–
P10.4	PDM Clock	–	–
P10.5	PDM Data	–	–
P11.2	QSPI FLASH CS	–	–
P11.3	QSPI FLASH DATA3	–	–
P11.4	QSPI FLASH DATA2	–	–
P11.5	QSPI FLASH DATA1	–	–
P11.6	QSPI FLASH DATA0	–	–
P11.7	QSPI FLASH CLK	–	–
P12.0	GPIO	–	–
P12.1	GPIO	CARD DETECT	Remove R61 and populate R62 to connect to Card Detect of microSD card slot
P12.3	GPIO	–	–
P12.4	SDHC CMD	–	–
P12.5	SDHC CLK	–	–
P13.0	SDHC DATA0	–	–
P13.1	SDHC DATA1	–	–
P13.2	SDHC DATA2	–	–
P13.3	SDHC DATA3	–	–

Table 1-1. Board Pinout (*continued*)

PSoC 6 MCU Pin	Primary On-board Function	Secondary On-board Function	Connection details
P13.4	GPIO	–	–
P13.5	CARD DETECT	GPIO	Remove R61 to disconnect from card detect of microSD card slot
P13.6	GPIO	–	–
P13.7	Red User LED (LED4)	GPIO	–
USB.DP	–	–	–
USB.DM	–	–	–
BT_UART.RXD	–	–	To connect to KitProg3, Remove R72 and populate R68
BT_UART.TXD	–	–	To connect to KitProg3, Remove R73 and populate R69
BT_UART.CTS	–	–	To connect to KitProg3, Remove R74 and populate R70
BT_UART.RTS	–	–	To connect to KitProg3, Remove R75 and populate R71
VREF	SAR BYPASS, J2.1, AREF	–	–
VDDIO.0	–	–	R63 is loaded by default, connects VDDIO.0 to VCC_3V3. Remove R63 and populate R64 to connect VDDIO.0 to VCC_1V8

## 1.3 ModusToolbox

**ModusToolbox** is a free development eco-system that includes the ModusToolbox IDE and the PSoC 6 SDK. ModusToolbox IDE brings together device resources, middleware and firmware to build an application. Using ModusToolbox IDE, you can enable and configure device resources, middleware libraries; write C source code; and program and debug the device. ModusToolbox IDE is supported on 64-bit versions of Windows, Linux and macOS.

The PSoC 6 SDK is the software development kit for the PSoC 6 MCU family and Cypress IoT devices. The SDK makes it easier to develop firmware for supported devices. It helps you to build firmware without the need to understand the intricacies of the device resources.

As [Figure 1-3](#) shows, with ModusToolbox IDE, you can:

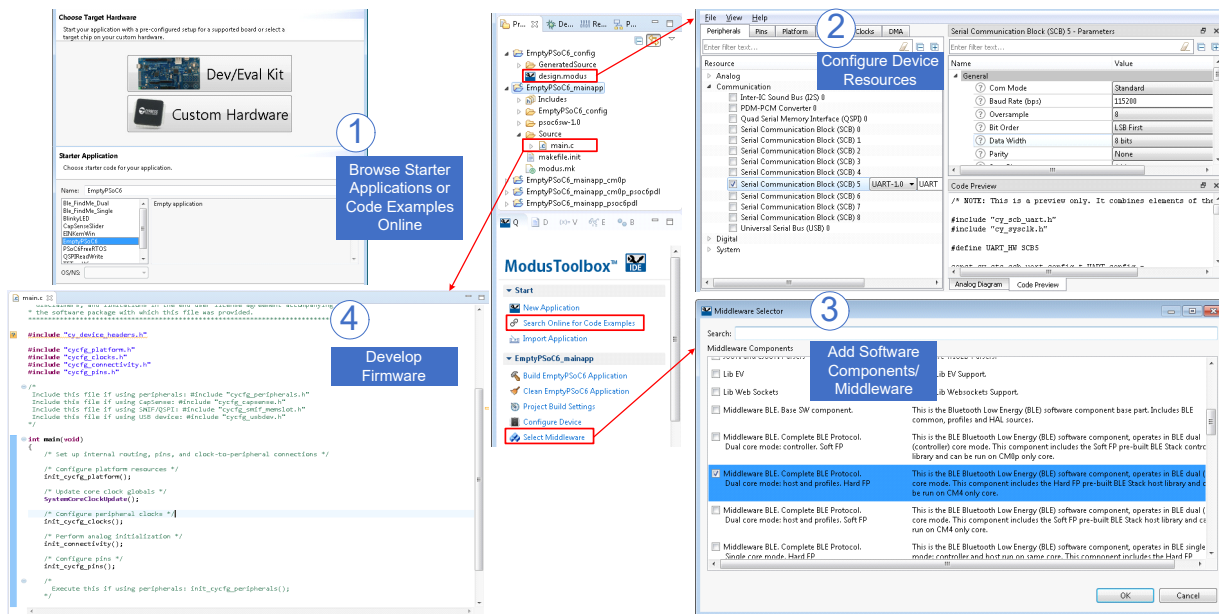
1. Browse the collection of starter applications during application set up.
  - a. Filter for applications based on Chip or Board.
  - b. Select from the menu of applications offered.
  - c. Create a new application based on the selection.

OR

Browse the collection of code examples online.

2. Configure device resources in *design.modus* to build your hardware system design in the workspace.
3. Configure the Software Components or middleware.
4. Develop your application firmware with the PSoC hardware.

Figure 1-3. ModusToolbox IDE Resources and Middleware



### 1.3.1 ModusToolbox Code Examples

ModusToolbox includes a large number of code examples. Many of these code example are compatible with this kit. You can either browse the collection of starter applications during application set up through **File > New > ModusToolbox IDE Application** or browse the collection of code examples on Cypress' GitHub repository. See [Figure 1-4](#) and [Figure 1-5](#) for details.

Figure 1-4. Code Examples in ModusToolbox IDE

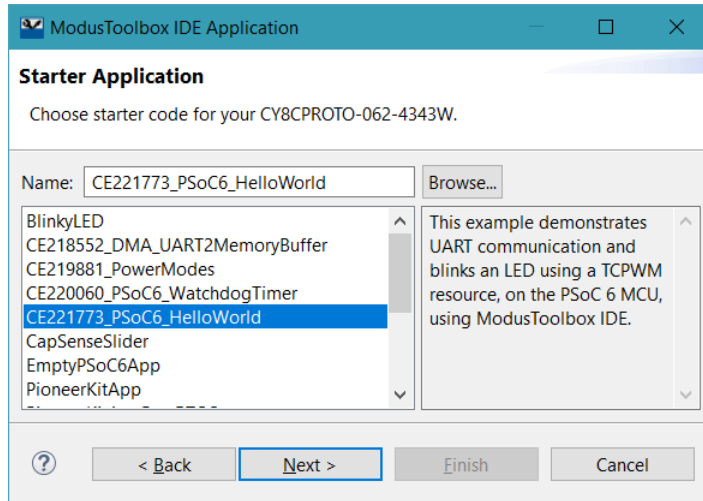
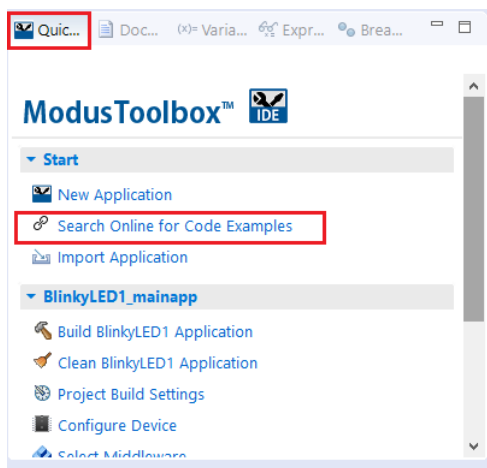


Figure 1-5. Browse Code Examples Online



### 1.3.2 ModusToolbox Help

Launch ModusToolbox and navigate to the following items:

- **Quick Start Guide:** Choose **Help > ModusToolbox IDE Documentation > Quick Start Guide**. This guide gives you the basics for using ModusToolbox IDE.
- **User Guide:** Choose **Help > ModusToolbox IDE Documentation > User Guide**. This is a comprehensive guide for creating, building, and programming ModusToolbox applications.
- **ModusToolbox Documentation:** Choose **ModusToolbox General Documentation > ModusToolbox Documentation Index**. This page provides link to various ModusToolbox documents.

## 1.4 Getting Started

This guide will help you to get acquainted with the PSoC 6 Wi-Fi BT Prototyping Kit:

- PSoC 6 Wi-Fi BT Prototyping Kit requires ModusToolbox 1.0 to design and debug applications. Download and install ModusToolbox from [www.cypress.com/modustoolbox](http://www.cypress.com/modustoolbox). See the [ModusToolbox Installation Guide](#) for additional information.
- The [Kit Operation chapter on page 18](#) describes the major features of the board and functionalities such as programming, debugging, and the USB-UART and USB-I2C bridges.
- The [Code Examples chapter on page 27](#) describes multiple PSoC 6 MCU code examples that will help you understand how to create your own applications.
- The [Appendix on page 26](#) provides a detailed hardware description, methods to use the onboard NOR Flash, kit schematics, and the bill of materials (BOM).

## 1.5 Additional Learning Resources

Cypress provides a wealth of data at [www.cypress.com/psoc6](http://www.cypress.com/psoc6) to help you to select the right PSoC device for your design and to help you to quickly and effectively integrate the device into your design.

## 1.6 Technical Support

For assistance, visit [Cypress Support](#) or contact customer support at +1(800) 541-4736 Ext. 3 (in the USA) or +1 (408) 943-2600 Ext. 3 (International).

You can also use the following support resources if you need quick assistance:

- [Self-help \(Technical Documents\)](#)
- [Local Sales Office Locations](#)

## 1.7 Documentation Conventions

Table 1-2. Document Conventions for Guides

Convention	Usage
Courier New	Displays file locations, user entered text, and source code: C:\...\cd\icc\
<i>Italics</i>	Displays file names and reference documentation: Read about the <i>sourcefile.hex</i> file in the <i>PSoC Creator User Guide</i> .
[Bracketed, Bold]	Displays keyboard commands in procedures: [Enter] or [Ctrl] [C]
File > Open	Represents menu paths: File > Open > New Project
<b>Bold</b>	Displays commands, menu paths, and icon names in procedures: Click the <b>File</b> icon and then click <b>Open</b> .
Times New Roman	Displays an equation: $2 + 2 = 4$
Text in gray boxes	Describes cautions or unique functionality of the product.

## 1.8 Acronyms

Table 1-3. Acronyms Used in this Document

Acronym	Definition
ADC	Analog-to-Digital Converter
API	Application Programming Interface
AWS	Amazon Web Services
BLE	Bluetooth Low Energy
BOM	Bill of Materials
CINT	Integration Capacitor
CMOD	Modulator Capacitor
CPU	Central Processing Unit
CSD	CapSense Sigma Delta
CSX	CapSense Crosspoint
CTANK	Shield Tank Capacitor
DC	Direct Current
Del-Sig	Delta-Sigma
DMA	Direct Memory Access
ECO	External Crystal Oscillator
ESD	Electrostatic Discharge
FPC	Flexible Printed Circuit
GDB	GNU Debugger
GPIO	General-Purpose Input/Output
HID	Human Interface Device
I <sup>2</sup> C	Inter-Integrated Circuit
I <sup>2</sup> S	Inter-IC Sound
IC	Integrated Circuit
ICSP	In-Circuit Serial Programming
IDAC	Current Digital-to-Analog Converter
IDE	Integrated Development Environment
IoT	Internet of Things
LED	Light-emitting Diode
LPO	Low Power Oscillator
PC	Personal Computer
PDL	Peripheral Driver Library
PDM	Pulse Density Modulation
PMOD	Peripheral Modules
PSoC	Programmable System-on-Chip
PTC	Positive Temperature Coefficient
PWM	Pulse Width Modulation



Table 1-3. Acronyms Used in this Document (*continued*)

Acronym	Definition
QSPI	Quad Serial Peripheral Interface
RTOS	Real Time Operating System
SAR	Successive Approximation Register
SDHC	Secure Digital Host Controller
SDIO	Secure Digital Input Output
SDK	Software Development Kit
SMIF	Serial Memory Interface
SPI	Serial Peripheral Interface
SRAM	Serial Random Access Memory
SSID	Service Set Identifier
SWD	Serial Wire Debug
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
WCO	Watch Crystal Oscillator
WICED	Wireless Internet Connectivity for Embedded Devices

# 2. Kit Operation



This chapter introduces you to various features of the PSoC 6 Wi-Fi BT Prototyping Kit, including the theory of operation and the onboard programming and debugging functionality, KitProg3 USB-UART and USB-I2C bridges.

## 2.1 Theory of Operation

The PSoC 6 Wi-Fi BT Prototyping Kit is built around a PSoC 6 MCU. [Figure 2-1](#) shows the block diagram of the PSoC 6 MCU device used in the kit. For details of device features, see the [device datasheet](#).

Figure 2-1. PSoC 6 MCU Block Diagram

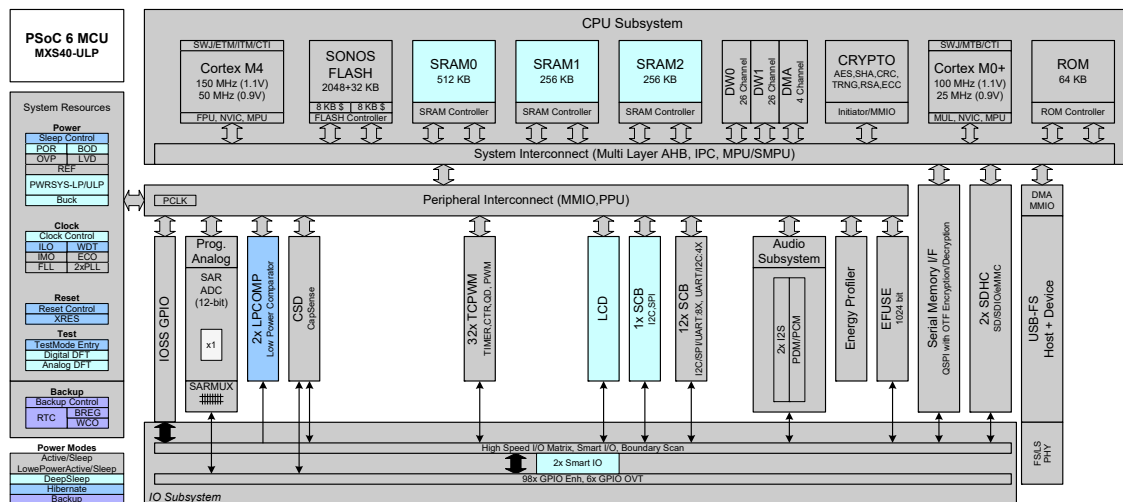
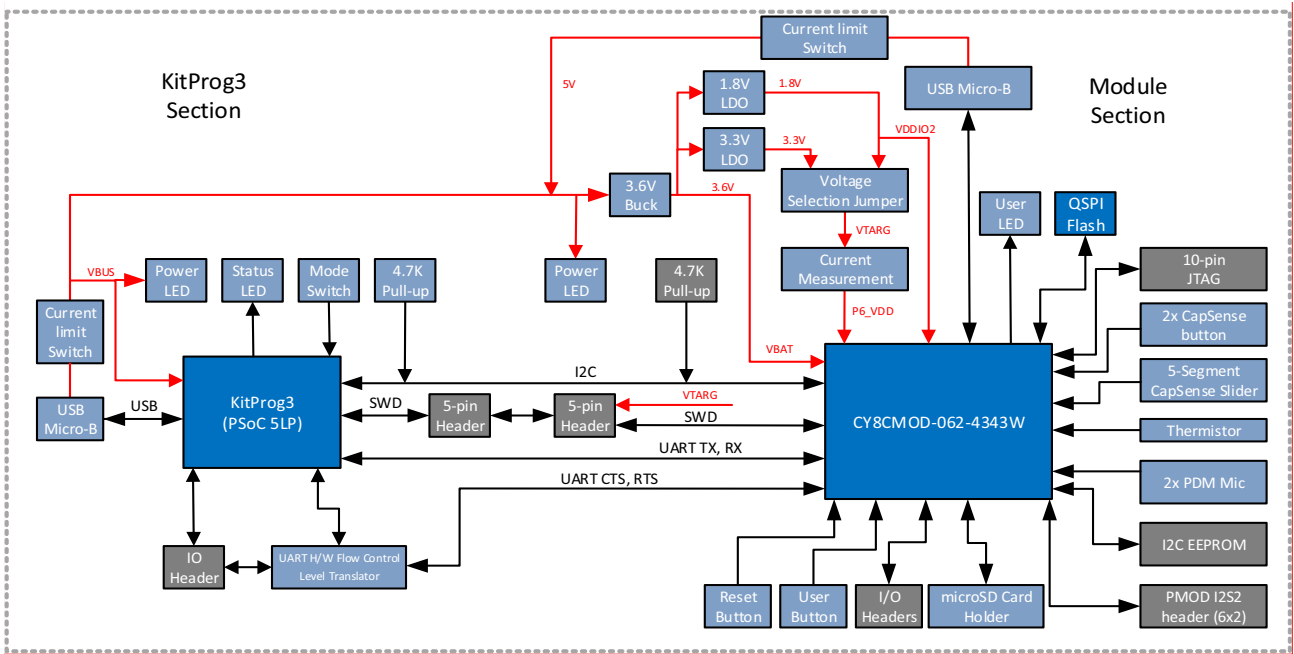
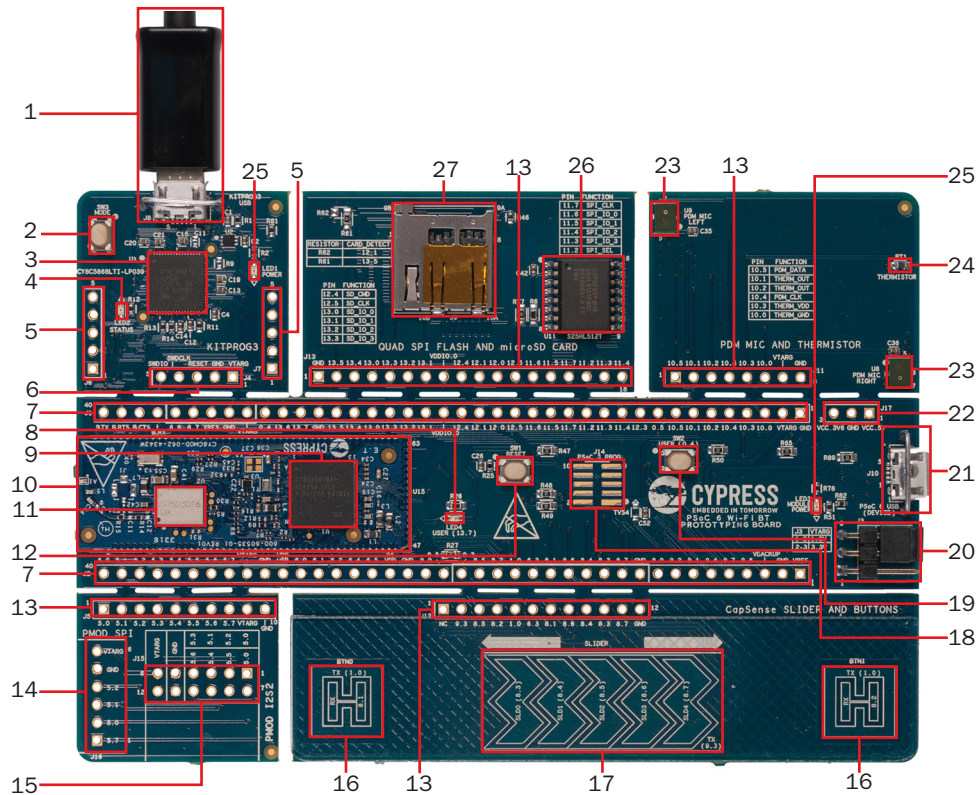


Figure 2-2. Block Diagram of the Board



The PSoC 6 Wi-Fi BT Prototyping Board consists of multiple sections, a KitProg3 section, PSoC 6 MCU section and other peripheral sections. An on-board programmer, KitProg3 is used to program and debug the target PSoC 6 MCU. Refer to [KitProg3 on page 23](#) and [Hardware Functional Description on page 26](#) for more details on these sections.

Figure 2-3. Board - Top View



The board has the following peripherals:

1. **KitProg3 USB connector (J8):** The USB cable provided along with the PSoC 6 Wi-Fi BT Prototyping Board connects between this USB connector and the PC to use the KitProg3 onboard programmer and debugger and to provide power to the board.
2. **KitProg3 programming mode selection button (SW3):** This button can be used to switch between various modes of operation of KitProg3 (CMSIS-DAP/Bulk or CMSIS-DAP/HID mode). This button can also be used to provide input to PSoC 5LP in custom application mode. For more details, see the [KitProg3 User Guide](#). By default, the programming mode is set to CMSIS-DAP/Bulk which allows faster programming than CMSIS-DAP/HID.
3. **KitProg3 (PSoC 5LP) programmer and debugger (CY8C5868LTI-LP039, U1):** The PSoC 5LP device (CY8C5868LTI-LP039) serving as KitProg3, is a multi-functional system, which includes a SWD programmer, debugger, USB-I2C bridge and USB-UART bridge. KitProg3 also supports custom applications. For more details, see the [KitProg3 User Guide](#).
4. **KitProg3 status LED (LED2):** Amber LED (LED2) indicates the status of KitProg3. For details on the KitProg3 status, see the [KitProg3 User Guide](#). By default this LED should be ON which indicates CMSIS-DAP/Bulk mode.

5. **KitProg3 I/O headers (J6, J7):** These headers bring out the USB-UART and USB-I2C interface pins of the KitProg3. If the KitProg3 Section is broken away, it is also necessary to connect VTARG and GND as those are used for voltage level translation. For more details on the KitProg3, see the [KitProg3 User Guide](#).
6. **KitProg3 5-pin programming header (J4):** This header brings out the SWD interface pins of the KitProg3. This is used to program and debug the PSoC 6 MCU. If KitProg3 section is broken away, it can be used to program any device over the 5-pin interface. Please note that VTARG is an input to KitProg3, and hence the target must be powered externally in that case. The on-board regulators on the PSoC 6 MCU section provide VTARG. For more details on the KitProg3, see the [KitProg3 User Guide](#).
7. **PSoC 6 MCU I/O headers (J1, J2):** These headers provide connectivity to PSoC 6 MCU GPIOs. Most of these I/Os are also connected to on-board peripherals.
8. **PSoC 6 MCU user LED (LED4):** The user LED can operate at the entire operating voltage range of PSoC 6 MCU. The LED is active LOW, so the pins must be driven to ground to turn ON the LED.
9. **PSoC 6 MCU:** This kit is designed to highlight the features of the PSoC 6 MCU. For details on PSoC 6 MCU pin mapping, see [Table 1-1 on page 10](#).
10. **Cypress PSoC 6 Wi-Fi BT Module (CY8CMOD-062-4343W, U1):** This kit is designed to highlight the features of the PSoC 6 MCU on the CY8CMOD-062-4343W. For details on see the module datasheet.
11. **CYW4343W based Murata 1DX Module:** The Type 1DX module is an ultra-small module that includes 2.4 GHz WLAN and Bluetooth functionality. Based on the Cypress CYW4343W, the module provides high-efficiency RF front end circuits. To ease Wi-Fi certification, the Type 1DX module complies with IEEE 802.11b/g/n and Bluetooth Version 4.1 plus EDR, Power Class 1 (10 dBm max) + BLE.
12. **Reset button (SW1):** This button is used to reset the PSoC 6 MCU. This button connects the PSoC 6 MCU reset (XRES) pin to ground.
13. **On-board peripheral headers (J5, J11, J12 and J13):** On-board peripherals are divided into sections. Each section is independent and can be broken away from the PSoC 6 MCU section.
14. **Digilent Pmod compatible SPI header (J16):** This header can be used to connect Digilent Pmod 1 × 6 pin SPI modules.
15. **Digilent Pmod compatible I2S2 header (J15):** This header can be used to connect Digilent Pmod 2 × 6 pin I2S2 modules.
16. **CapSense buttons (BTN0 and BTN1):** CapSense touch-sensing buttons, capable of both self-capacitance (CSD) and mutual-capacitance (CSX) operation, let you evaluate Cypress' fourth-generation CapSense technology.
17. **CapSense slider:** CapSense touch-sensing slider capable of both self-capacitance (CSD) and mutual-capacitance (CSX) operation. The slider and the buttons have a 1-mm acrylic overlay for smooth touch sensing.
18. **PSoC 6 MCU program and debug header (J14):** This 10-pin header allows you to program and debug the PSoC 6 MCU using an external programmer such as [MiniProg4](#). Please note that this header is not loaded by default.

19. **PSoC 6 MCU user button (SW2):** This button can be used to provide an input to the PSoC 6 MCU. Note that by default the button connects the PSoC 6 MCU pin to ground when pressed, so you need to configure the PSoC 6 MCU pin as a digital input with resistive pull-up for detecting the button press. This button also provides a wake-up source from low-power modes of the device. In addition, this button can be used to activate the PMIC control from PSoC 6 MCU.
20. **System power selection jumper (J3):** This jumper is used to select the PSoC 6 MCU's supply voltage (P6.VDD) between 1.8 V and 3.3 V.
21. **PSoC 6 USB Device Connector (J10):** The USB cable provided with the PSoC 6 Wi-Fi BT Prototyping Kit can also be connected between this USB connector and the PC to use the PSoC 6 MCU USB device applications.
22. **External Power Supply connector (J17):** This connector connects an external DC power supply input to the onboard regulators. The voltage input from the external supply should be between 4.5 V and 5.5 V.
23. **PDM Microphones(U8, U9):** Two microphones convert voice inputs to Pulse-Density Modulated (PDM) digital signals.
24. **Thermistor(RT1):** This thermistor can be used for temperature compensation or as a general purpose ambient temperature sensor.
25. **Power LEDs (LED1, LED3):** LED1 and LED3 are amber LEDs that indicate the status of power supplied to PSoC 5LP and PSoC 6 MCU respectively.
26. **Cypress 512-Mbit serial NOR flash memory (S25HL512T, U11):** The S25HL512T NOR flash of 512Mb capacity is connected to the serial memory interface (SMIF) of the PSoC 6 MCU. The NOR flash can be used for both data and code memory with execute-in-place (XIP) support and encryption.
27. **microSD Card holder (J9):** Provide SDHC interface with microSD cards with the option to detect the presence of the card.

See [Hardware Functional Description on page 26](#) for details on various hardware blocks.

## 2.2 KitProg3

KitProg3 is an onboard programmer/debugger with USB-UART and USB-I2C functionality. A Cypress PSoC 5LP device is used to implement KitProg3 functionality. For more details on the KitProg3 functionality, see the [KitProg3 User Guide](#).

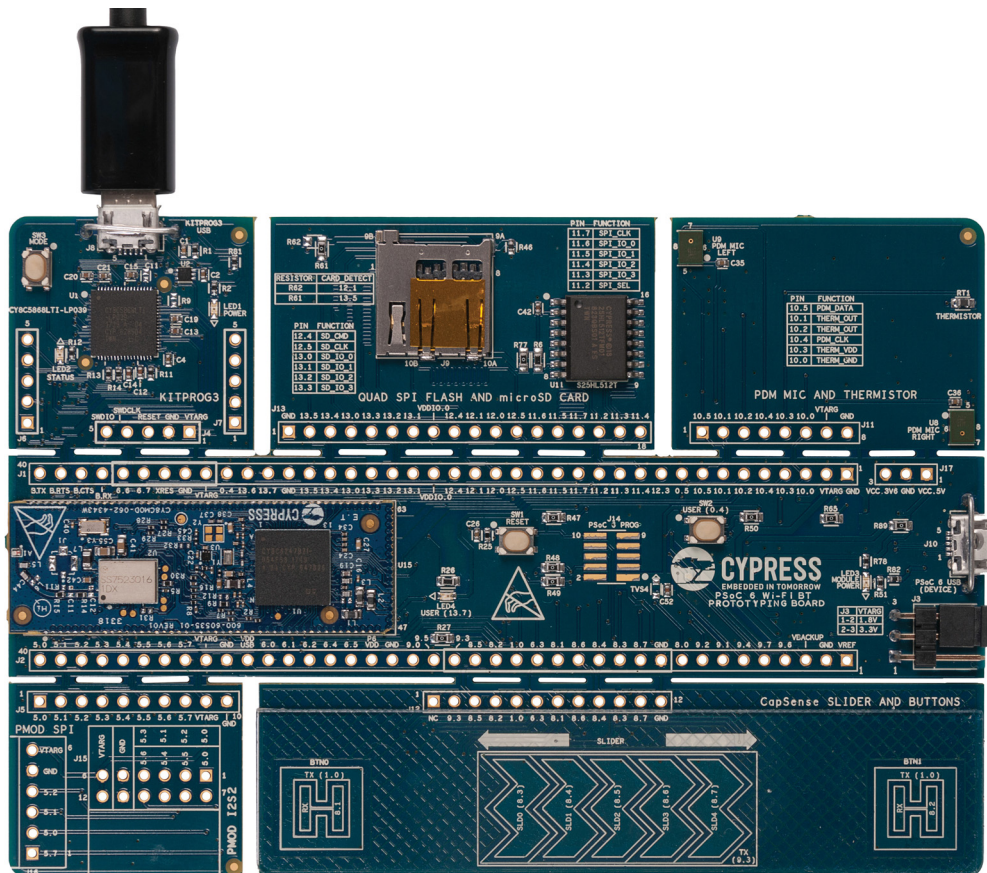
Before programming the device, ensure that ModusToolbox software is installed on the computer.

### 2.2.1 Programming and Debugging using ModusToolbox

This section presents a quick overview of programming and debugging using ModusToolbox. For detailed instructions, see **Help > ModusToolbox IDE Documentation > User Guide**.

1. Connect the board to the PC using the USB cable, as shown in [Figure 2-4](#). It enumerates as a USB Composite Device if you are connecting it to your PC for the first time. KitProg3 can operate either in CMSIS-DAP HID mode or CMSIS-DAP Bulk mode (default). Programming is faster with the Bulk mode. The status LED (Amber) is always ON in Bulk mode and is ramping (increasing and decreasing brightness) at 1 Hz rate in HID mode. Press and release the Mode select button (SW3) to switch between these modes. If you do not see the desired LED status, see the [KitProg3 User Guide](#) for details on the KitProg3 status and troubleshooting instructions.

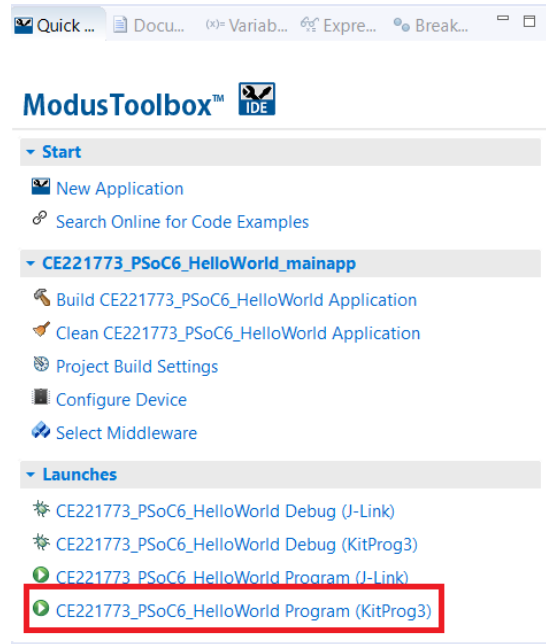
Figure 2-4. Connect USB Cable to USB Connector on the Board



2. In the ModusToolbox IDE, import the desired application into a new workspace. If you aren't familiar with this process, see [KBA225201](#).

3. To build and program a PSoC 6 MCU application, in the Project Explorer, select **<App\_Name>\_mainapp** project. In the Quick Panel, scroll to the **Launches** section and click the **Program (KitProg3)** configuration as shown in [Figure 2-5](#).

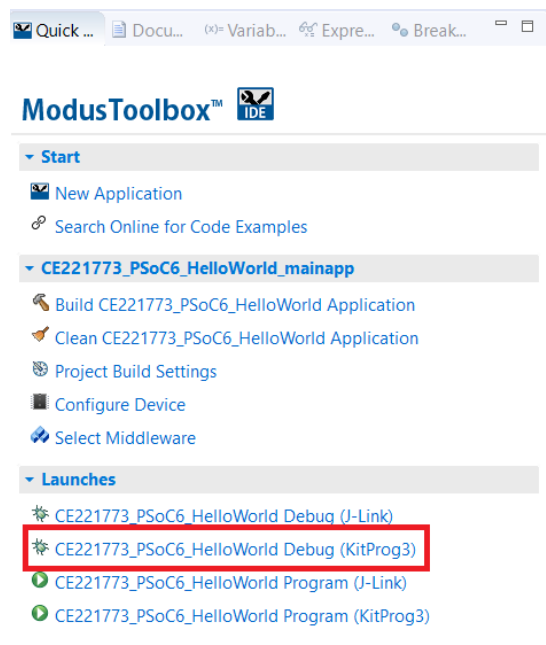
Figure 2-5. Programming in ModusToolbox



4. ModusToolbox has an integrated debugger. To debug a PSoC 6 MCU application, in the Project Explorer, select **<App\_Name>\_mainapp** project. In the Quick Panel, scroll to the **Launches** section and click the **Program (KitProg3)** configuration as shown in [Figure 2-6](#).

For a detailed explanation on how to debug using ModusToolbox, see [KBA224621](#).

Figure 2-6. Debugging in ModusToolbox

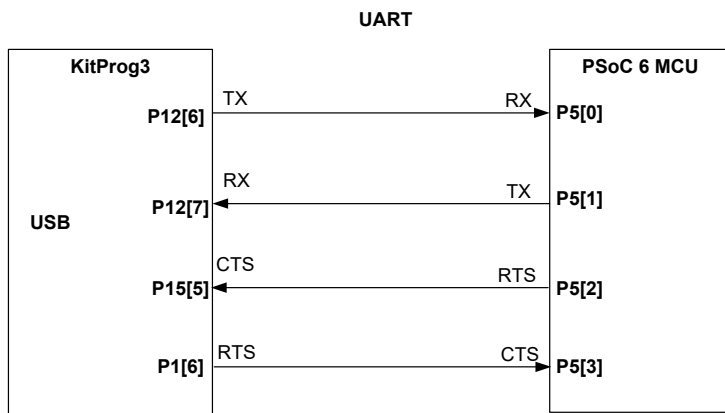




### 2.2.2 USB-UART Bridge

The onboard KitProg3 can function as a USB-UART bridge. The UART and flow-control lines between the PSoC 6 MCU and the KitProg3 are hard-wired on the board, as [Figure 2-7](#) shows. For more details on the KitProg3 USB-UART functionality, see the [KitProg3 User Guide](#).

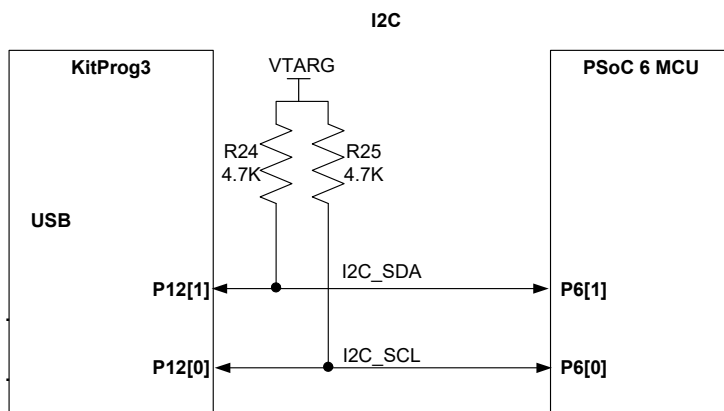
Figure 2-7. UART connection between KitProg3 and PSoC 6 MCU



### 2.2.3 USB-I2C Bridge

The onboard KitProg3 also functions as a USB-I2C bridge, for example, to communicate with the CapSense Tuner. The I2C lines on the PSoC 6 MCU are hard-wired on the board to the I2C lines of the KitProg3 with onboard pull-up resistors as [Figure 2-8](#) shows. The USB-I2C supports I2C speeds of 50 kHz, 100 kHz, 400 kHz, and 1 MHz. For more details on the KitProg3 USB-I2C functionality, see the [KitProg3 User Guide](#).

Figure 2-8. I2C connection between KitProg3 and PSoC 6 MCU



# A. Appendix



## A.1 Schematics

Schematics can be downloaded from [www.cypress.com/CY8CPROTO-062-4343W](http://www.cypress.com/CY8CPROTO-062-4343W).

## A.2 Hardware Functional Description

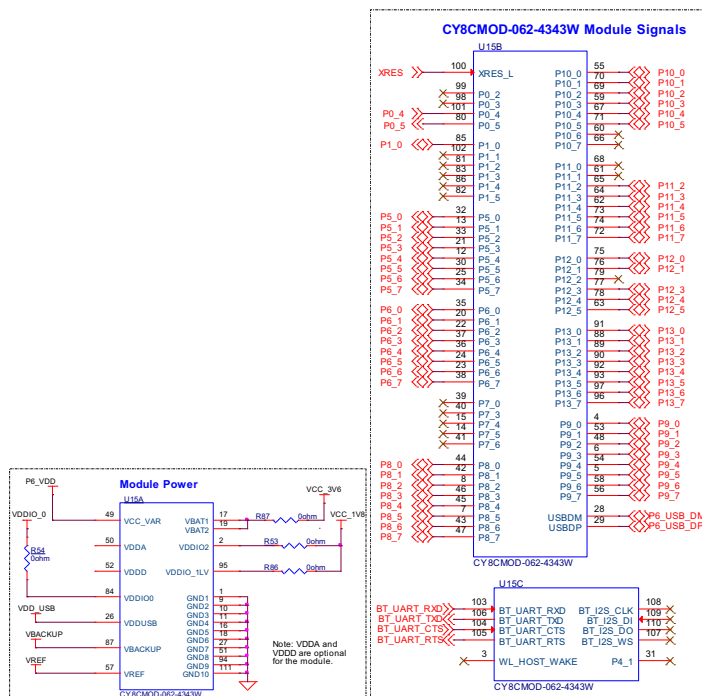
This section explains in detail the individual hardware blocks of the PSoC 6 Wi-Fi BT Prototyping Board.

### A.2.1 CY8CMOD-062-4343W (U15)

The Cypress CY8CMOD-062-4343W is a pre-certified module supporting 2.4 GHz WLAN and Bluetooth functionality. The CY8CMOD-062-4343W module is a turnkey solution and includes PSoC 6 MCU, CYW4343W Single-Chip radio, onboard oscillators, chip antenna and passive components. The CY8CMOD-062-4343W module provides up to 80 I/Os of PSoC 6 MCU and 9 I/Os of CYW4343W in a 47 × 16 × 2 mm package.

63 I/Os of PSoC 6 MCU and 4 I/Os of CYW4343W have been brought out on headers J1 and J2.

Figure A-1. Schematics of CY8CMOD-062-4343W (U15)



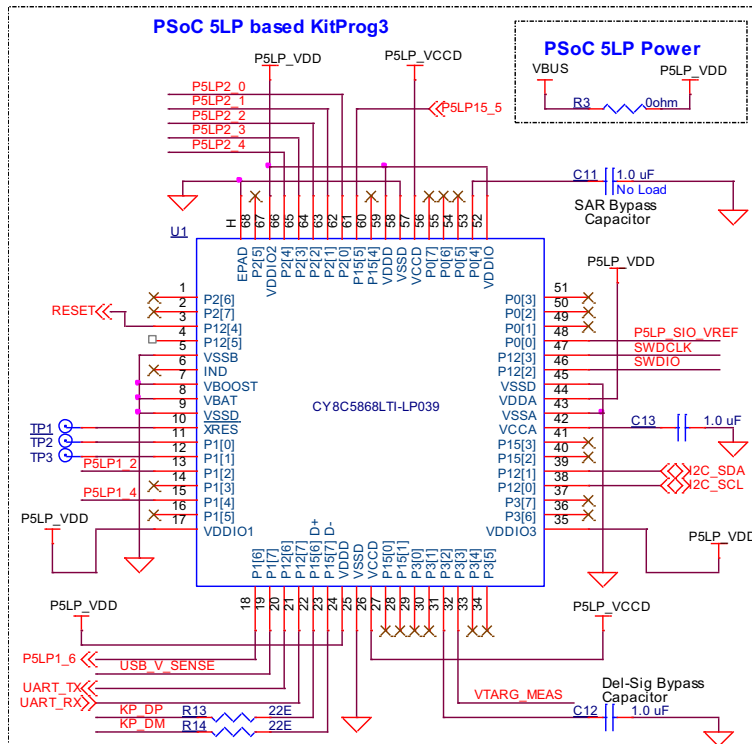
For more information, see the [CY8CMOD-062-4343W](http://www.cypress.com/CY8CMOD-062-4343W) web page and the [datasheet](#).

### A.2.2 PSoC 5LP (U1)

An onboard PSoC 5LP (CY8C5868LTI-LP039) is used as a KitProg3 to program and debug the PSoC 6 MCU. The PSoC 5LP is a bridge between the USB port of a PC and the SWD and other communication interfaces of the PSoC 6 MCU. The PSoC 5LP is a true system-level solution providing MCU, memory, analog, and digital peripheral functions in a single chip. The CY8C58LPxx family offers a modern method of signal acquisition, signal processing, and control with high accuracy, high bandwidth, and high flexibility. Analog capability spans the range from thermocouples (near DC voltages) to ultrasonic signals.

For more information, visit the [PSoC 5LP web page](#). Also, see the [CY8C58LPxx Family Datasheet](#).

Figure A-2. Schematics of PSoC 5LP (U1)



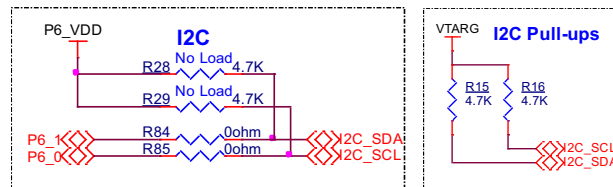
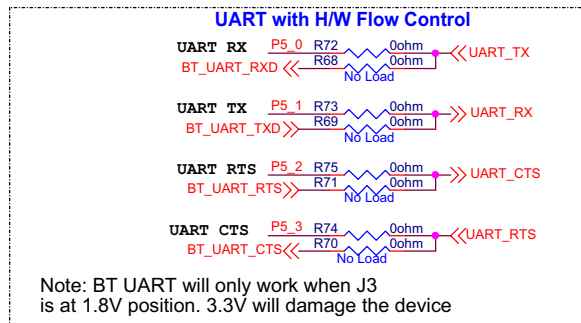
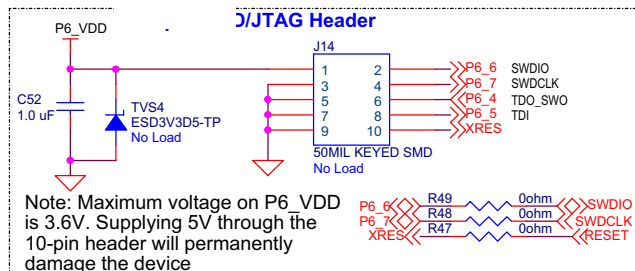
### A.2.3 Serial Interconnection between PSoC 5LP and PSoC 6 MCU

The PSoC 5LP functions as USB-UART and USB-I2C bridge as shown in [Figure A-3](#). The USB-Serial pins of the PSoC 5LP are hard-wired to the I2C/UART pins of the PSoC 6 MCU. These pins are also available on the breadboard-compatible I/O headers.

The 10-pin header **J14** allows you to program and debug PSoC 6 MCU using an external programmer such as MiniProg4.

Optionally, you can route BT\_UART to PSoC 5LP. This is used to debug BT on CYW4343W using the USB-UART. Note that VTARG must be 1.8 V in this configuration. Detailed instructions can be found in [PSoC 6 Wi-Fi BT Prototyping Board Rework on page 36](#).

Figure A-3. Schematics of Programming and Serial Interface Connections



## A.2.4 Power Supply System

The power supply system on this board allows the input supply to come from the following sources:

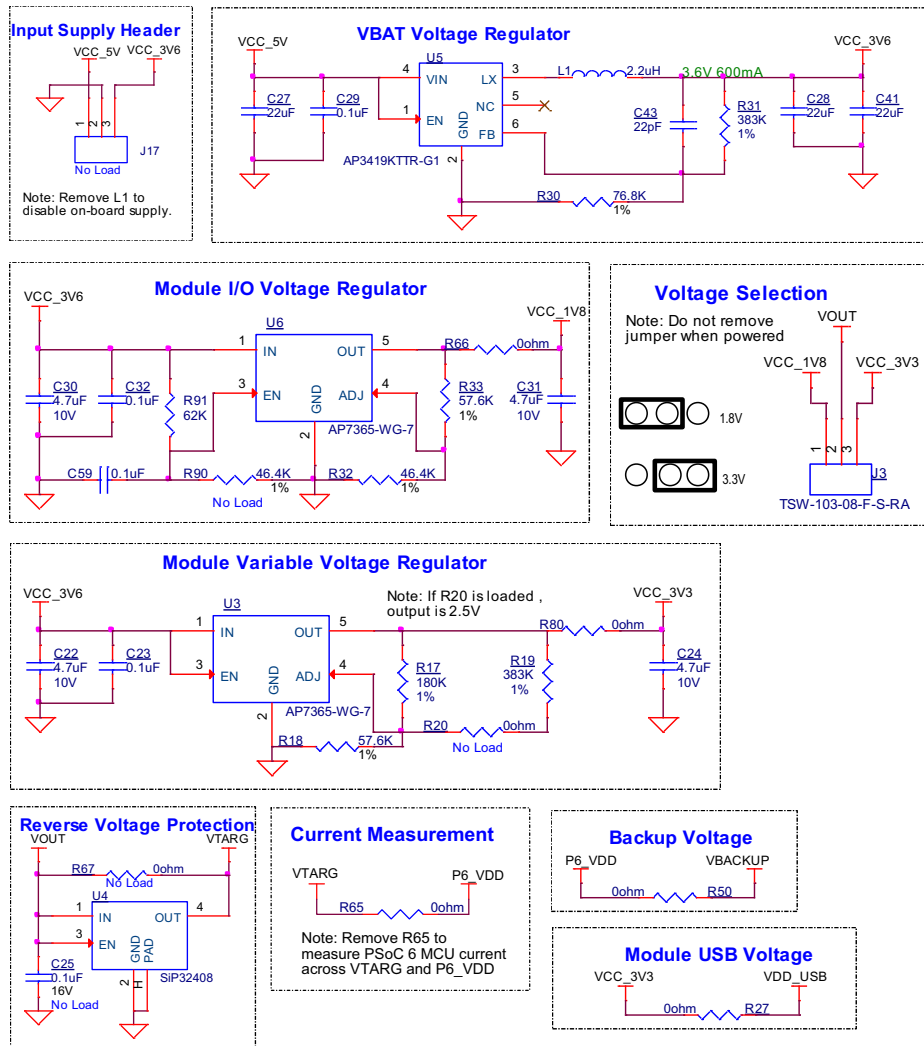
- 5 V from the onboard USB Micro-B connectors (**J8** and **J10**)
- 5 V from external power supply through VCC\_5V at **J17.1**
- 1.8 V–3.6 V from external programmer through VTARG at **J1.32**
- 1.8 V–3.6 V from external programmer through P6\_VDD at **J14**

The power supply system is designed to support 1.8 V to 3.3 V operation of the PSoC 6 MCU. A voltage of 5 V is provided from USB port and is required for the operation of KitProg3. Three regulators are used to achieve 1.8 V to 3.3 V and 3.6 V outputs - a buck regulator (**U5**) that generates a fixed 3.6 V from an input of 5 V, a fixed 3.3 V regulator (**U3**) and a fixed 1.8 V regulator (**U6**) is powered from the output of **U5**. **Figure A-4** shows the schematics of the voltage regulator and power selection circuits.

The voltage selection is made through jumper **J3**. Populate R20 to change output of U3 to 2.5 V.

**Note:** Do not power the board without a Jumper shunt present on J3.

Figure A-4. Schematics of Power Supply System

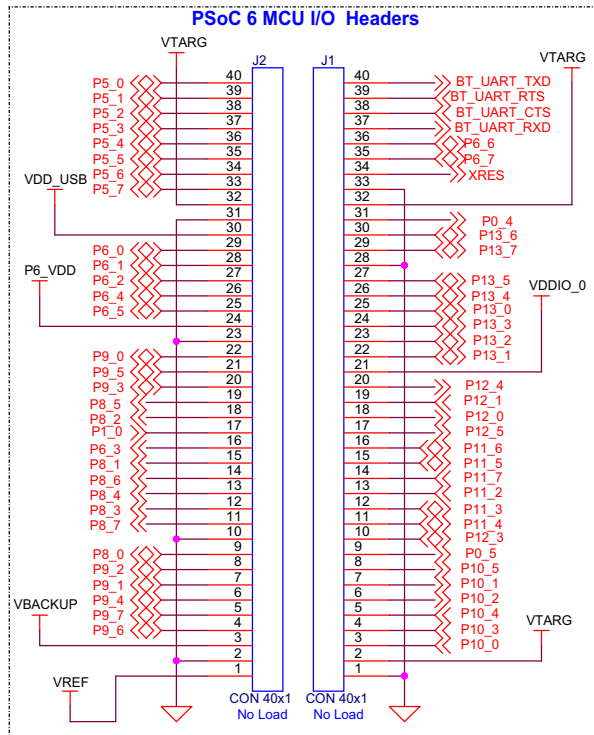


## A.2.5 Expansion Connectors

### A.2.5.1 PSoC 6 MCU I/O Headers (J1 and J2)

These headers provide connectivity to PSoC 6 MCU GPIOs. Most of these pins are multiplexed with onboard peripherals.

Figure A-5. Schematics of PSoC 6 MCU I/O Headers (J1 and J2)



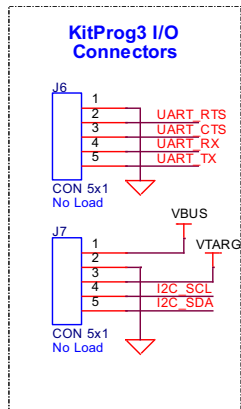
On-board peripherals are distributed in sections and each section can be broken away from the PSoC 6 MCU section. To re-connect the individual sections, headers **J5**, **J11**, **J12** and **J13** are provided. These are not loaded by default.

### A.2.5.2 KitProg3 GPIO Headers (J6 and J7)

J6 and J7 are 5x1 headers provided on the KitProg3 section of the board. These headers bring out the USB-UART and USB-I2C bridge pins that can be used when the section is broken apart. Note that the RTS, and CTS lines on these headers are from the level translators, not directly from PSoC 5LP. J6 and J7 are not loaded by default.

**Note:** when using the module separately for UART and I2C, make sure that VTARG is connected to the target voltage to ensure proper level translation.

Figure A-6. Schematics of PSoC 5LP GPIO Headers (J6 and J7)

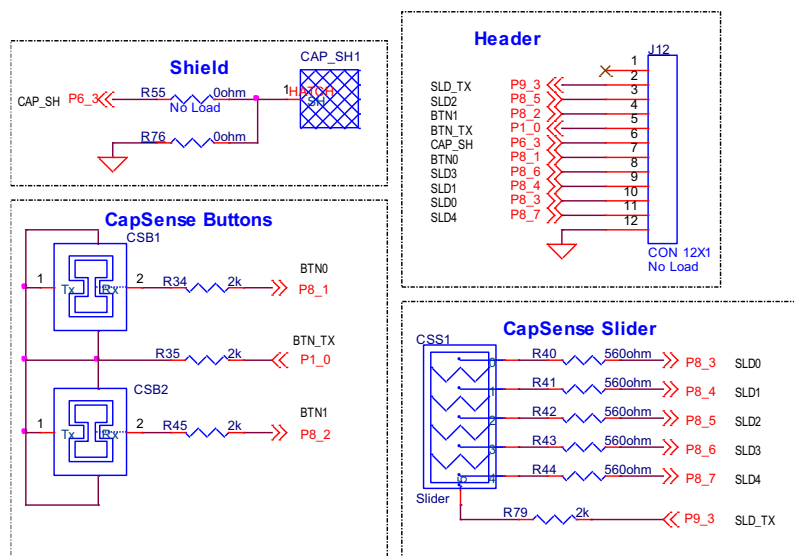


### A.2.6 CapSense Circuit

There is a CapSense slider and two buttons, all of which support both self-capacitance (CSD) and mutual-capacitance (CSX) sensing. These are connected to the PSoC 6 MCU as [Figure A-7](#) shows. Three external capacitors - CMOD (P7[7]) for CSD and CINTA (P7[1]), CINTB (P7[2]) for CSX are present on the CY8CMOD-062-4343W. Note that CINTA can be re-used as CSH. For details on using CapSense including design guidelines, see the [Getting Started with CapSense Design Guide](#).

The CapSense section can be broken away and re-connected to PSoC 6 MCU at **J2.10** to **J2.21** through **J12**.

Figure A-7. Schematics of CapSense Circuit

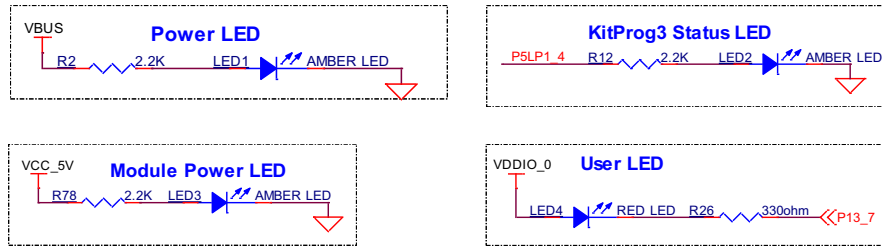


### A.2.7 LEDs

**LED2** (Amber) indicates the status of the KitProg3 (See the [KitProg3 User Guide](#) for details). **LED1** and **LED3** (Amber LEDs) indicate the status of power supplied to PSoC 5LP and CY8CMOD-062-4343W respectively.

The board also has one user controllable red LED (**LED4**) connected to PSoC 6 MCU pin P13[7] in active-low configuration for user applications.

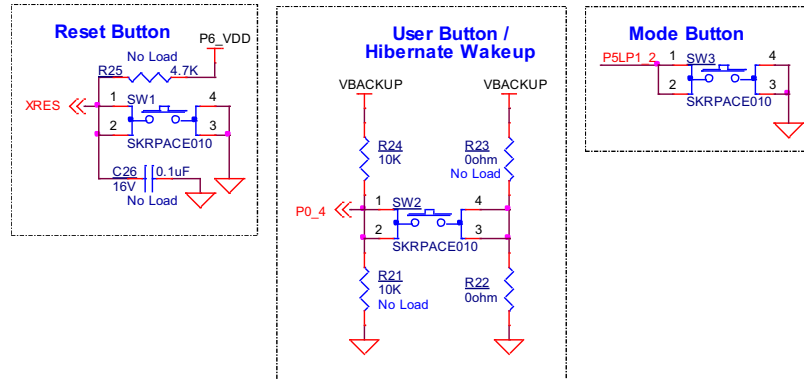
Figure A-8. Schematics of LEDs



### A.2.8 Push Buttons

The board has a reset button (**SW1**) is connected to the XRES pin of the PSoC 6 MCU and is used to reset the device. One user button (**SW2**) is connected to pin P0[4] of the PSoC 6 MCU. The remaining button - **SW3** is connected to the PSoC 5LP device for programming mode and custom app selection (Refer to the [KitProg3 User Guide](#) for details). All the buttons connect to ground on activation (active low) by default. User button (**SW2**) can be changed to active high mode by changing the zero resistors shown below.

Figure A-9. Schematics of Push Buttons





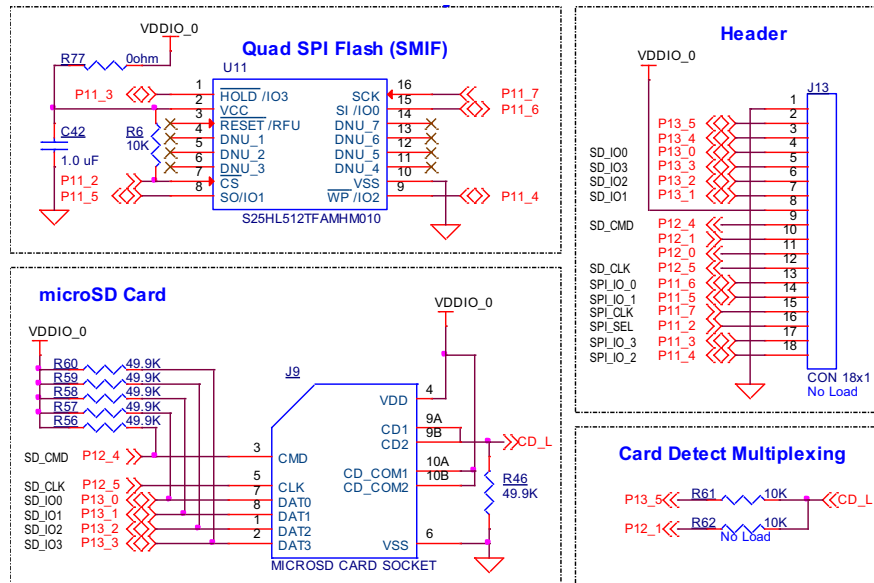
## A.2.9 Cypress Quad SPI NOR Flash and microSD card

The board has a Cypress NOR Flash memory ([S25HL512TFAMHM010](#)) of 512 Mbit capacity. The NOR Flash is connected to the serial memory interface (SMIF) of the PSoC 6 MCU. The NOR Flash device can be used for both data and code memory with execute-in-place (XIP) support and encryption.

The board contains a slot to insert a microSD card (see [Figure A-10](#)), which can be accessed through SDHC interface.

This section can be broken apart from the PSoC 6 MCU section at the built-in perforated edge between **J1** and **J13**. To connect them back, use right angled male-to-female connectors between **J13** and **J1** (**J1.11** to **J1.28**).

Figure A-10. Schematics of Quad SPI Flash and microSD card holder



### A.2.10 PDM Microphones and Thermistor

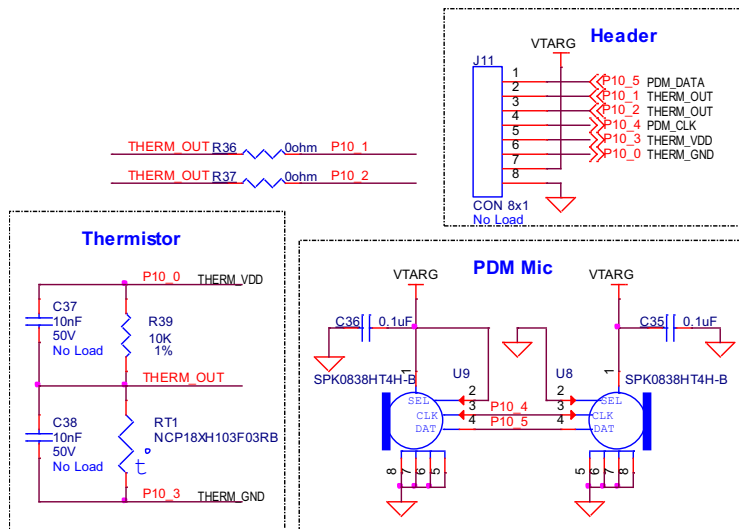
The board includes two PDM Microphones (U8 and U9) and a thermistor (RT1) connected to the PSoC 6 MCU device.

The PDM mics share the same clock and data lines and one is configured on the left channel and the other on the right channel. They are 40 mm apart.

This section can be broken apart from the PSoC 6 MCU section at the built-in perforated edge between **J1** and **J11**. To connect them back, use right angled male-to-female connectors between **J11** and **J1** (**J1.1** to **J1.8**).

**Note:** P10[1] and P10[2] are connected to THERM\_OUT by default. Remove R36 and R37 to disconnect P10[1] and P10[2] respectively.

Figure A-11. Schematics of PDM Mic and Thermistor



## A.2.11 Digilent Pmod™ Headers

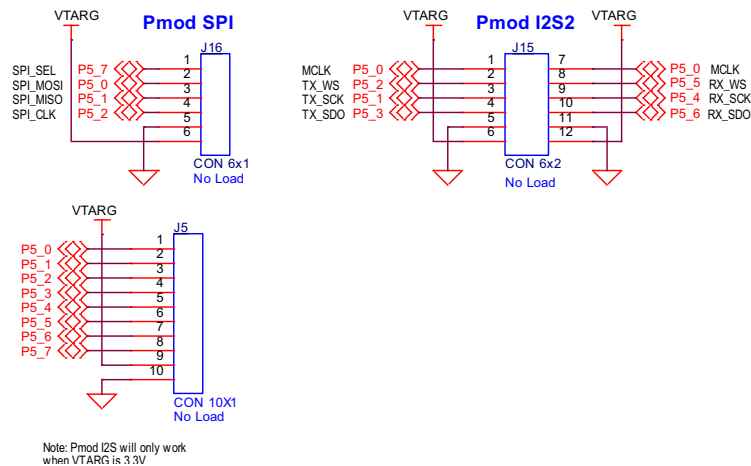
There are two Digilent Pmod™ headers present on the board. 6x1 pin header (J16) is compatible with Pmod SPI and a 6x2 pin header (J15) is compatible with Pmod I2S2.

Both are not loaded by default.

This section can be broken apart from the PSoC 6 MCU section at the built-in perforated edge between **J2** and **J5**. To connect them back, use right angled male-to-female connectors between **J5** and **J2** (**J2.30** to **J2.40**).

**Note:** Remove R72, R73, R74, R75 to use Pmod because the same pins (Port 5 of the PSoC 6 MCU) are used for UART by default.

Figure A-12. Schematics of Pmod Headers



## A.3 PSoC 6 Wi-Fi BT Prototyping Board Rework

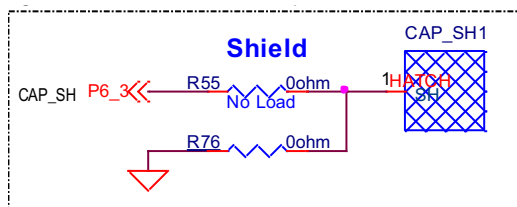
This section explains modifications that can be made to the board to evaluate different use cases.

### A.3.1 CapSense Shield

The hatched pattern around the CapSense buttons and slider are connected to ground. In case liquid tolerance is required, this pattern needs to be connected to the shield pin. This pattern can be connected to pin P6[3] by populating resistor R55. The resistor R76 connecting the hatched pattern to ground needs to be removed in that case. P6[3] needs to be configured as a shield pin in ModusToolbox.

Connecting the hatched pattern to shield instead of ground will also reduce parasitic capacitance of the sensors.

Figure A-13. Schematics of CapSense Shield



### A.3.2 BT (Bluetooth) UART

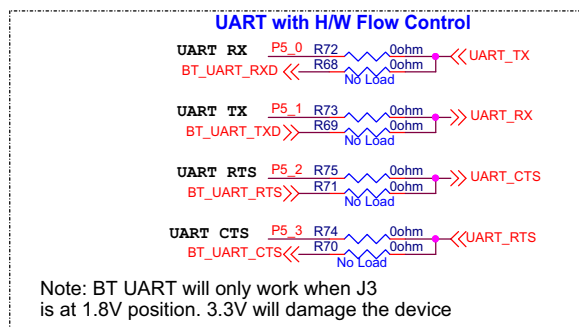
The BT\_UART Port is accessible on J1.37 to J1.40. The operating voltage for these pins is VDDIO\_2. By default this is 1.8V and there is no option to change it.

This option allows for debug of the BT core on the CWY4343W using KitProg3 USB-UART bridge interface.

Remove R72, R73, R74 and R75.

Populate R68, R69, R70 and R71.

Figure A-14. Schematics of BT UART



## A.4 Bill of Materials

BOM can be downloaded from [www.cypress.com/CY8CPROTO-062-4343W](http://www.cypress.com/CY8CPROTO-062-4343W).

## A.5 Frequently Asked Questions

1. How does CY8CPROTO-062-4343W handle voltage connection when multiple power sources are plugged in?

There are five different options to power the board; KitProg3 USB connector (**J8**), PSoC 6 Device USB connector (**J10**), External DC supply through VCC\_5V at **J17.1**, from an external programmer through VTARG at **J1.32**, and from an external programmer through P6\_VDD at **J14**. The voltage from each of the USB connectors passes through a current limiting switch that also protects against reverse voltage. The output of both current limit switches is given to the VCC.5V that is also present on **J17**.

Note that powering the board from an external programmer (VTARG at **J1.32** or P6\_VDD at **J14**) powers the P6\_VDD power domain only.

2. What are the input voltage tolerances? Is there any overvoltage protection on this kit?

Input voltage level are as follows:

Table A-1. Input voltage levels

Supply	Typical i/p voltage	Absolute max
USB Micro-B connector ( <b>J8</b> , <b>J10</b> )	4.5 V to 5.5 V	5.5 V
VCC_5V connector ( <b>J17</b> )	4.5 V to 5.5 V	6 V
Program and Debug header ( <b>J14</b> )	1.8 V to 3.3 V	3.6 V

There is no overvoltage protection on this Kit.

3. Why is the voltage of the board restricted to 3.3 V? Can't it drive external 5 V interfaces?  
 PSoC 6 MCU is not meant to be powered at more than 3.6 V. Powering PSoC 6 MCU at more than 3.3 V may damage the chip. You cannot drive the IO system with > 3.3 V supply voltages.
4. I am unable to program the target device.
  - a. Check **J3** to ensure it is connected.
  - b. Make sure that no external devices are connected from **J1.32** to **J1.36**.
  - c. Update your KitProg3 firmware to v1.01 or later using the steps mentioned in the KitProg3 User Guide.
  - d. Ensure that target device used in the ModusToolbox application is CY8C624ABZI-D44.
5. Does the board get powered when I power it from another Cypress Kit through the **J17** header?  
 Yes, VCC\_5V pin on **J17** header is a supply input/output pin and can take up to 5.5 V.
6. What additional overlays can be used with the CapSense?  
 Any kind of overlays (up to 5 mm thickness) like wood, acrylic, and glass can be used with CapSense. Note that additional tuning may be required when the overlay is changed.

7. What is Pmod?

Pmod interface or Peripheral Module interface is an open standard defined by Digilent Inc. in the Digilent Pmod Interface Specification for peripherals used with FPGAs or microcontrollers. Several types of modules are available from simple push buttons to more complex modules with network interfaces, analog to digital converters or LCD displays. PMOD peripheral modules are available from multiple vendors such as Diligent, Maxim Integrated, and Analog Devices. This Kit supports 1x6 pin Pmod SPI modules and 2x6 pin Pmod I2S2 modules.

8. Can I use this Kit as a programmer to program external PSoC devices?

Yes, the onboard KitProg3 can program any PSoC 4/5/6 devices connected to header **J4**. This is possible only after breaking away the KitProg3 section. Connecting two or more target devices will cause programming to fail.

9. Which third-party debuggers does this Kit support?

Multiple third-party IDEs are supported; IAR is one example. For more details on all supported devices and procedures to export to these IDEs, see the ModusToolbox 'Help' menu.

# Revision History



## Document Revision History

Document Title: CY8CPROTO-062-4343W PSoC 6 Wi-Fi BT Prototyping Kit Guide			
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Revision	ECN Number	Issue Date	Description of Change
**	6326228	11/12/2018	New kit guide.
*A	6670218	09/09/2019	Updated "Title" in <b>File &gt; Properties</b> . Updated to new template. Completing Sunset Review.