Click here for production status of specific part numbers.

MAX17250

2.7V to 18V Input, Boost Converter with 0.1µA True Shutdown, Short-Circuit Protection and Selectable Input Current Limit

General Description

The MAX17250 DC-DC boost converter is a high-efficiency, low quiescent current, synchronous boost (step-up) converter with True Shutdown™, programmable input current limit, and short-circuit protection. The MAX17250 has a wide input voltage range of 2.7V to 18V and generates an output voltage of 3V to 18V. The MAX17250 has a maximum on-time of 800ns and implements three modes of operation. The first mode of operation is a soft-start mode at power-up. The second mode of operation is normal operation and utilizes a fixed on-time/minimum off-time Pulse Frequency Modulation (PFM) architecture that uses only 60µA (typ) quiescent current due to the converter switching only when needed. The last mode is True Shutdown, where the output is completely disconnected from the input, and the battery drain is minimized to 0.1µA (typ) shutdown current. The MAX17250 is available in a compact, 12-bump, 1.72mm x 1.49mm WLP or a 14-pin, 3mm x 3mm TDFN package.

Applications

- Digital Cameras
- Battery Powered Internet of Things (IoT) Device
- 1 or 2 Cell Li-ion Battery Applications
- Display Supply
- Buzzer/Alarm Driver

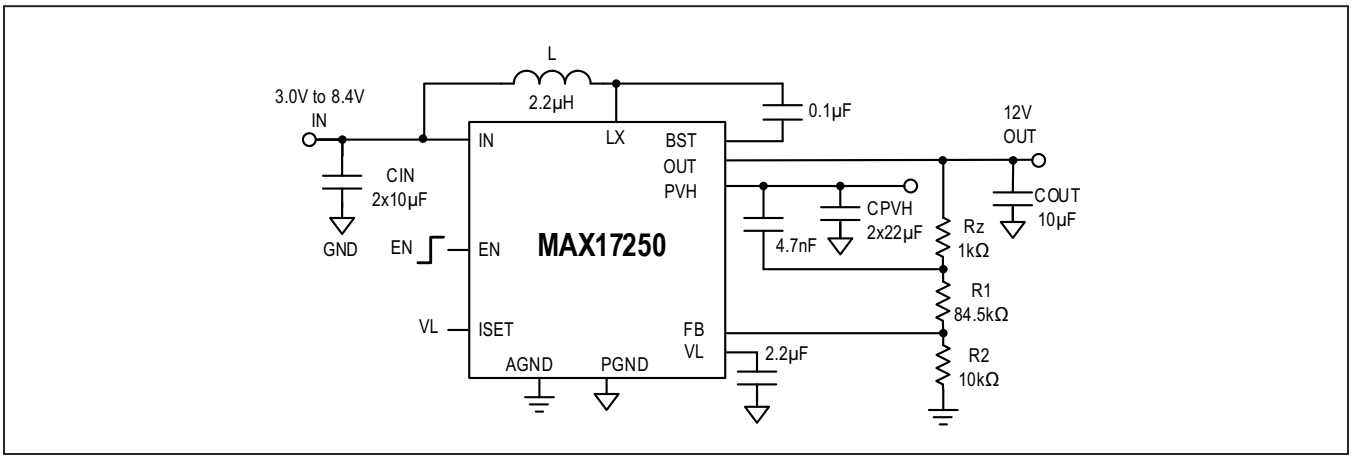
True Shutdown is a trademark of Maxim Integrated Products.

Benefits and Features

- Input Voltage Range 2.7V to 18V
  - 1 or 2 Cell Li-ion Batteries
- Output Voltage Range 3V to 18V, > V_{IN}
- Integrated Power FETs
- Selectable Input Peak Current Limit (ISET)
  - 3.5A, 2.7A, or 1.85A
- 93% Efficiency
- Low Power
  - 0.1µA True Shutdown Current
  - 60µA Quiescent Current
- Protection
  - True Shutdown Prevents Current Flowing Between Input and Output
  - Soft-Start Inrush Protection
  - Short-Circuit Protection
  - Overtemperature Protection
  - -40°C to +125°C Operation

Ordering Information *appears at end of data sheet.*

Typical Application Circuit



Absolute Maximum Ratings

IN, LX, OUT, PVH to AGND.....-0.3V to +22V
BST to LX.....-0.3V to +6V
EN, ISET, FB, VL to AGND.....-0.3V to +6V
PGND to AGND.....-0.3V to +0.3V
WLP LX RMS Current.....-3.2A_{RMS} to +3.2A_{RMS}
TDFN LX RMS Current.....-2.58A_{RMS} to +2.58A_{RMS}
Short-Circuit Between OUT and GND.....Continuous
WLP Continuous Power Dissipation
(T_A = +70°C, derate 13.7mW/°C above +70°C.).....1096mW
TDFN Continuous Power Dissipation
(T_A = +70°C, derate 24.4mW/°C above +70°C.).....1951.2mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10 seconds).....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

14-TDFN

Package Code	T1433+2C
Outline Number	**21-0137**
Land Pattern Number	**90-0063**
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	54°C/W
Junction to Case (θ_{JC})	8°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	41°C/W
Junction to Case (θ_{JC})	8°C/W

12-WLP

Package Code	N121B1+1
Outline Number	**21-100158**
Land Pattern Number	Refer to **Application Note 1891**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	72.82°C/W
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = 7.2V, V_{PVH} = V_{OUT} = 10V, V_{EN} = 5V, T_A = -40°C to +125°C, typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			2.7		18	V
Quiescent Supply Current	I_Q	Not switching, 105% of V_{OUT_TARGET},	T_A = 25°C		60	80	µA
			T_A = -40°C to 125°C			95	
Shutdown Current	I_{SD}	V_{EN} = V_{OUT} = 0V, V_{PVH} = 7.2V	T_A = 25°C		<0.001	1	µA
Output Voltage Range	V_{OUT}	V_{IN} < V_{OUT_TARGET}		3		18	V
FB Accuracy	ACC	V_{FB} falling, when LX starts switching		1.235	1.25	1.265	V
Input Undervoltage Threshold	V_{UVLO}	Rising, hysteresis typical 100mV			2.6	2.68	V
Inductor Peak Current Limit	I_{PEAK}	ISET = Open (Note 2)		1.48	1.85	2.31	A
		ISET = AGND (Note 2)		2.16	2.7	3.45	
		ISET = VL (Note 2)		2.8	3.5	4.55	
LX Switch Maximum On-Time	t_{ON}	V_{FB} = 1.2V, I_{OUT} = 0A		640	800	960	ns
LX Switch Minimum Off-Time	t_{OFF}	V_{FB} = 1.2V		160	200	260	ns
Startup Slew Rate	t_{ST_SR}	Using *Typical Application Circuit*			9		V/ms
LX Leakage Current	I_{LX_LEAK}	V_{LX} = V_{PVH} = 18V, V_{EN} = V_{OUT} = 0V, T_A = 25°C			9	1000	nA
		V_{LX} = V_{PVH} = 18V, V_{EN} = V_{OUT} = 0V, T_A = 125°C			570		
Output Short-Circuit Current Limit	I_{OUT_SHORT}	V_{IN} = V_{PVH} = 5V		2.6	3.4	4.25	A
N-Channel On-Resistance	$R_{DS(ON)}$	ISET = OPEN			175	380	mΩ
		ISET = AGND			120	260	
		ISET = V_L			95	200	
Load Switch-On Resistance	$R_{DS(ON)}$	V_{IN} = V_{PVH} = 5V			250	520	mΩ
Synchronous Rectifier Zero Crossing	I_{ZX}	ISET = OPEN (Note 2)			90		mA
		ISET = AGND (Note 2)			130		
		ISET = V_L (Note 2)			170		
Synchronous Rectifier Valley Current Crossing	I_{VX}	ISET = OPEN (Note 2)			1.2		A
		ISET = AGND (Note 2)			1.7		
		ISET = V_L (Note 2)			2.3		
Enable Voltage Threshold	V_{IL}	V_{IN} = 2.7V to 18V				0.4	V
	V_{IH}	V_{IN} = 2.7V to 18V		1.5V			

Electrical Characteristics (continued)

(V_{IN} = 7.2V, V_{PVH} = V_{OUT} = 10V, V_{EN} = 5V, T_A = -40°C to +125°C, typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Enable Input Leakage	I_{EN_LK}	0V ≤ V_{EN} ≤ 5.5V, T_A = 25°C, V_{EN} = 0V, V_{IN} = V_{LX} = V_{PVH} = V_{BST} = 7.2V, V_{OUT} = V_{FB} = 0V, V_{EN} = 5.5V, V_{IN} = V_{LX} = 7.2V, V_{PVH} = V_{BST} = V_{OUT} = 10V, V_{FB} = 1.3V		-1	+0.45	+1	µA
		0V ≤ V_{EN} ≤ 5.5V, T_A = 125°C, V_{EN} = 0V, V_{IN} = V_{LX} = V_{PVH} = V_{BST} = 7.2V, V_{OUT} = V_{FB} = 0V, V_{EN} = 5.5V, V_{IN} = V_{LX} = 7.2V, V_{PVH} = V_{BST} = V_{OUT} = 10V, V_{FB} = 1.3V			0.65		
FB Leakage	I_{FB_LK}	V_{FB} = 1.25V,	T_A = 25°C	-100	+10	+100	nA
			T_A = 125°C		60		
ISET Input Leakage	I_{SET_LK}	0V ≤ V_{ISET} ≤ V_L, T_A = 25°C		-1	+0.0005	+1	µA
		0V ≤ V_{ISET} ≤ V_L, T_A = 125°C			0.001		
ISET Maximum Tie-High (to V_L)/Tie-Low (to GND) Resistance					200		Ω
VL Voltage	VL	No load		3.29	3.38	3.47	V
BST Leakage	I_{BST_LK}	V_{BST} = V_{PVH} = 18V, V_{EN} = 0V, T_A = 25°C		-1	< +0.001	+1	µA
		V_{BST} = V_{PVH} = 18V, V_{EN} = 0V, T_A = 125°C			0.02		
OUT Leakage	I_{OUT_LK}	V_{PVH} = 18V, V_{EN} = V_{OUT} = 0V, T_A = 25°C		-1	+0.002	+1	µA
		V_{PVH} = 18V, V_{EN} = V_{OUT} = 0V, T_A = 125°C			0.25		
PVH Leakage	I_{PVH_LK}	V_{PVH} = 18V, V_{EN} = V_{LX} = VOUT = 0V, T_A = 25°C		-1	+0.015	+1	µA
		V_{PVH} = 18V, V_{EN} = V_{LX} = VOUT = 0V, T_A = 125°C			0.5		
Overtemperature Lockout Threshold		T_J rising, 15°C typical hysteresis			165		°C
VL_UVLO Voltage	VL_UVLO	Rising		2.03	2.185	2.34	V
		Falling		2	2.145	2.3	

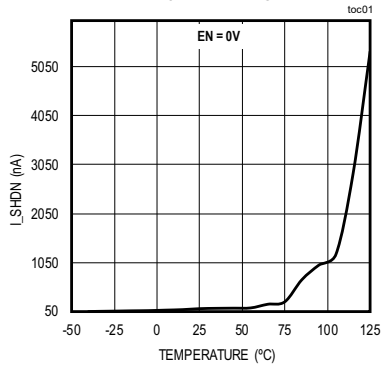
Note 1: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control (SQC) methods.

Note 2: This is a static measurement. The actual dynamic threshold depends upon V_{IN}, V_{OUT} and the inductor due to propagation delays.

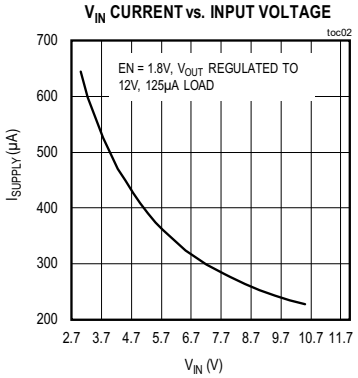
Typical Operating Characteristics

(MAX17250ANC+, V_{IN} = 7.2V, V_{OUT} = 12V, C_{IN} = 2 x 10µF, C_{OUT} = 10µF, C_{PVH} = 2 x 22µF, C_{VL} = 2.2µF, T_A = 25°C, unless otherwise noted.)

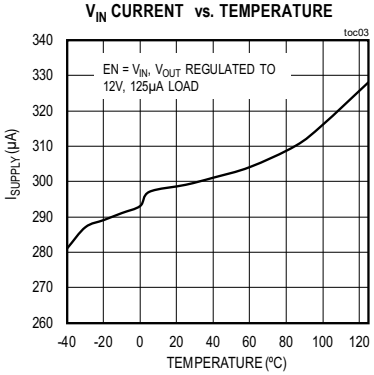
TOTAL SYSTEM SHUTDOWN CURRENT vs. TEMPERATURE



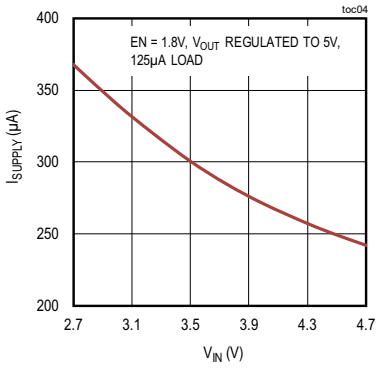
V_{IN} CURRENT vs. INPUT VOLTAGE



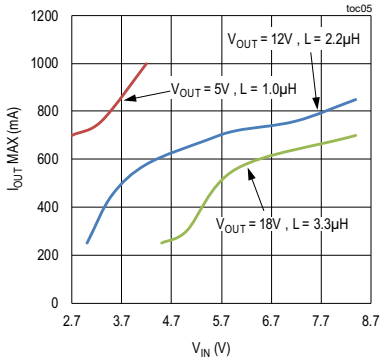
V_{IN} CURRENT vs. TEMPERATURE



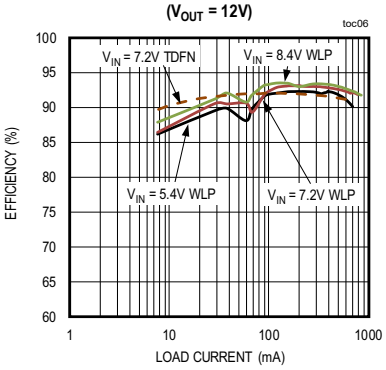
V_{IN} CURRENT vs. INPUT VOLTAGE



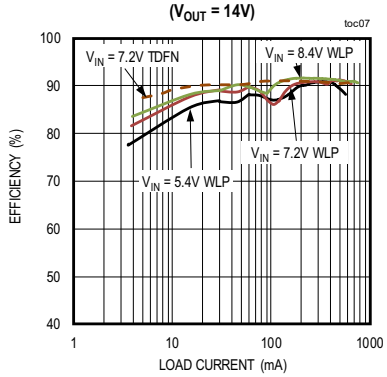
MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



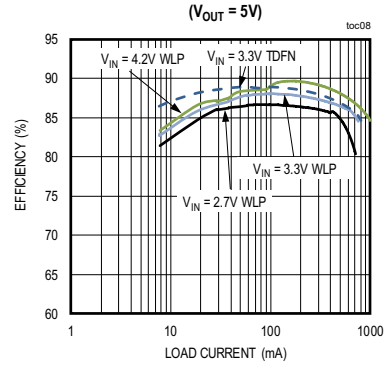
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 12V)



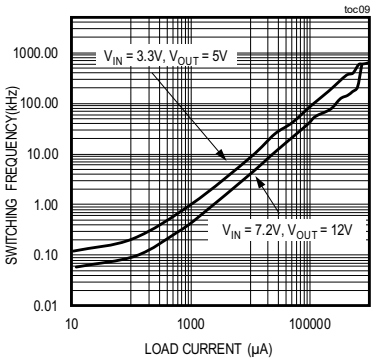
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 14V)



EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 5V)



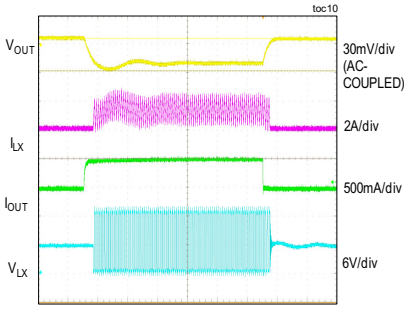
SWITCHING FREQUENCY vs. LOAD CURRENT



Typical Operating Characteristics (continued)

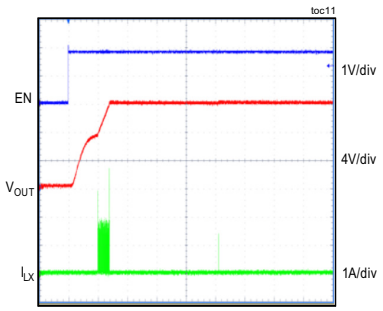
(MAX17250ANC+, V_{IN} = 7.2V, V_{OUT} = 12V, C_{IN} = 2 x 10µF, C_{OUT} = 10µF, C_{PVH} = 2 x 22µF, C_{VL} = 2.2µF, T_A = 25°C, unless otherwise noted.)

LOAD TRANSIENT



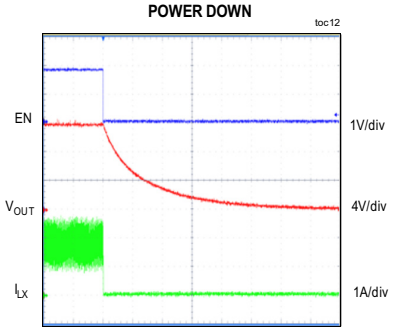
V_{IN} = 7.2V, V_{OUT} = 12V, I_{OUT} = 0 TO 500mA

STARTUP



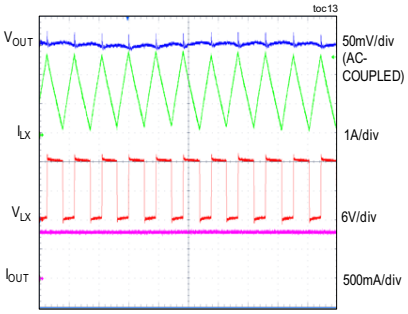
V_{IN} = 5.4V, V_{OUT} = 12V, I_{OUT} = 0A

POWER DOWN



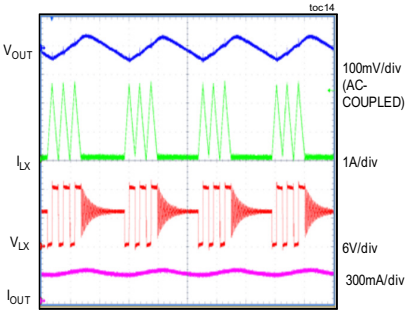
V_{IN} = 7.2V, V_{OUT} = 12V, I_{OUT} = 0A

HEAVY LOAD SWITCHING WAVEFORM



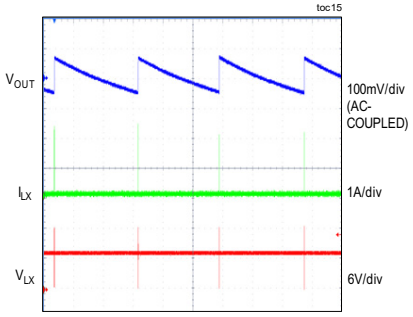
V_{IN} = 7.2V, V_{OUT} = 12V, I_{OUT} = 0.76A

MEDIUM LOAD SWITCHING WAVEFORM



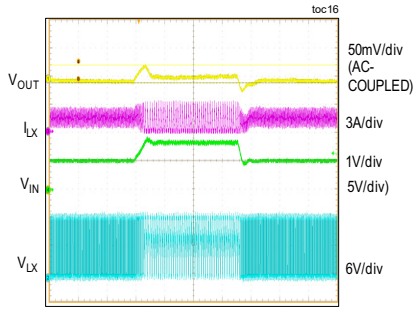
V_{IN} = 7.2V, V_{OUT} = 12V, I_{OUT} = 300mA

NO LOAD SWITCHING WAVEFORM



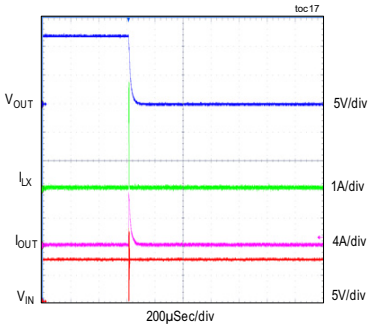
V_{IN} = 7.2V, V_{OUT} = 12V, I_{OUT} = 0A

LINE TRANSIENT



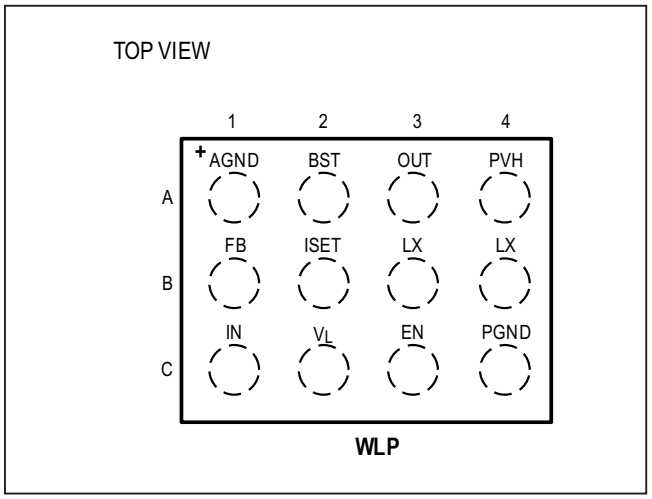
V_{IN} = 5.4V TO 8.4V, V_{OUT} = 12V, I_{OUT} = 680mA

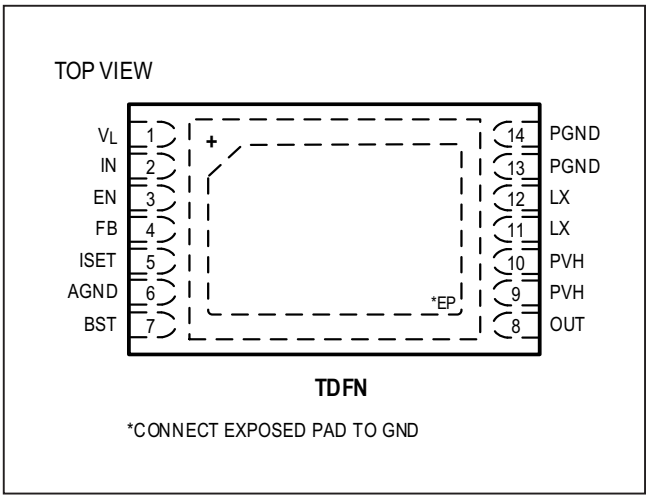
SHORT AT OUTPUT



V_{IN} = 7.2V, V_{OUT} = 12V, I_{OUT} = SHORT to GND

Pin Configurations



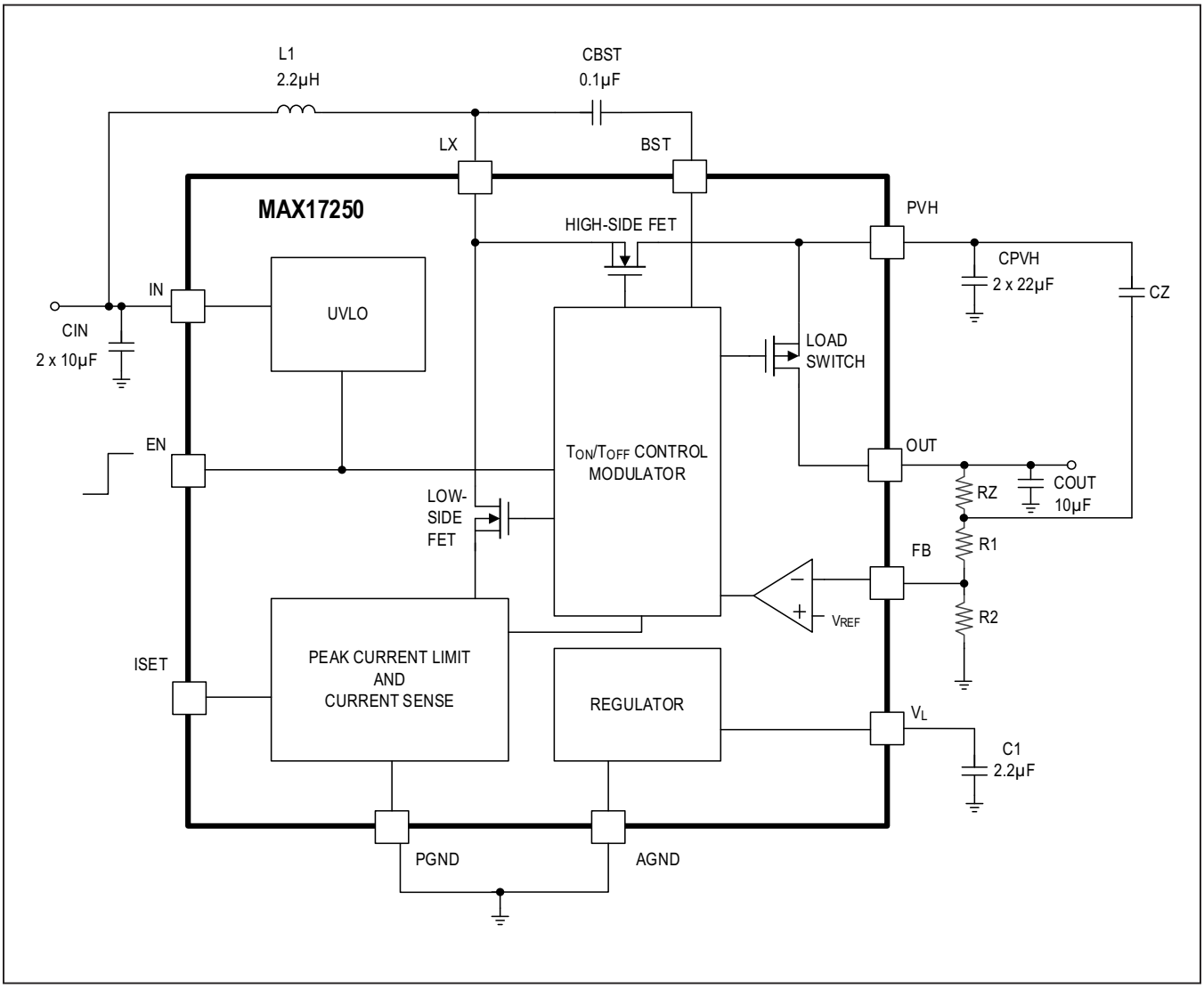


Pin Description

PIN		NAME	FUNCTION
WLP	TDFN		
A1	6	AGND	Analog Ground.
A2	7	BST	Boost Flying Capacitor Connection. Connect a 0.1µF cap from BST to LX.
A3	8	OUT	Output. Connect, at least, a 10µF capacitor from OUT to PGND.
A4	9, 10	PVH	Load Switch Gate Driver Supply. Connect two 22µF capacitors to PGND.
B1	4	FB	Feedback. Connect to the center point of a resistor-divider from OUT to AGND to set the target output voltage.
B2	5	ISET	Inductor Peak Current Limit Select. Set the inductor peak current limit by connecting this pin to either V_L (I_{PEAK} = 3.5A), AGND (I_{PEAK} = 2.7A) or leave unconnected (I_{PEAK} = 1.85A).
B3, B4	11, 12	LX	Inductor Switching Node.
C1	2	IN	Input Voltage Pin for the Device. Apply a voltage from 2.7V to 18V. Connect two 10µF ceramic capacitors to PGND. Additional capacitance may be needed for input voltages close to 2.7V to prevent disabling the part by input voltage spikes which result in $V_{IN} < V_{UVLO}$.
C2	1	V_L	Internal Supply. Connect at least a 2.2µF capacitor to AGND.
C3	3	EN	Active-High Enable Input. Drive with a logic-high to enable the device and drive low to put the device in True Shutdown mode. This pin should not be driven directly by IN, if IN is greater than 5.5V.
C4	13, 14, EP	PGND	Power Ground.

Functional Diagram

Boost Converter with Short-Circuit Protection and Programmable Input Current Limit



Detailed Description

The MAX17250 compact, high-efficiency, step-up DC-DC converters have low quiescent current and are guaranteed to operate with input voltages ranging from 2.7V to 18V. True Shutdown disconnects the input from the output, eliminating the need for external load switches. Switching frequencies up to 1MHz are supported. Tiny package options, short-circuit protection, 18V operation, 800ns fixed on time, and the three current-limit options allow the user to minimize the total solution size.

The MAX17250 utilizes a fixed on-time, current-limited, pulse-frequency-modulation (PFM) control scheme that allows low quiescent current and high efficiency over a wide output current range. The inductor current is limited by the 1.85A/2.7A/3.5A low-side FET current limit or by the 800ns switch maximum on-time. When the error comparator senses that the feedback signal has fallen below the regulation threshold, the low-side FET is turned on. This is the beginning of a switching cycle and the inductor current starts ramping up from the input source. Once the on-time elapses or the maximum current limit is reached the low-side FET turns off, the high-side FET turns on and the inductor current starts discharging to the output. The high-side FET turns off when the inductor current reaches zero or if the feedback signal falls below the regulation threshold after the minimum off time (200ns) has elapsed. The MAX17250 PFM control scheme allows for both continuous conduction mode (CCM) or discontinuous conduction mode (DCM) operation.

The switching frequency in CCM can be calculated by the equation below.

$$fsw = \left[\frac{1}{t_{ON} + t_{OFF}}\right] = \frac{1}{t_{ON}} \left[\frac{V_{OUT} - V_{IN}}{[V_{OUT}]}\right]$$

For example, with an input voltage of 7.2V and an output voltage of 12V, the switching frequency in CCM can be calculated as:

$$f_{SW} = 1/800ns \times (12 - 7.2)V/12V = 500kHz$$

In DCM, the switching frequency varies with load current.

If the input voltage (V_{IN}) is greater than the output voltage (V_{OUT}) by a diode drop (V_{DIODE} varies from ~0.2V at light load to ~0.7V at heavy load), the output voltage is clamped to a diode drop below the input voltage (i.e., $V_{OUT} = V_{IN} - V_{DIODE}$).

MAX17250 provides over temperature and output short-circuit protection. Should junction temperature be raised to undesired levels, the device will stop switching and will monitor temperature as it starts to decline. Once temperature has fallen to manageable levels, switching will resume. The output voltage short-circuit protection will cause the device to stop switching once an output short-circuit condition is detected upon which the output will be permanently latched off. The device will have to be reset either by power cycling or using enable signal to resume regulation.

Design Procedure

Feedback Resistor Divider Selection for Output Voltage

The output voltage of the MAX17250 is set through the resistor divider (R1, Rz, and R2) from VOUT to AGND, as shown in the *Typical Application Circuit*. The bottom resistor (R2) is recommended to be 10.0kΩ. This recommendation is to minimize noise levels at the feedback pin, which is relevant in continuous conduction mode of operation. In applications where lower output power is required and the device operates in discontinuous conduction mode of operation, larger divider impedance can be used to minimize current consumption. The top resistor (R1 + Rz) is calculated by the equation below, where 1.25V represents the internal reference voltage. Recommended Rz value is 1kΩ. Because resistor tolerance will have direct effect on V_{OUT} accuracy, these resistors should have 1% accuracy or better.

$$R1 + Rz = R2 \times (V_{OUT}/1.25 - 1)$$

Note: Recommended Cz values are: 10nF for output voltages up to 10V, 4.7nF for output voltages greater than 10V.

Inductor and Peak Current Limit Selection

Inductor value depends on the output voltage setting. For proper inductance selection, refer to Table 1.

Table 1. Inductance Selection

OUTPUT VOLTAGE RANGE	L (µH)
14V to 18V	3.3
8V to 14V	2.2
5V to 8V	1.5
3V to 5V	1.0

The MAX17250 has a three-state ISET input pin used to select the inductor peak current limit (I_{PEAK}), as shown in the Table 2. ISET value is read when VL crosses its UVLO threshold during power-up, or when EN transitions low-to-high. (See VL UVLO in the *Electrical Characteristics* table).

The inductor peak current limit setting should be determined as follows:

Calculate the inductor ripple current (ΔI) using the equation below.

$$\Delta I = \frac{V_{IN\_MIN} \times t_{ON}}{L}$$

where V_{IN_MIN} is the minimum input voltage, t_{ON} is the 800ns on time.

Calculate the maximum input current (I_{INPEAK}) using the equation below.

$$I_{INPEAK} = \frac{V_{OUT} \times I_{OUT}}{V_{INMIN} \times \eta} + \frac{\Delta I}{2}$$

where V_{OUT} is the output voltage, I_{OUT} is the maximum load current, V_{IN_MIN} is the minimum input voltage and η is the conversion efficiency.

If the calculated value of I_{INPEAK} is lower than 1.3A use the ISET = Open setting for I_{PEAK} (1.85A, typical).

If the calculated value of I_{INPEAK} is between 1.3A and 2A, use the ISET = AGND setting for I_{PEAK} (2.7A, typical).

If the calculated value of I_{INPEAK} is between 2A and 2.7A, use the ISET = VL setting for I_{PEAK} (3.5A, typical).

For example, if the minimum input voltage is 6V, the output voltage is 12V, and the output current is 500mA, assuming the conversion efficiency is 92%,

$$\Delta I = (V_{IN} \times t_{ON})/L = (6V \times 800ns)/(2.2\mu H) = 2.2A$$

$$I_{INPEAK} = (V_{OUT} \times I_{OUT})/(V_{IN} \times \eta) + \Delta I/2 = (12V \times 500mA)/(6V \times 0.92) + 2.2A/2 = 2.2A$$

So, the ISET = VL setting for I_{PEAK} (3.5A, typical) should be chosen.

Capacitor Selection

Input capacitors reduce current peaks from the battery and increase efficiency. For the input capacitor, choose a ceramic capacitor because they have the lowest equivalent series resistance (ESR), smallest size, and lowest cost. Choose an acceptable dielectric, such as X5R or X7R. Other capacitor types can be used as well but will have larger ESRs. Due to ceramic capacitors' capacitance drop with DC bias, two standard 10µF ceramic capacitors are recommended at the input for most applications. The minimum recommended effective capacitance at the input is 10µF for most applications. For lower input voltage applications, the input capacitor value can be reduced. However, additional capacitance may be needed for input voltages close to 2.7V to prevent disabling the part by input voltage ripple which results in $V_{IN} < V_{UVLO}$.

For output and PVH capacitors refer to Table 3 for proper selection.

The output ripple on the MAX17250 is small because the ripple at PVH pin gets further filtered and attenuated by the on-resistance of the load switch and the capacitance at OUT.

Table 2. Inductor I_{PEAK} Selection Table

ISET	I_{PEAK} (A)
VL	3.5
AGND	2.7
OPEN	1.85

Table 3. OUT and PVH Capacitor Selection

OUTPUT VOLTAGE RANGE	C_{PVH} (µF)	C_{OUT} (µF)
12V to 18V	3 x 22µF/25V/X7R	10µF/25V/X7R
8V to 12V	2 x 22µF/25V/X7R	10µF/25V/X7R
3V to 8V	2 x 22µF/16V/X5R	10µF/16V/X5R

Duty Cycle Limitation

Maximum duty ratio MAX17250 can provide is 78%. Whether specific application meets this reqirement can be checked using the following formula

$$D = (1 - ((V_{IN\ MIN} \times \eta))/V_{OUT}) < 78\%$$

Where,

D is duty cycle.
$V_{IN\ MIN}$ is minimum input voltage.
V_{OUT} is output voltage.
η is efficiency.

Output Current Limitation

The output current will be limited by the input peak current limit selection for a specific application. The output current expressed as a function of the Peak Input Current is shown below:

$$I_{OUT\ MAX} = ((I_{PEAK} - \Delta I/2) \times (V_{IN} \times \eta))/V_{OUT}$$

For example, for $7.2V_{IN}$, $12V_{OUT}$ application with efficiency of 92% maximum output current recommended is 0.76A which will allow 30% margin to the peak input current limit set to 3.5A.

$$I_{PEAK\ MAX} = I_{LIMIT}/1.3 = 3.5A/1.3 = 2.7A$$

$$\Delta I = (V_{IN}\ t_{ON})/L = (7.2V \times 800ns)/(2.2\mu H) = 2.62A$$

$$I_{OUT\ MAX} = ((I_{PEAK} - \Delta I/2) \times (V_{IN} \times \eta)) / V_{OUT} = 0.76A$$

In addition, the output current is a function of the device package and PCB thermal performance. The maximum junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable power dissipation and keep the actual power dissipation less than or equal to that. The maximum power dissipation limit is determined using the following equation.

$$\text{Power Disipation Max (W)} = ((125°C - T_A°C))/(R_{\theta JA}\ (°C)/W)$$

where,

T_A is the maximum ambient temperature for the application.

RθJA is the junction-to-ambient thermal resistance given in the *Package Information* section.

So, for the same example as above, $7.2V_{IN}$, $12V_{OUT}$, I_{OUT} = 0.76A internal power dissipation will be 0.3W. This will cause the junction temperature to rise 22°C above ambient temperature using the WLP package.

The TDFN package would have smaller junction to ambient thermal resistance and therefore better thermal performance.

At low V_{IN} and high V_{OUT} applications, where the MAX17250 is approaching maximum duty cycle limitation, output current will be limited. Please refer to the *Typical Operating Characteristics* for reference.

Enabling MAX17250

The MAX17250 has a dedicated EN pin. This pin can be driven by a digital signal. It is recommended that the digital signal to enable the device after V_{IN} crosses the UVLO threshold.

In applications where the EN pin is not driven, it can be pulled high to V_{IN}. If V_{IN} range is below 5.5V, EN can be connected directly to V_{IN}. If V_{IN} is above, resistor divider needs to be used. The divider should be designed that EN pin voltage is well above its threshold at the instant device starts regulation. This will assure that sag appearing at V_{IN} due to enabled regulation will not cause EN being toggled. Fast transient at enable that makes device disable and re-enable can cause device not to power up properly, including misreading the peak input current limit setting. In some cases, a small value capacitor from the EN pin to GND can be used. For high input voltage applications, voltage at the EN pin must not exceed its rating.

PCB Layout Guidelines

Minimize trace lengths to reduce parasitic capacitance, inductance and resistance, and radiated noise. Keep the main power path from IN, LX, PVH, OUT, and PGND as tight and short as possible. Minimize the surface area used for LX since this is the noisiest node. The trace between the feedback resistor divider and the FB pin should be as short as possible and should be isolated from the noisy power path. VL decoupling capacitor must be as close to the pin as possible referenced to PGND pin. Refer to the EV kit layout for best practices.

The PCB layout is important for robust thermal design. The junction to ambient thermal resistance of the package greatly depends on the PCB type, layout, and pad connections. Using thick PCB copper and having the SW, PVH, VOUT, and PGND copper pours will enhance the thermal performance. The TDFN package would have smaller junction to ambient thermal resistance and, therefore, better thermal performance. It has a large thermal pad under the package which creates excellent thermal path to PCB. This pad is electrically connected to PGND. Its PCB pad should have multiple thermal vias connecting the pad to internal PGND plane. Thermal vias should either be capped or have small diameter to minimize solder wicking and voids.

Ordering Information

PART NUMBER	T_{ON}	TEMPERATURE RANGE	PIN-PACKAGE
MAX17250ANC+	800ns	-40°C to +125°C	12 WLP
MAX17250ATD+	800ns	-40°C to +125°C	14 TDFN

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/18	Initial release	—
1	9/18	Updated *Typical Application Circuit*, *Electrical Characteristics*, *Typical Operating Characsteristics*, and *Ordering Information*	1, 3, 5, 12
2	8/19	Updated *Typical Application Circuit, Detailed Description, Table 3,* and *Ordering Information*	1, 9–12

