FXLH1T45

Level Translator, 1-Bit Bidirectional

Configurable Voltage Supplies and Bushold Data Inputs

The FXLH1T45 is a single bit configurable dual−voltage supply translator designed for both uni−directional and bi−directional voltage translation between two logic levels. The device allows translation between voltages as high as 3.6 V to as low as 1.1 V. The A port tracks the V_{CCA} level, and the B port tracks the V_{CCB} level. This allows for bi−directional voltage translation over a variety of voltage levels: 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V.

The device remains in 3−STATE until both V_{CC}s reach active levels allowing either V_{CC} to be powered−up first. Internal power down control circuits place the device in 3−STATE if either V_{CC} is removed.

The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the device. The FXLH1T45 is designed so that the control pin ($T/\overline{R}$) is supplied by V_{CCA}.

Features

- Bi−directional Interface between any 2 Levels from 1.1 V to 3.6 V
- Fully Configurable: Inputs Track V_{CC} level
- Non−preferential Power−up Sequencing; either V_{CC} may be Powered−up First
- Outputs Remain in 3−STATE until Active V_{CC} Level is Reached
- Outputs Switch to 3−STATE if either V_{CC} is at GND
- Power Off Protection
- Bushold On Data Inputs Eliminates the Need for External Pull−up/Pull−down Resistors
- Control Input ($T/\overline{R}$) Levels are Referenced to V_{CCA} Voltage
- Packaged in the MicroPak 6 SIP6 (1.0 mm x 1.45 mm)
- ESD Protections Exceeds:
  - 4 kV HBM ESD (per JESD22−A114 & Mil Std 883e 3015.7)
  - 8 kV HBM I/O to GND ESD (per JESD22−A114 & Mil Std 883e 3015.7)
  - 1 kV CDM ESD (per ESD STM 5.3)
  - 200 V MM ESD (per JESD22−A115 & ESD STM5.2)

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SIP6 1.45x1.0
CASE 127EB

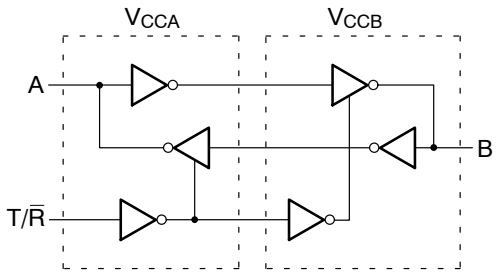
MARKING DIAGRAM

XD	= Device Code
KK	= Lot Code
XY	= Numeric Date Code
Z	= Assembly Plant Code

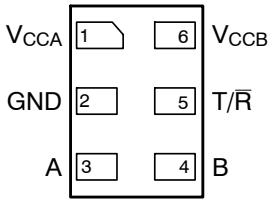
ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

FUNCTIONAL DIAGRAM



PINOUT



(Top Through View)

PIN ASSIGNMENT

Pin Number	Terminal Name
1	V_{CCA}
2	GND
3	A
4	B
5	T/$\overline{R}$
6	V_{CCB}

PIN DESCRIPTIONS

Pin Names	Description
T/$\overline{R}$	Transmit/Receive Input
A	Side A Input or Output
B	Side B Input or Output
V_{CCA}	Side A Power Supply
V_{CCB}	Side B Power Supply

FUNCTION TABLE

Inputs (T/$\overline{R}$)	Outputs
L	Bus B Data to Bus A
H	Bus A Data to Bus B

H = HIGH Logic Level L = LOW Logic Level

POWER−UP/POWER−DOWN SEQUENCING

FXL translators offer an advantage in that either V_{CC} may be powered up first. This benefit derives from the chip design. When either V_{CC} is at 0V, outputs are in a HIGH−Impedance state. To ensure that bus contention, excessive currents, or oscillations do not occur, a proper power−up sequence is recommended.

The recommended power−up sequence is the following:

1. Apply power to either V_{CC}
2. Apply power to the T/$\overline{R}$ input (Logic HIGH for A−to−B operation; Logic LOW for B−to−A operation) and to the respective data inputs (A Port or B Port). This may occur at the same time as Step 1
3. Apply power to other V_{CC}

The recommended power−down sequence is the following:

4. Remove power from either V_{CC}
5. Remove power from other V_{CC}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating
V_{CCA}, V_{CCB}	Supply Voltage	−0.5 V to +4.6 V
V_I	DC Input Voltage I/O Port A I/O Port B Control Input (T/$\overline{R}$)	 −0.5 V to +4.6 V −0.5 V to +4.6 V −0.5 V to +4.6 V
V_O	Output Voltage (Note 1) Outputs 3−STATE Outputs Active (A_n) Outputs Active (B_n)	 −0.5 V to +4.6 V −0.5 V to V_{CCA} + 0.5 V −0.5 V to V_{CCB} + 0.5 V
I_{IK}	DC Input Diode Current @ V_I < 0 V	−50 mA
I_{OK}	DC Output Diode Current @ V_O < 0 V V_O > V_{CC}	 −50 mA +50 mA
I_{OH} / I_{OL}	DC Output Source/Sink Current	−50 mA / +50 mA
I_{CC}	DC V_{CC} or Ground Current per Supply Pin	±100 mA
T_{STG}	Storage Temperature Range	−65°C to +150°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS (Note 2)

Symbol	Parameter	Rating
V_{CCA} or V_{CCB}	Power Supply Operating	1.1 V to 3.6 V
Vi	Input Voltage Port A Port B Control Input (T/$\overline{R}$)	 0.0 V to 3.6 V 0.0 V to 3.6 V 0.0 V to V_{CCA}
Vo	Output Current in I_{OH}/I_{OL} with V_{CC} @ 3.0 V to 3.6 V 2.3 V to 2.7 V 1.65 V to 1.95 V 1.4 V to 1.65 V 1.1 V to 1.4 V	 ±24 mA ±18 mA ±6 mA ±2 mA ±0.5 mA
T_A	Free Air Operating Temperature	−40°C to +125°C
$\Delta t/ \Delta V$	Maximum Input Edge Rate $V_{CCA/B}$ = 1.1 V to 3.6 V	10 ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

NOTES:

1. I_O Absolute Maximum Rating must be observed.
2. All unused inputs and I/O pins must be held at V_{CCI} or GND.

DC ELECTRICAL CHARACTERISTICS (T_A = −40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C)

Symbol	Parameter	Conditions	V_{CCI} (V)	V_{CCO} (V)	Min.	Typ.	Max.	Units
V_{IH}	High Level Input Voltage (Note 3)	Data Inputs A_n, B_n	2.7–3.6	1.1–3.6	2.0	–	–	V
			2.3–2.7		1.6	–	–	
			1.65–2.3		0.65 x V_{CCI}	–	–	
			1.4–1.65		0.65 x V_{CCI}	–	–	
			1.1–1.4		0.9 x V_{CCI}	–	–	
		Control Pin T/$\overline{R}$ (Referenced to V_{CCA})	2.7–3.6	1.1–3.6	2.0	–	–	
			2.3–2.7		1.6	–	–	
			1.65–2.3		0.65 x V_{CCA}	–	–	
			1.4–1.65		0.65 x V_{CCA}	–	–	
			1.1–1.4		0.9 x V_{CCA}	–	–	
V_{IL}	Low Level Input Voltage (Note 3)	Data Inputs A_n, B_n	2.7–3.6	1.1–3.6	–	–	0.8	V
			2.3–2.7		–	–	0.7	
			1.65–2.3		–	–	0.35 x V_{CCI}	
			1.4–1.65		–	–	0.35 x V_{CCI}	
			1.1–1.4		–	–	0.1 x V_{CCI}	
		Control Pin T/$\overline{R}$ (Referenced to V_{CCA})	2.7–3.6	1.1–3.6	–	–	0.8	
			2.3–2.7		–	–	0.7	
			1.65–2.3		–	–	0.35 x V_{CCA}	
			1.4–1.65		–	–	0.35 x V_{CCA}	
			1.1–1.4		–	–	0.1 x V_{CCA}	
V_{OH}	High Level Output Voltage (Note 4)	I_{OH} = –100 μA	1.1–3.6	1.1–3.6	V_{CCO}–0.2	–	–	V
		I_{OH} = –12 mA	2.7	2.7	2.2	–	–	
		I_{OH} = –18 mA	3.0	3.0	2.4	–	–	
		I_{OH} = –24 mA	3.0	3.0	2.2	–	–	
		I_{OH} = –6 mA	2.3	2.3	2.0	–	–	
		I_{OH} = –12 mA	2.3	2.3	1.8	–	–	
		I_{OH} = –18 mA	2.3	2.3	1.7	–	–	
		I_{OH} = –6 mA	1.65	1.65	1.25	–	–	
		I_{OH} = –2 mA	1.4	1.4	1.05	–	–	
		I_{OH} = –0.5 mA	1.1	1.1	0.75 x V_{CCO}	–	–	
V_{OL}	Low Level Output Voltage (Note 4)	I_{OL} = 100 μA	1.1–3.6	1.1–3.6	–	–	0.2	V
		I_{OL} = 12 mA	2.7	2.7	–	–	0.4	
		I_{OL} = 18 mA	3.0	3.0	–	–	0.4	
		I_{OL} = 24 mA	3.0	3.0	–	–	0.55	
		I_{OL} =12 mA	2.3	2.3	–	–	0.4	
		I_{OL} = 18 mA	2.3	2.3	–	–	0.6	
		I_{OL} = 6 mA	1.65	1.65	–	–	0.3	
		I_{OL} = 2 mA	1.4	1.4	–	–	0.35	
		I_{OL} = 0.5 mA	1.1	1.1	–	–	0.3 x V_{CCO}	
I_I	Input Leakage Current Control Pins	V_I = V_{CCA} or GND	1.1–3.6	3.6	–	–	±1.0	μA

DC ELECTRICAL CHARACTERISTICS (continued) (T_A = −40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C)

Symbol	Parameter	Conditions	V_{CCI} (V)	V_{CCO} (V)	Min.	Typ.	Max.	Units
$I_{I(HOLD)}$	Bushold Input Minimum Drive Current	V_{IN} = 0.8 V, T_A = −40°C to +85°C	3.0	3.0	75.0	–	–	μA
		V_{IN} = 0.8 V	3.0	3.0	60.0	–	–	
		V_{IN} = 2 V, T_A = −40°C to +85°C	3.0	3.0	−75.0	–	–	
		V_{IN} = 2 V	3.0	3.0	−60	–	–	
		V_{IN} = 0.7 V	2.3	2.3	45.0	–	–	
		V_{IN} = 1.6 V	2.3	2.3	−45.0	–	–	
		V_{IN} = 0.57 V	1.65	1.65	25.0	–	–	
		V_{IN} = 1.07 V	1.65	1.65	−25.0	–	–	
		V_{IN} = 0.49 V	1.4	1.4	10.0	–	–	
		V_{IN} = 0.91 V	1.4	1.4	−10.0	–	–	
		V_{IN} = 0.11 V	1.1	1.1	–	4.0	–	
		V_{IN} = 0.99 V	1.1	1.1	–	−4.0	–	
$I_{I(OD)}$	Bushold Input Over−Drive Current−to−Change State	(Note 5)	3.6	3.6	450	–	–	μA
		(Note 6)	3.6	3.6	−450	–	–	
		(Note 5)	2.7	2.7	300	–	–	
		(Note 6)	2.7	2.7	−300	–	–	
		(Note 5)	1.95	1.95	200	–	–	
		(Note 6)	1.95	1.95	−200	–	–	
		(Note 5)	1.6	1.6	120	–	–	
		(Note 6)	1.6	1.6	−120	–	–	
		(Note 5)	1.4	1.4	80.0	–	–	
		(Note 6)	1.4	1.4	−80.0	–	–	
I_{OFF}	Power Off Leakage Current	A_n, V_{CCA} = V_{CCI}, V_I = 0 V to 3.6 V	0	3.6	–	–	±10.0	μA
		B_n, V_{CCB} = V_{CCI}, V_I = 0 V to 3.6 V	0	3.6	–	–	±10.0	
I_{OZ}	3−STATE Output Leakage	A_n, V_{CCA} = V_{CCO}, V_O = 0 V or 3.6 V	0	3.6	–	–	±10.0	μA
		B_n, V_{CCB} = V_{CCO}, V_O = 0 V or 3.6 V	0	3.6	–	–	±10.0	
$I_{CCA/B}$	Quiescent Supply Current (Note 7)	V_I = V_{CCI} or GND; I_O = 0	1.1–3.6	1.1–3.6	–	–	20.0	μA
I_{CCA}	Quiescent Supply Current	V_I = V_{CCA} or GND; I_O = 0	0	1.1–3.6	–	–	−10.0	μA
		V_I = V_{CCA} or GND; I_O = 0	1.1–3.6	0	–	–	10.0	
I_{CCB}	Quiescent Supply Current	V_I = V_{CCB} or GND; I_O = 0	1.1–3.6	0	–	–	−10.0	μA
		V_I = V_{CCB} or GND; I_O = 0	0	1.1–3.6	–	–	10.0	
$\Delta I_{CCA/B}$	Increase in I_{CC} per Input; Other Inputs at V_{CC} or GND	V_{IH} = 3.0 V	3.6	3.6	–	–	500	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

3. V_{CCI} = the V_{CC} associated with the data input under test.
4. V_{CCO} = the V_{CC} associated with the output under test.
5. An external driver must source at least the specified current to switch LOW−to−HIGH.
6. An external driver must source at least the specified current to switch HIGH−to−LOW.
7. Reflects current per supply, V_{CCA} or V_{CCB}.

AC Electrical Characteristics (T_A = −40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

V_{CCA} = 3.0 V to 3.6 V

Symbol	Parameter	V_{CCB} = 3.0 V to 3.6 V		V_{CCB} = 2.3 V to 2.7 V		V_{CCB} = 1.65 V to 1.95 V		V_{CCB} = 1.4 V to 1.6 V		V_{CCB} = 1.1 V to 1.3 V		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.2	3.5	0.3	3.9	0.5	5.4	0.6	6.8	1.4	22.0	ns
	Propagation Delay B to A	0.2	3.5	0.2	3.8	0.3	4.0	0.5	4.3	0.8	13.0	
t_{PZH}, t_{PZL} (Note 8)	Output Enable T/$\overline{R}$ to B	0.4	7.2	0.5	7.6	0.7	9.1	0.8	10.5	1.6	25.7	ns
	Output Enable T/$\overline{R}$ to A	0.4	7.3	0.4	7.8	1.0	8.8	2.0	10.5	2.8	30.0	
t_{PHZ}, t_{PLZ}	Output Disable T/$\overline{R}$ to B	–	3.9	–	5.3	–	7.3	–	7.6	–	17.0	ns
	T_A = −40°C to +85°C	–	5.6	–	4.2	–	6.3	–	6.9	–	17.0	
	Output Disable T/$\overline{R}$ to A	–	4.9	–	5.8	–	3.7	–	5.7	–	3.7	
	T_A = −40°C to +85°C	–	4.6	–	4.8	–	4.5	–	4.9	–	4.5	

V_{CCA} = 2.3 V to 2.7 V

Symbol	Parameter	V_{CCB} = 3.0 V to 3.6 V		V_{CCB} = 2.3 V to 2.7 V		V_{CCB} = 1.65 V to 1.95 V		V_{CCB} = 1.4 V to 1.6 V		V_{CCB} = 1.1 V to 1.3 V		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.2	3.8	0.4	4.2	0.5	5.6	0.8	6.9	1.4	22.0	ns
	Propagation Delay B to A	0.3	3.9	0.4	4.2	0.5	4.5	0.5	4.8	1.0	7.0	
t_{PZH}, t_{PZL} (Note 8)	Output Enable T/$\overline{R}$ to B	0.4	7.8	0.6	8.2	0.7	9.6	1.0	10.9	1.6	26.0	ns
	Output Enable T/$\overline{R}$ to A	0.5	8.0	0.6	8.5	1.2	9.3	2.0	11.5	3.0	24.0	
t_{PHZ}, t_{PLZ}	Output Disable T/$\overline{R}$ to B	–	4.1	–	4.3	–	7.0	–	6.7	–	17.0	ns
	T_A = −40°C to +85°C	–	5.7	–	4.3	–	5.7	–	6.7	–	17.0	
	Output Disable T/$\overline{R}$ to A	–	5.3	–	5.9	–	4.0	–	6.0	–	5.9	
	T_A = −40°C to +85°C	–	4.8	–	4.8	–	4.8	–	5.0	–	4.8	

V_{CCA} = 1.65 V to 1.95 V

Symbol	Parameter	V_{CCB} = 3.0 V to 3.6 V		V_{CCB} = 2.3 V to 2.7 V		V_{CCB} = 1.65 V to 1.95 V		V_{CCB} = 1.4 V to 1.6 V		V_{CCB} = 1.1 V to 1.3 V		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.3	4.0	0.5	4.5	0.8	5.7	0.9	7.1	1.5	22.0	ns
	Propagation Delay B to A	0.5	5.4	0.5	5.6	0.8	5.7	1.0	6.0	1.2	8.0	
t_{PZH}, t_{PZL} (Note 8)	Output Enable T/$\overline{R}$ to B	0.8	9.0	1.0	9.5	1.3	10.7	1.4	12.1	2.0	27.0	ns
	Output Enable T/$\overline{R}$ to A	0.7	10.5	0.7	10.8	1.6	10.9	2.5	13.0	3.2	25.0	
t_{PHZ}, t_{PLZ}	Output Disable T/$\overline{R}$ to B	–	5.1	–	5.2	–	6.7	–	7.0	–	17.0	ns
	T_A = −40°C to +85°C	–	5.7	–	5.6	–	5.8	–	7.0	–	17.0	
	Output Disable T/$\overline{R}$ to A	–	5.0	–	6.5	–	5.0	–	5.0	–	5.0	
	T_A = −40°C to +85°C	–	5.0	–	5.0	–	5.0	–	5.0	–	5.0	

V_{CCA} = 1.4 V to 1.6 V

Symbol	Parameter	V_{CCB} = 3.0 V to 3.6 V		V_{CCB} = 2.3 V to 2.7 V		V_{CCB} = 1.65 V to 1.95 V		V_{CCB} = 1.4 V to 1.6 V		V_{CCB} = 1.1 V to 1.3 V		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.5	4.3	0.5	4.8	1.0	6.0	1.0	7.3	1.5	22.0	ns
	Propagation Delay B to A	0.6	6.8	0.8	6.9	0.9	7.1	1.0	7.3	1.3	9.5	
t_{PZH}, t_{PZL} (Note 8)	Output Enable T/$\overline{R}$ to B	1.5	10.3	1.5	10.8	2.0	12.0	2.0	13.3	2.5	28.0	ns
	Output Enable T/$\overline{R}$ to A	1.0	12.9	1.2	13.1	1.8	13.3	2.5	14.8	3.3	27.5	
t_{PHZ}, t_{PLZ}	Output Disable T/$\overline{R}$ to B	–	6.1	–	6.2	–	6.2	–	7.5	–	18.0	ns
	T_A = −40°C to +85°C	–	6.1	–	6.2	–	6.2	–	7.5	–	18.0	
	Output Disable T/$\overline{R}$ to A	–	8.0	–	7.5	–	6.0	–	6.0	–	6.0	
	T_A = −40°C to +85°C	–	6.5	–	6.3	–	6.0	–	6.0	–	6.0	

V_{CCA} = 1.1 V to 1.3 V

Symbol	Parameter	V_{CCB} = 3.0 V to 3.6 V		V_{CCB} = 2.3 V to 2.7 V		V_{CCB} = 1.65 V to 1.95 V		V_{CCB} = 1.4 V to 1.6 V		V_{CCB} = 1.1 V to 1.3 V		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.8	13.0	1.0	7.0	1.2	8.0	1.3	9.5	2.0	24.0	ns
	Propagation Delay B to A	1.4	22.0	1.4	22.0	1.5	22.0	1.5	22.0	2.0	24.0	
t_{PZH}, t_{PZL} (Note 8)	Output Enable T/$\overline{R}$ to B	2.8	28.0	3.0	19.0	3.2	20.0	3.3	21.5	4.0	36.0	ns
	Output Enable T/$\overline{R}$ to A	2.4	37.0	2.1	29.0	2.5	30.0	3.5	32.0	4.0	44.0	
t_{PHZ}, t_{PLZ}	Output Disable T/$\overline{R}$ to B	–	15.0	–	7.0	–	8.0	–	10.0	–	20.0	ns
	T_A = −40°C to +85°C	–	15.0	–	7.0	–	8.0	–	10.0	–	20.0	
	Output Disable T/$\overline{R}$ to A	–	15.0	–	12.0	–	12.0	–	12.0	–	12.0	
	T_A = −40°C to +85°C	–	15.0	–	12.0	–	12.0	–	12.0	–	12.0	

NOTES:

8. The enable time, t_{PZH} or t_{PZL}, is the time for the FXLH1T45 to return to active operation after a direction change. The enable time specifies the worst−case delay from the time the T/$\overline{R}$ pin is switched until a valid output signal is expected. For example, to change direction to B−to−A operation, the T/$\overline{R}$ pin is switched from HIGH−to−LOW. The enable time for this case is found by adding the disable time for T/$\overline{R}$ to B to the propagation delay for B to A. The formulas for calculating enable times are the following:
   t_{PZH} (T/$\overline{R}$ to A) = t_{PLZ} (T/$\overline{R}$ to B) + t_{PLH} (B to A)
   t_{PZL} (T/$\overline{R}$ to A) = t_{PHZ} (T/$\overline{R}$ to B) + t_{PHL} (B to A)
   t_{PZH} (T/$\overline{R}$ to B) = t_{PLZ} (T/$\overline{R}$ to A) + t_{PLH} (A to B)
   t_{PZL} (T/$\overline{R}$ to B) = t_{PHZ} (T/$\overline{R}$ to A) + t_{PHL} (A to B)

CAPACITANCE

Symbol	Parameter	Conditions	T_A = +25°C Typical	Units
C_{IN}	Input Capacitance Control Pin (T/$\overline{R}$)	V_{CCA} = V_{CCB} = 3.3 V, V_I = 0 V or $V_{CCA/B}$	4.0	pF
$C_{I/O}$	Input/Output Capacitance A_n, B_n Ports	V_{CCA} = V_{CCB} = 3.3 V, V_I = 0 V or $V_{CCA/B}$	5.0	pF
C_{PD}	Power Dissipation Capacitance	V_{CCA} = V_{CCB} = 3.3 V, V_I = 0 V or V_{CC}, F = 10 MHz	20.0	pF

AC Loading and Waveforms

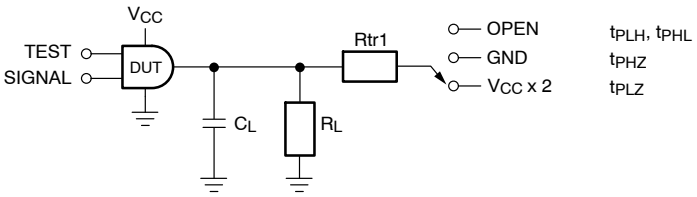


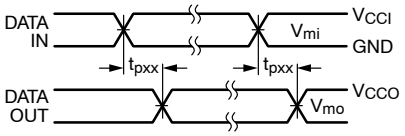
Figure 1. AC Test Circuit

AC TEST CIRCUIT

Test	Switch
t_{PLH}, t_{PHL}	OPEN
t_{PLZ}	V_{CCO} x 2 at V_{CCO} = 3.3 ±0.3 V, 2.5 V ±0.2 V, 1.8 V ±0.15 V, 1.5 V ±0.1 V, 1.2 V ±0.1 V
t_{PHZ}	GND

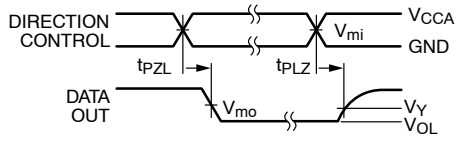
AC LOAD TABLE

V_{CCO}	C_L	R_L	Rtr1
1.2 V ±0.1 V	15 pF	2 kΩ	2 kΩ
1.5 V ±0.1 V	15 pF	2 kΩ	2 kΩ
1.8 V ±0.15 V	15 pF	2 kΩ	2 kΩ
2.5 V ±0.2 V	15 pF	2 kΩ	2 kΩ
3.3 V ±0.3 V	15 pF	2 kΩ	2 kΩ



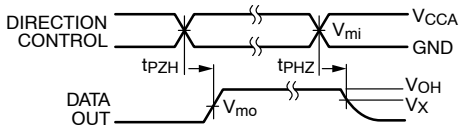
Input $t_R = t_F$ = 2.0 ns, 10% to 90%
Input $t_R = t_F$ = 2.5 ns, 10% to 90%, @ V_I = 3.0 V to 3.6 V only

Figure 2. Waveform for Inverting and Non−Inverting Functions



Input $t_R = t_F$ = 2.0 ns, 10% to 90%
Input $t_R = t_F$ = 2.5 ns, 10% to 90%, @ V_I = 3.0 V to 3.6 V only

Figure 3. 3−STATE Output Low Enable and Disable Times for Low Voltage Logic



Input $t_R = t_F$ = 2.0 ns, 10% to 90%
Input $t_R = t_F$ = 2.5 ns, 10% to 90%, @ V_I = 3.0 V to 3.6 V only

Figure 4. 3−STATE Output High Enable and Disable Times for Low Voltage Logic

Symbol	V_{CC}				
	3.3V ± 0.3V	2.5 V ± 0.2 V	1.8 V ± 0.15 V	1.5 V ± 0.1 V	1.2 V ± 0.1 V
V_{mi}	V_{CCI} / 2	V_{CCI} / 2	V_{CCI} / 2	V_{CCI} / 2	V_{CCI} / 2
V_{mo}	V_{CCO} / 2	V_{CCO} / 2	V_{CCO} / 2	V_{CCO} / 2	V_{CCO} / 2
V_X	V_{OH} − 0.3 V	V_{OH} − 0.15 V	V_{OH} − 0.15 V	V_{OH}− 0.1 V	V_{OH} − 0.1 V
V_Y	V_{OL} + 0.3 V	V_{OL} + 0.15 V	V_{OL} + 0.15 V	V_{OL}+ 0.1 V	V_{OL} + 0.1 V

9. For V_{mi}: $V_{CCI} = V_{CCA}$ for Control Pin T/$\overline{R}$ or V_{CCA} / 2.

ORDERING INFORMATION

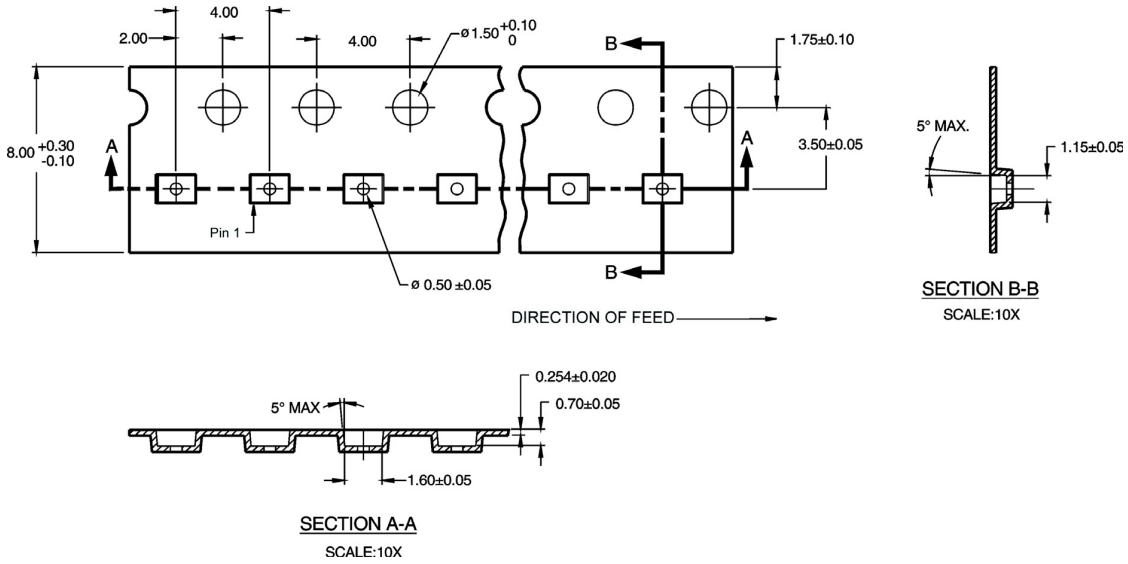
Order Number	Case Number	Pb−Free	Package Description	Supplied As
FXLH1T45L6X	127EB	Yes	6−Lead MicroPak/SIP6, 1.0 mm Wide	5k Units on Tape and Reel

Tape and Reel Specification

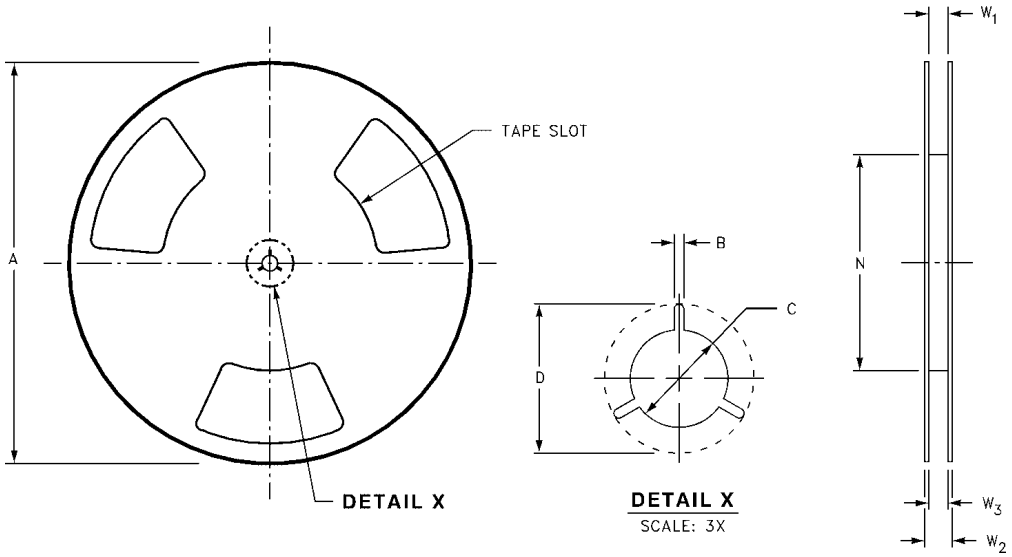
TAPE FORMAT FOR MICROPAK

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

Tape Dimensions Millimeters



Reel Dimensions Inches (Millimeters)



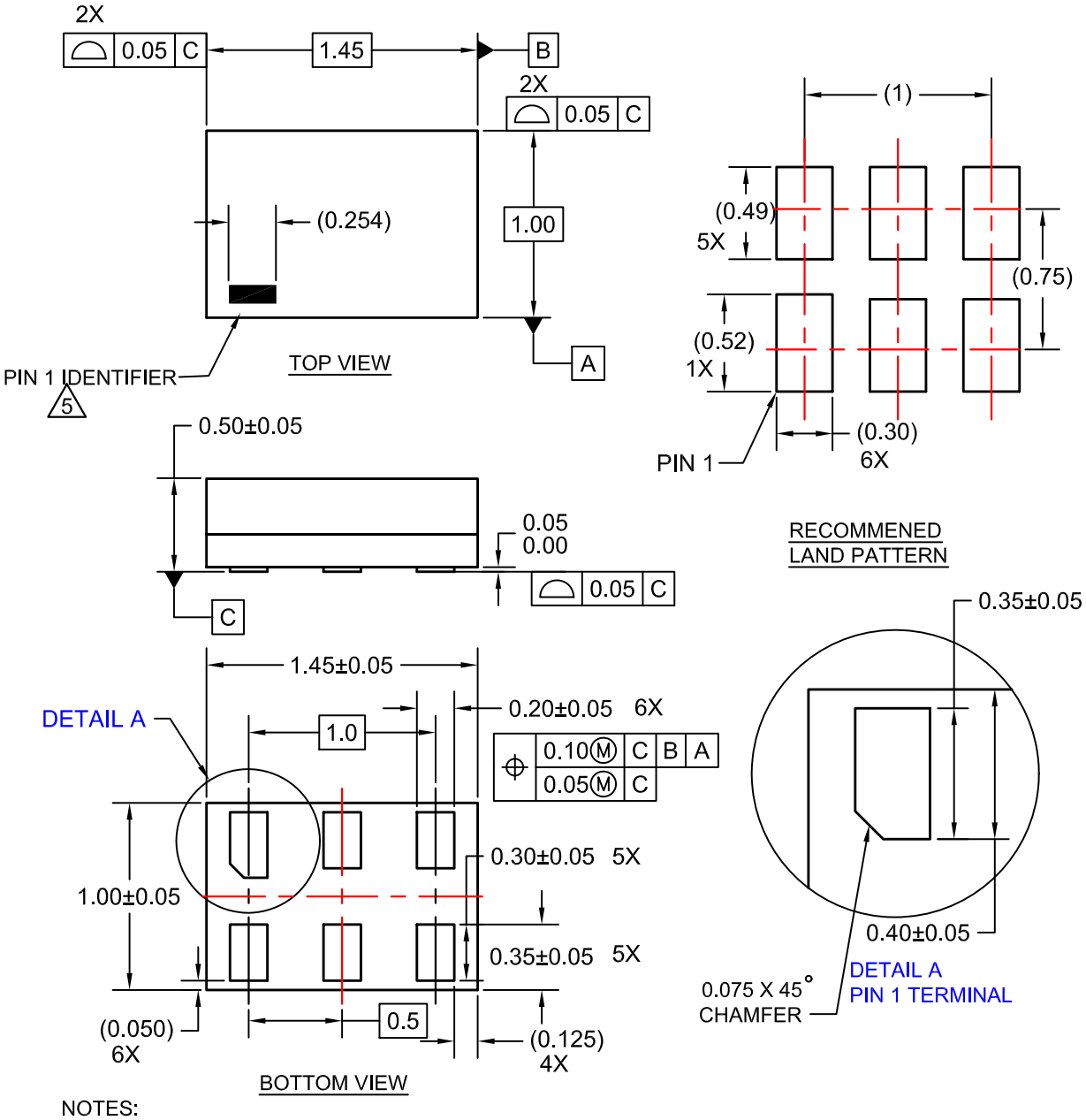
Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/−0.000 (8.40 + 1.50 /−0.00)	0.567 (14.40)	W1 + 0.078 /−0.039 (W1 + 2.00 /−1.00)

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SIP6 1.45X1.0
CASE 127EB
ISSUE O

DATE 31 AUG 2016



NOTES:

1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

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DESCRIPTION:	**SIP6 1.45X1.0**	**PAGE 1 OF 1**

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