

Mounting instructions for SMD (surface mounting device) packages

Introduction

The mounting instructions herein provide the main recommendations to appropriately handle, assemble and rework the surface mounting device packages. It is necessary to follow some basic assembly rules to limit thermal and mechanical stresses or ensure optimal thermal conduction and electrical insulation.

1 Package description

1.1 Package description 1.1

Surface mounting device packages (SMD packages): the gull-wing leads, soldering lands and heat slug or exposed die pads can be mounted on one side of a printed circuit board (PCB). Most commonly they are attached to the PCB by solder paste printing, pick&place and reflow soldering. The figure below shows examples of SMD packages.



Figure 1. Examples of SMD packages

1.2 Thermal resistance

Thermal resistance of a semiconductor characterizes the device's capability to dissipate the heat generated during operation. This parameter helps to calculate the junction temperature, taking into account the device environment (load current, ambient temperature, mounting conditions etc...). For SMD packages the thermal resistance between junction and ambient, called $R_{th(j-a)}$, depends on the copper surface used under the tab. The figure below shows curves giving the relation between $R_{th(j-a)}$ and the copper surface under the tab for an FR4 board - 35 µm copper thickness.

Figure 2. R_{th(j-a)} vs. copper surface under tabs (FR4 board - copper thickness = 35 μm) for several typical packages



1.3 Thermal impedance

When dealing with short duration pulses, the thermal impedance must be considered to calculate the junction temperature. Depending on the time scale, the following elements are thermally prevalent:

- t_p < 10 ms: die influence
- t_p < 0.1 s: package influence
- t_p < 10 s: PCB influence
- above 10 s: thermal exchange board-air (example: with / without forced cooling)



Figure 3. Typical $Z_{th(j-a)}$ for DPAK

2 Package handling

2.1 ESD protective measures

Semiconductors are normally electrostatic discharge sensitive (ESDS) devices requiring specific precautionary measures regarding handling and processing. Static discharges caused by human touch or by processing tools may cause high-current and/or high-voltage pulses, which may damage or even destroy sensitive semiconductor structures. On the other hand, integrated circuits (ICs) may also be charged by static during processing. Discharging which occurs too quickly (hard discharge) may also cause peak loads that can lead to damage. ESD protective measures must therefore prevent contact with charged parts as well as charging of the ICs. Protective measures against ESD include procedures for proper ESDS handling, processing and packing. A few handling and processing tips are provided below.

2.1.1 ESD protective measures in the workplace

- Standard marking of ESD-protected areas
- Access controls, with wrist strap and footwear testers
- Air conditioning
- Dissipative and grounded floor
- Dissipative and grounded working and storage areas
- Dissipative chairs
- Ground bonding point for wrist strap
- Trolleys with dissipative surfaces and wheels
- Suitable shipping and storage containers
- No sources of electrostatic fields

2.1.2 Personal equipment

- Dissipative/conductive footwear or heel straps
- · Suitable garments made of fabrics that do not generate excessive static electricity
- Wrist strap with safety resistor
- Volume conductive gloves or finger cots

2.1.3 Production installations and processing tools

- Machine and tool parts made of dissipative or metallic materials
- No materials having thin insulating layers for sliding tracks
- All parts properly connected to ground potential
- No potential difference between individual machine and tool parts
- No sources of electrostatic fields

Our recommendations are based on the internationally applicable standards IEC 61340-5-1 and ANSI/ESD S2020.

2.2 Packing of components

Please refer to product and package specifications and our sales department for information regarding what packaging is available for a given product. Generally, the following list of standards dealing with packing should be considered if applicable for a given package and packing:

- IEC 60286-4 packaging of components for automatic handling part 4: stick magazines for dual inline packages
- IEC 60286-5 packaging of components for automatic handling part 5: matrix trays

2.3 Moisture-Sensitive Components (MSL Classification)

For moisture-sensitive packages, it is necessary to control the moisture content of the components. The penetration of moisture into the package molding compound is generally caused by exposure to the ambient air. In many cases, moisture absorption leads to high moisture concentrations that damage the package during the reflow process. Thus it is necessary to dry moisture-sensitive components, to seal them in a moisture-resistant bag, and to remove them from the bag only immediately prior to assembly to the PCB. The permissible time (from opening the moisture-barrier bag until the final soldering process), during which a component can remain outside the moisture barrier bag, is a measure of the sensitivity of the component to ambient humidity (moisture-sensitivity level, MSL). The most commonly applied standard, IPC/JEDEC J-STD-033*, defines eight different MSLs. Please refer to the "Moisture Sensitivity Caution Label" on the packing material, which contains information about the MSLs of our products. IPC/JEDEC-J-STD-20 specifies the maximum reflow temperature that must not be exceeded during board assembly.

	Floor life (out of bag)	
Level	Time	Conditions
1	Unlimited	
2	1 year	
2a	4 weeks	
3	168 hours	
4	72 hours	≤ 30 °C / 85% RH
5	48 hours	
5a	24 hours	
6	Mandatory bake before use. After bake, it must be reflowed within the time limit specified on the label	

Table 1. Moisture sensivity levels (according to IPC/JEDEC J-STD-033*)

If moisture-sensitive components have been exposed to ambient air for longer than the time specified in their MSL, or the humidity indicator card indicates too much moisture after opening the dry package, the packages have to be baked prior to the assembly process. Please refer to IPC/JEDEC J-STD-033* for details. Baking a package too often can cause solderability problems due to oxidation and/or intermetallic growth. Notice that packing material may not be able to withstand the baking temperature. Please refer to imprints/labels on the packing for maximum temperature. Two moisture sensitivity levels can be given depending on the reflow peak temperature. For lower reflow peak temperature of tin-lead devices might withstand a longer soaking time, as for higher reflow peak temperature of lead-free the MSL might be derated.

2.4 Storage and transportation conditions

Improper transportation and unsuitable storage of components can lead to a number of problems during subsequent processing, such as poor solderability, delamination and package cracking effects. These relevant standards should be taken into account as appropriate:

- IEC 60721-3-0 Classification of environmental conditions: Part 3: Classification of groups of environmental parameters and their severities; introduction
- IEC 60721-3-1 Classification of environmental conditions: Part 3: Classification of groups of environmental parameters and their severities; Section 1: Storage
- IEC 60721-3-2 Classification of environmental conditions: Part 3: Classification of groups of environmental parameters and their severities; Section 2: Transportation
- IEC 61760-2 Surface mounting technology Part 2: Transportation and storage conditions of surface mounting devices (SMD) - Application guide
- IEC 62258-3 Semiconductor Die Products Part 3: Recommendations for good practice in handling, packing and storage ISO 14644-1 Clean rooms and associated controlled environments Part 1: Classification of airborne particulates

Table 2. General storage conditions - overview

Product	Storage conditions
Wafer / die	N2 or MBB (IEC 62258-3) ⁽¹⁾
Component - not moisture sensitive	1K2 (IEC 60721-3-1)

1. MBB = moisture barrier bag

Maximum storage time

The conditions to be complied with in order to ensure problem-free processing of active and passive components are described in standard IEC 61760-2.

References to standard institutes

- American National Standards Institute (ANSI)
- Electronics Industries Alliance (EIA)
- Association Connecting Electronics Industries (IPC)

2.5 Handling damage and contamination

Any mechanical damage during automatic or manual handling of components (in or out of the component packing) that may harm the package leads and/or body must be avoided. In particular, unintentional bending of the leads may cause a loosening in the package body which can result in electrical malfunction. Along with other factors, contamination of a component or packing may cause:

- Solderability problems
- Corrosion
- Electrical short-circuit (due to conductive particles)

2.6 Component solderability

The final plating of most semiconductor packages is sufficiently thick and wettable to assure good solderability, even after an extended storage time. Note that the cut edges of the pins should be ignored in any assessment of solderability. Suitable methods for the assessment of solderability can be derived from JESD22B 102 or IEC6068-2-58.

Components are plated with pure Sn, or preplated with noble metals on a Ni carrier (e.g. NiAu, NiPdAu). Tinplated and preplated components are compatible with both SnPb and Pb-free soldering.

3 Mounting process and mounting material

3.1 PCB Design

For information about leads and exposed die pad of PCB pad design, please refer to the footprint specifications of the respective package on www.st.com.

3.2 Pad Definition and Solder Mask Layer

Two basic types of solder pads are used.

"Solder mask defined" (SMD) pad (figure below): the copper metal pad is larger than the solder mask opening above this pad. Thus the pad area is defined by the opening in the solder mask.

Figure 4. SMD (solder mask defined) pad on PCB



"Non-solder mask defined" (NSMD) pad (figure below): around each copper metal pad there is solder mask clearance. Dimensions and tolerances of the solder mask clearance have to be specified to ensure that the solder pad is not overlapped by the solder mask. Depending on the PCB tolerances, 75 µm is a widely used value.

Figure 5. NSMD (non-solder mask defined) pad on PCB



Solder masking reduces the risk of solder bridging. Therefore it should be applied between all copper pads that are electrically separated.

Solder masking can also be used to divide big copper areas in smaller wettable areas. This often improves processability and results in balanced solder joints.

We recommend SMD pads because they offer a better heat distribution without violating the recommended dimensions for the wettable surface. For power-consuming and heat-dissipating products in SMD packages, it is necessary to have wide conductor paths or even big metal areas, which can be easily structured by solder masking to get a certain size for the wettable surface. When other mounting methods for exposed die pads of SMD packages are used, solder masking is not usually necessary. Generally it is possible to lay out the board pad 1:1 to the exposed die pad. If the exposed die pad protrudes one or more sides of the package body, the board pad size could be slightly increased in this area to get a better self-centering of the component during

reflow soldering. If the exposed die pad is fully hidden under the package body or even surrounded by peripheral pads, decreasing the board pad size is suggested to get more space for routing and vias.

To connect the exposed die pad thermally and electrically directly to inner and/or bottom copper planes of the board, plated through-hole vias are used. They help to distribute the heat coming from the chip over the package die pad and the solder joint to the thermal pad on the board.

A typical hole diameter for such thermal vias is 0.2 to 0.4 mm. This diameter and the number of vias in the thermal pad depend on the thermal requirements of the end product, the power consumption of the product, the application, and the construction of the PCB. However, an array of thermal vias with pitch 1.0 - 1.2 mm can be a reasonable starting point for most products/applications for further optimization. Thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. If the vias remain open during board manufacturing, solder may flow into the vias during board assembly ("solder wicking"). This results in lower stand-off (which is mostly controlled by the solder volume between the package die pad and thermal pad on the PCB), and/or solder protruding from the other side of the board, which may interfere with a second solder paste printing process on this opposite board side. To prevent solder beading, a wettable surface surrounding these vias should be provided to act as a buffer for the surplus solder. Under certain conditions, open vias could have the effect of large voids in the "thermal" solder joint under the die pad, but in general the open vias serve as venting holes for gas in the solder joint. If necessary, the solder wicking can be avoided by plugging (filling with epoxy) and overplating the vias. Having very small vias, so-called microvias (approx. 100 μ m), it is generally sufficient to overplate the via and get a filling by copper. In both cases it is necessary to specify a planar filling. Yet flat dents tend to increased voiding. They serve as traps for voids forming during reflow soldering.

Another method is so-called tenting. The vias in this case are covered with solder mask (e.g. dry-film solder mask). Via tenting is done from top, because with via tenting only from bottom side voiding rate is significantly higher. Combined with an intelligent soldermask layout for the thermal pad this method leads to good processability and balanced solder joints.

If it is not necessary to have a direct connection from the solder pad under the exposed die pad to inner layers of the PCB, it is recommended to place the vias near the package and cover them with solder mask.

3.3 PCB pad finishes

The solder paste should wet solder pads easily. In general, all finishes are well-proven for SMT assembly, but for fine pitch applications, the quality of the plating/finish is very important. Because of the uneven surface of the hot air solder leveling (HASL) finish, lead-free or lead-containing HASL finishes are less preferred for assembly (especially for pitch < 0.65 mm) than "flat" platings such as copper organic solderability preservative (Cu-OSP) or electroless Sn or NiAu.

Therefore, recommendations relative to PCB pad finish, depend on on board design, pad geometry, all the components on the board, and process conditions.

Finish	Typ. layer thickness [µm]	Properties	Concerns
HASL (SnAg) (hot air solder leveling)	> 5	Cheap, widely used, well- known in fabrication	Uneven surface, formation of humps, flatness of single pads have to be good for line- pitch applications
Electroless tin	0.3 - 1.2	Solder join consists of copper and solder only, no further metal is added to the solder join	Long-term stability of protection may be a concern, baking of PCB may be critical
Electroless silver	0.2 - 0.5	Solder join consists of copper and solder only, no further metal is added to the solder join	Long-term stability of protection may be a concern, baking of PCB may be critical
Electroless Ni/ immersion Au (ENIG)	3 - 7 / 0.05 - 0.15	Good solderability protection, high shear-force values	Expensive, concerns about brittle solder joints
Galvanic Ni/Au	> 3 / 0.1 - 2	Only for thicker layers, typically used for connectors	Expensive, not recommended for solder pads
OSP (organic solderability preservatives)	Typical 1	Cheap, simple, fast and automated fabrication	Must be handled carefully to avoid damaging the OSP;
			not as good long-term stability as other coatings;
			for double-sided reflow, suitable for inert gas reflow only

Table 3. Typical PCB pad finishes

4 Mounting on an SMD package

4.1 Main Influences on SMD Assembly Quality

The following factors have to be taken into account to achieve the best assembly quality for a given application:

- PCB
- Footprint and stencil layout
- Solder paste
- Solder paste application and inspection
- Component placement
- Reflow soldering process; especially reflow profile
- Solderability of package

4.2 Solder paste

Solder paste consists of solder alloy and a flux system. Normally the volume is split into about 50% alloy and 50% flux and solvents. In term of mass, this means approximately 90 wt% alloy and 10 wt% flux system and solvents. The flux system has to remove oxides and contamination from the solder joints during the soldering process. The capability of removing oxides and contamination is given by the respective activation level. The contained solvent adjusts the viscosity needed for the solder paste application process. The solvent has to evaporate during reflow soldering.

The metal alloy in Pb-containing solder pastes is typically eutectic SnPb or near eutectic SnPbAg. Lead-free solder pastes contain so-called SAC-alloys (typically 1 - 4% Ag and < 1% Cu). A "no-clean" solder paste is preferred for all packages where cleaning below the component (e.g. leadless packages, packages with exposed die pad) is difficult. The paste must be suitable for printing the solder stencil aperture dimensions; type 3 paste is recommended. Solder paste is sensitive to age, temperature, and humidity. Please follow the handling recommendations of the paste manufacturer.

4.3 Solder Paste Application

Solder paste is usually applied onto the PCB metal pads by stencil printing. Screen printing or dispensing is used only for special applications. The volume of the printed solder paste using screen printing is determined by the screen opening and the screen mesh. The volume of the printed solder paste using stencil printing is determined by the stencil aperture and the stencil thickness. In most cases, the solder paste volume, the screen mesh, and the stencil thickness must meet the needs of all components on the PCB. Using solder paste dispensing instead of paste printing enables a better adjustment of solder paste volume. As a sequential method it is less suitable for high volume production.

For packages in which all leads are the same size, a typical screen opening or stencil aperture is reduced to 90% of the landing pad size.

For packages in which the leads are different sizes, the solder paste volume has to be matched properly to avoid swimming, tilting, solder beading, or "tombstoning" by using appropriate screen openings and stencil apertures. Especially big exposed pads in the center of the component tend to tilt the component if the solder paste volume is not reduced sufficiently. Melted solder always tends to form a spherical shape (lowest surface tension) and therefore big pads that are fully covered with solder paste give a higher stand-off after reflow than smaller pads. This causes tilting of the component, and the different solder depots have to be adjusted.

A segmentation of the stencil for exposed pads or other big pads is shown in the figure below. It also shows open vias that are located in the cross-over points of the segmentation, which prevents direct printing of solder paste into these vias.

Figure 6. Stencil segmentation and vias location for exposed die pads

Due to the fact that the stand-off also depends on the wetting behavior of the board finish, the optimum volume has to be determined by the customer, and the via technology that is used also has to be taken into account. Beside the target stand-off and/or solder-joint volume, the stencil thickness is also determined by the smallest aperture of the stencil.

The following rule of thumb can be used:

- A_{apert} > F x A_{wall}
- A_{apert} : area of the aperture in the stencil

e.g. for a round aperture with radius r: $A_{apert} = \pi x r 2$

Where Awall : area of the wall of the aperture

e.g. for a round aperture with radius r and stencil thickness h : A_{wall} = $2\pi x r x h$

F: feasibility factor, which depends on the stencil and printing process quality and the used solder paste.

e.g. for conservative processes: F = 0.8; for advanced processes: F = 0.6

To ensure a uniform and high solder paste transfer to the PCB, laser-cut (mostly made from stainless steel) and electroformed stencils (Nickel) are preferred. Rounding the corners of rectangular apertures (radius \sim 50 µm) can also support good paste release, and a factor F = 0.6 can be achieved.

4.4 Solder Paste Inspection

For inspection of solder paste depots after printing, vision systems that are either integrated into the printer or separate automatic optical inline (AOI) equipment can be used.

The solder paste x-y-cover and solder paste volume can be measured. Adequate acceptance criteria have to be defined. 80% of maximum cover and volume are achievable values in mass production.

4.5 Component Placement

Although the self-alignment effect due to the surface tension of the liquid solder supports the formation of reliable solder joints, the components have to be placed accurately according to their geometry. Positioning the packages manually is not recommended but is possible, especially for packages with big terminals and pitch. For packages with a pad width of 0.3 mm or less and a pitch of 0.65 or less, an automatic pick&place machine is recommended to achieve reliable solder joints. Component placement accuracies of ±50 µm are obtained with modern automatic component placement machines using vision systems. With these systems, both the PCB and the components are optically measured and the components are placed on the PCB at their programmed positions. The fiducials on the PCB are located either on the edge of the PCB for the entire PCB or additionally on individual mounting positions (local fiducials). They are detected by a vision system immediately before the mounting process. Recognition of the packages is performed by a special vision system, enabling the complete package to be centered correctly. The maximum tolerable displacement of the components is 20% of the metal pad width on the PCB (for non-solder-mask defined pads). For example, for exposed die pad LQFP packages with 0.5 mm lead pitch, the device-pad-to-PCB-pad misalignment has to be less than 50 µm to assure a robust mounting process.

The following factors are important:

- Especially on large boards, local fiducials close to the device can compensate for PCB tolerances.
- The lead recognition capabilities of the placement system should be used rather than the outline centering. Outline centering can only be used for packages where the tolerances between pad and outline are small compared to the placement accuracy needed.
- To ensure the identification of the packages by the vision system, adequate lighting as well as the correct choice of measuring modes is necessary. The correct settings can be taken from the equipment manuals.
- Too much placement force can squeeze out solder paste and cause solder joint shorts. On the other hand, not enough placement force can lead to insufficient contact between package and solder paste and may result in insufficient sticking of the component on the solder paste, which may then lead to shifted or dropped devices.

A pick-up nozzle suitable for the package body size should be used. The nozzle should be slightly smaller than the package body. A bigger nozzle may lead to an irregular force distribution, especially to increased forces at the edges of the package body. On the other hand, a nozzle that is too small may lead to increased forces in the package center. Package bodies that are divided into different areas that have different heights require special care when choosing the nozzle. Nozzle shape and size are probably more critical in these cases.

4.6 Reflow Soldering

The goal of the reflow process is to melt the powder particles in the solder paste, with the surfaces being joined together, and solidify the solder to create a strong metallurgical bond. There are usually four process zones in a conventional reflow process, consisting of preheat, thermal soak, reflow, and cooling. Generally standard reflow soldering processes such as:

- Forced convection
- Vapor phase
- Infrared
- Vacuum (for special applications)

and typical temperature profiles are suitable for board assembly.

During the reflow process, solder joints have to be exposed to temperatures above the melting point of solder for a sufficient time to get the optimum solder-joint quality, whereas overheating the PCB with its components has to be avoided. Please refer to information provided for the maximum package body temperature. It is important that the maximum temperature of the package during the reflow does not exceed the specified peak temperature on the moisture level caution label.



When using infrared (IR) ovens without convection, special care may be necessary to assure a sufficiently homogeneous temperature profile for all solder joints on the PCB, especially on large, complex boards with different thermal masses of the components. In IR soldering, the components are heated as a result of absorbing IR radiation. Usually the heating is done with radiators positioned on either side in order to heat or preheat the whole area surrounding the solder joint, if possible. The temperature of the different components may vary significantly. Since the metallic terminals of the components exhibit only low absorption, i.e. they reflect IR radiation, the heat has to be supplied to the solder joints via the component itself, the similarly heated PCB, and the ambient air.

Absorption depends on the material and the wavelength, and the latter, in its turn, depends on the radiator temperature. Large and thick packages take longer to get hot than small and thin ones. Special care has to be taken when large exposed die pads are soldered by IR radiation, because the solder joints between the package and the PCB heat up much more slowly than the environment. Precautions must be taken by empirically varying the radiator temperature and the conveyor speed to ensure that neither the minimum soldering temperature nor the maximum temperature is exceeded at any point. This must be ensured by specific temperature measurements.

Compared to forced convection and especially IR soldering, a vapor-phase oven has the least risk of overheating because it uses special fluids with a vapor temperature slightly above the melting point of the solder alloy used. The atmosphere is free of oxygen. One disadvantage is that most vapor-phase ovens are designed for batch processing and not conveyor driven. This makes it difficult to use them in mass-production lines.

The most highly recommended reflow process is forced convection, which is normally used in mass production. The heat in forced convection is transferred to the PCB in different zones by heated air or nitrogen. The number of zones, volume of hot gas, and oven design determine the capacity and the ability to reproduce the optimum reflow profile, which is influenced by:

- Board thickness and layout
- Differences in thermal mass of all components
- Maximum allowed component temperatures
- Recommended reflow profile for the solder paste

Using a nitrogen atmosphere can generally improve solder-joint quality, but is normally not necessary for soldering the available package lead finishes. For the lead-free process with higher reflow temperatures, a nitrogen atmosphere may reduce oxidation and improve the solder-joint quality.

The temperature profile of a reflow process is divided into several phases, each with a special function. The individual parameters are influenced by various factors, not only by the package. First, it is essential to follow the solder paste manufacturer's application notes. Additionally, most PCBs contain more than one package type and therefore the reflow profile has to be matched to all components and materials' demands. We recommend measuring the solder joints' temperatures by thermocouples beneath the various packages. Components with large thermal masses do not heat up at the same speed as lightweight components, and the position and the surrounding of the package on the PCB, as well as the PCB thickness, can influence the solder-joint temperature significantly.

The figure below shows a generalized forced-convection reflow profile for soldering SMD packages. The given data is an example, not a recommendation (for reference only).



Figure 7. Recommended soldering reflow profile for SMD packages

5 Cleaning

After the soldering process, flux residues may be found around the solder joints. However, if the solder joints have to be cleaned, the cleaning method (e.g. ultrasonic, spray, or vapor cleaning) and solution must be selected with consideration of the packages to be cleaned, the flux used (rosin-based, water-soluble, etc.), and environmental and safety aspects. Removing/drying even of small residues of the cleaning solution should also be done very thoroughly.

6 Inspection of SMD packages

After component placement:

A visual inspection after component placement can be done by AOI. It is used to check if the mounting is done completely and if severe misplacements have occurred. The correct orientation of the component can also be checked.

After soldering:

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The solder joint meniscus of the leads of SMD packages can be inspected by optical microscope or AOI. Acceptable solder joints are described in international standards such as IPC-A-610.

The figure below shows an SMD package lead with optimal wetting. For SMD packages, it may also be necessary to assess the joint quality under leads with x-ray and/or cross sectioning.

Figure 8. Examples of correctly soldered SMD packages (gull-wing leads)





If exposed die pads are soldered, X-ray is the only reliable method to inspect the whole solder joint. The figure below shows an example of SMD package. The only optically accessible areas are leadframe areas that extend beyond the package body.

Figure 9. Example of a correctly soldered D²PAK package on PCB







Figure 10. Example of a correctly soldered TO-LL package on PCB

Automatic x-ray inspection (AXI) is the only reasonable method for efficient inline control. AXI systems are available as 2D and 3D solutions. They usually consist of an x-ray camera and the hardware and software needed for inspection, control, analysis and data transfer routines. These systems enable the user to reliably detect soldering defects such as poor soldering, bridging, voiding and missing parts. For the acceptability of electronic assemblies, please refer also to the IPC-A-610C standard.

Cross sectioning of a soldered package as well as dye penetrant analysis can serve as tools for sample monitoring only, because of their destructive character. Nonetheless, these analysis methods must be used during engineering of new products at customer production sites to obtain detailed information about the solder joint quality.

Lead-free (SnAgCu) solder joints typically do not have a bright surface. Lead-free solder joints are often dull and grainy. These surface properties are caused by the irregular solidification of the solder as the solder alloys are not exactly eutectic .This means that SnAgCu solders do not have a melting point but rather a melting range of several degrees. Although lead-free solder joints have a dull surface, this does not mean that lead-free joints are of lower quality or weaker. It is therefore necessary to teach the inspection staff what these lead-free joints look like, and/or to adjust optical inspection systems to handle lead-free solder joints.

7 Rework of device

If a defective component is observed after board assembly, the device can be removed and replaced with a new one. Repair of single solder joints is generally possible, but requires proper tools. For example, repairing the solder joint of an exposed die pad cannot be done with a soldering iron.

Whichever rework process is applied, it is important to recognize that heating a board and its components above 200 °C may result in damage. As a precaution, every board with its components should be baked prior to rework. For details, please refer to the international standard J-STD-033.

In any case, mechanical, thermal or thermo-mechanical overstress must be avoided, and rework must be performed according to JEDEC J-STD-033A, IPC-7711 and IPC-7721.

7.1 Device removal

If a defective component is going to be sent back to the supplier, no further defects must be caused during the removal of this component, as this may hinder the failure analysis by the supplier. The following recommendations should be considered:

- Temperature profile: during the de-soldering process, ensure that the package peak temperature is not higher and temperature ramps are not steeper than for the standard assembly wave process.
- Mechanics: be careful not to apply high mechanical forces during removal. Otherwise, failure analysis of the package may become impossible, or the PCB may be damaged. For large packages, pipettes can be used (implemented on most rework systems); for small packages, tweezers may be more practical.

7.2 Site redressing

After removing the defective component, the pads on the PCB must be cleaned to remove solder residues. This may be done by vacuum de-soldering or using a wick.

Do not use steel brushes because steel residues can lead to bad solder joints. Before placing a new component, it may be necessary to apply solder paste on the PCB pads by printing (special micro-stencil) or dispensing.

7.3 Reassembly and reflow

After preparing the site, the new package can be placed onto the PCB and the leads inserted into the holes. Regarding placement accuracy and placement force, the process should be comparable to the (automatic) pick&place process.

During the soldering process, ensure that the package peak temperature is not higher and temperature ramps are not steeper than for the standard assembly process. Soldering wire can be used to re-solder the leads. Only use no-clean solder paste, solder wire, and flux for repair.



8 Coating of assembled PCBs

In some applications, coatings are used to prevent damage due to external influences such as:

- Mechanical abrasion
- Vibration
- Shock
- Humidity
- Hand perspiration
- Chemicals and corrosive gases

These influences may cause:

- Electrical leakage due to humidity
- Corrosion that leads to degradation of conductor paths, solder joints, and any other metallized areas; and/or formation of electrical leakage paths. These can eventually result in electrical shorts (electrical leakage) or open contacts
- Mechanical damage to conductor paths, solder joints and components. This damage can lead to electrical failures

Coatings act as electrically isolating and impervious covers that adhere well to the different PCB materials. A wide variety of different coatings are available on the market. They differ in:

- Price
- Process complexity (spray, dip, casting, curing, etc.)
- Reparability
- Controllability
- Homogeneity

It is important to understand the chemical, electrical, mechanical and thermo-mechanical interaction between the coating and the PCB and its components. Coatings can affect component reliability.

Revision history

Table 4. Document revision history

Date	Revision	Changes
23-Oct-2015	1	Initial release.
17-May-2019	2	Updated Figure 1, Figure 3 and Figure 9. Added Figure 10.

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