No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.3.7.6	Input Current LIN Dominant	$I_{LINPASdom}$	V_{LIN} = 0V; VB = 12V; driver off	-1			mA
1.3.7.7	Input Current LIN Recessive, No GND for Bus	I_{LIN_NOGND}	0V ≤ V_{LIN} ≤ 18V; V_{GND} = V_{VB}; VB = 12V	-1		1	mA
1.3.7.8	Input Current LIN No GND for Bus	I_{LIN_LOSTVB}	-40°C ≤ T_{AMB} ≤ 125°C; V_{GND} = V_{SUP} = 0V; 0V ≤ V_{LIN} ≤ 18V		3	20	µA
			125°C ≤ T_{AMB} ≤ 150°C; V_{GND} = V_{SUP} = 0V; 0V ≤ V_{LIN} ≤ 18V		3	50	µA
1.3.7.9	Slew Rate [3)]	SR_{LIN}	Rising and falling edges, transmit and receive	0.5	1.3	3	V/µs
1.3.7.10	Input Low Level Receiver	V_{RECL}				0.4	VB
1.3.7.11	Input High Level Receiver	V_{RECH}		0.6			VB
1.3.7.12	Input Hysteresis Receiver	V_{RECHYS}	V_{RECHYS} = V_{RECH} - V_{RECL}	0.08		0.12	VB
1.3.7.13	Input Center Point Receiver	V_{BUS_CNT}	V_{BUS_CNT} = (V_{RECL} + V_{RECH})/2	0.475	0.5	0.525	VB
1.3.7.14	Duty Cycle 1	D1	$TH_{Rec(max)}$ = 0.744 * VB; $TH_{Dom(max)}$ = 0.581 * VB; VB = 7.0 to 18V; t_{Bit} = 50µs; D1 = $t_{BUS\_rec(min)}$/(2 * t_{Bit}) (See *ZSSC3170 LIN Interface Description* for details.)	0.396			-
1.3.7.15	Duty Cycle 2	D2	$TH_{Rec(min)}$ = 0.422 * VB; $TH_{Dom(min)}$ = 0.284 * VB; VB = 7.6 to 18V; t_{Bit} = 50µs; D1 = $t_{BUS\_rec(max)}$/(2 * t_{Bit}) (See *ZSSC3170 LIN Interface Description* for details.)			0.581	-
1.3.7.16	Duty Cycle 3	D3	$TH_{Rec(max)}$ = 0.778 * VB; $TH_{Dom(max)}$ = 0.616 * VB; VB = 7.0 to 18V; t_{Bit} = 96µs; D3 = $t_{BUS\_rec(min)}$/(2 * t_{Bit}) (See *ZSSC3170 LIN Interface Description* for details.)	0.417			-

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.3.7.17	Duty Cycle 4	D4	$TH_{Rec(min)}$ = 0.389 * VB; $TH_{Dom(min)}$ = 0.251 * VB; VB = 7.6 to 18V; t_{Bit} = 96µs; D4 = $t_{BUS\_rec(max)}/(2 * t_{Bit})$ (See *ZSSC3170 LIN Interface Description* for details.)			0.590	-
1.3.8	**System Response**						
1.3.8.1	Start-Up Time [1]	t_{START}	Until first valid output; f_{OSC} = 2MHz			30	ms
1.3.8.2	Response Time LIN_Mode; Typical LIN Configuration [4]	$t_{RESP\_LIN\_2\_14\_5}$	f_{OSC} = 2.2MHz; 14-bit resolution; LIN Mode; 100% final value (see Table 2.5)			3.6	ms
1.3.8.3	Response Time PWM Mode; Typical PWM Configuration [5]	$t_{RESP\_PWM\_2\_14\_2}$	f_{OSC} = 1.8MHz; 14-bit resolution; PWM Mode; 100% final value (see Table 2.4)			20	ms
1.3.8.4	Overall Error AFE [6, 7] (f_{OSC} = 2MHz, XZC off; no sensor related errors; relative to digital value)	F_{AFE_85}	T_{AMB}: -20°C to 85°C			0.25	%FS
		F_{AFE_125}	T_{AMB}: -40°C to 125°C			0.5	%FS
		F_{AFE_150}	T_{AMB}: -40°C to 150°C			1.0	%FS

1) No measurement in mass production; parameter is guaranteed by design and/or quality observation.

2) In PWM Mode with Low-Side Switch (LSS) and PWM Mode with High-Side Switch (HSS), the sensor connection check (SCC) and the sensor short check (SSC) diagnostics are available only for ZSSC3170 silicon revision “F” and any subsequent revisions

3) For complete specification, see the *ZSSC3170 LIN Interface Description.*

4) 2-step A/D conversion (ADCORD=1), 14-bit resolution (ADCRES=1), resolution 2nd conversion step 5-bit (ADCMODE=11)

5) 2-step A/D conversion (ADCORD=1), 14-bit resolution (ADCRES=1), resolution 2nd conversion step 2-bit (ADCMODE=00)

6) Deviation from ideal line including INL, gain, offset, and temperature errors.

7) With XZC active: additional total error of max. 25ppm/K at XZC = 31. Error decreases linearly at XZC < 31.

1.4 Interface Characteristics

Table 1.4 Interface Characteristics

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.4.1	**I^2C™ Interface**						
1.4.1.1	Input High Level [1]	$V_{I2C\_IN\_H}$		0.8			VDDA
1.4.1.2	Input Low Level [1]	$V_{I2C\_IN\_L}$				0.2	VDDA
1.4.1.3	Output Low Level [1]	$V_{I2C\_OUT\_L}$	Open drain output current: < 2mA			0.15	VDDA
1.4.1.4	SDA Load Capacity [1]	C_{SDA}				400	pF
1.4.1.5	SCL Clock Frequency [1]	f_{SCL}				400	kHz
1.4.1.6	Internal Pull-Up Resistor [1]	R_{I2C}		25		100	kΩ
1.4.2	**One-Wire Interface at HOUT and LOUT (LIN Protocol)**						
1.4.2.1	Input Low Level [1]	$V_{OWI\_IN\_L}$				1	V
1.4.2.2	Input High Level [1]	$V_{OWI\_IN\_H}$		4			V
1.4.2.3	Start Window [1]	t_{START_WIN}	At f_{OSC} = 2MHz			30	ms

1) No measurement in mass production; parameter is guaranteed by design and/or quality observation.

1.5 EEPROM

Table 1.5 EEPROM

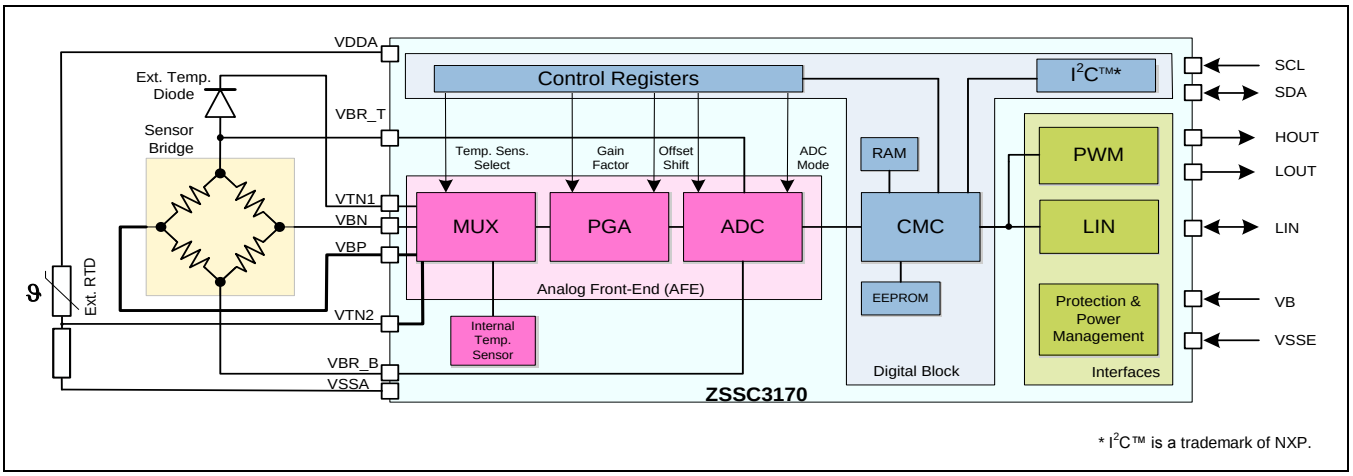
No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.5.1	Write Cycles	$n_{EEP\_WRI\_85}$	T_{AMB} < 85°C			1000	
		$n_{EEP\_WRI\_150}$	T_{AMB} < 150°C			100	
1.5.2	Read Cycles	n_{EEP_RD}				$8 * 10^8$	
1.5.3	Data Retention	t_{EEP_RET}	100000h@55°C + 27000h@125°C + 3000h@150°C			15	a
1.5.4	Programming Time	t_{EEP_WRI}	Per written word, at f_{OSC} = 2MHz		12		ms

2 Circuit Description

2.1 Signal Flow and Block Diagram

The signal path of the ZSSC3170 consists of the analog front end (AFE), the digital signal processing block, and interfaces including protection circuitry. Based on a differential structure, the bridge inputs VBP and VBN are handled by two signal lines each with a dynamic range symmetrical to the common mode potential (analog ground equal to VDDA/2). Therefore it is possible to amplify positive and negative input signals within the common mode range of the signal input.

Figure 2.1 Block Diagram of ZSSC3170



The multiplexer (MUX) transmits the signals from either the bridge sensor or the selected temperature sensors to the analog-to-digital converter (ADC) in a defined sequence. The temperature sensor can either be an external or internal diode or an external thermistor (RTD), selected by EEPROM configuration. In LIN Mode, temperature output is available. For this temperature measurement, the same temperature sensor can be used as for calibration temperature, or a second temperature sensor input can be selected. The differential signal from the bridge sensor is pre-amplified by the programmable gain amplifier (PGA). The ADC converts bridge sensor and temperature signals into digital values.

The digital signal conditioning takes place in the calibration microcontroller (CMC) using a ROM-resident conditioning formula and sensor-specific coefficients stored in the EEPROM during calibration. The configuration data and the correction parameters can be programmed into the EEPROM by digital communication at the output pins or at the I²C™ interface. Depending on the programmed output configuration, the corrected sensor signal is output as a PWM signal (high-side switch or low-side switch) or as a digital value within a LIN frame. During the calibration procedure, the I²C™ interface can provide measurement values as well.

2.2 Application Modes

For each application, a configuration set must be established (generally prior to calibration) by programming the on-chip EEPROM for the following modes:

Table 2.1 Configuration for Application Modes

Bridge Sensor Channel	
Input Voltage Range	Select gain stage of the AFE with respect to the maximum sensor signal span and the zero point of the ADC.
Bridge Sensor Offset Compensation (XZC)	Activate the analog sensor offset compensation if required; e.g., if the sensor offset voltage is close to or larger than the sensor span.
Resolution/Response Time	Select appropriate resolution of the ADC. Settings will influence sampling rate, signal integration time, and therefore sensitivity to noise and disturbances.
Temperature Measurement	
Temperature Measurement for the Correction of the Bridge Signal	Select temperature sensor to calibrate temperature related errors.
Temperature Measurement for the Temperature Output in LIN Mode	Select temperature sensor for temperature measurement.
Output Signal	
Output Mode	Select PWM or LIN according to application requirements.
LIN Mode	Select LIN compatibility to specification package LIN2.1, LIN2.0, or LIN1.3.
PWM Mode	Select switch type: high-side switch (HSS) or low-side switch (LSS).

2.3 Analog Front End (AFE)

The analog front end (AFE) consists of the signal multiplexer (MUX), the programmable gain amplifier (PGA) and the analog-to-digital converter (ADC).

2.3.1 Programmable Gain Amplifier (PGA)

Table 2.2 shows the adjustable gains, corresponding sensor signal spans, and common mode range limits. See section 2.3.2 for details for XZC.

Table 2.2 Adjustable Gain Stages, Corresponding Sensor Signal Spans, and Common Mode Ranges

Overall Gain a_{IN}	Maximum Input Voltage Range V_{IN_SPAN} [mV/V] 1)	Gain Amp1	Gain Amp2	Gain Amp3	Input Common Mode Range V_{IN_CM} [%VDDA] 2)	
					XZC off	XZC on
420	1.8	30	7	2	29 to 65	45 to 55
280	2.7	30	4.66	2	29 to 65	45 to 55
210	3.6	15	7	2	29 to 65	45 to 55
140	5.4	15	4.66	2	29 to 65	45 to 55
105	7.1	7.5	7	2	29 to 65	45 to 55
70	10.7	7.5	4.66	2	29 to 65	45 to 55
52.5	14.3	3.75	7	2	29 to 65	45 to 55
35	21.4	3.75	4.66	2	29 to 65	45 to 55
26.3	28.5	3.75	3.5	2	29 to 65	45 to 55
14	53.75	1	7	2	29 to 65	45 to 55
9.3	80	1	4.66	2	29 to 65	45 to 55
7	107	1	3.5	2	29 to 65	45 to 55
2.8	267	1	1.4	2	32 to 57	Not applicable

1) Recommended internal signal range: maximum 80% supply voltage. Range is defined by 80% of supply voltage divided by selected gain.

2) At maximum input signal (with XZC: +300% offset).

2.3.2 Offset Compensation

The ZSSC3170 supports two methods of sensor offset compensation:

- Digital offset correction is processed during the digital signal conditioning by the calibration microcontroller (CMC).
- Bridge sensor offset compensation (XZC) is achieved by adding a compensation voltage at the analog signal path that removes coarse offset. XZC is needed for large offset values that would otherwise overdrive the analog signal path, and it can be adjusted by 6 EEPROM bits. Depending on the gain adjustment, XZC can handle offset values of up to 300% of the sensor signal range.

Table 2.3 Bridge Sensor Offset Shift Ranges

Overall Gain a_{IN}	Maximum Input Voltage Range V_{IN_SPAN} (mV/V)	Offset Shift per Step (%Full Span)	Approximate Maximum Offset Shift (mV/V)	Approximate Maximum Offset Shift (%V_{IN_SPAN})
420	1.8	12.5	7.8	388
280	2.7	7.6	7.1	237
210	3.6	12.5	15.5	388
140	5.4	7.6	14.2	237
105	7.1	12.5	31	388
70	10.7	7.6	28	237
52.5	14.3	12.5	62	388
35	21.4	7.6	57	237
26.3	28.5	5.2	52	161
14	53.6	12.5	233	388
10	80	7.6	207	237
7	107	5.2	194	161
2.8	267	0.83	78	26

2.3.3 Analog-to-Digital Converter

The analog-to-digital converter (ADC) is designed in full differential switched capacitor technology with a selectable resolution of 13 or 14 bits. The ADC can operate in first or second order configuration. The conversion is largely insensitive to short-term and long-term instabilities of the clock frequency.

- **MSB segment conversion:** In this first step of the A/D conversion, the measurement value is integrated over the complete conversion time ensuring a high degree of noise suppression. To extend the integration phase to the maximum, this fraction of the complete conversion time is selected to be as long as possible corresponding to the time available.
- **LSB segment conversion:** To achieve a higher resolution, the residual value of the first step is converted in a subsequent step by a second converter. In first-order configuration, the second step is skipped (single-step conversion).

Table 2.4 A/D Resolution and Conversion Time in PWM Modes

Mode	A/D Resolution Total (bit)	A/D Resolution MSB Segment Conversion (bit)	A/D Resolution LSB Segment Conversion (bit)	A/D Conversion Mode ADC MODE [1]	PWM Cycle Time (f_{OSC} = 1.8MHz) (ms)
PWM / ADC 2 step[1]	14	12	2	00	19.9
	14	11	3	01	10.8
	14	10	4	10	6.3
	14	9	5	11	4.0
	13	11	2	00	10.8
	13	10	3	01	6.3
	13	9	4	10	4.0
	13	8	5	11	2.8
PWM / ADC 1 step	14	14	n/a	n/a	37.5
	13	13	n/a	n/a	19.3

1) See the *ZSSC3170 Functional Description* for details.

Table 2.5 A/D Resolution and Conversion Time in LIN Modes

Mode	A/D Resolution Total (bit)	A/D Resolution MSB Segment Conversion (bit)	A/D Resolution LSB Segment Conversion (bit)	A/D Conversion Mode ADC MODE [1]	Response Time [2] in LIN Mode (f_{OSC} = 2.2MHz) (ms)
LIN / ADC 2 step	14	12	2	00	16.3
	14	11	3	01	8.9
	14	10	4	10	5.2
	14	9	5	11	3.3
	13	11	2	00	8.9
	13	10	3	01	5.2
	13	9	4	10	3.3
	13	8	5	11	2.4
LIN / ADC 1 step	14	14	n/a	n/a	61.5
	13	13	n/a	n/a	31.7

1) See the *ZSSC3170 Functional Description* for details.
2) Total response time.

Equation (1) describes the conversion result:

$$Z_{ADC} = 2^r * \left(\frac{V_{ADC\_IN}}{V_{ADC\_REF} - RS_{ADC}} \right) \quad (1)$$

Where

Z_{ADC}	A/D conversion result
r	A/D resolution in bits
V_{ADC_IN}	Differential input voltage of ADC
V_{ADC_REF}	Differential reference voltage of ADC
RS_{ADC}	ADC range shift adjustable by EEPROM configuration (RS_{ADC} = $^1/_{16}$, $^1/_8$, $^1/_4$, $^1/_2$)

By selecting different values of RS_{ADC}, the user can match the sensor input signal to the optimum input voltage range of the ADC. The ADC reference voltage V_{ADC_REF} is defined as the difference between the bridge supply potentials at pins VBR_T and VBR_B. The theoretical ADC input voltage range ADC_{INP_R} is equal to this ADC reference voltage.

A major constraint required for achieving the specified precision as well as the stability and nonlinearity parameters of the AFE is to use a maximum ADC input voltage range of 10% to 90% of ADC_{INP_R} within the application. This is of special importance for ensuring the specified parameters for the entire operating temperature range as well as all possible sensor bridge tolerances. The validity of these conditions is not checked by the ZSSC3170's failsafe functions and therefore must be ensured by the customer-specific configuration.

2.4 Temperature Measurement

The following temperature sensors are supported by ZSSC3170 for both temperature and calibration temperature measurement:

- Internal pn-diode
- External pn-diode; anode to pin VBR_T
- External resistive half-bridge with the thermistor connected in the upper branch

In PWM Mode, the conditioning calculation for the bridge sensor signal is based on values of the selected temperature sensor.

In LIN Mode, two temperature measurements are executed using either two different sensors or one sensor for both measurements. The temperature output value is the result of a conditioning calculation including offset compensation, gain correction, and 2nd order nonlinearity compensation. The conditioning coefficients are stored in the EEPROM.

2.5 System Control and Conditioning Calculation

The system control performs the following tasks:

- Sequencing of the start-up phase
- Control of measurement cycle based on EEPROM configuration data
- 16-bit conditioning calculation for each measurement signal based on EEPROM conditioning coefficients and ROM-resident signal conditioning algorithm
- Processing of communication requests received at the serial interfaces
- Control of calibration mode
- Processing of diagnostic and failsafe tasks

For a detailed description, refer to the *ZSSC3170 Functional Description*.

2.5.1 Operating Modes

Three main modes are implemented in the integrated state machine:

- Normal Operation Mode (NOM) with continuous signal conditioning
- Command Mode (CM), which provides access to all internal registers and provides the basis for configuration and calibration of the ZSSC3170
- Diagnostic Mode (DM), which indicates detected error conditions

2.5.2 Start-Up Phase

The start-up phase consists of the following time periods:

- Settling of the internal voltage supply represented by the voltage VDDA-VSSA. At the end of this period, the power-on-reset circuit (POR) switches off the reset signal.
- System start, readout of EEPROM, and signature check.
- Processing of the signal conditioning start routine containing bridge sensor signal and temperature measurements, associated auto-zero measurements, and the conditioning calculation itself. Within this period, the output pins are ready to receive special LIN frames resulting in entering the Command Mode (CM). This start window is active for up to 30ms.

The ZSSC3170 switches into Normal Operation Mode (NOM) after the start window is passed. It proceeds with the cyclic processing of the measurement and conditioning tasks.

2.5.3 Measurement Cycle

Depending on the EEPROM settings, the multiplexer selects the following inputs in a defined sequence:

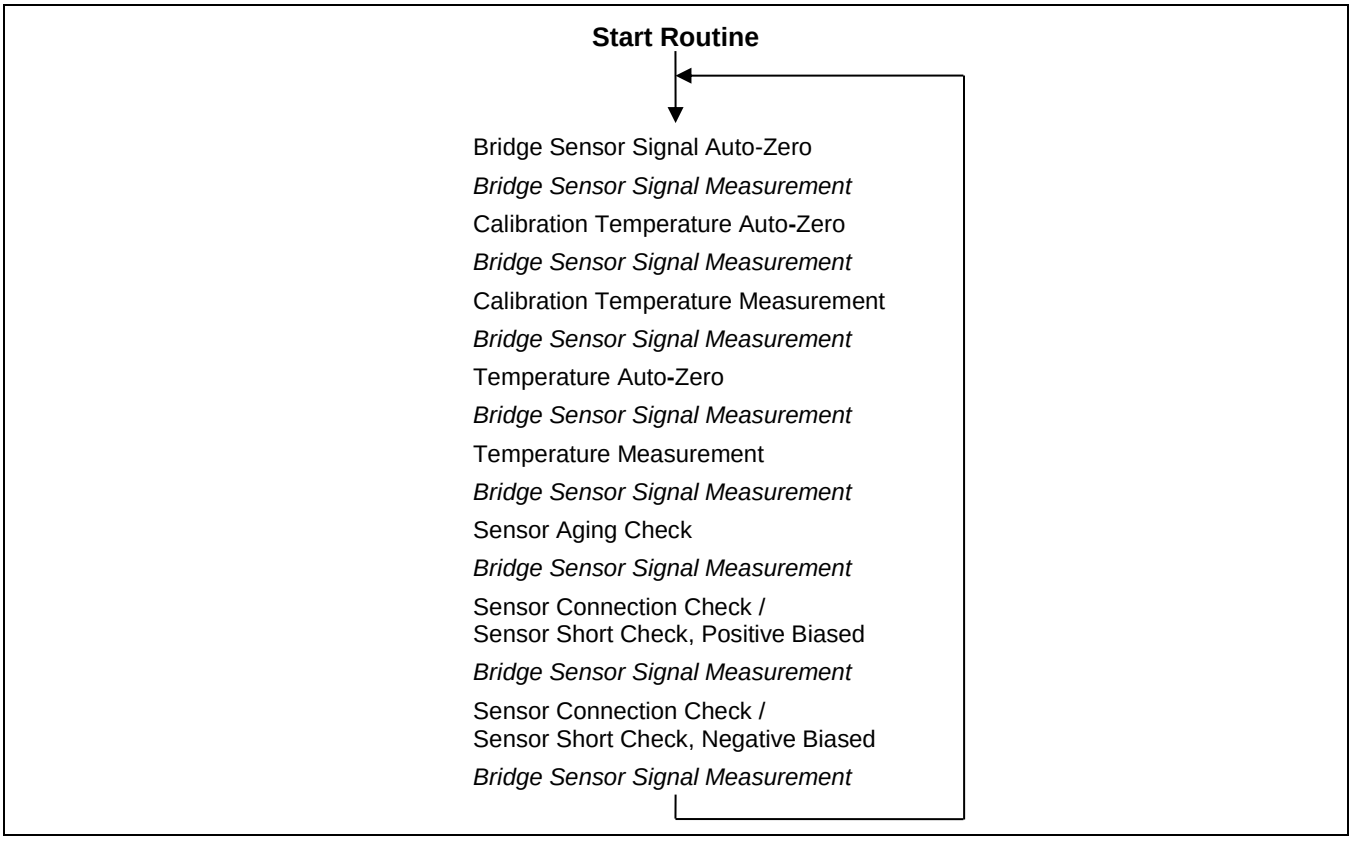
- Pre-amplified sensor bridge signal
- Temperature sensor defined by EEPROM configuration for calibration temperature
- Temperature sensor defined by EEPROM configuration for temperature measurement
- Auto-zero signal
- Diagnostic signals

The CMC controls the complete measurement cycle following a basic flow shown in Figure 2.2.

All necessary measurements for bridge sensor and temperature signal are executed once after power-on within the start-up routine. This initial phase is followed by continuous processing of the complete measurement cycle. The sensor connection check (SCC), sensor short check (SSC), and sensor aging check (SAC) for diagnostic tasks (see section 2.8) are continuously executed within the regular measurement cycle even if the processing of the diagnostic function is disabled by the EEPROM configuration.

For details, refer to the *ZSSC3170 Functional Description.*

Figure 2.2 Measurement Cycle



2.5.4 Conditioning Calculation

After digital auto-zero correction of the bridge sensor measurement value, the interim result is further processed based on the correction formula. Offset and gain with temperature effects up to 2nd order and non-linearity up to 3rd order can be compensated for, resulting in a positive 15-bit bridge sensor result value normalized to the range of [0;1].

In LIN Mode, the digital measurement value of the temperature is processed based on a proprietary correction formula as well. Offset, gain, and non-linearity up to 2nd order can be compensated for yielding a positive 15-bit temperature value normalized to the range of [0;1].

2.6 Signal Outputs

ZSSC3170 provides three signal outputs:

- LIN – LIN Interface revision 2.1/2.0 with compatibility to revision 1.3
- HOUT – PWM high-side switch (HSS)
- LOUT – PWM low-side switch (LSS)

For the respective application, one signal output must be selected and configured as the active output. Idle outputs must be not connected.

To enter the Command Mode (CM), communication can be established at each of the three output pins. A dedicated command must be sent during the start window immediately after power-on (duration t_{START_WN}; see specification 1.4.2.3). The communication protocol at all pins is based on the LIN Data Link Layer. Note that communication at the HOUT pin uses the inverted signal levels of the LIN frame. In LIN Mode, communication at the LIN pin is always possible during Normal Operation Mode (NOM).

To enable communication within the start window, the output drivers are set to tri-state during this time. The outputs HOUT and LOUT are connected to internal pull-up resistors to ensure the necessary resistive stage. For the LIN transceiver, an internal pull-up resistor is implemented by default (according to the LIN Specification Package, Physical Layer section).

If not switched into CM before expiration of the 30ms start window, depending on the configuration, the ZSSC3170 will start to provide a PWM signal or can respond to communication requests of the LIN master.

The function set of the signal outputs is specified in detail in the following documents: the *ZSSC3170 Functional Description* and the *ZSSC3170 LIN Interface Description.*

Note: LIN Sleep Mode must be disabled for proper PWM operation.

2.6.1 PWM Outputs HOUT and LOUT

In PWM Mode, the output signal is provided at the pins HOUT or LOUT accordingly.

The outputs are protected from short circuit overload by current limiters and time monitoring. Driving the signal lines with slew-rate-limited edges reduces electromagnetic emission. At the HOUT pin, a voltage higher than the maximum supply voltage can be tolerated. The notably low leakage current of LOUT is designed to cover the requirements of some unique electronic control units (ECU).

2.6.2 LIN Output

The output of the integrated LIN transceiver at the LIN pin is compatible with the LIN revisions 2.1, 2.0 and 1.3. For details, refer to the *ZSSC3170 LIN Interface Description*. For LIN Physical Layer Conformance Tests, the control pins of the integrated LIN transceiver can be accessed separately in a LIN Conformance Test Mode.

2.7 Digital Test and Calibration Interface

Beyond the digital communication features accessed via the output pins, the ZSSC3170 provides an I²C™ compatible test and calibration interface with slave functionality. For a detailed description of the I²C™ interface, refer to the *ZSSC3170 Functional Description.*

2.8 Diagnostic and Failsafe Features, Watchdog, and Error Detection

The ZSSC3170 detects various possible failures. An identified failure is indicated by the ZSSC3170 entering the Diagnostic Mode (DM). With PWM active, the respective output is switched to the resistive mode. In LIN Mode, depending on the error classification, the correlated status bits are activated. A watchdog continuously monitors the operations of the CMC and the running measurement loop. The operation of the internal clock oscillator is monitored by the oscillator failure detection. A check of the sensor bridge for broken or shorted wires is performed continuously (the sensor connection check (SCC) and the sensor short check (SSC). In PWM Mode with Low-Side Switch (LSS) and PWM Mode with High-Side Switch (HSS), the diagnosis functions SCC and SSC are only available from ZSSC3170 silicon revision “F” and any subsequent revisions. The common mode voltage of the sensor (CMV) is monitored continuously (sensor aging check (SAC)). A check for a broken chip (BCC) can be applied in the start-up phase after power-on. RAM, ROM, EEPROM, registers, and the arithmetic unit are monitored continuously. Refer to the *ZSSC3170 Functional Description* for a detailed description.

2.9 High Voltage, Reverse Polarity, and Short Circuit Protection

The ZSSC3170 is designed for a direct 12V supply, which can be provided by a vehicle power system. Internal sub-assemblies are supplied and protected by integrated voltage regulators and limiters. Specific protection circuits allow tolerance of permanent reverse polarity at supply and output pins. These functions are described in detail in the document *ZSSC3170 High Voltage Protection Description.* When operated in the application circuits shown in section 3, the protection features of the ZSSC3170 are guaranteed without time limit.

3 Application Circuit Examples and External Components

3.1 Application Circuit Examples

Note: Pad locations shown in the following figures are approximate. For specific pad locations, refer to the *ZSSC3170 Technical Note – Die Dimensions and Pad Coordinates* (see section 8).

Figure 3.1 Application Circuit in PWM Mode with Low-Side Switch

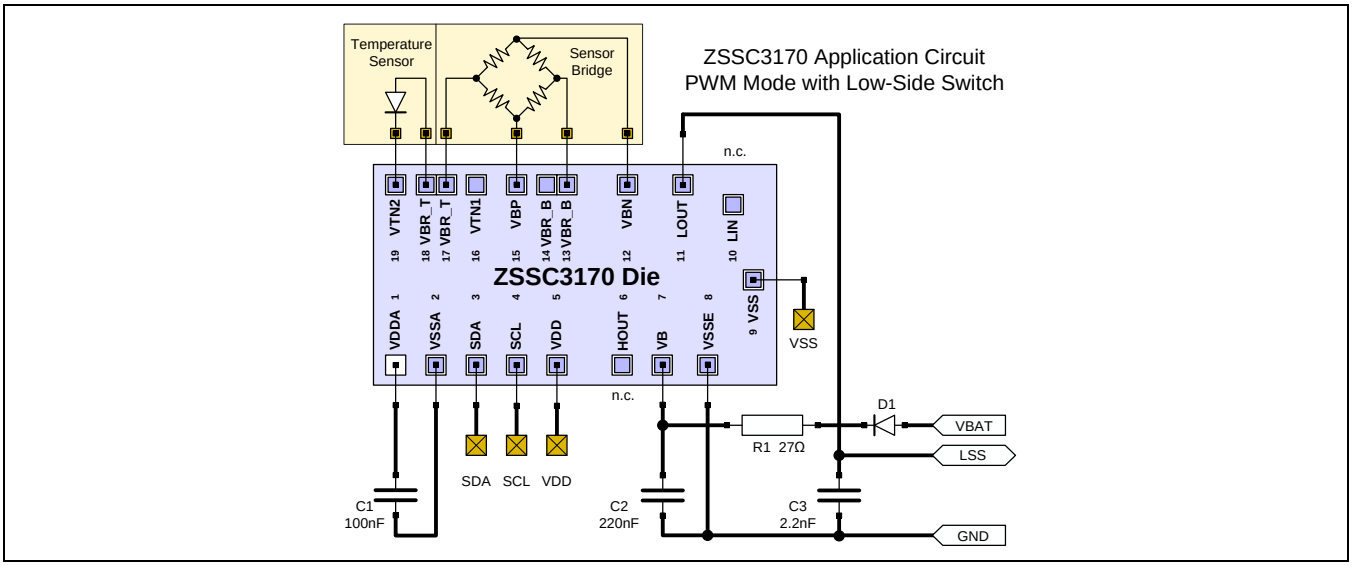


Figure 3.2 Application Circuit in PWM Mode with High-Side Switch

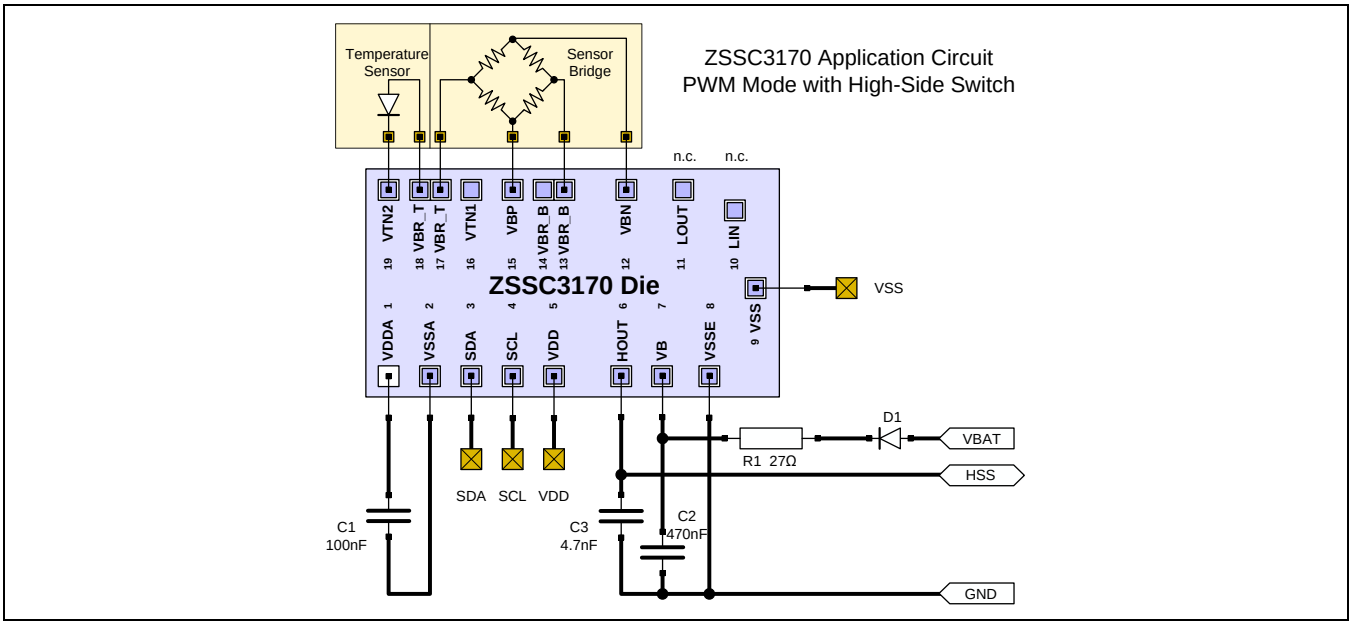
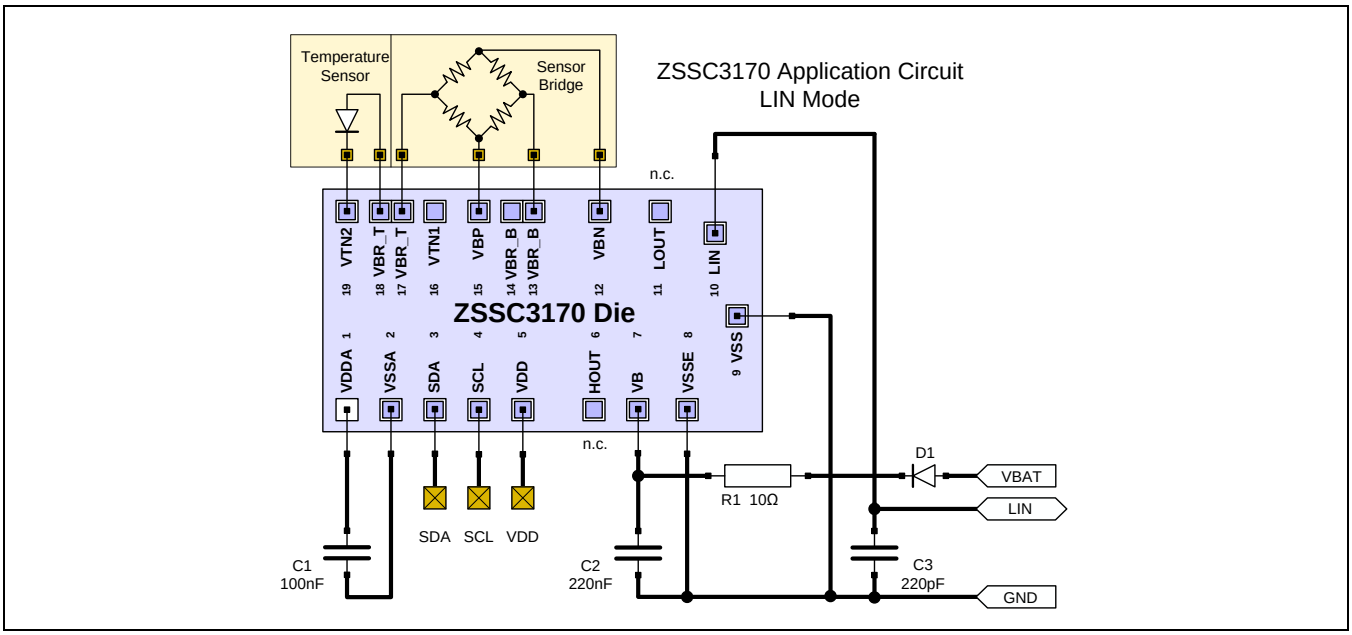


Figure 3.3 Application Circuit in LIN Mode



3.2 Dimensioning of External Components

For application circuits, refer to Figure 3.1, Figure 3.2, and Figure 3.3.

Table 3.1 Dimensioning of External Components for Application Examples

No.	Component	Symbol	Condition	Min	Typ	Max	Unit
3.2.1	Capacitor	C1	All modes		100		nF
3.2.2	Capacitor	C2	HSS		470		nF
3.2.3	Capacitor	C2	LSS, LIN		220		nF
3.2.4	Capacitor	C3	HSS		4.7		nF
3.2.5	Capacitor	C3	LSS		2.2		nF
3.2.6	Capacitor	C3	LIN		220		pF
3.2.7	Resistor	R1	LIN		10		Ω
3.2.8	Resistor	R1	LSS, HSS		27		Ω
3.2.9	Diode	D1	All modes		Standard Si diode		

The capacitor values are examples and must be adapted to the requirements of the specific application, in particular to the EMC requirements. In the LIN application, the voltage drop over the series connection of D1 and R1 must not exceed 1V at maximum supply current. For overvoltage pulses at VBAT, R1 serves as a current limiter.

4 Pinout and Package Options

4.1 Die Pad Definitions and Configuration

Table 4.1 Die Pad Definitions for ZSSC3170

Die Pad	Name	Description	Notes
1	VDDA	Positive Analog Supply Voltage	Power supply
2	VSSA	Negative Analog Supply Voltage	Ground
3	SDA	I²C™ Data I/O	Analog I/O, internal pull-up
4	SCL	I²C™ Clock	Analog input, internal pull-up
5	VDD	Positive Digital Supply Voltage	Power supply
6	HOUT	PWM High-Side Switch	High voltage I/O
7	VB	Positive External Supply Voltage	High voltage I/O
8	VSSE	External Ground (PWM Modes)	High voltage I/O
9	VSS	Ground (LIN Mode)	Ground
10	LIN	LIN	LIN high voltage I/O
11	LOUT	PWM Low-Side Switch	High voltage I/O
12	VBN	Negative Input Sensor Bridge	Analog input
13 / 14	VBR_B	Negative (Bottom) Bridge Supply Voltage	Analog I/O
15	VBP	Positive Input Sensor Bridge	Analog input
16	VTN1	Temperature Sensor 1	Analog I/O
17 / 18	VBR_T	Positive (Top) Bridge Supply Voltage	Analog I/O
19	VTN2	Temperature Sensor 2	Analog I/O

The two-fold implementation of the bridge supply bond pads enables direct bonding from the ZSSC3170 pads to supply pads on the sensor die. The backside of the die is electrically connected to the potential VSS and VSSA within the package.

For the die layout and exact bond pad positions, refer to the *ZSSC3170 Technical Note – Die Dimensions and Pad Coordinates.*

4.2 SSOP20 Package

An RoHs-compliant SSOP20 package (5.3mm body, 0.65mm lead pitch) is one of the two standard delivery forms available for packaged parts. Refer to the *ZSSC3170 Technical Note – SSOP20 and DFN20 Package Dimensions* for package dimensions, land patterns, and additional details.

Table 4.2 Pin Definition of SSOP20 Package

SSOP20 Pin	Name	Description	Notes
1	n.c.	No connection	
2	VDDA	Positive Analog Supply Voltage	Power supply
3	VSSA	Negative Analog Supply Voltage	Ground
4	SDA	I²C™ Data I/O	Analog I/O, internal pull-up
5	SCL	I²C™ Clock	Analog input, internal pull-up
6	VDD	Positive Digital Supply Voltage	Power supply
7	HOUT	PWM High-Side Switch	High voltage I/O
8	VB	Positive External Supply Voltage	High voltage I/O
9	VSSE	External Ground (PWM Modes)	High voltage I/O
10	VSS	Ground (LIN Mode)	Ground
11	LIN	LIN	LIN high voltage I/O
12	LOUT	PWM Low-Side Switch	High voltage I/O
14	VBN	Negative Input Sensor Bridge	Analog input
15	VBR_B	Negative (Bottom) Bridge Supply Voltage	Analog I/O
16	VBP	Positive Input Sensor Bridge	Analog input
17	VTN1	Temperature Sensor 1	Analog I/O
18	VBR_T	Positive (Top) Bridge Supply Voltage	Analog I/O
19	VTN2	Temperature Sensor 2	Analog I/O
20	n.c.	No connection	

4.3 DFN20 Package

An RoHs-compliant DFN20 package (6x5 mm body, 0.5mm lead pitch) with wettable flanks is one of the two standard delivery forms available for packaged parts. Refer to the *ZSSC3170 Technical Note – SSOP20 and DFN20 Package Dimensions* for package dimensions, land patterns, and additional details.

The pin definitions for the DFN20 package are the same as for the SSOP20 package described in Table 4.2.

5 ESD Protection and EMC Specification

All pins have an ESD protection of >2000V according to the Human Body Model (HBM). In addition, the pins VDDE, VSSE, VSS, HOUT, and LOUT have an ESD protection of >4000V and the pin LIN has an ESD protection of >8000V (system level).

The level of ESD protection has been tested with devices in SSOP20 packages during the product qualification. The ESD test follows the Human Body Model with 1.5kOhm/100pF based on MIL883, Method 3015.7 (except the LIN pin tests). The ESD test of the LIN pin follows the system level specification with 330Ω/150 pF (according to DIN EN 61000-4-2).

The EMC performance regarding external disturbances as well as EMC emission is documented in the *ZSSC3170 High Voltage Protection Description.*

6 Reliability and RoHS Conformity

The ZSSC3170 is qualified according to the AEC-Q100 standard, operating temperature grade 0.

The ZSSC3170 complies with the RoHS directive and does not contain hazardous substances.

7 Ordering Information

Product Sales Code	Description	Package
ZSSC3170FE1B	ZSSC3170 Die Revision F — Temperature range: -40°C to +150°C	Unsawn on Wafer, 2450 pcs.
ZSSC3170FE1C	ZSSC3170 Die Revision F — Temperature range: -40°C to +150°C	Sawn on Wafer Frame, 2450 pcs.
ZSSC3170FE2R	ZSSC3170 SSOP20 Revision F — Temperature range: -40°C to +150°C	13” Reel, 2000 pcs.
ZSSC3170FE2T	ZSSC3170 SSOP20 Revision F — Temperature range: -40°C to +150°C	Tube, 660 pcs.
ZSSC3170EE1B	ZSSC3170 Die Revision E — Temperature range: -40°C to +150°C	Unsawn on Wafer, 2450 pcs.
ZSSC3170EE1C	ZSSC3170 Die Revision E — Temperature range: -40°C to +150°C	Sawn on Wafer Frame, 2450 pcs.
ZSSC3170EE2R	ZSSC3170 SSOP20 Revision E — Temperature range: -40°C to +150°C	13” Reel, 2000 pcs.
ZSSC3170EE2T	ZSSC3170 SSOP20 Revision E — Temperature range: -40°C to +150°C	Tube, 660 pcs.
ZSSC3170EE3R	ZSSC3170 DFN20 Revision E — Temperature Range -40°C to +150°C	13” Reel, 4500 pcs.
ZSSC3170EA1B	ZSSC3170 Die Revision E — Temperature range: -40°C to +125°C	Unsawn on Wafer, 2450 pcs.
ZSSC3170EA1C	ZSSC3170 Die Revision E — Temperature range: -40°C to +125°C	Sawn on Wafer Frame, 2450 pcs.
ZSSC3170EA2R	ZSSC3170 SSOP20 Revision E — Temperature range: -40°C to +125°C	13” Reel, 2000 pcs.
ZSSC3170EA2T	ZSSC3170 SSOP20 Revision E — Temperature range: -40°C to +125°C	Tube, 660 pcs.
ZSSC3170EA3R	ZSSC3170 DFN20 Revision E — Temperature Range -40°C to +125°C	13” Reel, 4500 pcs.
ZSSC3170KIT	ZSSC3170 Evaluation Kit and 5 SSOP20 Samples	Kit

8 Related Documents

Document
ZSSC3170 Evaluation Kit Description
ZSSC3170 Functional Description
ZSSC3170 Application Note – LIN and PWM Operation
ZSSC3170 Technical Note – SSOP20 and DFN20 Package Dimensions
ZSSC3170 High Voltage Protection Description
ZSSC3170 LIN Interface Description
*ZSSC3170 Technical Note – Die Dimensions and Pad Coordinates **

Visit the ZSSC3170 product page www.IDT.com/ZSSC3170 or contact your nearest sales office for the latest version of these documents.

* Note: Documents marked with an asterisk (*) are available on request only.

9 Glossary

Term	Description
ADC	Analog-to-Digital Converter
AEC	Automotive Electronics Council
AFE	Analog Front-End
Amp	Amplifier
BCC	Broken Chip Check (diagnostic task)
CM	Command Mode
CMC	Calibration Micro Controller (optimized micro controller architecture for IDT signal conditioners)
CMV	Common Mode Voltage (of the sensor bridge signal)
DM	Diagnostic Mode
DNL	Differential Nonlinearity
EEPROM	Electrically Erasable Programmable Read Only Memory
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FSO	Full Scale Output
HSS	High-Side Switch (open-drain output; connects to positive supply when active)
I/O	Input/Output
I²C	Inter-Integrated Circuit (serial two-wire data bus, trademark of NXP.)

Term	Description
INL	Integral Nonlinearity
LIN	Local Interconnect Network (international communication standard)
LSB	Least Significant Bit
LSS	Low-Side Switch (open-drain output; connects to ground when active)
MSB	Most Significant Bit
MUX	Multiplexer
NOM	Normal Operation Mode
P	Bridge Sensor Signal (e.g., pressure)
PGA	Programmable Gain Amplifier
POR	Power-On Reset (defined start-up procedure until nominal supply voltage is reached)
PWM	Pulse Width Modulation
Rev.	Revision
RISC	Reduced Instruction Set Computing
RoHS	Restrictions of Hazardous Substances
ROM	Read Only Memory
RTD	Resistance Temperature Detector
SAC	Sensor Aging Check (diagnostic measurement task)
SCC	Sensor Connection Check (diagnostic measurement task)
SSC	Sensor Short Check (diagnostic measurement task); Sensor Signal Conditioner
T	Temperature
XZC	Extended Zero Compensation (bridge sensor offset compensation)

10 Document Revision History

Revision	Date	Description
1.00	April 5, 2009	First release.
1.30	September 20, 2010	Full revision.
2.00	January 17, 2011	Silicon revision from C to D. Minor edits.
2.10	April 4, 2013	Silicon revision from D to E. Update for contact information and imagery on cover and headers. Minor edits.
2.20	July 5, 2013	SSOP20 is now only available for evaluation purposes as samples in the Evaluation Kit.
2.30	September 16, 2013	Revision to recommendation in footnote 1 in Table 2.2. PWM operation and LIN Sleep mode incompatibility note added in section 2.6. Waffle pack option is no longer available; removed from part order table (ZSSC3170EE1D and ZSSC3170EA1D). References to SSOP20 package for samples removed. Minor edits for clarity.
2.40	January 22, 2014	SSOP20 is now available again. Update for imagery for cover.
2.50	December 10, 2014	DFN20 package added. Update for Table 1.2 conditions for specification 1.2.4. Update for external temperature resistor input range specification 1.3.3.5. Correction for Table 4.2. Update for block diagram on page 3 and in Figure 2.1. Contact information and related documents section updated.
2.51	November 4, 2015	Table note 2 added for specifications 1.3.4 and 1.3.6 of Table 1.3. Revisions in section 2.8 for new silicon revision F. Ordering information in section 7 updated to add part numbers ZSSC3170FE1B and ZSSC3170FE1C. Moved content for SSOP20 and DFN20 package drawings to new separate document: *ZSSC3170 Technical Note – SSOP20 and DFN20 Package Dimensions.* Addition of AEC-Q100 information on page 2. Minor edits and updates for related documents section.
160118	January 18, 2016	Changed to IDT branding.
160530	May 30, 2016	Added revision F for SSOP20 tube and reel part codes in order information table.