National Semiconductor

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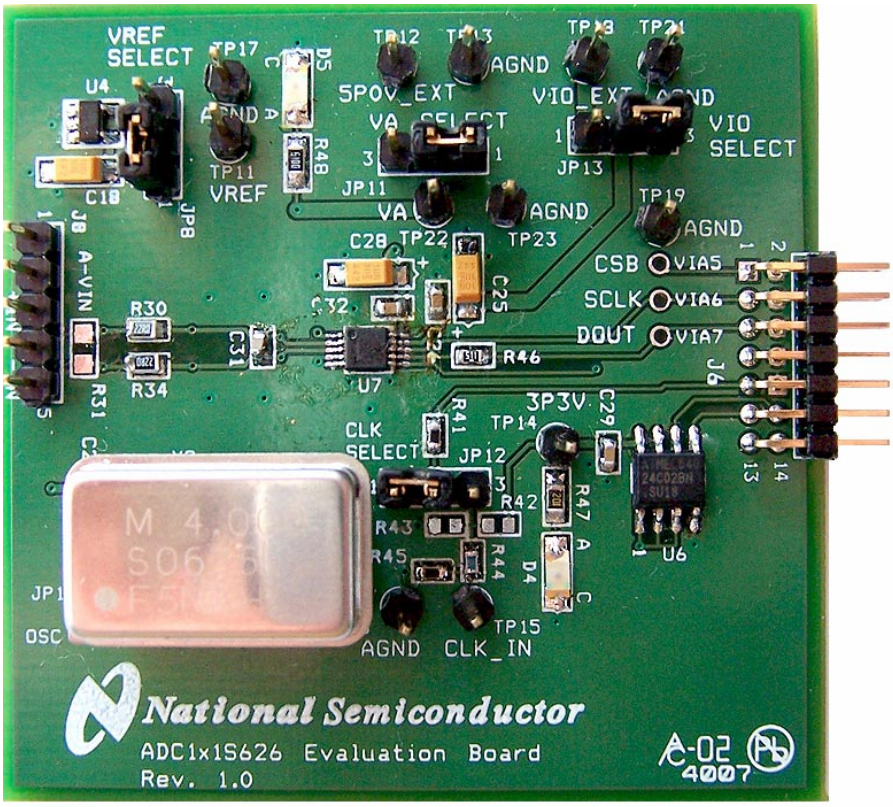
RoHS Compliant

Evaluation Board User's Guide

ADC141S626 14-Bit, 50 kSPS to 250 kSPS, Differential Input, Micro-Power Sampling A/D Converter



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1. Introduction

The ADC141S626EB/RoHS Design Kit (consisting of the ADC141S626 Evaluation Board and this User's Guide) is designed to ease evaluation and design-in of the National Semiconductor ADC141S626 14-bit Analog-to-Digital Converter, which can operate at speeds up to 250 kSPS.

The evaluation board can be used in either the 'Stand-Alone mode' or the 'Computer mode'. In the 'Stand-Alone mode', suitable test equipments, such as a logic analyzer, can be used with the board to evaluate the ADC141S626's performance.

In the 'Computer mode', data capture and evaluation are simplified by connecting this evaluation board to National Semiconductor's WaveVision Data Capture (WV) board, which is connected to a personal computer through a USB port and is running WaveVision software. WV board 4.1 or higher and WaveVision software version 4.4 or higher are necessary to interface the ADC141S626 Evaluation Board in 'Computer mode'. The hardware can be purchased and the software and can be downloaded for free from the web at http://www.national.com/appinfo/adc/wv4.html

The WaveVision software operates under Microsoft Windows. The signal at the Analog Input is digitized, captured, and displayed on a PC monitor in the time and frequency domain.

The software will perform an FFT on the captured data upon command. This FFT plot shows dynamic performance in the form of SNR, SINAD, THD, SFDR and ENOB. A histogram of the captured data is also available.

The differential signal applied across analog inputs J8.P3 and J8.P5 is digitized by U7, the ADC141S626.

The ADC141S626 uses an oscillator that is provided on this board by Y2 or is supplied at TP15.

2. Board Assembly

The ADC141S626 evaluation board comes fully assembled and ready for use. Refer to the Bill of Materials on page 14 for a description of components, to Figure 1 for major component placement, and to the schematic on page 13.

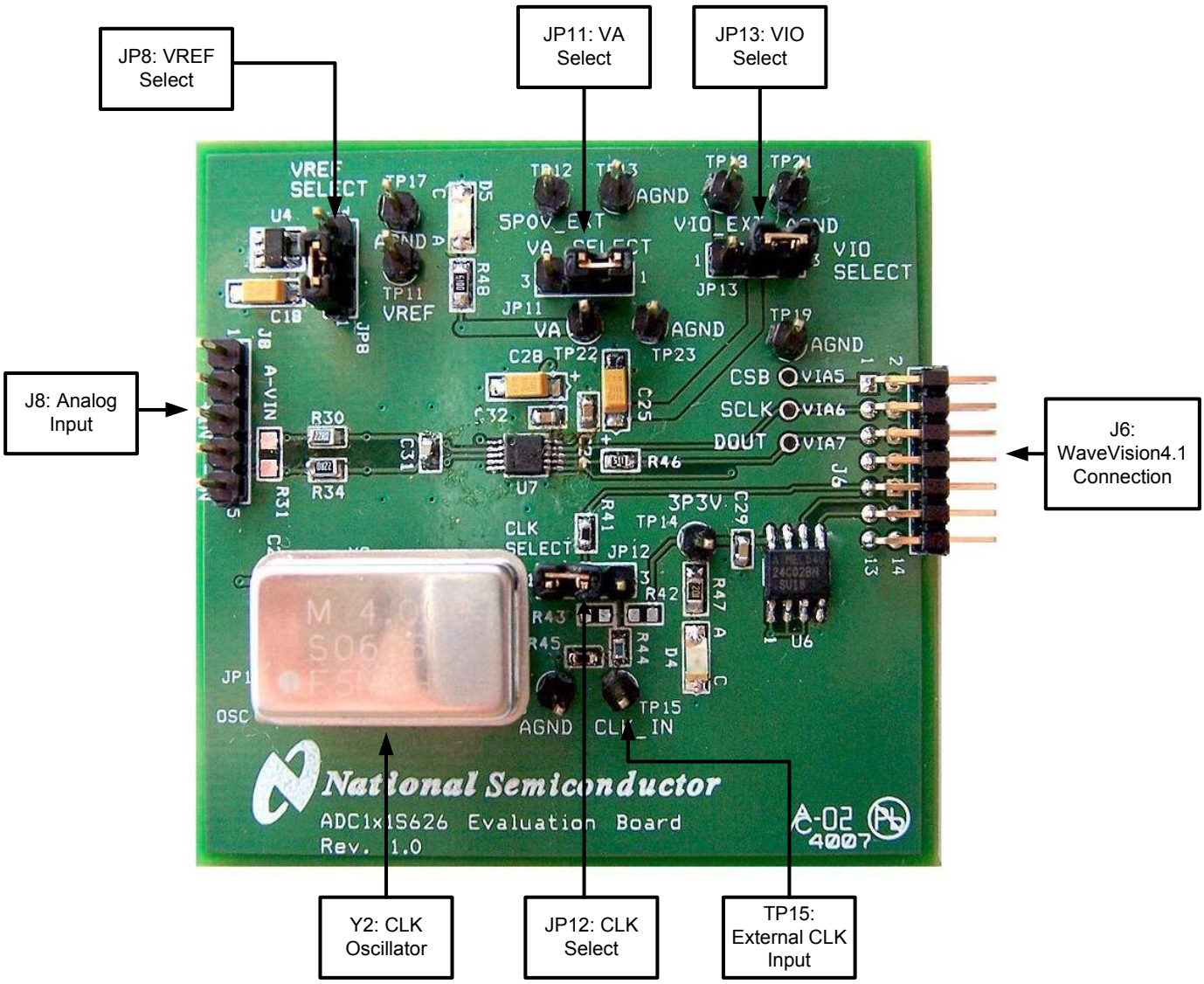


Figure 1 – Components Locations

3. Quick Start

The ADC141S626 evaluation board may be used in the 'Stand-Alone mode' to capture data with a logic analyzer or other suitable test equipment, or it may be used in the 'Computer mode' with the WV board. In both cases, the data may be analyzed with the WaveVision software.

3.1 Stand Alone Mode

Refer to Figure 1 for locations of test points and major components.

1. Connect a desired differential input signal across pins 3 and 5 of J8.

a. To create an ac-coupled input signal, stuff C21 and C22 with 1 uF capacitors but leave R30 and R34 unpopulated. To shift the input signal above ground, stuff R27, R28, R29, and R33 with 4.99k Ω resistors. Figure 2 shows the schematic for driving for ADC input with an ac-coupled signal.

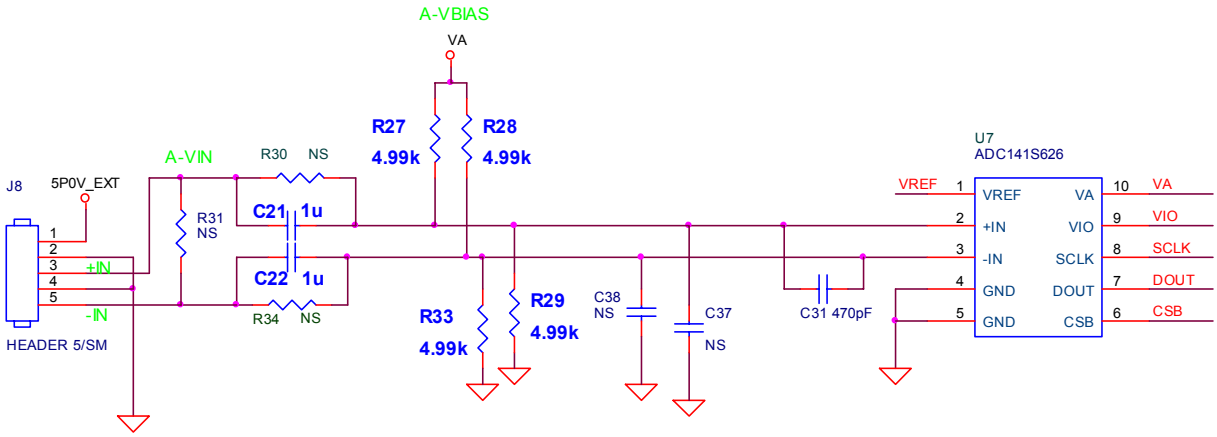


Figure 2 – Schematic to Drive ADC with an AC-Coupled Input Signal

b. To create a dc-coupled input signal, stuff R30 and R34 with 20 Ω resistors but leave C21, C22, R27, R28, R29, and R33 unpopulated. Figure 3 shows the schematic for driving the ADC input with a dc-coupled signal.

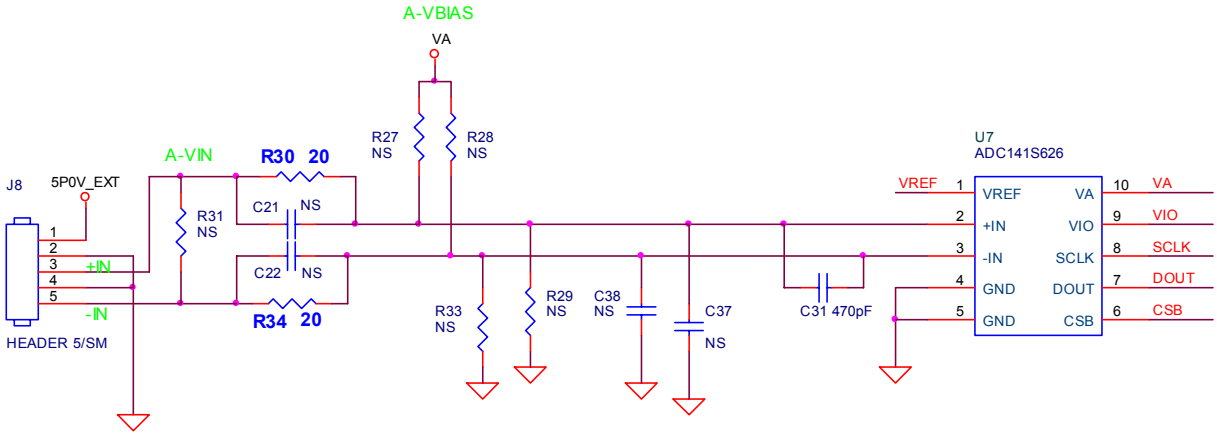


Figure 3 – Schematic to Drive ADC with a DC-Coupled Input Signal

2. Short pins 2 and 3 of JP11 to bias VA (analog voltage) via an external source. In this case, connect a clean +2.7 V to +5.5 V power supply to TP12 and AGND.
3. There are three ways to bias the reference voltage VREF. Choose one of the following:
   a. Short pins 1 and 2 of JP8 to use VA to bias VREF.
   b. Short pins 2 and 3 of JP8 to use the 4.1V Reference Voltage (LM4132-4.1) to bias VREF.
   c. Supply a voltage less than or equal to VA at TP11 to source VREF externally. In this case, remove the jumper from JP8.

4. There are two ways to bias the input/output driver voltage VIO. Choose one of the following:
   a. Short pins 1 and 2 of JP13 to use an external source to bias VIO. In this case, connect a clean +2.7 V to +5.5 V power supply to TP18 and AGND.
   b. Short pins 2 and 3 of JP13 to use VA to bias VIO.
5. Remove the jumper from JP12 and the oscillator Y2 from its socket. The presence of Y2 could add noise to the sampling process.
6. Apply signals to control the SPI interface.
   a. Use a Logic Analyzer or other suitable test equipment to drive CSB (via 5 or pin 1 of J6) and SCLK (via 6 or pin 2 of J6). Refer to the ADC141S626 datasheet to correctly drive these pins.
   b. Monitor DOUT at via 7 or pin 5 of J6 using a Logic Analyzer or a similar test equipment.

   Note: Vias 5, 6, and 7 are 100 mil spaced apart.

3.2 Computer Mode

Refer to Figure 1 for locations of test points and major components.

1. Source the WV board with a clean +5 V supply and connect the ADC141S626 Evaluation Board to the WV board via J6. Visit http://www.national.com/appinfo/adc/wv4.html for more information on the WV board and its configuration.
2. Run the WaveVision software program (http://www.national.com/appinfo/adc/wv4.html). Version 4.4 or higher is required to interface the WV board with the ADC141S626 Evaluation Board. While the program is loading, continue below.
3. Connect a desired differential input signal across pins 3 and 5 of J8.
   a. To create an ac-coupled input signal, stuff C21 and C22 with 1 uF capacitors but leave R30 and R34 unpopulated. To shift the input signal above ground, stuff R27, R28, R29, and R33 with 4.99k Ω resistors. The schematic for this mode can be seen in figure 2.
   b. To create a dc-coupled input signal, stuff R30 and R34 with 20 Ω resistors but leave C21, C22, R27, R28, R29, and R33 unpopulated. Refer to figure 3 for the schematic.
4. There are two ways to bias the analog voltage VA. Choose one of the following:
   a. Short pins 1 and 2 of JP11 to bias VA via the +5.0V from the WV board.
   b. Short pins 2 and 3 of JP11 to bias VA (analog voltage) via an external source. In this case, connect a clean +2.7 V to +5.5 V power supply to TP12 and AGND.
5. There are three ways to bias the reference voltage VREF. Choose one of the following:
   c. Short pins 1 and 2 of JP8 to use VA to bias VREF.
   d. Short pins 2 and 3 of JP8 to use the 4.1V Reference Voltage (LM4132-4.1) to bias VREF.

e. Supply a voltage less than or equal to VA at TP11 to source VREF externally. In this case, remove the jumper from JP8.

6. There are two ways to bias the input/output driver voltage VIO. Choose one of the following:
   a. Short pins 1 and 2 of JP13 to use an external source to bias VIO. In this case, connect a clean +2.7 V to +5.5 V power supply to TP18 and AGND.
   b. Short pins 2 and 3 of JP13 to use VA to bias VIO.
7. There are two ways to select a clock source. Choose one of the following:
   a. Short pins 1 and 2 of JP12 to use an external crystal oscillator. Then, install an appropriate crystal oscillator into socket Y2.
   b. Short pins 2 and 3 of JP12 to use a signal generator as an oscillator. Connect a clean signal generator with 3.3 V CMOS logic levels to TP15 and AGND. Remember not to place any crystal oscillator into socket Y2.
8. After configuring the ADC141S626 Evaluation board and connecting the board to the WV board, refer to section 5 - Software Operation and Settings to use the WaveVision software program to analyze the ADC141S626.

4. Functional Description

Table I describes the functions of the jumpers on the ADC141S626 Evaluation Board. The board schematic is shown on page 11.

Jumper	Name	Pins 1 & 2	Pins 2 & 3
JP8	VREF	Select VA to source VREF	Select +4.1V Voltage Regular (U4) to source VREF
JP11	VA	Select +5.0V from the WV board to source VA.	Select an external power supply to source VA.
JP12	CLK	Select on-board clock OSC Y2.	Select clock OSC at TP15.
JP13	VIO	Select an external power supply to source VIO.	Select VA to source VIO.

Table I – Jumper Functions

4.1 Analog Input Signal

The ADC141S626 has dual differential inputs as shown in figure 4. The signal to be digitized should be applied across pins 3 and 5 of J8.

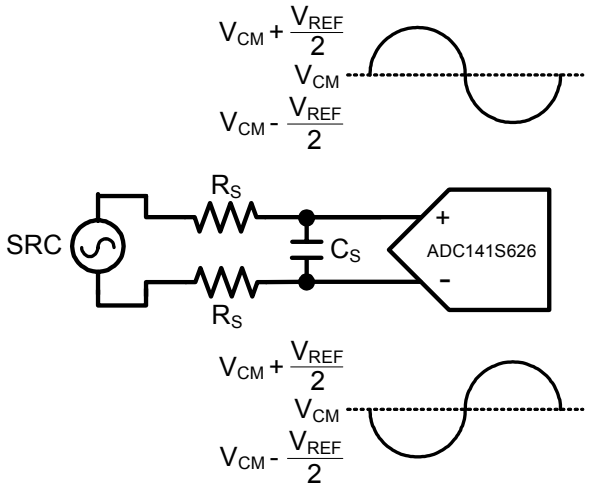


Figure 4 – Differential Input

Generating an ac-coupled input signal only requires stuffing capacitors C21 and C22 with 1uF capacitors. For signal generators that do not have an offset function, stuff resistors R27, R28, R29, and R33 with 4.99k Ω resistors to shift the ac-coupled input signal above ground. Leave resistors R30, R34, and capacitors C37 and C38 unpopulated. Refer to figure 2 to see the schematic for driving the ADC input with an ac-coupled signal.

To properly create a dc-coupled input signal, stuff R30 and R34 with 20 Ω resistors. However, leave capacitors C21, C22, and resistors R27, R28, R29, and R33 unpopulated. A schematic of this explanation can be seen in figure 3.

For single-ended operation, the non-inverting input of the ADC can be driven with a sinusoidal input signal, and the inverting input of the ADC can be driven with a dc voltage. The sinusoidal input signal driving the non-inverting input should have a minimum to maximum value range that is equal to or less than twice the reference voltage. The inverting input should be biased at a common mode voltage, VCM, which is a stable voltage that is halfway between these maximum and minimum values. Figure 5 shows the ADC141S626 being driven by a single-ended source.

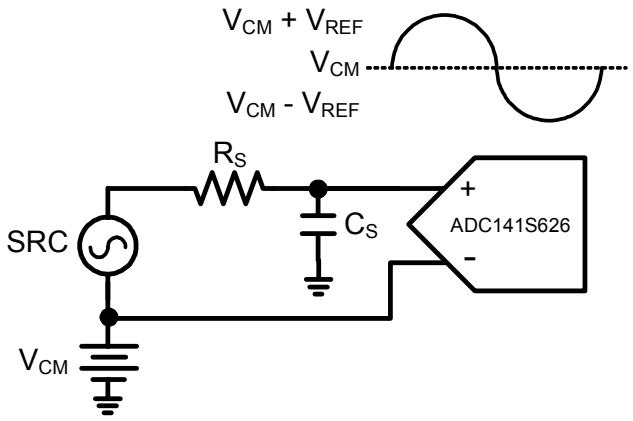


Figure 5 – Single-Ended Input

Dynamic input signals should be applied through a lowpass or bandpass filter to eliminate the noise and harmonics commonly associated with signal sources. To accurately evaluate the performance of the ADC141S626, the source must be better than -100dBFS THD (Total Harmonic Distortion).

4.2 ADC Reference Circuitry

This evaluation board includes three options to source the voltage reference, VREF. These options include selecting a fixed +4.1V voltage reference to source VREF, using VA to source VREF, or using a power supply to source VREF. To select the +4.1V reference, short pins 2 & 3 of JP8. To select VA, short pins 1 & 2 of JP8. If it is desirable to provide an external reference voltage, the jumper must be removed from JP8, and TP11 may be driven directly by a power supply set between +2.7 V and +5.5 V.

4.3 SPI Interface

The ADC141S626 requires three SPI input and output pins. These pins are Serial Clock (SCLK), Chip Select Bar (CSB), and Digital Data Output (DOUT). The user must provide input signals for SCLK and CSB in order to receive an output signal DOUT from the ADC141S626. Further descriptions of those pins are discussed below.

4.3.1 Serial Clock (SCLK)

The crystal-based oscillator provided on the evaluation board is selected by shorting pins 1 & 2 of JP12. It is best to remove any external signal generator from TP15 when using this oscillator to reduce any unnecessary noise.

This board will also accept a clock signal from an external source by connecting that source to TP15 and AGND and shorting pins 2 & 3 of JP12. The input applied at TP15 is 51 ohm terminated by R45. The external clock signal must meet the 3.3 V CMOS input requirements. If the external source is an ac-source centered around ground, populate R42 and R43 with 4.99k Ω resistors to shift the clock level. To reduce any unnecessary noise, it is best to remove the oscillator at Y2 when using an external clock source.

Regardless of the clock source selected by JP12, the clock signal is designed to be routed off the ADC141S626 Evaluation Board to the WV board. This assumes a 'Computer mode' operation of the evaluation board. For applications utilizing the evaluation board in 'Stand-Alone mode', the clock is applied directly at via 6 or at pin 3 of J6.

4.3.2 Chip Select Bar (CSB)

In the 'Stand-Alone mode', CSB has to be driven directly at via 5 or at pin 1 of J6. In the 'Computer mode', CSB can be monitored at via 5 or at pin 1 of J6. The signal level for CSB needs to be TTL compatible. See the ADC141S626 datasheet for logic threshold limits.

4.3.3 Digital Data Output (DOUT)

In the 'Stand-Alone mode', DOUT can be monitored at via 7 or at pin 5 of J6. In the 'Computer mode', DOUT is monitored by the WV board. The signal level for DOUT is CMOS and TTL compatible. See the ADC141S626 datasheet for logic output levels.

4.4 Power Supply Connection

Voltages VA and VIO can be driven using an external power supply.

In the 'Stand-Alone mode', the user has to use the external power supply to drive VA. Do not short pins 1 and 2 of JP11 when operating in the 'Stand-Alone mode'. To drive VA correctly, short pins 2 and 3 of JP11, and drive TP12 with an external power supply set between +2.7 V and +5.5 V.

In the 'Computer mode', VA can be driven with an external power supply or with the +5.0V from WV board. Short pins 1 and 2 of JP11 to automatically use the +5.0 V from the WV board.

The driver input/output voltage VIO can also be driven from VA or externally with a power supply. To use the voltage VA to drive VIO, short pins 2 and 3 of JP13. To drive VIO with an external source, short pins 1 and 2 of JP13, then set TP18 to a voltage between +2.7 V and +5.5V.

5. Software Operation and Settings

The WaveVision software is included with the WV board and the latest version can be downloaded for free from National's web site at http://www.national.com/appinfo/adc/wv4.html. To install this software, follow the procedure in the WV board User's Guide. Once the software is installed, run and set it up as follow:

1. After configuring the ADC141S626 Evaluation Board and connecting it to the WV board as discussed in Section 3.2, connect the WV board to the host computer with a USB cable.
2. From the WaveVision software main menu, go to '**Settings'**, then '**Capture Settings'** and select the following from the menu:
   a. Board Type: WaveVision 4.0 (USB)
   b. Number of Samples: 2k to 32k, as desired
   c. Data Format: Two's Complement
3. Click on the **"Reset"** button and await the firmware to download.
4. Click on the **"Close"** button.
5. Click on **"Acquire"** then **"Samples"** from the Main Menu (you can also press the *F1* shortcut key). If a dialog box opens, select **"Discard"** or press the ***Escape*** key to start collecting new, updated samples.

A plot of the selected number of samples will be displayed. Make sure there is no clipping of data samples. If clipping occurs, lower the analog input voltage. The samples may be further analyzed by clicking on the magnifying glass icon, then clicking and dragging across a specific area of the plot for better data inspection.

To view an FFT of the data captured, click on the 'FFT' tab. This plot may be zoomed in like the data plot. A display of dynamic performance parameters in the form of SINAD, SNR, THD, SFDR and ENOB will be displayed at the top right hand corner of the FFT plot.

Acquired data may be saved to a file. Plots may also be exported as graphics.

For more information, view the WV board's User Guide at
http://www.national.com/appinfo/adc/wv4.html.

6. Evaluation Board Specifications

Board Size:	2.250" x 2.3" (7.6 cm x 7.6 cm)	
Power Requirements	Min: +2.7 V, 100mA	Max: +5.5 V, 100 mA
Clock Frequency Range:	800 kHz to 4.0 MHz	
Analog Input	0 V to (2 * VREF) Vpp	

Table II – ADC141S626 Evaluation Board Specifications

7. Tables of Test Points, Jumpers, and Connectors

Test Points on the ADC141S626 Evaluation Board

TP11: VREF	VREF test point. Located at the top left area of the board.
TP12: 5P0V_EXT	VA external supply. Located at the middle top area of the board.
TP13: AGND	Ground. Located at the middle top area of the board.
TP14: 3P3V	+3.3V test point. Located at the middle right area of the board.
TP15: CLK_IN	External Clock. Located at the bottom middle of the board.
TP16: AGND	Ground. Located at the bottom middle of the board.
TP17: AGND	Ground. Located at the top left area of the board.
TP18: VIO_EXT	VIO external supply. Located at the top right corner of the board.
TP19: AGND	Ground. Located at the top right corner of the board.
TP21: AGND	Ground. Located at the top right corner of the board.
TP22: VA	VA test point. Located at the middle top area of the board.
TP23: AGND	Ground. Located at the middle top area of the board.

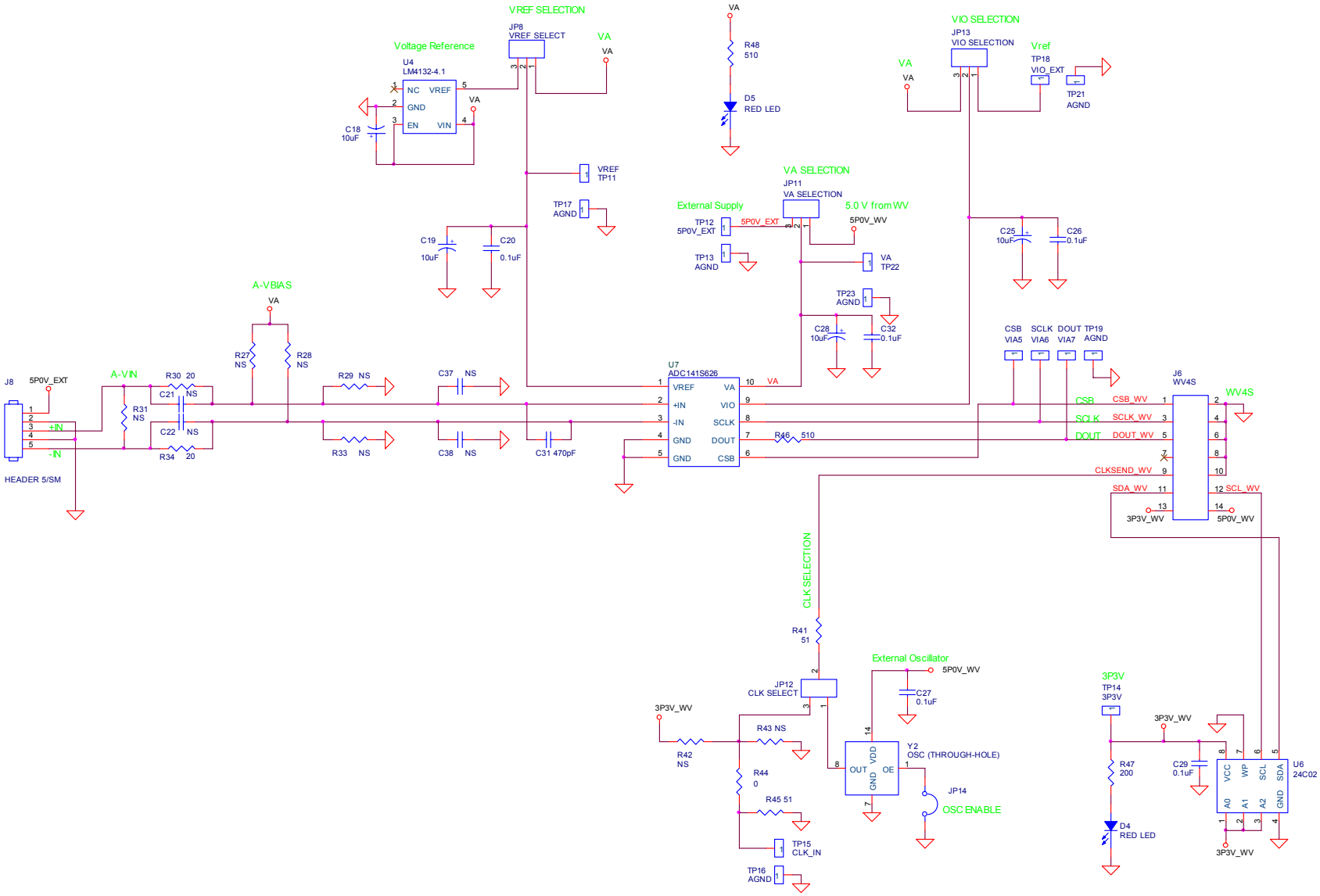
Connectors on the ADC141S626 Evaluation Board

J6: WV4S	14 pin dual row right angle male header. Connect to WV board.
J8: VIN	Five pin male header. Differential AC and DC input.

Selection Jumpers on the ADC141S626 Evaluation Board (Refer to Table 1 in Section 4.0 for configuration details)

JP8: VREF SELECT	Selects reference source for VREF. Located at the top left corner of the board.
JP11: VA SELECT	Selects source for VA. Located at the top middle area of the board.
JP12: CLK SELECT	Selects source for the clock. Located at the bottom middle area of the board.
JP13: VIO SELECT	Selects source for VIO. Located on the top right corner of the board.
JP14: OSC Enable	Not Stuffed. If jumpered, pin 1 of the oscillator is grounded. Located on the bottom left corner of the board to the left of Y2.

8. Hardware Schematic



9. ADC141S626 Evaluation Board Bill of Materials

Item	Qunty	Reference	Part	Source	Source Part #
1	4	C18,C19,C25,C28	10uF	N/A	N/A
2	5	C20,C26,C27,C29,C32	0.1uF	N/A	N/A
3	2	C21,C22	Not Stuffed (1uF)	N/A	N/A
4	1	C31	470pF	N/A	N/A
5	2	C37,C38	Not Stuffed (0.1uF)	N/A	N/A
6	2	D4,D5	RED LED	Digikey	516-1440-1-ND
7	1	JP8	3-Pin Post Header	Digikey	S1011E-36-ND
8	1	JP11	3-Pin Post Header	Digikey	S1011E-36-ND
9	1	JP12	3-Pin Post Header	Digikey	S1011E-36-ND
10	1	JP13	3-Pin Post Header	Digikey	S1011E-36-ND
11	1	JP14	Not Stuffed (Jumper)	N/A	N/A
12	1	J6	RIGHT ANGLE MALE HEADER 100Mil	Digikey	S5803-21-ND
13	1	J8	HEADER 5/SM	N/A	N/A
14	6	R27,R28,R29,R33,R42,R43	Not Stuffed (4.99k ohm)	N/A	N/A
15	2	R30,R34	20	N/A	N/A
16	1	R31	Not Stuffed	N/A	N/A
17	2	R41, R45	51	N/A	N/A
18	1	R44	0	N/A	N/A
20	1	R47	200	N/A	N/A
21	1	R48	510	N/A	N/A
22	1	R46	510	N/A	N/A
23	1	TP11	Test Pin for VREF	Digikey	5003K-ND
24	1	TP12	Test Pin for 5P0V_EXT	Digikey	5003K-ND
25	6	TP13,TP16,TP17,TP19,TP21,TP23	Test Pin for AGND	Digikey	5011K-ND
26	1	TP14	Test Pin for 3P3V	Digikey	5003K-ND
27	1	TP15	Test pin for CLK_IN	Digikey	5003K-ND
28	1	TP18	Test Pin for VIO_EXT	Digikey	5003K-ND
29	1	TP22	Test pin for VA	Digikey	5003K-ND
30	1	U4	LM4132-4.1	N/A	N/A
31	1	U6	24C02	N/A	N/A
32	1	U7	ADC141S626	N/A	N/A
33	1	VIA5	CSB	Digikey	N/A
34	1	VIA6	SCLK	Digikey	N/A
35	1	VIA7	DOUT	Digikey	N/A
36	1	Y2	OSC (THROUGH-HOLE)	Digikey	A400-ND

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