

Application Manual

RV-3028-C7

Extreme Low Power Real-Time Clock Module with I²C-Bus Interface

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RV-3028-C7

Extreme Low Power Real-Time Clock (RTC) Module with I²C-Bus Interface

1. OVERVIEW

- RTC module with built-in 32.768 kHz “Tuning Fork” crystal oscillator
- Counters for seconds, minutes, hours, date, month, year and weekday
- 32-bit UNIX Time counter
- Automatic leap year correction: 2000 to 2099
- Aging compensation with user programmable EEPROM Offset value (Factory Calibrated value may be changed by the user)
- Periodic Countdown Timer Interrupt function; interrupt output also in VBACKUP Power state
- Periodic Time Update Interrupt function (seconds, minutes); interrupt output also in VBACKUP Power state
- Alarm Interrupts for weekday or date, hour and minute settings; interrupt output also in VBACKUP Power state
- External Event Input with Interrupt and Time Stamp function; interrupt output also in VBACKUP Power state
- Factory calibrated time accuracy: ± 1 ppm @ 25°C (EEPROM Offset value may be changed by the user)
- 32.768 kHz Xtal oscillator frequency accuracy: ± 5 ppm @ 25°C
- 43 bytes of user EEPROM
- Configuration registers stored in EEPROM and mirrored in RAM
- User programmable password for write protection of the time, control and configuration registers
- I²C-bus interface (up to 400 kHz)
- Programmable Clock Output
 - Enable/disable by CLKOE bit
 - Enable by an Interrupt function
 - 32.768 kHz, 8192 Hz, 1024 Hz, 64 Hz, 32 Hz, 1 Hz
 - Periodic countdown timer interrupt as clock output frequency
 - Synchronized enable/disable
- Automatic Backup switchover with Interrupt and Time Stamp function
- Internal Power On Reset (POR) with Interrupt function
- Trickle charger
- Wide Timekeeping voltage range: 1.1 to 5.5 V
- Wide interface operating voltage: 1.2 to 5.5 V
- Extreme low current consumption: 45 nA ($V_{DD} = 3.0$ V, $T_A = 25^\circ\text{C}$)
- Operating temperature range: -40 to +85°C
- Ultra small and compact C7 package size (3.2 x 1.5 x 0.8 mm), RoHS-compliant and 100% lead-free
- Automotive qualification according to AEC-Q200 available

1.1. GENERAL DESCRIPTION

The RV-3028-C7 is a CMOS real-time clock/calendar module with an automatic backup switchover circuit and is optimized for extreme low power consumption. It provides full RTC function with programmable counters, alarm, selectable interrupt and clock output functions and also a 32-bit UNIX Time counter. The internal EEPROM memory hosts all configuration settings and allows for additional user memory. An EEOffset value allows compensating the frequency deviation of the 32.768 kHz clock. Addresses and data are transmitted via an I²C-bus interface for communication with a host controller. The Address Pointer is incremented automatically after each written or read data byte.

This ultra small RTC module has been specially designed for miniature and cost sensitive high volume applications.

1.2. APPLICATIONS

The RV-3028-C7 RTC module combines key functions with outstanding performance in an ultra small ceramic package:

- Extreme Low Power consumption
- Smallest RTC module (embedded XTAL) in an ultra-small 3.2 x 1.5 x 0.8 mm lead-free ceramic package

These unique features make this product perfectly suitable for many applications:

- Communication: IoT / Wearables / Wireless Sensors and Tags / Handsets
- Automotive: M2M / Navigation & Tracking Systems / Dashboard / Tachometers / Engine Controller
Car Audio & Entertainment Systems
- Metering: E-Meter / Heating Counter / Smart Meters / PV Converter/ Utility metering
- Outdoor: ATM & POS systems / Surveillance & Safety systems / Ticketing Systems
- Medical: Glucose Meter / Health Monitoring Systems
- Safety: Security & Camera Systems / Door Lock & Access Control / Tamper Detection
- Consumer: Gambling Machines / TV & Set Top Boxes / White Goods
- Automation: PLC / Data Logger / Home & Factory Automation / Industrial and Consumer Electronics

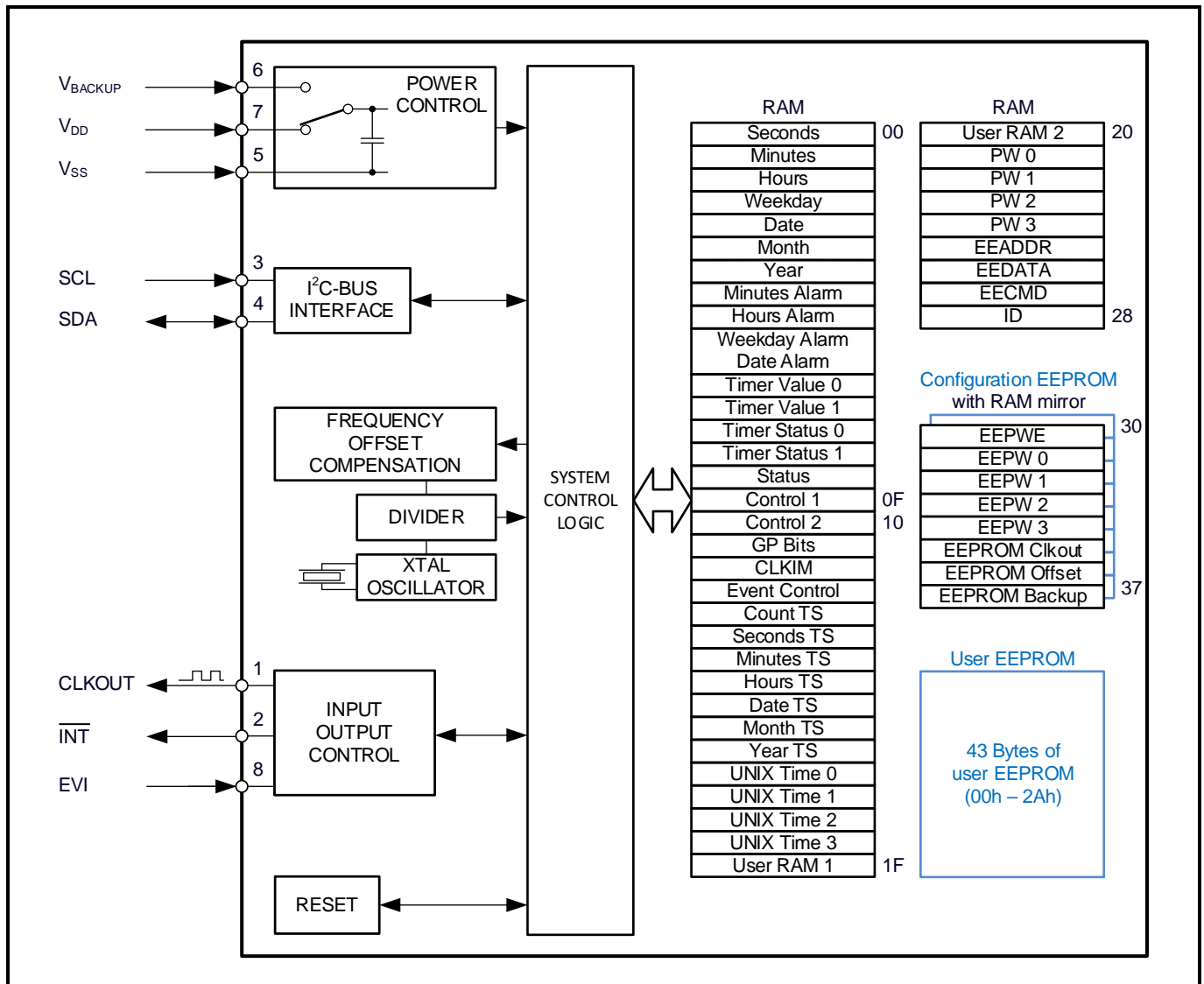
1.3. ORDERING INFORMATION

Example: RV-3028-C7 TA QC

| Code | Operating temperature range |
|---------------|-----------------------------|
| TA (Standard) | -40 to +85°C |

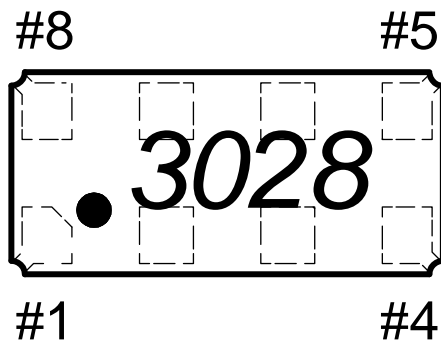
| Code | Qualification |
|---------------|---------------------------|
| QC (Standard) | Commercial Grade |
| QA | Automotive Grade AEC-Q200 |

2. BLOCK DIAGRAM



2.1. PINOUT

RV-3028-C7 Package: (top view)



| | |
|----|-------------------------|
| #1 | CLKOUT |
| #2 | $\overline{\text{INT}}$ |
| #3 | SCL |
| #4 | SDA |
| #5 | V _{SS} |
| #6 | V _{BACKUP} |
| #7 | V _{DD} |
| #8 | EVI |

2.2. PIN DESCRIPTION

| Symbol | Pin # | Description |
|-------------------------|-------|---|
| CLKOUT | 1 | <p>Clock Output; push-pull; Normal and Interrupt driven clock output can be activated concurrently:</p> <ol style="list-style-type: none"> 1. Normal clock output can be controlled by the CLKOE bit (EEPROM 35h) when CLKF = 0. When CLKOE is set to 1 (default), the CLKOUT pin drives the square wave on the CLKOUT pin. When CLKOE bit is set to 0, the CLKOUT pin is LOW. 2. Interrupt driven clock output can be controlled by interrupt events when CLKOE = 0. When CLKIE bit (10h) is set to 1 the occurrence of the interrupt selected in the Clock Interrupt Mask Register (12h) allows the square wave output on the CLKOUT pin. Writing 0 to CLKIE will disable new interrupts from driving square wave on CLKOUT. When CLKF flag is cleared, the CLKOUT pin is LOW. <p>Depending of the settings in the FD field (EEPROM 35h), the CLKOUT pin can drive the square wave of 32.768 kHz (default), 8192 Hz, 1024 Hz, 64 Hz, 32 Hz or 1 Hz, or the predefined periodic countdown timer interrupt. When FD field is 111 the CLKOUT pin is LOW.</p> <p>When CLKSY bit (EEPROM 35h) set to 1, the enabling and disabling of the clock output is synchronized. CLKSY has no effect on the timer interrupt signal.</p> <p>In VBACKUP Power state, the CLKOUT pin is LOW.</p> |
| $\overline{\text{INT}}$ | 2 | Interrupt Output; open-drain; active LOW; requires pull-up resistor when used; used to output Periodic Countdown Timer, Periodic Time Update, Alarm, External Event, Automatic Backup Switchover and Power On Reset Interrupt signals. Interrupt output also in VBACKUP Power state. |
| SCL | 3 | I ² C Serial Clock Input; requires pull-up resistor. In VBACKUP Power state, the SCL pin is disabled. |
| SDA | 4 | I ² C Serial Data Input-Output; open-drain; requires pull-up resistor. In VBACKUP Power state, the SDA pin is disabled (high impedance). |
| V _{SS} | 5 | Ground. |
| V _{BACKUP} | 6 | Backup Supply Voltage. When the backup switchover function is not needed, V _{BACKUP} must be tied to V _{SS} with a 10 kΩ resistor. |
| V _{DD} | 7 | Power Supply Voltage. |
| EVI | 8 | External Event Input; used for interrupt generation, interrupt driven clock output and time stamp function. Remains active also in VBACKUP Power state. This pin should not be left floating. |

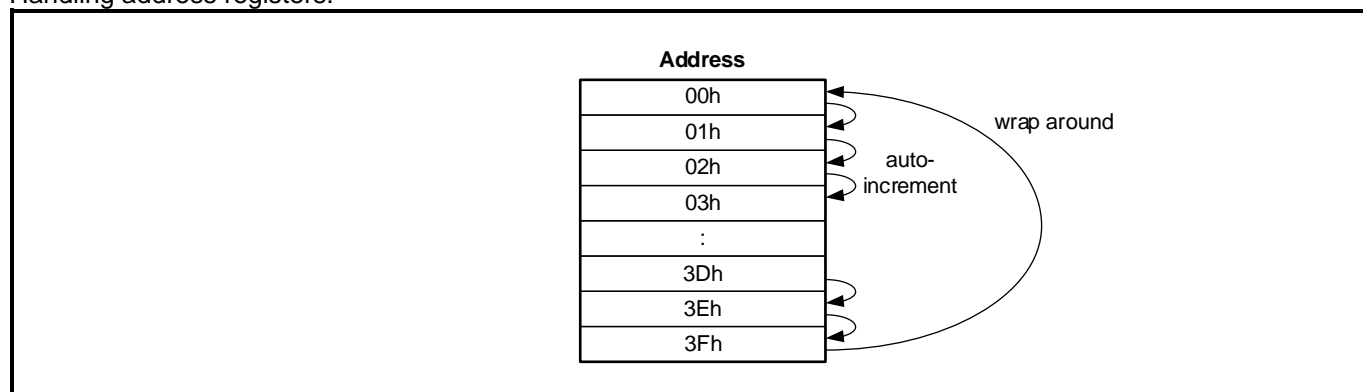
2.3. FUNCTIONAL DESCRIPTION

The RV-3028-C7 is an extreme-low power CMOS based Real-Time-Clock Module with embedded 32.768 kHz crystal oscillator. It includes an Automatic Backup switchover function with a Trickle charger where the interrupt output pin \overline{INT} is also working in VBACKUP Power state. The clock output on CLKOUT pin can be enabled normally via command over I²C interface or can be interrupt driven and synchronized clock output enable/disable on CLKOUT pin can be freely selected. The configuration registers are stored permanently in EEPROM and mirrored in RAM in order that the RTC module is still configured correctly even after power down. For safety against inadvertent overwriting the time, control and configuration registers can be protected by a User Programmable Password. Additionally, there is an EEPROM Offset value customer use for aging correction.

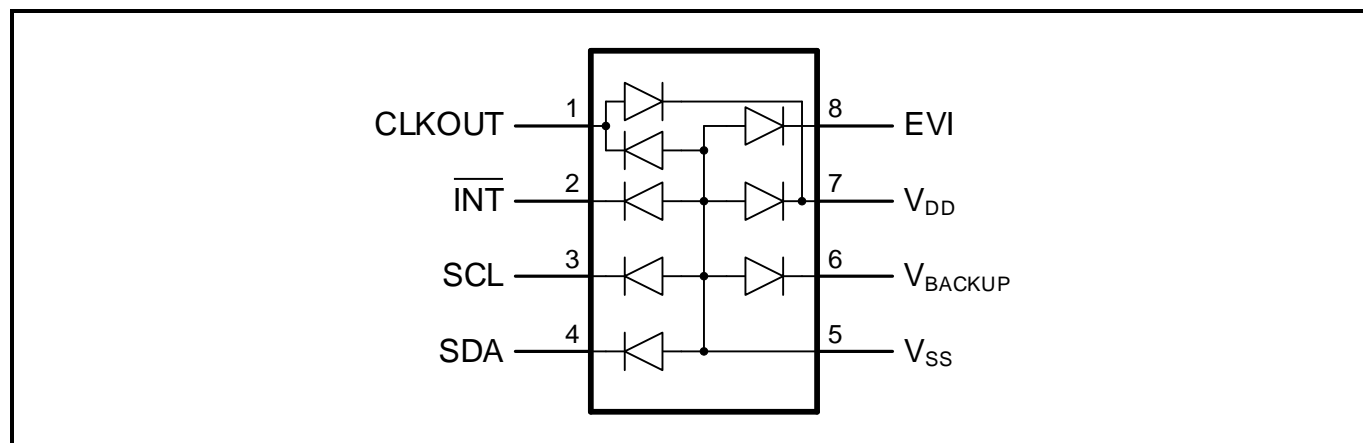
The RV-3028-C7 provides standard Clock & Calendar function including seconds, minutes, hours (12 or 24 h), weekdays, date, months, years (with leap year correction) and interrupt functions for the Periodic Countdown Timer, Periodic Time Update, Alarm, External Event, Automatic Backup Switchover and Power On Reset. All is accessible via I²C-bus (2-wire Interface). The interrupt functions and the Time Stamp of the External Event function are also working in VBACKUP Power state. Beside the standard RTC functions a 32-bit UNIX Time counter and 43 Bytes of User Memory EEPROM and 2 Bytes of User RAM are provided. A further Byte can be used as User RAM when the Periodic Countdown Timer is not used (Timer Value register 0Ah) and a further Byte when the Alarm function is not used (Alarm register 07h).

The registers are accessed by selecting a register address and then performing read or write operations. Multiple reads or writes can be performed in a single access, with the address automatically incremented after each byte by the Address Pointer. When address is automatically incremented, wrap around occurs from address 3Fh to address 00h (see figure below). All registers are designed as addressable 8-bit registers despite the fact that not all registers and bits are implemented.

Handling address registers:



2.4. DEVICE PROTECTION DIAGRAM



3. REGISTER ORGANIZATION

- RAM Registers at addresses 00h to 28h are accessed by selecting a register address and then performing read or write operations. Multiple reads or writes may be executed in a single access, with the address automatically incrementing after each byte.
- The Configuration Registers at addresses 30h to 37h are memorized in EEPROM and mirrored in RAM. For the RAM mirror, multiple reads or writes may be executed in a single access, with the address automatically incrementing after each byte.
- There are 43 bytes of non-volatile user memory EEPROM at addresses 00h to 2Ah for general use.

The following tables summarize the function of each register.

3.1. REGISTER CONVENTIONS

The conventions in this table serve as a key for the register overview and individual register diagrams:

| Convention (Conv.) | Description |
|--------------------|--|
| R | Read only. Writing to this register has no effect. |
| W | Write only. Returns 0 when read. |
| R/WP | Read: Always readable. Write: Can be write-protected by password. |
| WP | Write only. Returns 0 when read. Can be write-protected by password. |
| *WP | EEPW registers: RAM mirror is Write only. Returns 0 when read. EEPROM can be READ when Unlocked. |
| Prot. | Protected. Writing to this register has no effect. |

3.2. REGISTER OVERVIEW

After reset, all registers are set according to Table in section REGISTER RESET VALUES SUMMARY.

Register Definitions; RAM, Address 00h to 3Fh:

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-----------------------|-------|----------------|-------|-------|-------|-------|-------|-------|-------|
| 00h | Seconds | R/WP | ○ | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 01h | Minutes | R/WP | ○ | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 02h | Hours (24 hour) | R/WP | ○ | ○ | 20 | 10 | 8 | 4 | 2 | 1 |
| | Hours (12 hour) | | | | AMPM | 10 | 8 | 4 | 2 | 1 |
| 03h | Weekday | R/WP | ○ | ○ | ○ | ○ | ○ | 4 | 2 | 1 |
| 04h | Date | R/WP | ○ | ○ | 20 | 10 | 8 | 4 | 2 | 1 |
| 05h | Month | R/WP | ○ | ○ | ○ | 10 | 8 | 4 | 2 | 1 |
| 06h | Year | R/WP | 80 | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 07h | Minutes Alarm | R/WP | AE_M | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 08h | Hours Alarm (24h) | R/WP | AE_H | ○ | 20 | 10 | 8 | 4 | 2 | 1 |
| | Hours Alarm (12h) | | | | AMPM | 10 | 8 | 4 | 2 | 1 |
| 09h | Weekday Alarm | R/WP | AE_WD | ○ | ○ | ○ | ○ | 4 | 2 | 1 |
| | Date Alarm | | | | 20 | 10 | 8 | 4 | 2 | 1 |
| 0Ah | Timer Value 0 | R/WP | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| 0Bh | Timer Value 1 | R/WP | ○ | ○ | ○ | ○ | 2048 | 1024 | 512 | 256 |
| 0Ch | Timer Status 0 | R | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| 0Dh | Timer Status 1 shadow | R | ○ | ○ | ○ | ○ | 2048 | 1024 | 512 | 256 |
| 0Eh | Status | R/WP | EEbusy | CLKF | BSF | UF | TF | AF | EVF | PORF |
| 0Fh | Control 1 | R/WP | TRPT | - | WADA | USEL | EERD | TE | TD | |
| 10h | Control 2 | R/WP | TSE | CLKIE | UIE | TIE | AIE | EIE | 12_24 | RESET |
| 11h | GP Bits | R/WP | - | GP6 | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 |
| 12h | Clock Int. Mask | R/WP | - | - | - | - | CEIE | CAIE | CTIE | CUIE |
| 13h | Event Control | R/WP | ○ | EHL | ET | | ○ | TSR | TSOW | TSS |
| 14h | Count TS | R | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| 15h | Seconds TS | R | ○ | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 16h | Minutes TS | R | ○ | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 17h | Hours TS (24h) | R | ○ | ○ | 20 | 10 | 8 | 4 | 2 | 1 |
| | Hours TS (12h) | | | | AMPM | 10 | 8 | 4 | 2 | 1 |
| 18h | Date TS | R | ○ | ○ | 20 | 10 | 8 | 4 | 2 | 1 |
| 19h | Month TS | R | ○ | ○ | ○ | 10 | 8 | 4 | 2 | 1 |
| 1Ah | Year TS | R | 80 | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 1Bh | UNIX Time 0 | R/WP | UNIX 0 [7:0] | | | | | | | |
| 1Ch | UNIX Time 1 | R/WP | UNIX 1 [15:8] | | | | | | | |
| 1Dh | UNIX Time 2 | R/WP | UNIX 2 [23:16] | | | | | | | |
| 1Eh | UNIX Time 3 | R/WP | UNIX 3 [31:24] | | | | | | | |
| 1Fh | User RAM 1 | R/WP | RAM 1 data | | | | | | | |
| 20h | User RAM 2 | R/WP | RAM 2 data | | | | | | | |
| 21h | Password 0 | W | PW 0 [7:0] | | | | | | | |
| 22h | Password 1 | W | PW 1 [15:8] | | | | | | | |
| 23h | Password 2 | W | PW 2 [23:16] | | | | | | | |
| 24h | Password 3 | W | PW 3 [31:24] | | | | | | | |
| 25h | EE Address | R/WP | EEADDR | | | | | | | |
| 26h | EE Data | R/WP | EEDATA | | | | | | | |
| 27h | EE Command | WP | EECMD | | | | | | | |
| 28h | ID | R | HID | | | | VID | | | |
| 29h and 2Ah | RESERVED | Prot. | RESERVED | | | | | | | |
| 2Ch to 2Fh | RESERVED | Prot. | RESERVED | | | | | | | |
| 38h to 3Fh | RESERVED | Prot. | RESERVED | | | | | | | |

○ Read only. Always 0.
- Bit not implemented. Will return a 0 when read.

Register Definitions; Configuration EEPROM with RAM mirror, Address 2Bh and 30h to 37h:

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------------------|-------|------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| 2Bh | EEPROM Reserved | R/WP | RESERVED (Must not be overwritten) | | | | | | | |
| 30h | EEPROM PW Enable | R/WP | EEPWE | | | | | | | |
| 31h | EEPROM Password 0 | *WP | EEPW 0 [7:0] | | | | | | | |
| 32h | EEPROM Password 1 | *WP | EEPW 1 [15:8] | | | | | | | |
| 33h | EEPROM Password 2 | *WP | EEPW 2 [23:16] | | | | | | | |
| 34h | EEPROM Password 3 | *WP | EEPW 3 [31:24] | | | | | | | |
| 35h | EEPROM Clkout | R/WP | CLKOE | CLKSY | - | - | PORIE | FD | | |
| 36h | EEPROM Offset | R/WP | EEOffset [8:1] | | | | | | | |
| 37h | EEPROM Backup | R/WP | EEOffset [0] | BSIE | TCE | FEDE | BSM | | TCR | |

- Bit not implemented. Will return a 0 when read.
* EEPROM registers: RAM mirror is Write only. Returns 0 when read. EEPROM can be READ when Unlocked.

Register Definitions; User EEPROM, Address 00h to 2Ah:

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------|------------------------|-------|--------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| 00h to 2Ah | User EEPROM (43 Bytes) | R/WP | 43 Bytes of non-volatile User EEPROM | | | | | | | |

Register Definitions; Reserved EEPROM, Address 2Ch to 2Fh and 38h to 3Fh:

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------|-----------------|-------|----------|-------|-------|-------|-------|-------|-------|-------|
| 2Ch to 2Fh | Reserved EEPROM | Prot. | RESERVED | | | | | | | |
| 38h to 3Fh | Reserved EEPROM | Prot. | RESERVED | | | | | | | |

3.3. CLOCK REGISTERS

00h – Seconds

This register holds the count of seconds, in two binary coded decimal (BCD) digits. Values will be from 00 to 59.
Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|----------|--|-------|-------|-------|-------|-------|-------|-------|
| 00h | Seconds | R/WP | ○ | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 6:0 | Seconds | 00 to 59 | Holds the count of seconds, coded in BCD format. When writing to the Seconds register an eventual present memorized 1 Hz update is reset and the prescaler frequencies from 8192 Hz to 1 Hz will be reset (same effect as RESET BIT FUNCTION). When writing 1 to the RESET bit (10h) the Seconds register value remains unchanged. | | | | | | | |

01h – Minutes

This register holds the count of minutes, in two binary coded decimal (BCD) digits. Values will be from 00 to 59.
Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|----------|--|-------|-------|-------|-------|-------|-------|-------|
| 01h | Minutes | R/WP | ○ | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 6:0 | Minutes | 00 to 59 | Holds the count of minutes, coded in BCD format. | | | | | | | |

02h – Hours

This register holds the count of hours, in two binary coded decimal (BCD) digits. If the 12_24 bit is cleared (default) (see STATUS AND CONTROL REGISTERS, 10h – Control 2) the values will be from 0 to 23. If the 12_24 bit is set, the hour values will range from 1 to 12 and the AMPM bit will be 0 for AM hours and 1 for PM hours.

The value in the Hours register changes automatically between 12 and 24 hour mode when 12_24 bit is changed.

The value in the Hours Alarm register (08h) however must be rewritten.

Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| 02h | Hours (24 hour mode) – default value | R/WP | ○ | ○ | 20 | 10 | 8 | 4 | 2 | 1 |
| | Hours (12 hour mode) | | | | AMPM | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Hours (24 hour mode), 12_24 = 0 – default value

| Bit | Symbol | Value | Description |
|-----|---|---------|--|
| 7:6 | ○ | 0 | Read only. Always 0. |
| 5:0 | Hours (24 hour mode) – default value | 0 to 23 | Holds the count of hours, coded in BCD format. |

Hours (12 hour mode), 12_24 = 1

| Bit | Symbol | Value | Description |
|-----|----------------------|---------|--|
| 7:6 | ○ | 0 | Read only. Always 0. |
| 5 | AMPM | 0 | AM hours. |
| | | 1 | PM hours. |
| 4:0 | Hours (12 hour mode) | 1 to 12 | Holds the count of hours, coded in BCD format. |

Hours values:

| 24 hour mode | 12 hour mode | 24 hour mode | 12 hour mode |
|--------------|--------------|--------------|--------------|
| 00 | 12 (AM 12) | 12 | 32 (PM 12) |
| 01 | 01 (AM 1) | 13 | 21 (PM 1) |
| 02 | 02 (AM 2) | 14 | 22 (PM 2) |
| : | : | : | : |
| 10 | 10 (AM 10) | 22 | 30 (PM 10) |
| 11 | 11 (AM 11) | 23 | 31 (PM 11) |

3.4. CALENDAR REGISTERS

03h – Weekday

This register holds the current day of the week. Each value represents one weekday that is assigned by the user. Values will range from 0 to 6. The weekday counter is simply a 3-bit counter which counts up to 6 and then resets to 0.

Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------------------|----------|--------|----------------------------------|-------|-------|-------|-------|-------|-------|-------|
| 03h | Weekday | R/WP | ○ | ○ | ○ | ○ | ○ | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:3 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 2:0 | Weekday | 0 to 6 | Holds the weekday counter value. | | | | | | | |
| Weekday | | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Weekday 1 – Default value | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Weekday 2 | | | | | | | | 0 | 0 | 1 |
| Weekday 3 | | | | | | | | 0 | 1 | 0 |
| Weekday 4 | | | | | | | | 0 | 1 | 1 |
| Weekday 5 | | | | | | | | 1 | 0 | 0 |
| Weekday 6 | | | | | | | | 1 | 0 | 1 |
| Weekday 7 | | | | | | | | 1 | 1 | 0 |

04h – Date

This register holds the current day of the month, in two binary coded decimal (BCD) digits. Values will range from 01 to 31. Leap years are correctly handled from 2000 to 2099.

Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|----------|---|-------|-------|-------|-------|-------|-------|-------|
| 04h | Date | R/WP | ○ | ○ | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:6 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 5:0 | Date | 01 to 31 | Holds the current date of the month, coded in BCD format. – Default value = 01 | | | | | | | |

05h – Month

This register holds the current month, in two binary coded decimal (BCD) digits. Values will range from 01 to 12. Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------------------|----------|----------|---|-------|-------|-------|-------|-------|-------|-------|
| 05h | Month | R/WP | ○ | ○ | ○ | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:5 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 4:0 | Month | 01 to 12 | Holds the current month, coded in BCD format. | | | | | | | |
| Months | | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| January – Default value | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| February | | | | | | 0 | 0 | 0 | 1 | 0 |
| March | | | | | | 0 | 0 | 0 | 1 | 1 |
| April | | | | | | 0 | 0 | 1 | 0 | 0 |
| May | | | | | | 0 | 0 | 1 | 0 | 1 |
| June | | | | | | 0 | 0 | 1 | 1 | 0 |
| July | | | | | | 0 | 0 | 1 | 1 | 1 |
| August | | | | | | 0 | 1 | 0 | 0 | 0 |
| September | | | | | | 0 | 1 | 0 | 0 | 1 |
| October | | | | | | 1 | 0 | 0 | 0 | 0 |
| November | | | | | | 1 | 0 | 0 | 0 | 1 |
| December | | | | | | 1 | 0 | 0 | 1 | 0 |

06h – Year

This register holds the current year, in two binary coded decimal (BCD) digits. Values will range from 00 to 99. Leap years are correctly handled from 2000 to 2099.

Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|----------|---|-------|-------|-------|-------|-------|-------|-------|
| 06h | Year | R/WP | 80 | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | Year | 00 to 99 | Holds the current year, coded in BCD format. – Default value = 00 | | | | | | | |

3.5. ALARM REGISTERS

07h – Minutes Alarm

This register holds the Minutes Alarm Enable bit AE_M and the alarm value for minutes, in two binary coded decimal (BCD) digits. Values will range from 00 to 59.

Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------|--|---|-------|-------|-------|-------|-------|-------|-------|
| 07h | Minutes Alarm | R/WP | AE_M | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | AE_M | Minutes Alarm Enable bit. Enables alarm together with AE_H and AE_WD (see USE OF THE ALARM INTERRUPT). | | | | | | | | |
| | | 0 | Minutes Alarm is enabled. | | | | | | | |
| | | 1 | Minutes Alarm is disabled. – Default value | | | | | | | |
| 6:0 | Minutes Alarm | 00 to 59 | Holds the alarm value for minutes, coded in BCD format. | | | | | | | |

08h – Hours Alarm

This register holds the Hours Alarm Enable bit AE_H and the alarm value for hours, in two binary coded decimal (BCD) digits. If the 12_24 bit is cleared (default value) (see STATUS AND CONTROL REGISTERS, 10h – Control 2) the values will range from 0 to 23. If the 12_24 bit is set, the hour values will be from 1 to 12 and the AMPM bit will be 0 for AM hours and 1 for PM hours.

If the 12_24 hour mode bit is changed then the value in the Hours Alarm register must be re-initialized.

Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|--|--|---|-------|-------|-------|-------|-------|-------|-------|
| 08h | Hours Alarm (24 hour mode) – default value | R/WP | AE_H | ○ | 20 | 10 | 8 | 4 | 2 | 1 |
| | Hours Alarm (12 hour mode) | | | | AMPM | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Hours Alarm (24 hour mode), 12_24 = 0 – default value | | | | | | | | | | |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | AE_H | Hours Alarm Enable bit (see USE OF THE ALARM INTERRUPT). | | | | | | | | |
| | | 0 | Enabled | | | | | | | |
| | | 1 | Disabled – Default value | | | | | | | |
| 6 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 5:0 | Hours Alarm (24 hour mode) – default value | 0 to 23 | Holds the alarm value for hours, coded in BCD format. | | | | | | | |
| Hours Alarm (12 hour mode), 12_24 = 1 | | | | | | | | | | |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | AE_H | Hours Alarm Enable bit (see USE OF THE ALARM INTERRUPT). | | | | | | | | |
| | | 0 | Enabled | | | | | | | |
| | | 1 | Disabled – Default value | | | | | | | |
| 6 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 5 | AMPM | 0 | AM hours. | | | | | | | |
| | | 1 | PM hours. | | | | | | | |
| 4:0 | Hours Alarm (12 hour mode) | 1 to 12 | Holds the alarm value for hours, coded in BCD format. | | | | | | | |

09h – Weekday/Date Alarm

This register holds the Weekday/Date Alarm Enable bit AE_WD. If the WADA bit is 0 (Bit 5 in Register 0Fh), it holds the alarm value for the weekday (weekdays assigned by the user), in two binary coded decimal (BCD) digits. Values will range from 0 to 6. If the WADA bit is 1, it holds the alarm value for the date, in two binary coded decimal (BCD) digits. Values will range from 01 to 31. Leap years are correctly handled from 2000 to 2099.

Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--|-------------------------------|--|---|-------|-------|-------|-------|-------|-------|-------|
| 09h | Weekday Alarm – default value | R/WP | AE_WD | ○ | ○ | ○ | ○ | 4 | 2 | 1 |
| | Date Alarm | | | | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Weekday Alarm, WADA = 0 – default value | | | | | | | | | | |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | AE_WD | Weekday/Date Alarm Enable bit. Enables alarm together with AE_M and AE_H (see USE OF THE ALARM INTERRUPT). | | | | | | | | |
| | | 0 | Enabled | | | | | | | |
| | | 1 | Disabled – Default value | | | | | | | |
| 6:3 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 2:0 | Weekday Alarm | 0 to 6 | Holds the weekday alarm value, coded in BCD format. | | | | | | | |
| Date Alarm, WADA = 1 | | | | | | | | | | |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | AE_WD | Weekday/Date Alarm Enable bit. Enables alarm together with AE_M and AE_H (see USE OF THE ALARM INTERRUPT). | | | | | | | | |
| | | 0 | Enabled | | | | | | | |
| | | 1 | Disabled – Default value | | | | | | | |
| 6 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 5:0 | Date Alarm | 01 to 31 | Holds the alarm value for the date, coded in BCD format. The Reset value 00 after POR has to be replaced by a valid value (01 to 31). | | | | | | | |

3.6. PERIODIC COUNTDOWN TIMER CONTROL REGISTERS

0Ah – Timer Value 0

This register is used to set the lower 8 bits of the 12 bit Timer Value (preset value) for the Periodic Countdown Timer. This value will be automatically reloaded into the Countdown Timer when it reaches zero if the TRPT bit is 1. This allows for periodic timer interrupts (see calculation below).

Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------|------------|---|-------|-------|-------|-------|-------|-------|-------|
| 0Ah | Timer Value 0 | R/WP | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | Timer Value 0 | 00h to FFh | The Timer Value for the Periodic Countdown Timer in binary format (lower 8 bit) (see USE OF THE PERIODIC COUNTDOWN TIMER). When read, only the preset value is returned and not the actual value. When the Periodic Countdown Timer Interrupt function is not used, register 0Ah can be used as RAM byte. | | | | | | | |

0Bh – Timer Value 1

This register is used to set the upper 4 bits of the 12 bit Timer Value (preset value) for the Periodic Countdown Timer. This value will be automatically reloaded into the Countdown Timer when it reaches zero if the TRPT bit is 1. This allows for periodic timer interrupts (see calculation below).

Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------|----------|---|-------|-------|-------|-------|-------|-------|-------|
| 0Bh | Timer Value 1 | R/WP | ○ | ○ | ○ | ○ | 2048 | 1024 | 512 | 256 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:4 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 3:0 | Timer Value 1 | 0h to Fh | The Timer Value for the Periodic Countdown Timer in binary format (upper 4 bit) (see USE OF THE PERIODIC COUNTDOWN TIMER). When read, only the preset value is returned and not the actual value. | | | | | | | |

Countdown Period in seconds:

$$\text{Countdown Period} = \frac{\text{Timer Value}}{\text{Timer Clock Frequency}}$$

0Ch – Timer Status 0

This register holds the lower 8 bits of the current 12 bit value of the Periodic Countdown Timer.
Read only. Writing to this register has no effect.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------------|------------|---|-------|-------|-------|-------|-------|-------|-------|
| 0Ch | Timer Status 0 | R | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | Timer Status 0 | 00h to FFh | The current value of the Periodic Countdown Timer in binary format (lower 8 bit) (see USE OF THE PERIODIC COUNTDOWN TIMER). | | | | | | | |

0Dh – Timer Status 1 shadow

This register holds the upper 4 bits of the current 12 bit value of the Periodic Countdown Timer.
Read only. Writing to this register has no effect.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------------|----------|---|-------|-------|-------|-------|-------|-------|-------|
| 0Dh | Timer Status 1 | R | ○ | ○ | ○ | ○ | 2048 | 1024 | 512 | 256 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:4 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 3:0 | Timer Status 1 | 0h to Fh | The current value of the Periodic Countdown Timer in binary format (upper 4 bit) (see USE OF THE PERIODIC COUNTDOWN TIMER). | | | | | | | |

When TE bit (0Fh) is set to 1, the Timer Status 0 and Timer Status 1 shadow registers hold the current countdown value. When a 0 is written to the TE bit, the Timer Status 0 and Timer Status 1 registers store the last updated value. Reading the Timer Status 0 value updates the Timer Status 1 shadow register. Reading only the Timer Status 1 shadow register will return the not-updated Timer Status 1 shadow register value, memorized while reading Timer Status 0.

3.7. STATUS AND CONTROL REGISTERS

0Eh – Status

This register is used to detect the occurrence of various interrupt events and reliability problems in internal data.
Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
|---------|----------|--|--|-------|-------|-------|-------|-------|-------|-------|--|
| 0Eh | Status | R/WP | EEbusy | CLKF | BSF | UF | TF | AF | EVF | PORF | |
| | Reset | | 1 → 0 | 0 | 0 | 0 → 1 | 0 | 0 | 0 | 1 | |
| Bit | Symbol | Value | Description | | | | | | | | |
| 7 | EEbusy | EEPROM Memory Busy Status Bit – (Read Only) (see EEPROM READ/WRITE) | | | | | | | | | |
| | | 0 | The transfer is finished. | | | | | | | | |
| | | 1 | Indicates that the EEPROM is currently handling a read or write request and will ignore any further commands until the current one is finished. At power up (POR) a refresh is automatically generated. The time of this first refreshment is $t_{PREFR} = \sim 66$ ms. After the refreshment is finished; EEbusy is cleared to 0 automatically. | | | | | | | | |
| 6 | CLKF | Clock Output Interrupt Flag (see PROGRAMMABLE CLOCK OUTPUT) | | | | | | | | | |
| | | 0 | No event detected. When cleared to 0 the frequency output will stop depending on CLKS _Y and CLKOUT settings. | | | | | | | | |
| | | 1 | If set to 0 beforehand, indicates the occurrence of an interrupt driven clock output on CLKOUT pin. The value 1 is retained until a 0 is written by the user. | | | | | | | | |
| 5 | BSF | Backup Switch Flag (see AUTOMATIC BACKUP SWITCHOVER FUNCTION) | | | | | | | | | |
| | | 0 | No backup switchover detected. At power up (POR) this flag is automatically cleared to 0. When the backup switchover function is disabled (BSM field = 00 or 10) BSF is always logic 0. | | | | | | | | |
| | | 1 | If set to 0 beforehand, indicates that a switchover from main power V_{DD} to V_{BACKUP} has occurred. The value 1 can be cleared by writing a 0 to the bit if RTC module is in VDD Power state. Caution: The EVF flag is also set by an event of the Backup Switchover function when bits TSS (13h) and TSE (10h) are set to 1. | | | | | | | | |
| 4 | UF | Periodic Time Update Flag (see PERIODIC TIME UPDATE INTERRUPT FUNCTION) | | | | | | | | | |
| | | 0 | No event detected. | | | | | | | | |
| | | 1 | If set to 0 beforehand, indicates the occurrence of a Periodic Time Update Interrupt event. The value 1 is retained until a 0 is written by the user. After power up (POR) the Second update is selected and the UF flag is set to 1 within one second. | | | | | | | | |
| 3 | TF | Periodic Countdown Timer Flag (see PERIODIC COUNTDOWN TIMER INTERRUPT FUNCTION) | | | | | | | | | |
| | | 0 | No event detected. When the \overline{INT} and CLKOUT pins are LOW because of a Countdown Timer event, their t_{RTN1} – signals are cancelled as soon as TF flag is cleared to 0. | | | | | | | | |
| | | 1 | If set to 0 beforehand, indicates the occurrence of a Periodic Countdown Timer Interrupt event. The value 1 is retained until a 0 is written by the user. | | | | | | | | |
| 2 | AF | Alarm Flag (see ALARM INTERRUPT FUNCTION) | | | | | | | | | |
| | | 0 | No event detected. | | | | | | | | |
| | | 1 | If set to 0 beforehand, indicates the occurrence of an Alarm Interrupt event. The value 1 is retained until a 0 is written by the user. | | | | | | | | |
| 1 | EVF | Event Flag (see EXTERNAL EVENT INTERRUPT FUNCTION) | | | | | | | | | |
| | | 0 | No event detected. | | | | | | | | |
| | | 1 | If set to 0 beforehand, indicates the occurrence of an External Event or a Backup Switchover. The value 1 is retained until a 0 is written by the user. The EVF flag is set to 1 when: <ul style="list-style-type: none"> External event occurs and TSS = 0 and (EIE = 1 or TSE = 1). Backup switchover occurs and TSS = 1 and (EIE = 1 or TSE = 1). | | | | | | | | |
| 0 | PORF | Power On Reset Flag | | | | | | | | | |
| | | 0 | No voltage drop detected. | | | | | | | | |
| | | 1 | If set to 0 beforehand, indicates a voltage drop below V_{POR} . The data in the device are no longer valid and all registers must be initialized. The value 1 is retained until a 0 is written by the user. At power up (POR) the value is set to 1, the user has to write 0 to the flag to use it. | | | | | | | | |

0Fh – Control 1

This register is used to specify the target for the Alarm Interrupt function and the Periodic Time Update Interrupt function and to select or set operations for the Periodic Countdown Timer.

Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------|-------------------------|------------------|---|-------|--|-------|-------|-------|-------|-------|
| 0Fh | Control 1 | R/WP | TRPT | - | WADA | USEL | EERD | TE | TD | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | TRPT | | Timer Repeat bit. Specifies either Single or Repeat Mode for the Periodic Countdown Timer Interruption function (see PERIODIC COUNTDOWN TIMER INTERRUPT FUNCTION). | | | | | | | |
| | | 0 | Single Mode is selected. When the Countdown Timer is enabled (TE = 1) it will halt when it reaches zero and TE is automatically cleared. – Default value | | | | | | | |
| | | 1 | Repeat Mode is selected. When the Countdown Timer is enabled (TE = 1) it automatically reloads the value from the Timer Value registers upon reaching 0, and continues counting. | | | | | | | |
| 6 | - | 0 | Bit not implemented. Will return a 0 when read. | | | | | | | |
| 5 | WADA | | Weekday Alarm / Date Alarm selection bit. This bit is used to specify either the Weekday or Date as the source for the Alarm Interrupt function (see ALARM INTERRUPT FUNCTION). | | | | | | | |
| | | 0 | Weekday is the source for the Alarm Interrupt function. – Default value | | | | | | | |
| | | 1 | Date is the source for the Alarm Interrupt function. | | | | | | | |
| 4 | USEL | | Update Interrupt Select bit. Specifies either Second or Minute update for the Periodic Time Update Interrupt function (see PERIODIC TIME UPDATE INTERRUPT FUNCTION). Writing 1 to the RESET bit or writing to the Seconds register affects the length of the current update period (see RESET BIT FUNCTION). | | | | | | | |
| | | 0 | Second update (Auto reset time $t_{RTN2} = 500$ ms). – Default value | | | | | | | |
| | | 1 | Minute update (Auto reset time $t_{RTN2} = 7.813$ ms). | | | | | | | |
| 3 | EERD | | EEPROM Memory Refresh Disable bit. When 1, disables the automatic refresh of the Configuration Registers from the EEPROM Memory (see AUTOMATIC REFRESH (ALL CONFIGURATION EEPROM → RAM)). | | | | | | | |
| | | 0 | Refresh is active. All data in the Configuration Registers are refreshed by the data stored in the EEPROM each 24 hours, at date increment (at the beginning of the last second before midnight). The time of this automatic refreshment is $t_{AREFR} = \sim 3.5$ ms. Refresh is only active when RTC is not in VBACKUP mode. – Default value | | | | | | | |
| | | 1 | Refresh is disabled. | | | | | | | |
| 2 | TE | | Periodic Countdown Timer Enable bit. This bit controls the start/stop setting for the Periodic Countdown Timer Interruption function (see PERIODIC COUNTDOWN TIMER INTERRUPT FUNCTION). | | | | | | | |
| | | 0 | Stops the Periodic Countdown Timer Interruption function. TE is also automatically cleared when Single Mode is selected (TRPT = 0) and when the Countdown Timer reaches zero. – Default value | | | | | | | |
| | | 1 | Starts the Periodic Countdown Timer Interruption function (a countdown starts from the preset value set in Timer Value registers). | | | | | | | |
| 1:0 | TD | 00 to 11 | Timer Clock Frequency selection. Sets the countdown source clock for the Periodic Countdown Timer Interruption function. With this setting the Auto reset time t_{RTN1} is also defined. When the clock source has been set to Second update (1 Hz) or Minute update (1/60 Hz), the timing of both, countdown and interrupts, is coordinated with the clock update timing. See table below (see also PERIODIC COUNTDOWN TIMER INTERRUPT FUNCTION). Writing 1 to the RESET bit or writing to the Seconds register affects the length of the current countdown period (see RESET BIT FUNCTION). | | | | | | | |
| TD value | Timer Clock Frequency | Countdown period | t_{RTN1} | | Effect when writing 1 to the RESET bit or when writing to the Seconds register | | | | | |
| 00 | 4096 Hz – Default value | 244.14 μ s | 122 μ s | | Affects current period | | | | | |
| 01 | 64 Hz | 15.625 ms | 7.813 ms | | | | | | | |
| 10 | 1 Hz | 1 s | | | | | | | | |
| 11 | 1/60 Hz | 60 s | | | | | | | | |

10h – Control 2

This register is used to control the interrupt event output for the $\overline{\text{INT}}$ pin, the stop/start status of clock and calendar operations, the interrupt controlled clock output on CLKOUT pin, the hour mode and the time stamp enable.

Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | | |
|--|-----------|--|--|-------|-------|-------|-------|-------|-------|-------|--|--|
| 10h | Control 2 | R/WP | TSE | CLKIE | UIE | TIE | AIE | EIE | 12_24 | RESET | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| Bit | Symbol | Value | Description | | | | | | | | | |
| 7 | TSE | Time Stamp Enable bit (see TIME STAMP FUNCTION) | | | | | | | | | | |
| | | 0 | Disables the time stamp function. – Default value | | | | | | | | | |
| | | 1 | Enables the Time stamp function. | | | | | | | | | |
| 6 | CLKIE | Interrupt Controlled Clock Output Enable bit. When enabled, it is possible to wake-up an external system by outputting a frequency. (see PROGRAMMABLE CLOCK OUTPUT) | | | | | | | | | | |
| | | 0 | Disabled – Default value | | | | | | | | | |
| 1 | | 1 | When set to 1, the clock output on CLKOUT pin is automatically enabled when an interrupt occurs, based on the Clock Interrupt Mask Register (12h) and according to clock setting defined by the FD field. This function is disabled in VBACKUP Power state. | | | | | | | | | |
| | | Periodic Time Update Interrupt Enable bit (see PERIODIC TIME UPDATE INTERRUPT FUNCTION) | | | | | | | | | | |
| 5 | UIE | 0 | No interrupt signal is generated on $\overline{\text{INT}}$ pin when a Periodic Time Update event occurs or the t_{RTN2} - signal on $\overline{\text{INT}}$ pin is cancelled. – Default value | | | | | | | | | |
| | | 1 | An interrupt signal is generated on $\overline{\text{INT}}$ pin when a Periodic Time Update event occurs. The low-level output signal is automatically cleared after $t_{\text{RTN2}} = 500 \text{ ms}$ (Second update) or $t_{\text{RTN2}} = 7.813 \text{ ms}$ (Minute update). | | | | | | | | | |
| Periodic Countdown Timer Interrupt Enable bit (see PERIODIC COUNTDOWN TIMER INTERRUPT FUNCTION) | | | | | | | | | | | | |
| 4 | TIE | 0 | No interrupt signal is generated on $\overline{\text{INT}}$ pin when a Countdown Timer event occurs or the t_{RTN1} - signal on $\overline{\text{INT}}$ pin is cancelled. – Default value | | | | | | | | | |
| | | 1 | An interrupt signal is generated on $\overline{\text{INT}}$ pin when a Periodic Countdown Timer event occurs. The low-level output signal is automatically cleared after $t_{\text{RTN1}} = 122 \mu\text{s}$ (TD = 00) or $t_{\text{RTN1}} = 7.813 \text{ ms}$ (TD = 01, 10, 11). | | | | | | | | | |
| Alarm Interrupt Enable bit (see ALARM INTERRUPT FUNCTION) | | | | | | | | | | | | |
| 3 | AIE | 0 | No interrupt signal is generated on $\overline{\text{INT}}$ pin when an Alarm event occurs or the signal is cancelled on $\overline{\text{INT}}$ pin. – Default value | | | | | | | | | |
| | | 1 | An interrupt signal is generated on $\overline{\text{INT}}$ pin when an Alarm event occurs. This setting is retained until the AF flag is cleared to 0 (no automatic cancellation). | | | | | | | | | |
| Event Interrupt Enable bit (see EXTERNAL EVENT INTERRUPT FUNCTION and INTERRUPT SCHEME) | | | | | | | | | | | | |
| 2 | EIE | 0 | No interrupt signal is generated on $\overline{\text{INT}}$ pin when an External Event on EVI pin occurs or when an Automatic Backup Switchover occurs or the signal is cancelled on $\overline{\text{INT}}$ pin. – Default value | | | | | | | | | |
| | | 1 | An interrupt signal is generated on $\overline{\text{INT}}$ pin when an External Event on EVI pin occurs and TSS = 0, or when an Automatic Backup Switchover occurs and TSS = 1. The signal on $\overline{\text{INT}}$ pin is retained until the EVF flag is cleared to 0 (no automatic cancellation). | | | | | | | | | |
| 1 | 12_24 | 12 or 24 hour mode (see CLOCK REGISTERS and ALARM REGISTERS). The value in the Hours register changes automatically between 12 and 24 hour mode when 12_24 bit is changed. The value in the Hours Alarm register (08h) however must be rewritten. | | | | | | | | | | |
| | | 0 | 24 hour mode is selected (0 to 23). – Default value | | | | | | | | | |
| | | 1 | 12 hour mode is selected (1 to 12). | | | | | | | | | |
| Reset bit. This bit is used for a software-based time adjustment (synchronization). (see RESET BIT FUNCTION). | | | | | | | | | | | | |
| 0 | RESET | 0 | No reset. – Default value | | | | | | | | | |
| | | 1 | Resets the clock prescaler frequencies from 8192 Hz to 1 Hz (writing to the Seconds register has same effect). This bit always returns 0 when read. An eventual present memorized 1 Hz update is also reset. Because the upper stage of the prescaler is not reset (16.384 kHz) and the I ² C interface is asynchronous, the first 1 Hz period after reset will be 0 to 244 μs shorter than 1 second. Resetting the prescaler will have an influence on the length of the current clock period on all subsequent peripherals (clock and calendar, CLKOUT, timer clock, update timer clock, UNIX clock, EVI input filter). | | | | | | | | | |

11h – GP Bits

This register holds the bits for general purpose use (7 bits).

Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|--------|---|-------|-------|-------|-------|-------|-------|-------|
| 11h | GP Bits | R/WP | - | GP6 | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | - | 0 | Bit not implemented. Will return a 0 when read. | | | | | | | |
| 6:0 | GPx | 0 or 1 | Register bits for general purpose use (7 bits). | | | | | | | |

12h – Clock Interrupt Mask

This register is used to select a predefined interrupt for automatic clock output. Setting a bit to 1 selects the corresponding interrupt. Multiple interrupts can be selected. After power on, no interrupt is selected (see CLOCK OUTPUT SCHEME).

Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------------------|--|---|-------|-------|-------|-------|-------|-------|-------|
| 12h | Clock Interrupt Mask | R/WP | - | - | - | - | CEIE | CAIE | CTIE | CUIE |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:4 | - | 0 | Bit not implemented. Will return a 0 when read. | | | | | | | |
| 3 | CEIE | Clock output when Event Interrupt bit. The source for the Event Interrupt can be the External Event from EVI pin or the Automatic Backup Switchover (see INTERRUPT SCHEME). | | | | | | | | |
| | | 0 | Disabled – Default value | | | | | | | |
| | | 1 | Enabled. Internal signal EI is selected. | | | | | | | |
| 2 | CAIE | Clock output when Alarm Interrupt bit. | | | | | | | | |
| | | 0 | Disabled – Default value | | | | | | | |
| | | 1 | Enabled. Internal signal AI is selected. | | | | | | | |
| 1 | CTIE | Clock output when Periodic Countdown Timer Interrupt bit. | | | | | | | | |
| | | 0 | Disabled – Default value | | | | | | | |
| | | 1 | Enabled: Internal signal TI is selected. | | | | | | | |
| 0 | CUIE | Clock output when Periodic Time Update Interrupt bit. | | | | | | | | |
| | | 0 | Disabled – Default value | | | | | | | |
| | | 1 | Enabled. Internal signal UI is selected. | | | | | | | |

3.8. EVENT CONTROL REGISTER

13h – Event Control

This register controls the event detection on the EVI pin. Depending of the EHL bit, high or low level (or rising or falling edge) can be detected. Moreover a digital glitch filtering can be applied to the EVI signal by selecting a sampling period t_{SP} in the ET field. Furthermore this register holds control functions for the Time Stamp data. And the switching over to VBACKUP Power state can be selected as source for an event.

Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------|--|--|-------|-------|-------|-------|-------|-------|-------|
| 13h | Event Control | R/WP | ○ | EHL | ET | | ○ | TSR | TSOW | TSS |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 6 | EHL | Event High/Low Level (Rising/Falling Edge) selection for detection (see EXTERNAL EVENT INTERRUPT FUNCTION) | | | | | | | | |
| | | 0 | The falling edge (ET = 00) or low level (ET ≠ 00) is regarded as the External Event on pin EVI. – Default value | | | | | | | |
| | | 1 | The rising edge (ET = 00) or high level (ET ≠ 00) is regarded as the External Event on pin EVI. | | | | | | | |
| 5:4 | ET | Event Filtering Time set. Applies a digital filtering to the EVI pin by sampling the EVI signal. (see EXTERNAL EVENT INTERRUPT FUNCTION). | | | | | | | | |
| | | 00 | No filtering. Edge detection. – Default value | | | | | | | |
| | | 01 | Sampling period $t_{SP} = 3.9$ ms (256 Hz). Level detection. | | | | | | | |
| | | 10 | Sampling period $t_{SP} = 15.6$ ms (64 Hz). Level detection. | | | | | | | |
| | | 11 | Sampling period $t_{SP} = 125$ ms (8 Hz). Level detection. | | | | | | | |
| 3 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 2 | TSR | Time Stamp Reset bit (see TIME STAMP FUNCTION) | | | | | | | | |
| | | 0 | Disables the Time Stamp Reset. – Default value | | | | | | | |
| | | 1 | Resets all seven time stamp registers (Count TS to Year TS) to 00h; this bit always returns 0 when read. | | | | | | | |
| 1 | TSOW | Time Stamp Overwrite bit. Controls the overwrite function of the TS registers (Seconds TS to Year TS). The counter Count TS is always working, independent of the settings of the overwrite bit TSOW. (see TIME STAMP FUNCTION) | | | | | | | | |
| | | 0 | The time stamp of the first occurred event is recorded and remains in TS registers. To initialize or reinitialize the first event detection function, the EVF has to be cleared. – Default value | | | | | | | |
| | | 1 | The time stamp of the last occurred event is recorded and TS registers are overwritten. The EVF flag does not need to be cleared. | | | | | | | |
| 0 | TSS | Time Stamp Source Selection bit (see TIME STAMP FUNCTION) | | | | | | | | |
| | | 0 | External Event is selected as Time Stamp source. A time stamp is generated (when TSE = 1) and an interrupt is issued (when EIE = 1) when an External Event on EVI pin occurs – Default value | | | | | | | |
| | | 1 | Automatic Backup Switchover is selected as Time Stamp source. A time stamp is generated (when TSE = 1) and an Interrupt is issued (when BSIE = 1) when the circuit goes to VBACKUP Power state. | | | | | | | |

3.9. TIME STAMP REGISTERS

Seven Time Stamp registers (Count TS to Year TS), (see TIME STAMP FUNCTION).

14h – Count TS

This register contains the number of occurrences of the corresponding event in standard binary format. The values range from 0 to 255.

Read only. Writing to this register has no effect.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|----------|--|-------|-------|-------|-------|-------|-------|-------|
| 14h | Count TS | R | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | Count TS | 0 to 255 | Number of occurrences of the corresponding event, coded in binary. In case of an overflow the counter starts again with 00h When bit TSE = 0, the counter stops counting events. When bit TSE = 1, the counter is increased when event occurs. The counter Count TS is always working, independent of the settings of the overwrite bit TSOW. The Count TS register is reset to 00h when 1 is written to the Time Stamp Reset bit TSR (see TIME STAMP FUNCTION). | | | | | | | |

15h – Seconds TS

This register holds a recorded Time Stamp of the Seconds register, in two binary coded decimal (BCD) digits. The values are from 00 to 59.

Read only. Writing to this register has no effect.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------------|----------|--|-------|-------|-------|-------|-------|-------|-------|
| 15h | Seconds TS | R | 0 | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | 0 | 0 | Read only. Always 0. | | | | | | | |
| 6:0 | Seconds TS | 00 to 59 | Holds a recorded Time Stamp of the Seconds register, coded in BCD format. When enabled (bit TSE = 1), Depending on the setting of the TSOW bit it contains the time stamp of the first or last occurred event. The Seconds TS register is reset to 00h when 1 is written to the Time Stamp Reset bit TSR. | | | | | | | |

16h – Minutes TS

This register holds a recorded Time Stamp of the Minutes register, in two binary coded decimal (BCD) digits. The values are from 00 to 59.

Read only. Writing to this register has no effect.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------------|----------|--|-------|-------|-------|-------|-------|-------|-------|
| 16h | Minutes TS | R | 0 | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | 0 | 0 | Read only. Always 0. | | | | | | | |
| 6:0 | Minutes TS | 00 to 59 | Holds a recorded Time Stamp of the Minutes register, coded in BCD format. When enabled (bit TSE = 1), Depending on the setting of the TSOW bit it contains the time stamp of the first or last occurred event. The Minutes TS register is reset to 00h when 1 is written to the Time Stamp Reset bit TSR. | | | | | | | |

17h – Hours TS

This register holds a recorded Time Stamp of the Hours register, in two binary coded decimal (BCD) digits. If the 12_24 bit is cleared (default) (see STATUS AND CONTROL REGISTERS, 10h – Control 2) the values will be from 0 to 23. If the 12_24 bit is set, the hour values will range from 1 to 12 and the AMPM bit will be 0 for AM hours and 1 for PM hours.

Read only. Writing to this register has no effect.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--|---|---------|---|-------|-------|-------|-------|-------|-------|-------|
| 17h | Hours TS (24 hour mode) – default value | R | ○ | ○ | 20 | 10 | 8 | 4 | 2 | 1 |
| | Hours TS (12 hour mode) | | AMPM | 10 | 8 | 4 | 2 | 1 | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Hours TS (24 hour mode) – default value | | | | | | | | | | |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:6 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 5:0 | Hours TS (24 hour mode) – default value | 0 to 23 | Holds a recorded Time Stamp of the Hours register, coded in BCD format. When enabled (bit TSE = 1), Depending on the setting of the TSOW bit it contains the time stamp of the first or last occurred event. The Hours TS register is reset to 00h when 1 is written to the Time Stamp Reset bit TSR. | | | | | | | |
| Hours TS (12 hour mode) | | | | | | | | | | |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:6 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 5 | AMPM | 0 | AM hours, from the recorded Time Stamp of the Hours register. | | | | | | | |
| | | 1 | PM hours, from the recorded Time Stamp of the Hours register. | | | | | | | |
| 4:0 | Hours TS (12 hour mode) | 1 to 12 | Holds a recorded Time Stamp of the Hours register, coded in BCD format. When enabled (bit TSE = 1), Depending on the setting of the TSOW bit it contains the time stamp of the first or last occurred event. The Hours TS register is reset to 00h when 1 is written to the Time Stamp Reset bit TSR. | | | | | | | |

18h – Date TS

This register holds a recorded Time Stamp of the Date register, in two binary coded decimal (BCD) digits. The values will range from 01 to 31.

Read only. Writing to this register has no effect.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|----------|--|-------|-------|-------|-------|-------|-------|-------|
| 18h | Date TS | R | ○ | ○ | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:6 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 5:0 | Date TS | 01 to 31 | Holds a recorded Time Stamp of the Date register, coded in BCD format. When enabled (bit TSE = 1), Depending on the setting of the TSOW bit it contains the time stamp of the first or last occurred event. The Date TS register is reset to 00h when 1 is written to the Time Stamp Reset bit TSR. After POR or when reset with TSR bit and when a Time Stamp is recorded, the value 00 will be replaced by a valid value (01 to 31). | | | | | | | |

19h – Month TS

This register holds a recorded Time Stamp of the Month register, in two binary coded decimal (BCD) digits. The values will range from 01 to 12.

Read only. Writing to this register has no effect.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|----------|---|-------|-------|-------|-------|-------|-------|-------|
| 19h | Month TS | R | ○ | ○ | ○ | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:5 | ○ | 0 | Read only. Always 0. | | | | | | | |
| 4:0 | Month TS | 01 to 12 | Holds a recorded Time Stamp of the Month register, coded in BCD format. When enabled (bit TSE = 1), Depending on the setting of the TSOW bit it contains the time stamp of the first or last occurred event. The Month TS register is reset to 00h when 1 is written to the Time Stamp Reset bit TSR. After POR or when reset with TSR bit and when a Time Stamp is recorded, the value 00 will be replaced by a valid value (01 to 12). | | | | | | | |

1Ah – Year TS

This register holds a recorded Time Stamp of the Year register, in two binary coded decimal (BCD) digits. Values will range from 00 to 99.

Read only. Writing to this register has no effect.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|----------|---|-------|-------|-------|-------|-------|-------|-------|
| 1Ah | Year TS | R | 80 | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | Year TS | 00 to 99 | Holds a recorded Time Stamp of the Year register, coded in BCD format. When enabled (bit TSE = 1), Depending on the setting of the TSOW bit it contains the time stamp of the first or last occurred event. The Year TS register is reset to 00h when 1 is written to the Time Stamp Reset bit TSR. | | | | | | | |

3.10. UNIX TIME REGISTERS

The UNIX Time counter is a 32-bit counter with the value in binary format. The counter will roll-over to 00000000h when reaching FFFFFFFFh. The 4 counter registers are fully readable and writable. The counter source clock is the digitally offset compensated 1 Hz clock frequency. The UNIX Time counter increment is inhibited during I²C write access to the 4 UNIX Time registers to allow coherent data values (see UNIX TIME COUNTER and SETTING AND READING THE TIME).

Read: Always readable. Write: Can be write-protected by password.

1Bh – UNIX Time 0

Bit 0 to 7 from 32-bit UNIX Time counter.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|--------------|------------|--------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| 1Bh | UNIX Time 0 | R/WP | UNIX 0 [7:0] | | | | | | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | UNIX 0 [7:0] | 00h to FFh | Bit 0 to 7 from 32-bit UNIX counter. | | | | | | | |

1Ch – UNIX Time 1

Bit 8 to 15 from 32-bit UNIX Time counter.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------|------------|---------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| 1Ch | UNIX Time 1 | R/WP | UNIX 1 [15:8] | | | | | | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | UNIX 1 [15:8] | 00h to FFh | Bit 8 to 15 from 32-bit UNIX counter. | | | | | | | |

1Dh – UNIX Time 2

Bit 16 to 23 from 32-bit UNIX Time counter.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------------|------------|--|-------|-------|-------|-------|-------|-------|-------|
| 1Dh | UNIX Time 2 | R/WP | UNIX 2 [23:16] | | | | | | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | UNIX 2 [23:16] | 00h to FFh | Bit 16 to 23 from 32-bit UNIX counter. | | | | | | | |

1Eh – UNIX Time 3

Bit 24 to 31 from 32-bit UNIX Time counter.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------------|------------|--|-------|-------|-------|-------|-------|-------|-------|
| 1Eh | UNIX Time 3 | R/WP | UNIX 3 [31:24] | | | | | | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | UNIX 3 [31:24] | 00h to FFh | Bit 24 to 31 from 32-bit UNIX counter. | | | | | | | |

3.11. RAM REGISTERS

Two free RAM bytes, which can be used for any purpose, for example, status bytes of the system.

1Fh – User RAM 1

This register holds the bits for general purpose use.

Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------------|------------|-------------|-------|-------|-------|-------|-------|-------|-------|
| 1Fh | User RAM 1 | R/WP | RAM 1 | | | | | | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | RAM 1 | 00h to FFh | RAM 1 data | | | | | | | |

20h – User RAM 2

This register holds the bits for general purpose use.

Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------------|------------|-------------|-------|-------|-------|-------|-------|-------|-------|
| 20h | User RAM 2 | R/WP | RAM 2 | | | | | | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | RAM 2 | 00h to FFh | RAM 2 data | | | | | | | |

3.12. PASSWORD REGISTERS

After a Power up and the first refreshment time $t_{PREFR} = \sim 66$ ms, the Password PW registers are reset to 00h. When enabled by writing 255 into the EEPROM Password Enable register EEPWE (EEPROM 30h) the Password PW registers are used to be written with the 32-Bit Password necessary to be able to write in all writable registers that have the convention WP (time, control, user RAM, configuration EEPROM and user EEPROM registers). The 32-Bit Password PW is compared to the 32 bits stored in the RAM mirror of the EEPROM Password EEPW (see EEPROM PASSWORD REGISTERS).

21h – Password 0

Bit 0 to 7 from 32-bit Password.
Write only. Returns 0 when read.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------------|------------|---------------------------------|-------|-------|-------|-------|-------|-------|-------|
| 21h | Password 0 | W | PW 0 [7:0] | | | | | | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | PW 0 [7:0] | 00h to FFh | Bit 0 to 7 from 32-bit Password | | | | | | | |

22h – Password 1

Bit 8 to 15 from 32-bit Password.
Write only. Returns 0 when read.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------------|------------|----------------------------------|-------|-------|-------|-------|-------|-------|-------|
| 22h | Password 1 | W | PW 1 [15:8] | | | | | | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | PW 1 [15:8] | 00h to FFh | Bit 8 to 15 from 32-bit Password | | | | | | | |

23h – Password 2

Bit 16 to 23 from 32-bit Password.
Write only. Returns 0 when read.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|--------------|------------|-----------------------------------|-------|-------|-------|-------|-------|-------|-------|
| 23h | Password 2 | W | PW 2 [23:16] | | | | | | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | PW 2 [23:16] | 00h to FFh | Bit 16 to 23 from 32-bit Password | | | | | | | |

24h – Password 3

Bit 24 to 31 from 32-bit Password.
Write only. Returns 0 when read.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|--------------|------------|-----------------------------------|-------|-------|-------|-------|-------|-------|-------|
| 24h | Password 3 | W | PW 3 [31:24] | | | | | | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | PW 3 [31:24] | 00h to FFh | Bit 24 to 31 from 32-bit Password | | | | | | | |

3.13. EEPROM MEMORY CONTROL REGISTERS

See also EEPROM READ/WRITE.

25h – EE Address

This register holds the Address used for read or write from/to a single EEPROM Memory byte.

Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------------|------------|--|-------|-------|-------|-------|-------|-------|-------|
| 25h | EE Address | R/WP | EEADDR | | | | | | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | EEADDR | 00h to FFh | Address for direct read or write one EEPROM Memory byte. | | | | | | | |

26h – EE Data

This register holds the Data that are read from, or that are written to a single EEPROM Memory byte.

Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|------------|--|-------|-------|-------|-------|-------|-------|-------|
| 26h | EE Data | R/WP | EEDATA | | | | | | | |
| | Reset | | X | X | X | X | X | X | X | X |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | EEDATA | 00h to FFh | Data from direct read or for direct write to one EEPROM Memory byte. | | | | | | | |

27h – EE Command

This register must be written with specific values, in order to Update or Refresh all (readable/writeable) Configuration EEPROM registers or to read or write from/to a single EEPROM Memory byte.

Before using this commands, the automatic refresh function has to be disabled (EERD = 1) and the busy status bit EEbusy has to indicate, that the last transfer has been finished (EEbusy = 0). Before entering the command 11h, 12h, 21h or 22h, EECMD has to be written with 00h.

Write only. Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------------|-------|--|-------|-------|-------|-------|-------|-------|-------|
| 27h | EE Command | WP | EECMD | | | | | | | |
| | Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | EECMD | | Commands for EEPROM Memory (see EEPROM READ/WRITE) | | | | | | | |
| | | 00h | First command must be 00h. – Default value | | | | | | | |
| | | 11h | UPDATE (ALL CONFIGURATION RAM → EEPROM). When writing a value of 11h, data from all Configuration RAM mirror bytes (address 30h to 37h) are written (stored) into the corresponding Configuration EEPROM bytes. See also USE OF THE CONFIGURATION REGISTERS. | | | | | | | |
| | | 12h | REFRESH (ALL CONFIGURATION EEPROM → RAM). When writing a value of 12h, data from all Configuration EEPROM bytes are read and copied into the corresponding Configuration RAM mirror bytes (address 30h to 37h). Functions become active as soon as the RAM bytes are written. | | | | | | | |
| | | 21h | WRITE TO ONE EEPROM BYTE (EEDATA (RAM) → EEPROM). When writing a value of 21h, data from the EEDATA (RAM) byte are written (stored) into the EEPROM byte with the address specified in the EEADDR byte. For Configuration EEPROM (address 30h to 37h) and User EEPROM (address 00h to 2Ah). | | | | | | | |
| | | 22h | READ ONE EEPROM BYTE (EEPROM → EEDATA (RAM)). When writing a value of 22h, data from the EEPROM byte with the address specified in EEADDR byte are read and copied into the EEDATA (RAM) byte. For Configuration EEPROM (address 30h to 37h) and User EEPROM (address 00h to 2Ah). | | | | | | | |

3.14. ID REGISTER

28h – ID

This register holds the 4 bit Hardware Identification number (HID) and the 4 bit Version Identification number (VID). The ID can be used to monitor a hardware modification and the version in the production line. Read only. Writing to this register has no effect.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|---------|---------------------------------|-------|-------|-------|---------------------|-------|-------|-------|
| 28h | ID | R | HID | | | | VID | | | |
| | Reset | | Preconfigured Value | | | | Preconfigured Value | | | |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:4 | HID | 0 to 15 | Hardware Identification number. | | | | | | | |
| 3:0 | VID | 0 to 15 | Version Identification number. | | | | | | | |

3.15. CONFIGURATION EEPROM WITH RAM MIRROR REGISTERS

All **Configuration EEPROM** at addresses 2Bh and 30h to 37h are memorized in the EEPROM and mirrored in the RAM. Functions become active as soon as the RAM mirror bytes are written. See also USE OF THE CONFIGURATION REGISTERS.

3.15.1. EEPROM RESERVED

2Bh – EEPROM RESERVED

This preconfigured (Factory Calibrated) value must not be overwritten. Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------------------|-------|---|-------|-------|-------|-------|-------|-------|-------|
| 2Bh | EEPROM Reserved | R/WP | RESERVED (Must not be overwritten) | | | | | | | |
| | Default value on delivery | | Preconfigured (Factory Calibrated) | | | | | | | |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | RESERVED | | Preconfigured (Factory Calibrated) – Must not be overwritten. | | | | | | | |

3.15.2. EEPROM PASSWORD ENABLE REGISTER

After a Power up and the first refreshment time $t_{PREFR} = \sim 66$ ms, the Password Enable value EEPWE is copied from the EEPROM to the corresponding RAM mirror. The default value preset on delivery is 00h.

30h – EEPROM Password Enable

Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------------------|----------|--|-------|-------|-------|-------|-------|-------|-------|
| 30h | EEPROM Password Enable | R/WP | EEPWE | | | | | | | |
| | Default value on delivery | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | EEPWE | | EEPROM Password Enable | | | | | | | |
| | | 0 to 254 | Password function disabled. When writing a value not equal 255, the password function is disabled. – 00h is the default value preset on delivery | | | | | | | |
| | | 255 | Password function enabled. When writing a value of 255, the Password registers (21h to 24h) can be used to enter the 32-bit Password. | | | | | | | |

3.15.3. EEPROM PASSWORD REGISTERS

After a Power up and the first refreshment time $t_{PREFR} = \sim 66$ ms, the EEPROM Password registers 0 to 3 with the 32-bit EEPROM Password are copied from the EEPROM to the corresponding RAM mirror. The default values preset on delivery are 00h.

31h – EEPROM Password 0

Bit 0 to 7 from 32-bit EEPROM Password.

RAM mirror is Write only. Returns 0 when read. EEPROM can be READ when Unlocked.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--|---------------------------|------------|--|-------|-------|-------|-------|-------|-------|-------|
| 31h | EEPROM Password 0 | *WP | EEPW 0 [7:0] | | | | | | | |
| | Default value on delivery | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | EEPW 0 [7:0] | 00h to FFh | Bit 0 to 7 from 32-bit EEPROM Password | | | | | | | |
| * EEPROM registers: RAM mirror is Write only. Returns 0 when read. EEPROM can be READ when Unlocked. | | | | | | | | | | |

32h – EEPROM Password 1

Bit 8 to 15 from 32-bit EEPROM Password.

RAM mirror is Write only. Returns 0 when read. EEPROM can be READ when Unlocked.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--|---------------------------|------------|---|-------|-------|-------|-------|-------|-------|-------|
| 32h | EEPROM Password 1 | *WP | EEPW 1 [15:8] | | | | | | | |
| | Default value on delivery | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | EEPW 1 [15:8] | 00h to FFh | Bit 8 to 15 from 32-bit EEPROM Password | | | | | | | |
| * EEPROM registers: RAM mirror is Write only. Returns 0 when read. EEPROM can be READ when Unlocked. | | | | | | | | | | |

33h – EEPROM Password 2

Bit 16 to 23 from 32-bit EEPROM Password.

RAM mirror is Write only. Returns 0 when read. EEPROM can be READ when Unlocked.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--|---------------------------|------------|--|-------|-------|-------|-------|-------|-------|-------|
| 33h | EEPROM Password 2 | *WP | EEPW 2 [23:16] | | | | | | | |
| | Default value on delivery | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | EEPW 2 [23:16] | 00h to FFh | Bit 16 to 23 from 32-bit EEPROM Password | | | | | | | |
| * EEPROM registers: RAM mirror is Write only. Returns 0 when read. EEPROM can be READ when Unlocked. | | | | | | | | | | |

34h – EEPROM Password 3

Bit 24 to 31 from 32-bit EEPROM Password.

RAM mirror is Write only. Returns 0 when read. EEPROM can be READ when Unlocked.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--|---------------------------|------------|--|-------|-------|-------|-------|-------|-------|-------|
| 34h | EEPROM Password 3 | *WP | EEPW 3 [31:24] | | | | | | | |
| | Default value on delivery | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | EEPW 3 [31:24] | 00h to FFh | Bit 24 to 31 from 32-bit EEPROM Password | | | | | | | |
| * EEPROM registers: RAM mirror is Write only. Returns 0 when read. EEPROM can be READ when Unlocked. | | | | | | | | | | |

3.15.4. EEPROM CLKOUT REGISTER

35h – EEPROM Clkout

A programmable square wave output is available at CLKOUT pin. Clock output can be controlled by the CLKOE bit (or by the CLKF flag) (see PROGRAMMABLE CLOCK OUTPUT). After a Power up and the first refreshment time $t_{PREFR} = \sim 66$ ms, the EEPROM Clkout values CLKOE, CLKS_Y, PORIE and FD are copied from the EEPROM to the corresponding RAM mirror. The default values preset on delivery are: CLKOUT = enabled, synchronization enabled, F = 32.768 kHz.

Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
|---|---|--|---|-------------------|-------|-------|-------|-------|-------|-------|--|
| 35h | EEPROM Clkout | R/WP | CLKOE | CLKS _Y | - | - | PORIE | FD | | | |
| | Default value on delivery | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | |
| Bit | Symbol | Value | Description | | | | | | | | |
| 7 | CLKOE | CLKOUT Enable bit (see PROGRAMMABLE CLOCK OUTPUT) | | | | | | | | | |
| | | 0 | The CLKOUT pin is LOW (if CLKF flag is 0). | | | | | | | | |
| | | 1 | The clock output signal on CLKOUT pin is enabled. – Default value on delivery | | | | | | | | |
| 6 | CLKS _Y | CLKOUT Synchronized enable/disable (see SYNCHRONIZED ENABLE/DISABLE) | | | | | | | | | |
| | | 0 | Disabled | | | | | | | | |
| | | 1 | Enables the Synchronized enable/disable (by CLKOE bit or CLKF flag) of the CLKOUT frequency. – Default value on delivery | | | | | | | | |
| 5:4 | - | 0 | Bit not implemented. Will return a 0 when read. | | | | | | | | |
| 3 | PORIE | Power On Reset Interrupt Enable bit (see POWER ON RESET INTERRUPT FUNCTION) | | | | | | | | | |
| | | 0 | No interrupt signal is generated on INT pin when a Power On Reset occurs or the signal is cancelled on INT pin. – Default value on delivery | | | | | | | | |
| | | 1 | An interrupt signal is generated on INT pin when a Power On Reset occurs. This setting is retained until the PORF flag is cleared to 0 (no automatic cancellation). | | | | | | | | |
| 2:0 | FD | 000 to 111 | CLKOUT Frequency Selection (see CLKOUT FREQUENCY SELECTION) | | | | | | | | |
| FD value | CLKOUT Frequency Selection | | Effect when writing 1 to the RESET bit or when writing to the Seconds register | | | | | | | | |
| 000 | 32.768 kHz – Default value on delivery | | No effect | | | | | | | | |
| 001 | 8192 Hz ⁽¹⁾ | | Affects current period | | | | | | | | |
| 010 | 1024 Hz ⁽¹⁾ | | Affects current period | | | | | | | | |
| 011 | 64 Hz ⁽¹⁾ | | Affects current period | | | | | | | | |
| 100 | 32 Hz ⁽¹⁾ | | Affects current period | | | | | | | | |
| 101 | 1 Hz ⁽¹⁾ | | Affects current period | | | | | | | | |
| 110 | Predefined periodic countdown timer interrupt ⁽¹⁾ ⁽²⁾ | | Affects current period | | | | | | | | |
| 111 | CLKOUT = LOW | | No effect | | | | | | | | |
| ⁽¹⁾ 8192 Hz to 1 Hz clock pulses and the timer interrupt pulses can be affected by compensation pulses (see FREQUENCY OFFSET CORRECTION). ⁽²⁾ CLKS _Y bit has no effect. | | | | | | | | | | | |

3.15.5. EEPROM OFFSET REGISTER

The registers EEPROM Offset and EEPROM Backup hold the EEOffset value to digitally compensate the initial frequency deviation of the 32.768 kHz oscillator or for aging adjustment. EEOffset defines correction pulses in steps. Each pulse introduces a deviation of 0.9537 ppm, the maximum range is from +243.2 ppm to -244.1 ppm. The value of 0.9537 ppm is based on a nominal 32.768 kHz clock (see FREQUENCY OFFSET CORRECTION). The preconfigured (Factory Calibrated) EEOffset value may be changed by the user.

36h – EEPROM Offset

This register holds the upper 8 bits of the EEOffset value. The preconfigured (Factory Calibrated) EEOffset value may be changed by the user. The least significant bit (LSB) of the EEOffset value is located in register EEPROM Backup (37h) (see also EEPROM BACKUP REGISTER).

After a Power up and the first refreshment time $t_{\text{PREFR}} = \sim 66$ ms, the EEPROM Offset value is copied from the EEPROM to the corresponding RAM mirror.

Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------|---------------------------|--------------|--|-------|-------|-------|-------|-------|-------|-------|
| 36h | EEPROM Offset | R/WP | EEOffset [8:1] | | | | | | | |
| | Default value on delivery | | Preconfigured (Factory Calibrated) | | | | | | | |
| Bit | Symbol | Value | Description | | | | | | | |
| 7:0 | EEOffset [8:1] | 00h to FFh | Upper 8 bits of the EEOffset value. See table below. | | | | | | | |

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------|---------------------------|--------------|---|-------|-------|-------|-------|-------|-------|-------|
| 37h | EEPROM Backup | R/WP | EEOffset [0] | BSIE | TCE | FEDE | BSM | | TCR | |
| | Default value on delivery | | Preconfigured | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | EEOffset [0] | 0 or 1 | LSB of the EEOffset value. See table below. | | | | | | | |

EEOffset (9 bits):

| EEOffset [8:0] | EEOffset correction value in decimal | Correction pulses in steps | CLKOUT frequency correction in ppm ^(*) |
|----------------|--------------------------------------|----------------------------|---|
| 01111111 | 255 | 255 | 243.187 |
| 01111110 | 254 | 254 | 242.233 |
| : | : | : | : |
| 00000001 | 1 | 1 | 0.954 |
| 00000000 | 0 | 0 | 0.000 |
| 11111111 | 511 | -1 | -0.954 |
| 11111110 | 510 | -2 | -1.907 |
| : | : | : | : |
| 10000001 | 257 | -255 | -243.187 |
| 10000000 | 256 | -256 | -244.141 |

(*) Each correction pulse corresponds to $1 / (16384 \times 64) = 0.9537$ ppm.

The frequency deviation measured at CLKOUT pin can be compensated by computing the correction value EEOffset and writing it into the EEPROM Offset and EEPROM Backup registers (see FREQUENCY OFFSET CORRECTION).

3.15.6. EEPROM BACKUP REGISTER

37h – EEPROM Backup

This register is used to control the switchover function and the trickle charger and it holds bit 0 (LSB) of the EEOffset value. The preconfigured (Factory Calibrated) EEOffset value may be changed by the user.

After a Power up and the first refreshment time $t_{PREFR} = \sim 66$ ms, the EEPROM Backup value is copied from the EEPROM to the corresponding RAM mirror.

Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------------------|--|---|-------|-------|-------|-------|-------|-------|-------|
| 37h | EEPROM Backup | R/WP | EEOffset [0] | BSIE | TCE | FEDE | BSM | | TCR | |
| | Default value on delivery | | Preconfigured | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 | EEOffset [0] | 0 to 1 | LSB of the EEOffset value (see EEPROM OFFSET REGISTER). | | | | | | | |
| 6 | BSIE | Backup Switchover Interrupt Enable bit (see AUTOMATIC BACKUP SWITCHOVER FUNCTION and AUTOMATIC BACKUP SWITCHOVER INTERRUPT FUNCTION) | | | | | | | | |
| | | 0 | No interrupt signal is generated on \overline{INT} pin when an Automatic Backup Switchover occurs or the signal is cancelled on \overline{INT} pin. – Default value on delivery | | | | | | | |
| | | 1 | An interrupt signal is generated on \overline{INT} pin when an Automatic Backup Switchover occurs. This setting is retained until the BSF flag is cleared to 0 (no automatic cancellation). | | | | | | | |
| 5 | TCE | Trickle Charger Enable bit (see TRICKLE CHARGER) | | | | | | | | |
| | | 0 | Disabled – Default value on delivery | | | | | | | |
| | | 1 | Enabled | | | | | | | |
| 4 | FEDE | Fast Edge Detection Enable bit (see AUTOMATIC BACKUP SWITCHOVER FUNCTION and AUTOMATIC BACKUP SWITCHOVER INTERRUPT FUNCTION) | | | | | | | | |
| | | 0 | Disabled. | | | | | | | |
| | | 1 | FEDE should always be set to 1. When the FEDE bit is 1, the Fast Edge Detection for the Automatic Backup Switchover function is enabled. A voltage on V_{DD} power supply pin with an increasing or falling edge with a slew rate typically greater than 7 V/ms can be correctly detected and the Automatic Backup Switchover function is adapted to this particular situation. – Default value on delivery | | | | | | | |
| 3:2 | BSM | Backup Switchover Mode (see AUTOMATIC BACKUP SWITCHOVER FUNCTION and AUTOMATIC BACKUP SWITCHOVER INTERRUPT FUNCTION) To read/write from/to the EEPROM, the user has to disable the Backup Switchover function by setting the BSM field to 00 or 10 (see routine in EEPROM READ/WRITE CONDITIONS) | | | | | | | | |
| | | 00 | Switchover Disabled. – Default value on delivery | | | | | | | |
| | | 01 | Enables the Direct Switching Mode (DSM). Switchover when $V_{DD} < V_{BACKUP}$. | | | | | | | |
| | | 10 | Switchover Disabled. | | | | | | | |
| | | 11 | Enables the Level Switching Mode (LSM). Switchover when $V_{DD} < V_{TH,LSM}$ (2.0 V) AND $V_{BACKUP} > V_{TH,LSM}$ (2.0 V). | | | | | | | |
| 1:0 | TCR | Trickle Charger Series Resistance (see TRICKLE CHARGER) | | | | | | | | |
| | | 00 | TCR 3 k Ω – Default value on delivery | | | | | | | |
| | | 01 | TCR 5 k Ω | | | | | | | |
| | | 10 | TCR 9 k Ω | | | | | | | |
| | | 11 | TCR 15 k Ω | | | | | | | |

3.16. USER EEPROM

00h – 2Ah – User EEPROM

43 Bytes of User EEPROM for general purpose storage are provided.

Read: Always readable. Write: Can be write-protected by password.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------|-------------|-------|--------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| 00h to 2Ah | User EEPROM | R/WP | 43 Bytes of non-volatile User EEPROM | | | | | | | |

3.17. RESERVED EEPROM

2Ch – 2Fh and 38h – 3Fh – Reserved EEPROM

Protected. Writing to this register has no effect.

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------|-----------------|-------|----------|-------|-------|-------|-------|-------|-------|-------|
| 2Ch to 2Fh | Reserved EEPROM | Prot. | RESERVED | | | | | | | |
| 38h to 3Fh | Reserved EEPROM | Prot. | RESERVED | | | | | | | |

3.18. REGISTER RESET VALUES SUMMARY

Reset values; RAM, Address 00h to 3Fh:

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|----------------------------|-------|---------------------|-------|-------|-------|---------------------|-------|-------|-------|
| 00h | Seconds | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 01h | Minutes | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 02h | Hours (24h / 12h) | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 03h | Weekday | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 04h | Date | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 05h | Month | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 06h | Year | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 07h | Minutes Alarm | R/WP | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 08h | Hours Alarm (24h / 12h) | R/WP | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 09h | Weekday Alarm / Date Alarm | R/WP | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Ah | Timer Value 0 | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Bh | Timer Value 1 | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Ch | Timer Status 0 | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Dh | Timer Status 1 shadow | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Eh | Status | R/WP | 1 → 0 | 0 | 0 | 0 → 1 | 0 | 0 | 0 | 1 |
| 0Fh | Control 1 | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 10h | Control 2 | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 11h | GP Bits | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 12h | Clock Int. Mask | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 13h | Event Control | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 14h | Count TS | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 15h | Seconds TS | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 16h | Minutes TS | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 17h | Hours TS (24h / 12h) | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 18h | Date TS | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 19h | Month TS | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1Ah | Year TS | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1Bh | UNIX Time 0 | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1Ch | UNIX Time 1 | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1Dh | UNIX Time 2 | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1Eh | UNIX Time 3 | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1Fh | User RAM 1 | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 20h | User RAM 2 | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 21h | Password 1 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 22h | Password 2 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 23h | Password 3 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 24h | Password 4 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 25h | EE Address | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 26h | EE Data | R/WP | X | X | X | X | X | X | X | X |
| 27h | EE Command | WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 28h | ID | R | Preconfigured Value | | | | Preconfigured Value | | | |
| 29h and 2Ah | RESERVED | Prot. | XXh | | | | | | | |
| 2Ch to 2Fh | RESERVED | Prot. | XXh | | | | | | | |
| 38h to 3Fh | RESERVED | Prot. | XXh | | | | | | | |

X = not defined

Default values on delivery; **Configuration EEPROM** with RAM mirror, Address 2Bh and 30h to 37h:

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------------------|-------|---|-------|-------|-------|-------|-------|-------|-------|
| 2Bh | EEPROM Reserved | R/WP | Preconfigured (Factory Calibrated) – Must not be overwritten. | | | | | | | |
| 30h | EEPROM PW Enable | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 31h | EEPROM Password 0 | WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 32h | EEPROM Password 1 | WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 33h | EEPROM Password 2 | WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 34h | EEPROM Password 3 | WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 35h | EEPROM Clkout | R/WP | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 36h | EEPROM Offset | R/WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 37h | EEPROM Backup | R/WP | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

Default values on delivery; **User EEPROM**, Address 00h to 2Ah:

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------|------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| 00h to 2Ah | User EEPROM (43 Bytes) | R/WP | 00h | | | | | | | |

Default values on delivery; **Reserved EEPROM**, Address 2Ch to 2Fh and 38h to 3Fh:

| Address | Function | Conv. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------|-----------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| 2Ch to 2Fh | Reserved EEPROM | Prot. | XXh | | | | | | | |
| 38h to 3Fh | Reserved EEPROM | Prot. | XXh | | | | | | | |

X = not defined

RV-3028-C7 reset values after power on (RAM) and default values on delivery (EEPROM):

RAM, reset values:

| | | |
|-------------------------|---|--|
| Time (hh:mm:ss) | = | 00:00:00 |
| Date (YY-MM-DD) | = | 00-01-01 |
| Weekday | = | 0 |
| Hour mode | = | 24 hour mode (0 to 23) |
| Count TS | = | 0 (read only) |
| Time TS (hh:mm:ss) | = | 00:00:00 (read only) |
| Date TS (YY-MM-DD) | = | 00-00-00 (read only) |
| UNIX Time | = | 00000000h |
| Alarm function | = | disabled, weekday is selected |
| Timer function | = | disabled, Timer Clock Frequency = 4096 Hz, Single Mode selected |
| Update function | = | Second update is selected |
| External Event function | = | Falling edge is regarded as External Event on pin EVI, first event is recorded |
| Time Stamp function | = | disabled, External Event selected, Time Stamp overwrite disabled, Time Stamp Reset disabled |
| EEPROM Memory Refresh | = | enabled |
| Interrupts | = | disabled |
| EEbusy status bit | = | 1 → 0 (1 for the time $t_{PREFR} = \sim 66$ ms, then it is cleared to 0 automatically) |
| UF Flag | = | 0 → 1 (Second update is selected) |
| EVF Flag | = | 0 |
| PORF Flag | = | 1 (can be cleared by writing 0 to the bit) |
| Int. Controlled Clock | = | disabled, no interrupt selected |
| Password | = | 00000000h (write only) |
| EE Address | = | 00h |
| EE Data | = | XXh |
| EE Command | = | 00h (first command) (write only) |
| ID | = | Preconfigured Value (read only) |
| General Purpose Bits | = | 0 (7 bits) |
| User RAM 1, 2 | = | 00h (2 bytes) |

Configuration EEPROM with RAM mirror, default values on delivery:

| | | |
|--------------------------|---|---|
| EEPROM Reserved (2Bh) | = | Preconfigured Value – Must not be overwritten |
| EEPROM Password Enable | = | disabled |
| EEPROM Password | = | 00000000h (write only) |
| CLKOUT | = | enabled, synchronization enabled, F = 32.768 kHz |
| Power On Reset Interrupt | = | disabled |
| EEOffset value | = | Preconfigured Value (9 bits) (may be changed by the user) |
| Backup Switchover | = | disabled, interrupt disabled, Fast Edge Detection enabled |
| Trickle charger | = | disabled, TCR 3 kΩ is selected |

User EEPROM, default values on delivery:

| | | |
|------------------------|---|-----|
| User EEPROM (43 Bytes) | = | 00h |
|------------------------|---|-----|

Reserved EEPROM, Address 2Ch to 2Fh and 38h to 3Fh, default values on delivery:

| | | |
|-----------------|---|-----------------|
| Reserved EEPROM | = | XXh (protected) |
|-----------------|---|-----------------|

4. DETAILED FUNCTIONAL DESCRIPTION

4.1. POWER ON RESET (POR)

The power on reset (POR) is generated at start-up (see POWER ON AC ELECTRICAL CHARACTERISTICS). All RAM registers including the Counter Registers are initialized to their reset values and the Configuration EEPROM registers with the RAM mirror registers are set to their preset default values. At power up a refresh of the RAM mirror values by the values in the Configuration EEPROM is automatically generated. The time of this first refreshment is $t_{\text{PREFR}} = \sim 66$ ms. The EEBusy bit in the Status register (0Eh) can be used to monitor the status of the refreshment (see REGISTER RESET VALUES SUMMARY).

The Power On Reset Flag PORF indicates the occurrence of a voltage drop of the internal power supply voltage below V_{POR} threshold needed to cause the generation of the device POR. A PORF value of 1 indicates that the voltage had dropped below the threshold level V_{POR} and that the time information is corrupted. The value 1 is retained until a 0 is written by the user.

When PORIE bit (EEPROM 35h) is set and the PORF flag was cleared beforehand, an interrupt signal on $\overline{\text{INT}}$ pin can be generated when a Power On Reset occurs (see POWER ON RESET INTERRUPT FUNCTION).

4.2. AUTOMATIC BACKUP SWITCHOVER FUNCTION

Basic Hardware Definitions:

- The RV-3028-C7 has two power supply pins.
 - V_{DD} is the main power supply input pin.
 - V_{BACKUP} is the backup power supply input pin.
- $V_{TH:LSM}$ (typical value 2.0 V) is the backup switchover threshold voltage in Level Switching Mode.
- A debounce logic provides a debounce time t_{DEB} of 122 μ s to 183 μ s, which will filter V_{DD} oscillation when the backup switchover will switch back from V_{BACKUP} to V_{DD} . I²C access is possible in VDD Power state after the debounce time t_{DEB} .
- The FEDE bit (EEPROM 37h) should always be set to 1, so that Fast Edge Detection (≥ 7 V/ms) is always enabled. – Default value on delivery

Switchover Modes:

The RV-3028-C7 has three backup switchover modes. The desired mode can be selected by the BSM field in the Configuration EEPROM, see EEPROM BACKUP REGISTER:

- BSM = 00 Switchover disabled (default value on delivery), see SWITCHOVER DISABLED.
- BSM = 01 Direct Switching Mode (DSM): when $V_{DD} < V_{BACKUP}$, switchover occurs from V_{DD} to V_{BACKUP} without requiring V_{DD} to drop below $V_{TH:LSM}$ (2.0 V), see DIRECT SWITCHING MODE (DSM).
- BSM = 10 Switchover disabled, see SWITCHOVER DISABLED.
- BSM = 11 Level Switching Mode (LSM): when $V_{DD} < V_{TH:LSM}$ (2.0 V) AND $V_{BACKUP} > V_{TH:LSM}$ (2.0 V), switchover occurs from V_{DD} to V_{BACKUP} , see LEVEL SWITCHING MODE (LSM).

Function Overview:

When a valid backup switchover condition occurs (Direct or Level Switching Mode) and the internal power supply switches to the V_{BACKUP} voltage (VBACKUP Power state) the following sequence applies:

- The Backup Switch Flag BSF is set and, if BSIE bit is 1 (EEPROM 37h), an interrupt will be generated on \overline{INT} pin and remains as long as BSF is not cleared to 0. If BSIE is 0 no interrupt will be generated (see AUTOMATIC BACKUP SWITCHOVER INTERRUPT FUNCTION).
- The I²C-bus interface is automatically disabled (high impedance) and reset.
- EVI input remains active for interrupt generation, interrupt driven clock output and time stamp function
- CLKOUT pin is held LOW during VBACKUP Power state.
- The interrupt output pin \overline{INT} remains active in VBACKUP Power state for any previously configured interrupt condition.
- Going into VBACKUP Power state can be used as a time stamp condition (see TIME STAMP FUNCTION).
- The backup switchover condition can also be used to enable the clock output on CLKOUT pin automatically, when again in VDD Power state (see AUTOMATIC BACKUP SWITCHOVER INTERRUPT FUNCTION).

The Backup Switch Flag BSF can be cleared using the I²C-bus interface as soon as the circuit resumes from VBACKUP Power state and switched back to V_{DD} .

4.2.1.SWITCHOVER DISABLED

The switchover function is disabled when BSM field (EEPROM 37h) is set to 00 or 10 (BSM = 00 is the default value on delivery).

1. Used when only one power supply is available (device is always in VDD Power state). The power supply is applied on VDD pin and the VBACKUP pin must be tied to VSS with a 10 kΩ resistor. The Backup Switch Flag BSF is always logic 0.
2. Used when VDD is turned off and VBACKUP is still present and the device must not draw any current from the backup source (IBACKUP = 0 nA). The backup source on VBACKUP pin is in standby mode until the device is powered up again from main supply VDD and a switchover mode is selected (see also TYPICAL CHARACTERISTICS).

When the device is first powered up from the backup supply (VBACKUP) but without a main supply (VDD), switchover is also disabled and the backup source is automatically in standby mode (IBACKUP = 0 nA).

4.2.2.DIRECT SWITCHING MODE (DSM)

This mode is selected with BSM = 01 (EEPROM 37h).

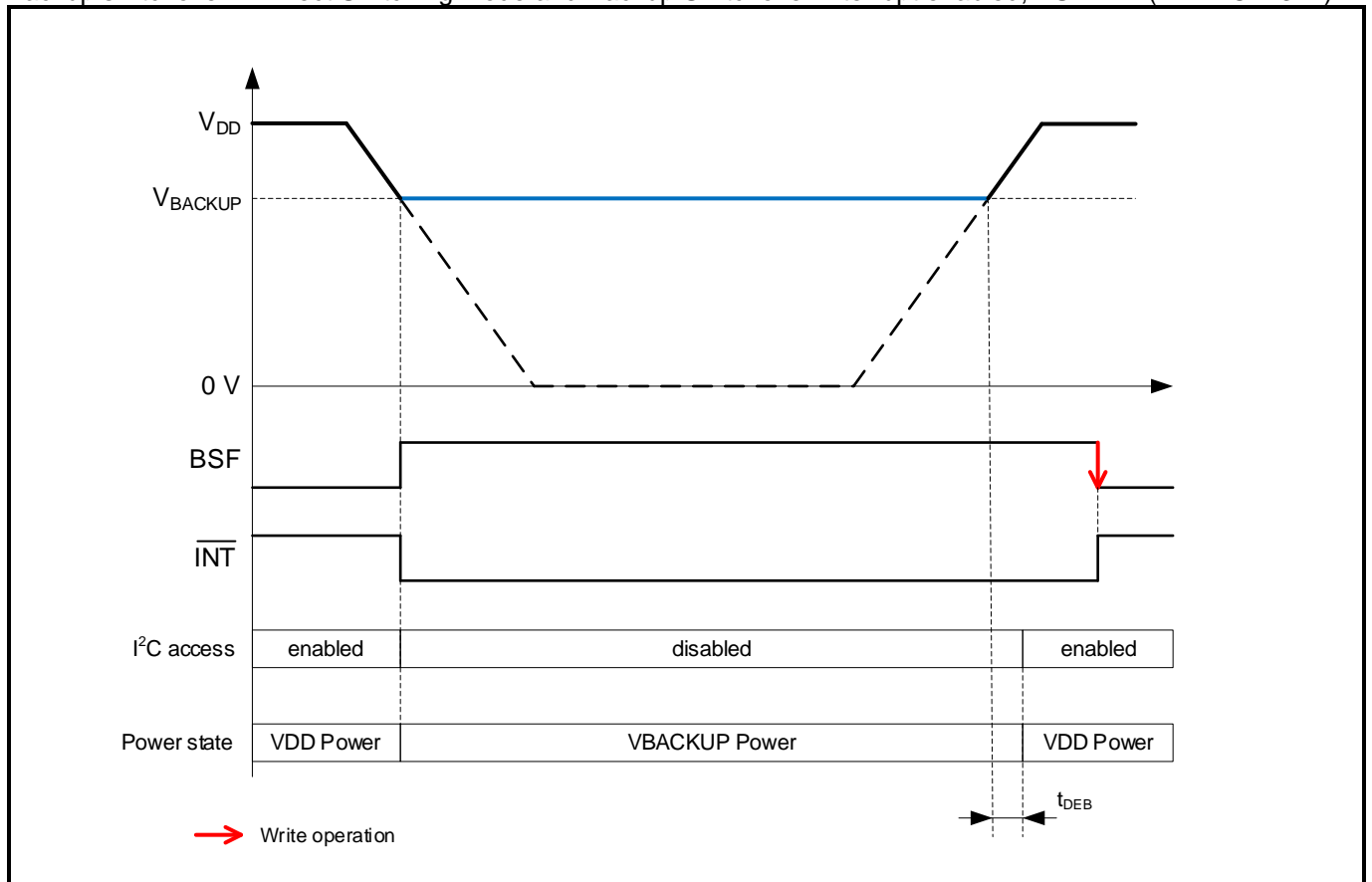
- If VDD > VBACKUP the internal power supply is VDD.
- If VDD < VBACKUP the internal power supply is VBACKUP.

The Direct Switching Mode is useful in systems where VDD is normally higher than VBACKUP (for example, VDD = 5.0 V, VBACKUP = 3.5 V). If the VDD and VBACKUP values are similar (for example, VDD = 3.3 V, VBACKUP ≥ 3.0 V), the Direct Switching Mode is not recommended as this can lead to unnecessary switching.

In Direct Switching Mode, the power consumption is reduced compared to the Level Switching Mode (LSM) because VDD is not monitored and compared to the threshold voltage VTH:LSM = 2.0 V (typical IDD:DSM = 95 nA). See also OPERATING PARAMETERS and TYPICAL CHARACTERISTICS.

Note that the circuit needs in worst case 2 ms to react when changing from disabled switchover to DSM.

Backup switchover in Direct Switching Mode and Backup Switchover Interrupt enabled, BSIE = 1 (EEPROM 37h):



4.2.3.LEVEL SWITCHING MODE (LSM)

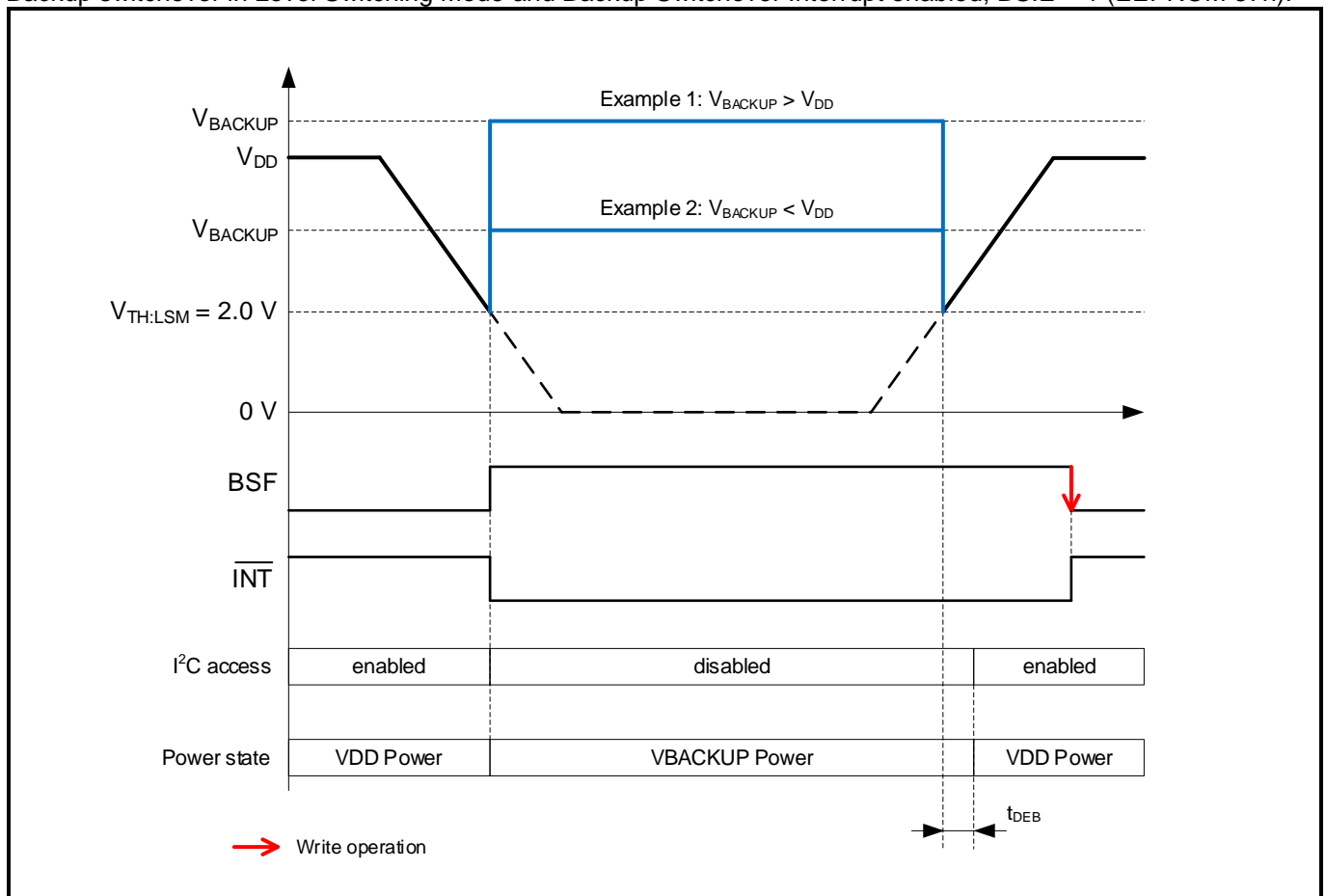
This mode is selected with BSM = 11 (EEPROM 37h).

- If $V_{DD} > V_{TH:LSM}$ (2.0 V), the internal power supply is V_{DD} .
- If $V_{DD} < V_{TH:LSM}$ (2.0 V) AND $V_{BACKUP} > V_{TH:LSM}$ (2.0 V), the internal power supply is V_{BACKUP} .

In Level Switching Mode, the power consumption is slightly increased compared to the Direct Switching Mode (DSM) because V_{DD} is monitored and compared to the threshold voltage $V_{TH:LSM} = 2.0$ V (typical $I_{DD:LSM} = 115$ nA). See also OPERATING PARAMETERS and TYPICAL CHARACTERISTICS.

Note that the circuit needs in worst case 15.625 ms to react when changing from disabled switchover to LSM.

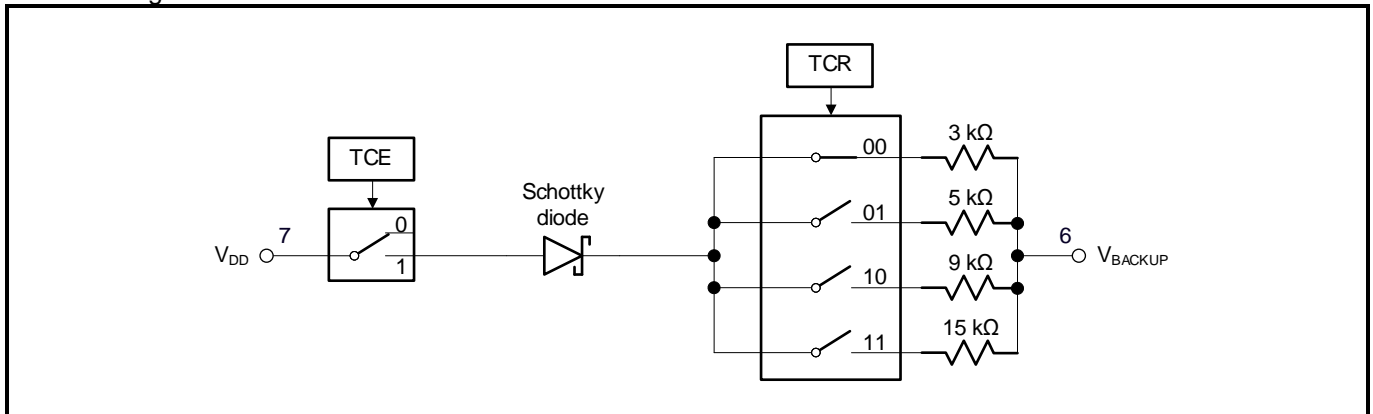
Backup switchover in Level Switching Mode and Backup Switchover Interrupt enabled, BSIE = 1 (EEPROM 37h):



4.3. TRICKLE CHARGER

The device supporting the V_{BACKUP} pin include a trickle charging circuit which allows a battery or supercapacitor connected to the V_{BACKUP} pin to be charged from the power supply connected to the V_{DD} pin. See figure below. In the register EEPROM 37h the Trickle Charger is enabled with bit TCE (default value on delivery is disabled) and the series current limiting resistor is selected by the TCR field (default value on delivery is 3 k Ω). A schottky diode, with a typical voltage drop of 0.25 V, is inserted in the charging path.

Trickle Charger:



The trickle charger is disabled when the device is in V_{BACKUP} Power state.

4.4. PROGRAMMABLE CLOCK OUTPUT

Six different frequencies or the countdown timer interrupt signal can be output on CLKOUT pin, the signal selection is done in the FD field (EEPROM 35h).

- 32.768 kHz, direct from Xtal oscillator, not offset compensated.
- 8192 Hz, 1024 Hz, 64 Hz, 32 Hz, 1 Hz; divided Xtal oscillator frequencies, digitally compensated according to the oscillator offset value EEOffset (EEPROM 36h and 37h).
- Timer interrupt is controlled by the Countdown Timer Control Registers and the Control 1 register.

The negative edge of the original 32,768 kHz clock signal is used to turn on and off a subsequent selected clock signal. The negative edge is also used to control the clock signal by flag CLKF , bit CLKOE and the FD field. Whenever the clock signal is LOW, it is pulled to V_{SS} .

CLKOUT is tied to V_{SS} in V_{BACKUP} Power state independent of the CLKOUT configuration settings.

The frequency output can be controlled directly via the I²C-bus interface commands (normal operation) or can be interrupt driven to allow waking up an external system by supplying a clock.

At POR the synchronization function is active since the bit CLKSY is set to 1 (default), the 32.768 kHz frequency is output to CLKOUT pin since the bit CLKOE is set to 1 (default) and FD field is set to 000 (default). Hint: These are the default values on delivery, stored in the Configuration EEPROM with RAM mirror. To customize these POR values, the user can change the values in the Configuration EEPROM.

4.4.1. CLKOUT FREQUENCY SELECTION

A programmable square wave is available at pin CLKOUT. Operation is controlled by the FD field (EEPROM 35h). Frequencies from 32.768 kHz (Default value on delivery) to 1 Hz and countdown timer interrupt can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the crystal oscillator.

Pin CLKOUT is a push-pull output that is enabled at power on (Default value on delivery). CLKOUT can be disabled by setting CLKOE bit to 0 (if CLKF flag is 0) or by setting FD field to 111. When disabled, the CLKOUT pin is LOW.

The RESET bit function can affect the CLKOUT signal depending on the selected frequency. When writing 1 to the RESET bit or when writing to the Seconds register and the CLKOUT is enabled, the current period of the frequencies 8192 Hz to 1 Hz are affected (for more details, see RESET BIT FUNCTION).

CLKOUT Frequency Selection:

| FD value | CLKOUT Frequency Selection | Effect when writing 1 to the RESET bit or when writing to the Seconds register |
|----------|---|--|
| 000 | 32.768 kHz –Default value on delivery | No effect |
| 001 | 8192 Hz ⁽¹⁾ | Affects current period |
| 010 | 1024 Hz ⁽¹⁾ | Affects current period |
| 011 | 64 Hz ⁽¹⁾ | Affects current period |
| 100 | 32 Hz ⁽¹⁾ | Affects current period |
| 101 | 1 Hz ⁽¹⁾ | Affects current period |
| 110 | Predefined periodic countdown timer interrupt ⁽¹⁾ ⁽²⁾ | Affects current period |
| 111 | CLKOUT = LOW | No effect |

⁽¹⁾ 8192 Hz to 1 Hz clock pulses and the timer interrupt pulses can be affected by correction pulses (see FREQUENCY OFFSET CORRECTION).
⁽²⁾ CLKSY bit has no effect.

4.4.2. NORMAL CLOCK OUTPUT

Condition: The CLKF flag is 0.

Setting bit CLKOE to 1 will drive the selected frequency on CLKOUT, setting CLKOE to 0 will clear the selected frequency on CLKOUT. See CLOCK OUTPUT SCHEME.

4.4.3. INTERRUPT CONTROLLED CLOCK OUTPUT

Condition: The CLKOE bit is 0.

Writing 1 to CLKIE the occurrence of the selected interrupt condition allows frequency output on CLKOUT. This function allows waking up an external system by outputting a clock.

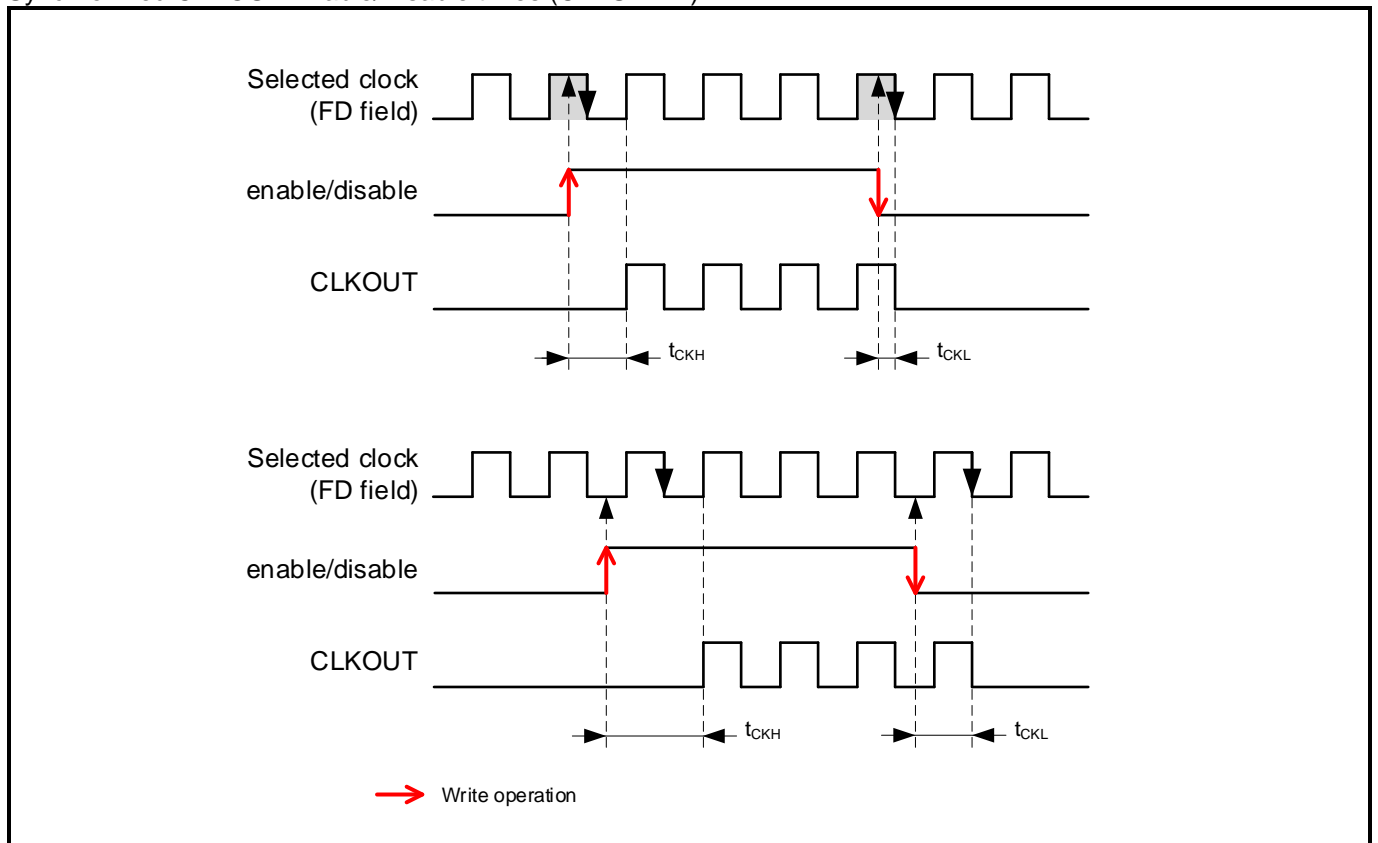
Writing 0 to CLKIE will disable new interrupts from driving frequencies on CLKOUT, but if there is already an active interrupt driven frequency output (CLKF flag is set), the active frequency output will not be stopped. Writing the CLKF flag to 0 will clear the flag and frequency output will stop. See CLOCK OUTPUT SCHEME.

4.4.4.SYNCHRONIZED ENABLE/DISABLE

The enabled Synchronized CLKOUT Enable/Disable function (CLKSY = 1) consists of two sub-functions.

- Synchronized CLKOUT enable (t_{CKH}). For enabling clock output on CLKOUT pin the internal first negative clock edge of the selected clock source (FD field) is detected after CLKF or CLKOE are set.
- Synchronized CLKOUT disable (t_{CKL}). Clock output on CLKOUT will be disabled at the next negative clock edge of the selected clock source (FD field) after both CLKF and CLKOE are cleared and after the I²C-bus interface stop condition. When disabled, CLKOUT is tied to V_{SS} .
(CLKF and CLKOE = 0 → disable condition → next negative clock edge → CLKOUT driven to V_{SS})

Synchronized CLKOUT Enable/Disable times (CLKSY = 1):

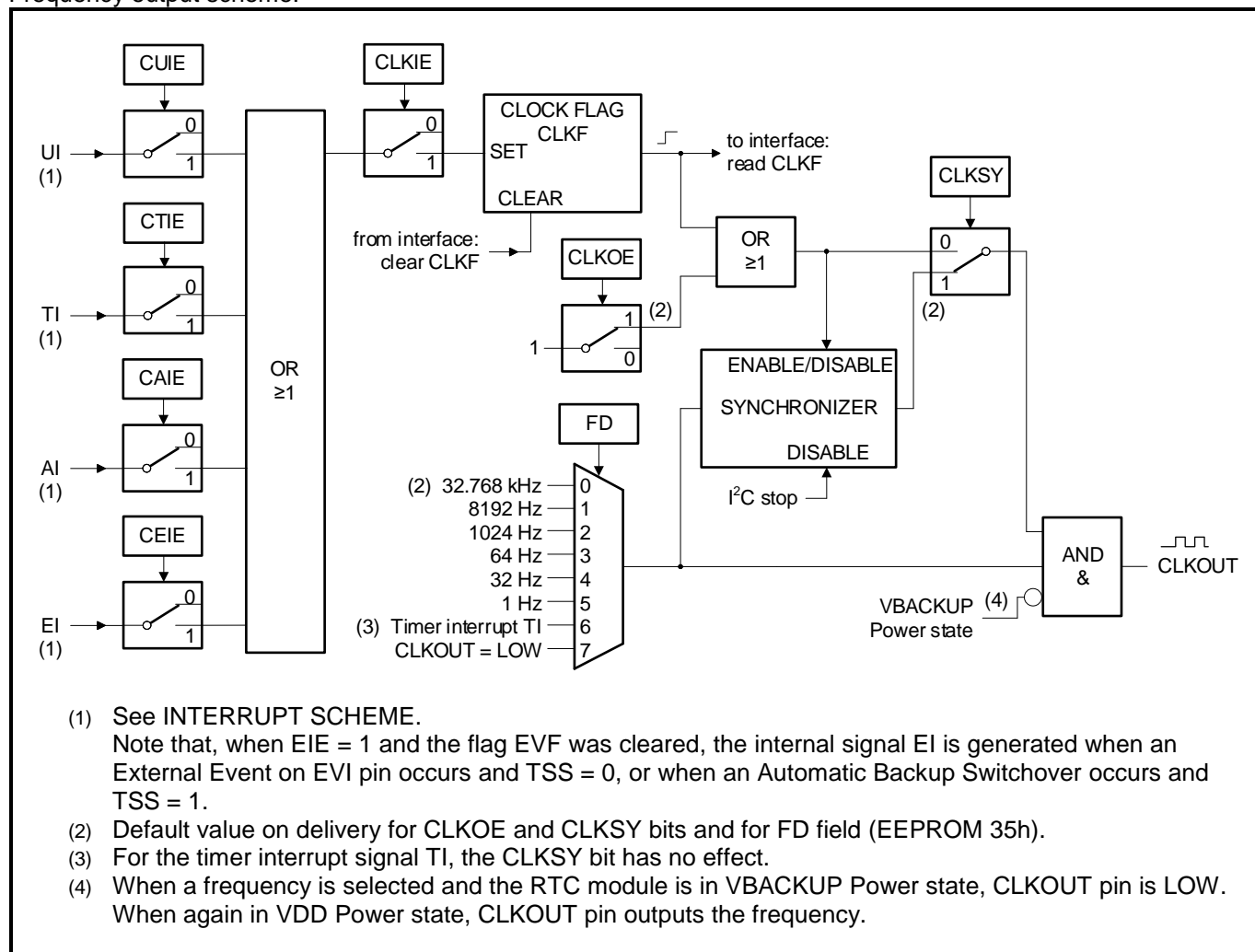


Hint: Glitch free frequency change on CLKOUT requires clearing flag CLKF and bit CLKOE to 0 before the new clock is selected in FD field.

(CLKF and CLKOE = 0 → disable condition → next negative clock edge → CLKOUT driven to V_{SS} → FD field selection → CLKF and/or CLKOE = 1 → enable condition → next negative clock edge)

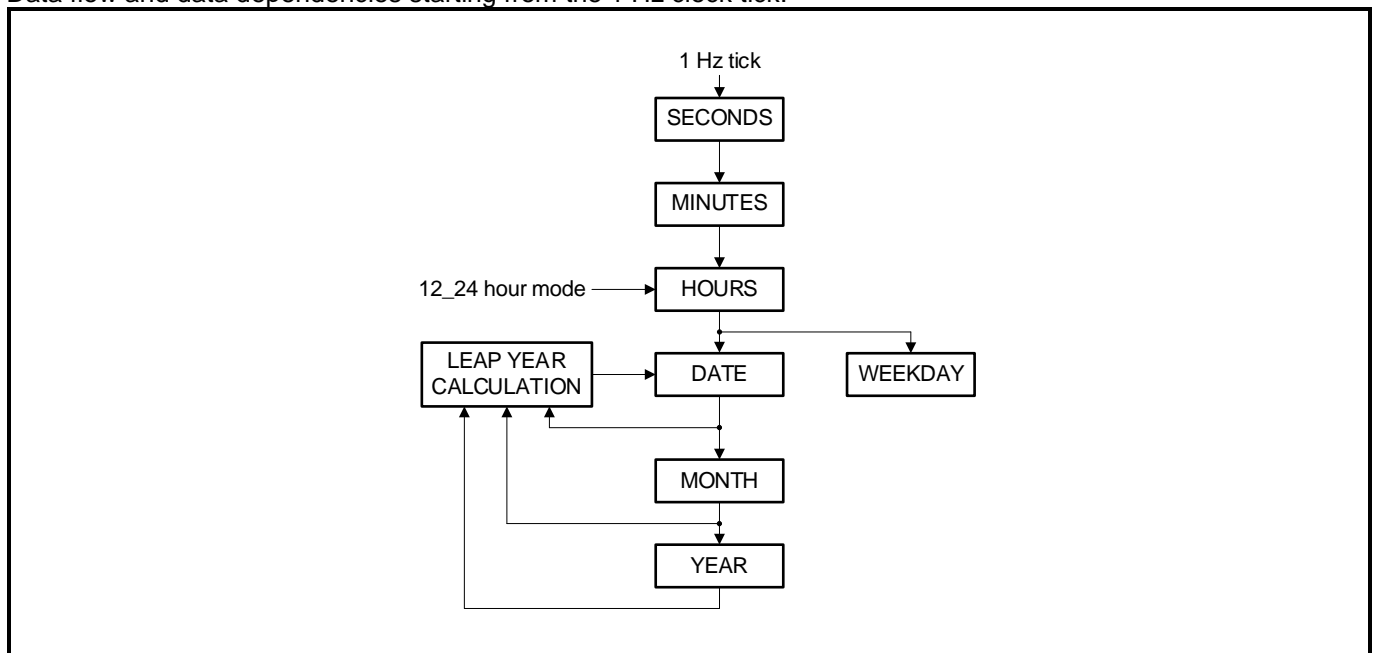
4.4.5.CLOCK OUTPUT SCHEME

Frequency output scheme:



4.5. SETTING AND READING THE TIME

Data flow and data dependencies starting from the 1 Hz clock tick:

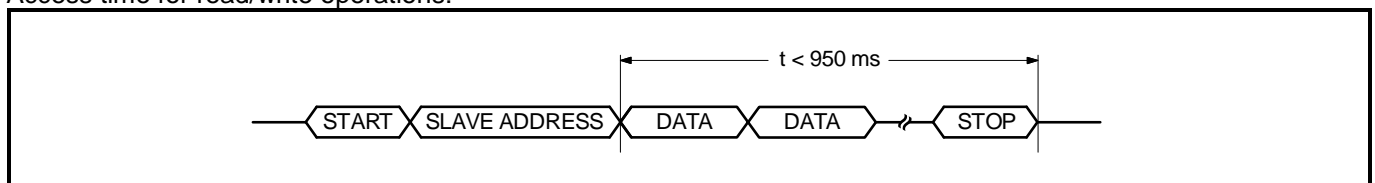


During an I²C read/write access to any RTC register that takes less than 950 milliseconds, all time counters (clock and calendar registers 00h to 06h) of the RV-3028-C7 are blocked. During this time the clock counter increment (1 Hz tick) is inhibited to allow coherent data values. One counter increment (maximum one 1 Hz tick) occurring during inhibition time is memorized and will be realized after the I²C STOP condition.

Exception: If during the inhibition time a 1 is written to the RESET bit or a value is written to the Seconds register an eventual present memorized 1 Hz update is reset and the prescaler frequencies from 8192 Hz to 1 Hz are reset. Resetting the prescaler will have an influence on the length of the current clock period on all subsequent peripherals (clock and calendar, CLKOUT, timer clock, update timer clock, UNIX clock, EVI input filter), (see also RESET BIT FUNCTION).

When I²C read/write access has been terminated within 950 milliseconds ($t < 950 \text{ ms}$), the time counters are unblocked with the I²C STOP condition and a pending request to increment the time counters that occurred during read or write access is correctly applied. Maximum one 1 Hz tick can be handled (see following Figure).

Access time for read/write operations:



Because of this method, it is very important to make a read or write access in one go, that is, setting or reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

Hint: The UNIX Time counter does not know such register blocking (see UNIX TIME COUNTER).

4.5.1.SETTING THE TIME

During an I²C read/write access to any RTC register with an access time of less than 950 ms, the time counters are blocked. After I²C STOP condition a possibly memorized 1 Hz tick is realized.

Advantage of register blocking:

- Prevents faulty writing to the clock and calendar registers during an I²C write access (no incrementing of time registers during the write access).
- After writing, one memorized 1 Hz tick is handled. Clock and calendar are updated.
- No reading is needed for control. The written data are coherent.

If the I²C write access takes longer than 950 ms the I²C bus interface is reset by the internal bus timeout function. In this case the previous time counter values are maintained, the pending 1 Hz tick is realized and the clock counter increment (1 Hz tick) continues to operate normally. Restarting of communications begins with transfer of the START condition again.

The I²C auto increment Address Pointer is not reset by the I²C STOP condition nor by the internal stop forced after timeout.

Two methods for setting the time can be distinguished:

1. Setting the time registers including Seconds register. Writing to the Seconds register resets an eventual present memorized 1 Hz update and resets the prescaler frequencies from 8192 Hz to 1 Hz (synchronization).
2. Setting the time registers without Seconds register. A possibly memorized 1 Hz tick during write access will be realized. Old synchronicity persists.

Hint: Instead of writing to the Seconds register to synchronize the time counters the RESET BIT FUNCTION can be applied. When writing 1 to the RESET bit, the value in the Seconds register does not change, but it also resets the prescaler frequencies from 8192 Hz to 1 Hz (synchronization).

4.5.2.READING THE TIME

During an I²C read/write access to any RTC register with an access time of less than 950 ms, the time counters are blocked. After I²C STOP condition a possibly memorized 1 Hz tick is realized.

Advantage of register blocking:

- Prevents faulty reading of the clock and calendar registers during an I²C read access (no incrementing of time registers during the read access).
- After reading, one memorized 1 Hz tick is handled. Clock and calendar are updated.
- No second reading is needed for control. The read data are coherent.

If the I²C read access takes longer than 950 ms the I²C bus interface is reset by the internal bus timeout function. In this case all data that is read has a value of FFh, the pending 1 Hz tick is realized and the clock counter increment (1 Hz tick) continues to operate normally. Restarting of communications begins with transfer of the START condition again.

The I²C auto increment Address Pointer is not reset by the I²C STOP condition nor by the internal stop forced after timeout.

4.6. EEPROM READ/WRITE

4.6.1. POR REFRESH (ALL CONFIGURATION EEPROM → RAM)

Automatic read of all Configuration EEPROM registers at Power On Reset (POR):

- At power up a refresh of the Configuration RAM mirror values by the values in the Configuration EEPROM is automatically generated (see REGISTER RESET VALUES SUMMARY).
- The time of this first refreshment is $t_{\text{PREFR}} = \sim 66$ ms.
- The EEbusy bit in the register Status (0Eh) can be used to monitor the status of the refreshment.

4.6.2. AUTOMATIC REFRESH (ALL CONFIGURATION EEPROM → RAM)

Read all Configuration EEPROM registers automatically:

- To keep the integrity of the configuration data, all data of the Configuration RAM are refreshed by the data in the Configuration EEPROM each 24 hours, at date increment (at the beginning of the last second before midnight).
- The time of this automatic refreshment is $t_{\text{AREFR}} = \sim 3.5$ ms.
- Refresh is only active when RV-3028-C7 is not in VBACKUP mode and not disabled by EERD (EEPROM Memory Refresh Disable) bit.
- Hint: It is not always necessary/meaningful to turn off the auto-refresh (EERD = 1) before an EEPROM access. e.g. if the current RTC time is 1 hour AM, etc.

4.6.3. UPDATE (ALL CONFIGURATION RAM → EEPROM)

Write to all Configuration EEPROM registers (see also USE OF THE CONFIGURATION REGISTERS):

- Before starting to change the configuration stored in the EEPROM, the auto refresh of the registers from the EEPROM has to be disabled by writing 1 into the EERD control bit.
- Then the new configuration can be written into the configuration RAM registers, when the whole new configuration is in the registers, writing the command 00h into the register EECMD, then the second command 11h into the register EECMD will start the copy of the configuration into the EEPROM.
- The time of the update is $t_{\text{UPDATE}} = \sim 63$ ms.
- When the transfer is finished (EEbusy = 0), the user can enable again the auto refresh of the registers by writing 0 into the EERD bit in the Control 1 register.

4.6.4. REFRESH (ALL CONFIGURATION EEPROM → RAM)

Read all Configuration EEPROM registers:

- Before starting to read the configuration stored in the EEPROM, the auto refresh of the registers from the EEPROM has to be disabled by writing 1 into the EERD control bit.
- Then the actual configuration can be read from the Configuration EEPROM registers, writing the command 00h into the register EECMD, and then the second command 12h into the register EECMD will start the copy of the configuration into the RAM.
- The time of this controlled refreshment is $t_{\text{REFR}} = \sim 3.5$ ms.
- Functions become active as soon as the RAM bytes are written.
- When the transfer is finished (EEbusy = 0), the user can enable again the auto refresh of the registers by writing 0 into the EERD bit in the Control 1 register.

4.6.5. WRITE TO ONE EEPROM BYTE (EEDATA (RAM) → EEPROM)

Write to one EEPROM byte of the Configuration EEPROM or User EEPROM registers:

- Before starting to change data stored in the EEPROM, the auto refresh of the registers from the EEPROM has to be disabled by writing 1 into the EERD control bit.
- In order to write a single byte to the EEPROM, the address to which the data must be written is entered in the EEADDR register and the data to be written is entered in the EEDATA register, then the command 00h is written in the EECMD register, then a second command 21h is written in the EECMD register to start the EEPROM write.
- The time to write to one EEPROM byte is $t_{WRITE} = \sim 16$ ms.
- When the transfer is finished (EEbusy = 0), the user can enable again the auto refresh of the registers by writing 0 into the EERD bit in the Control 1 register.

4.6.6. READ ONE EEPROM BYTE (EEPROM → EEDATA (RAM))

Read one EEPROM byte from Configuration EEPROM or User EEPROM registers:

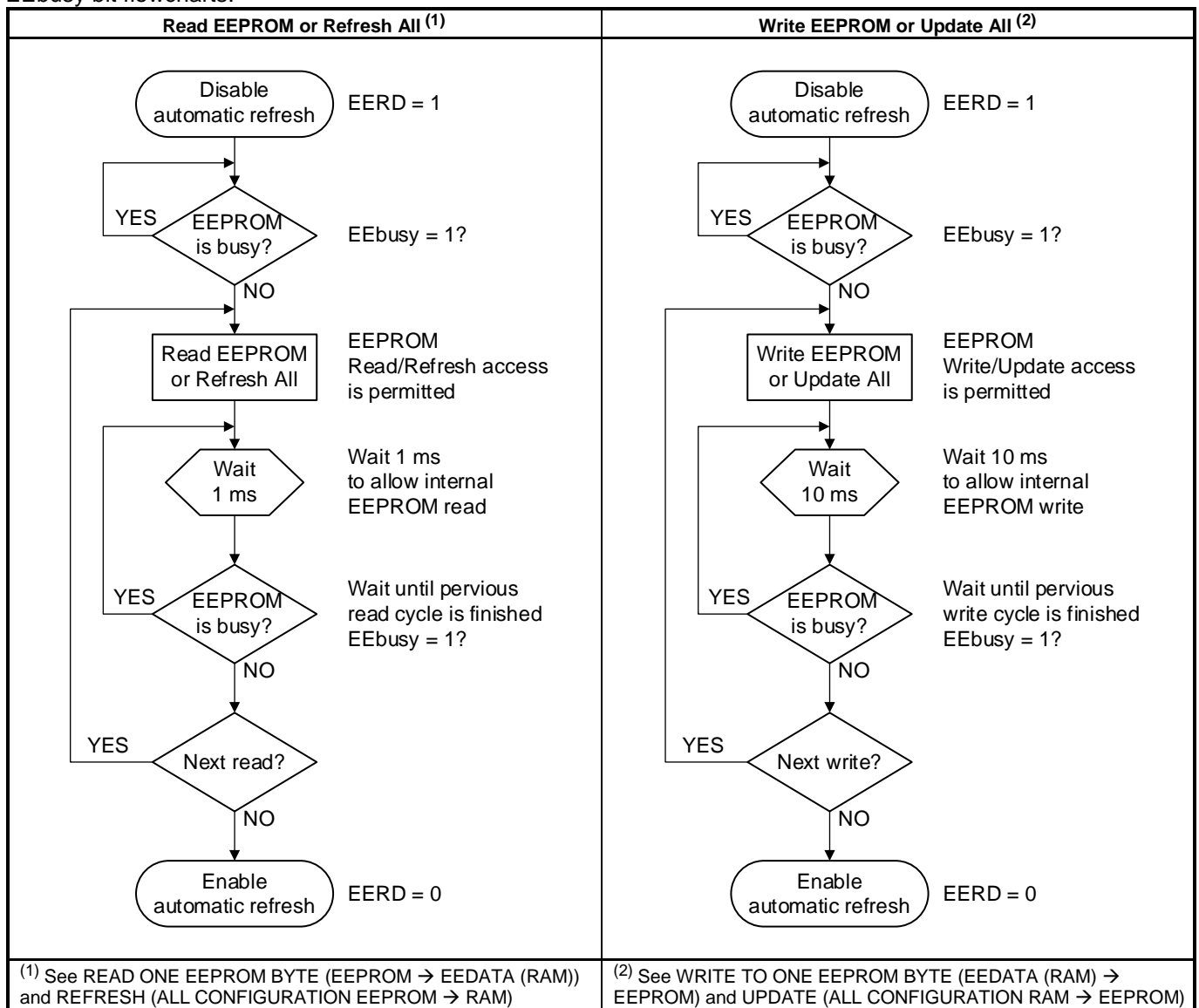
- Before starting to read a byte in the EEPROM, the auto refresh of the registers from the EEPROM has to be disabled by writing 1 into the EERD control bit.
- In order to read a single byte from the EEPROM, the address to be read is entered in the EEADDR register, then the command 00h is written in the EECMD register, then the second command 22h is written in the EECMD register and the resulting byte can be read from the EEDATA register.
- The time to read one EEPROM byte is $t_{READ} = \sim 1.4$ ms.
- When the transfer is finished (EEbusy = 0), the user can enable again the auto refresh of the registers by writing 0 into the EERD bit in the Control 1 register.

4.6.7.EEBUSY BIT

The set EEBusy status bit (bit 7 in the Status register 0Eh) indicates that the EEPROM is currently handling a read or write request and will ignore any further commands until the current one is finished. At power up a refresh is automatically generated. The time of this first refreshment is $t_{PREFR} = \sim 66$ ms. After the refreshment is finished; EEBusy is cleared to 0 automatically. The cleared EEBusy status bit indicates that the EEPROM transfer is finished. To prevent access collision between the internal automatic EEPROM refresh cycle (EERD = 0) and external EEPROM read/write access through interface the following procedures have to be applied.

- Set EERD = 1 Automatic EEPROM Refresh needs to be disabled before EEPROM access.
- Check for EEBusy = 0 Access EEPROM only if not busy.
- Clear EERD = 0 It is recommended to enable Automatic EEPROM Refresh at the end of read/write access.
- Write EEPROM Wait 10 ms after each written EEPROM register before checking for EEBusy = 0 to allow internal data transfer (for Read EEPROM, wait 1 ms).

EEbusy bit flowcharts:



Note: A minimum power supply voltage of $V_{DD:WRITE} = 1.5$ V during the whole EEPROM write procedure is required; i.e. until EEBusy = 0.

4.6.8. EEPROM READ/WRITE CONDITIONS

During a read/write of the EEPROM, if the V_{DD} supply drops, the device will continue to operate and communicate until a switchover to V_{BACKUP} occurs (in DSM or LSM mode). It is not recommended to operate during this time and all I²C communication should be halted as soon as V_{DD} failure is detected.

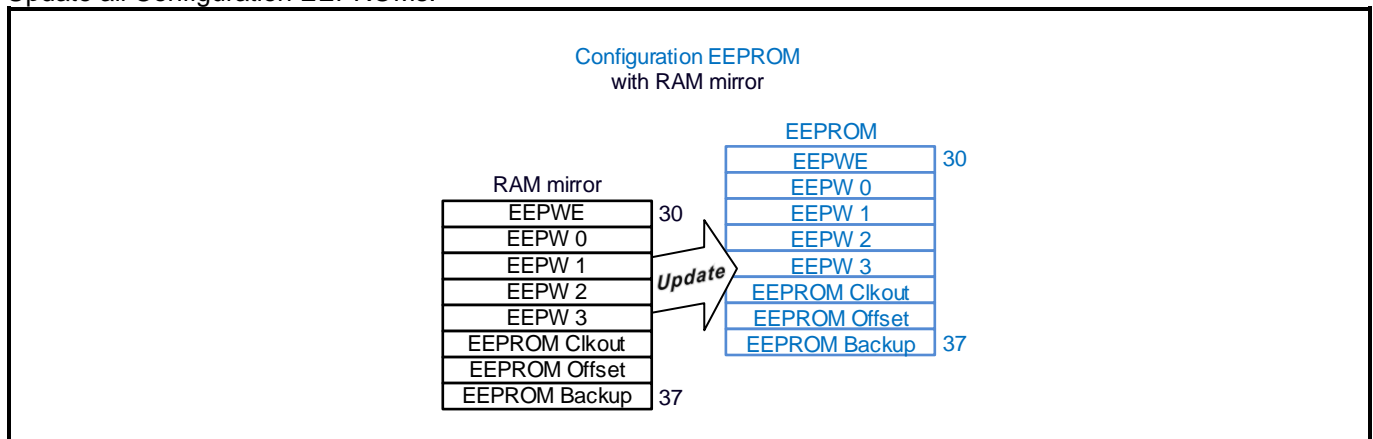
During the time that data is being written to the EEPROM, V_{DD} should remain above the minimum write voltage $V_{DD:WRITE} = 1.5$ V. If at any time V_{DD} drops below this voltage, the data written to the device get corrupted.

To write to the EEPROM, the backup switchover circuit must switch back to the main power supply V_{DD} . See also AUTOMATIC BACKUP SWITCHOVER FUNCTION.

4.6.9. USE OF THE CONFIGURATION REGISTERS

The best practice method to use the Configuration EEPROM with RAM mirror registers at addresses 30h to 37h is to make all Configuration settings in the RAM first and then to update all Configuration EEPROMs by the Update EEPROM command.

Update all Configuration EEPROMs:



The method, how to enable/disable write protection and how to change the reference password can be found in section USER PROGRAMMABLE PASSWORD (Configuration Registers 30h to 34h).

Configuration Registers 35h to 37h:

- EEPROM CLKOUT REGISTER, 35h – EEPROM Clkout
- EEPROM OFFSET REGISTER, 36h – EEPROM Offset
- EEPROM BACKUP REGISTER, 37h – EEPROM Backup

Edit the Configuration settings (example, when write protection is enabled (EEPWE = 255)):

1. Enter the correct password PW (PW = EEPW) to unlock write protection
2. Disable automatic refresh by setting EERD = 1
3. Edit Configuration settings in registers 35h to 37h (RAM)
4. Update EEPROM (all Configuration RAM → EEPROM) by setting EECMD = 00h followed by 11h
5. Enable automatic refresh by setting EERD = 0
6. Enter an incorrect password PW (PW ≠ EEPW) to lock the device

Note: RAM mirror of the Configuration registers defines the active zone. By writing only to the EEPROM, the configurations are not active. The configurations are activated as soon as a refresh occurs (POR refresh, Automatic refresh or Refresh by software).

Note: To perform certain tests, it is sufficient to use only the RAM mirror. But the new, changed configurations are lost as soon as a refresh occurs (POR refresh, Automatic refresh or Refresh by software).

4.7. INTERRUPT OUTPUT

The interrupt pin $\overline{\text{INT}}$ can be triggered by six different functions:

- PERIODIC COUNTDOWN TIMER INTERRUPT FUNCTION
- PERIODIC TIME UPDATE INTERRUPT FUNCTION
- ALARM INTERRUPT FUNCTION
- EXTERNAL EVENT INTERRUPT FUNCTION
- AUTOMATIC BACKUP SWITCHOVER INTERRUPT FUNCTION
- POWER ON RESET INTERRUPT FUNCTION

4.7.1. SERVICING INTERRUPTS

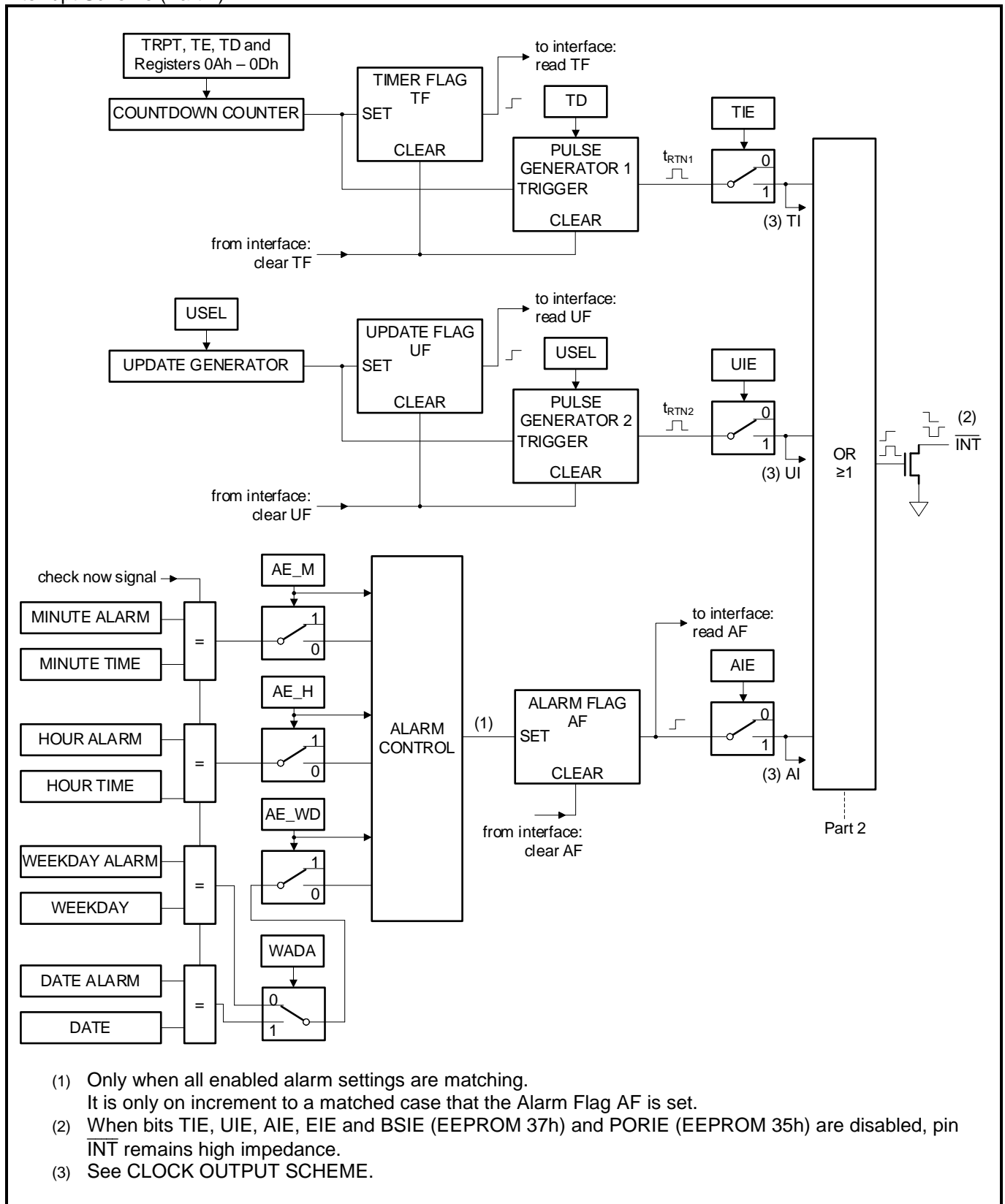
The $\overline{\text{INT}}$ pin can indicate six types of interrupts. It outputs the logic OR operation result of these interrupt outputs. When an interrupt is detected (when $\overline{\text{INT}}$ pin produces a negative pulse or is at low level), the TF, UF, AF, EVF, BSF and PORF flags can be read to determine which interrupt event has occurred.

To keep $\overline{\text{INT}}$ pin from changing to low level, clear the TIE, UIE, AIE, EIE and BSIE (EEPROM 37h) and PORIE (EEPROM 35h) bits. To check whether an event has occurred without outputting any interrupts via the $\overline{\text{INT}}$ pin, software can read the TF, UF, AF, EVF, BSF and PORF interrupt flags (polling).

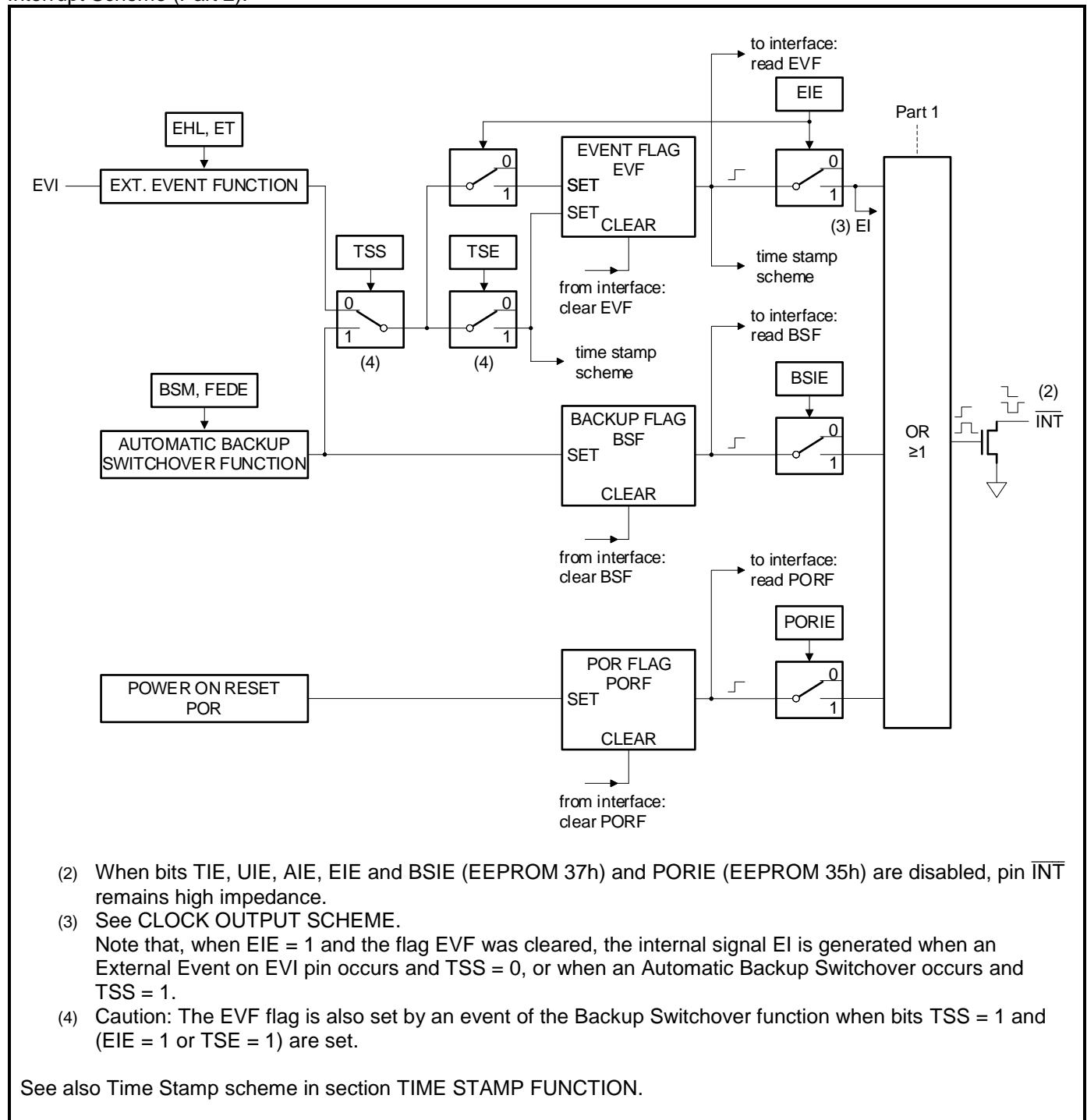
Caution: The EVF flag is also set by an event of the Backup Switchover function when bits TSS and TSE are set to 1.

4.7.2. INTERRUPT SCHEME

Interrupt Scheme (Part 1):



Interrupt Scheme (Part 2):



4.8. PERIODIC COUNTDOWN TIMER INTERRUPT FUNCTION

The Periodic Countdown Timer Interrupt function generates an interrupt event once (see SINGLE MODE (TRPT = 0)) or periodically (see REPEAT MODE (TRPT = 1)) at any period set from 244.14 μ s to 4095 minutes.

When starting the countdown timer for the first time, only the first period does not have a fixed duration. The amount of inaccuracy for the first timer period depends on the selected source clock (see FIRST PERIOD DURATION).

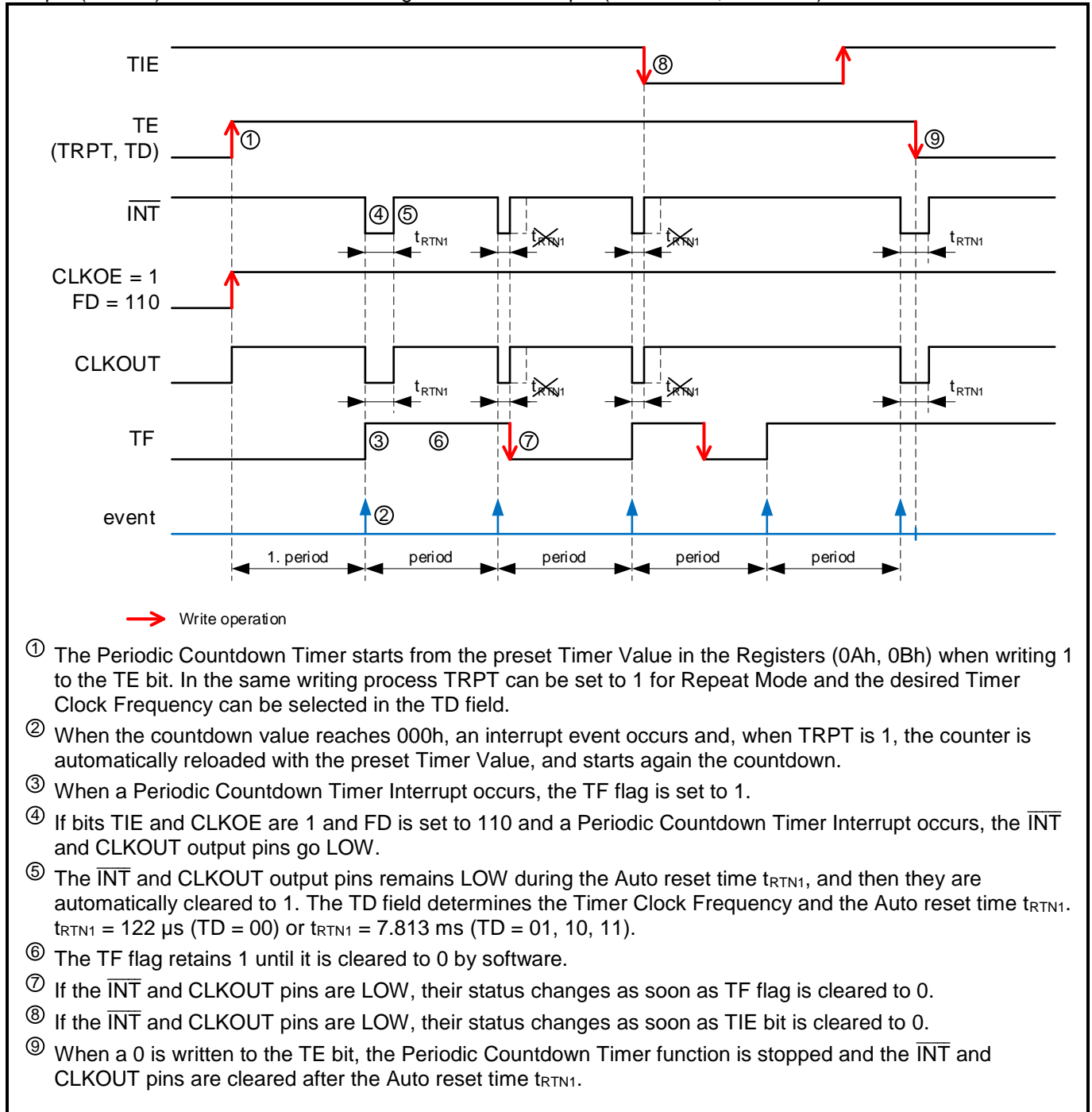
When an interrupt event is generated, the $\overline{\text{INT}}$ pin goes to the low level and the TF flag is set to 1 to indicate that an event has occurred. The output on the $\overline{\text{INT}}$ pin is only effective if the TIE bit in the Control 2 register is set to 1. The low-level output signal on $\overline{\text{INT}}$ pin (and on CLKOUT pin, when driven by TI signal) is automatically cleared after the Auto reset time t_{RTN1} or it is cancelled when TF flag is cleared to 0.

- When TD = 00, $t_{\text{RTN1}} = 122 \mu\text{s}$
- When TD = 01, 10 or 11, $t_{\text{RTN1}} = 7.813 \text{ ms}$

When bit TIE is set to 1, the internal countdown timer interrupt pulse (TI) can be used to enable the clock output on CLKOUT pin automatically if CTIE and CLKIE bits are set to 1 and CLKOE bit is cleared to 0 and a frequency is selected in the FD field. The interrupt pulses (TI) can even be used as CLKOUT frequency, when selecting 110 in the FD field (see CLOCK OUTPUT SCHEME).

4.8.1.PERIODIC COUNTDOWN TIMER DIAGRAM

Diagram of the Periodic Countdown Timer Interrupt function: Example with Repeat Mode (TRPT = 1), Interrupt on INT pin (TIE = 1) and Countdown Timer Signal on CLKOUT pin (CLKOE = 1, FD = 110).



4.8.2.USE OF THE PERIODIC COUNTDOWN TIMER INTERRUPT

The following registers, fields and bits are related to the Periodic Countdown Timer Interrupt and Automatic Clock output function:

- Timer Value 0 Register (0Ah) (see PERIODIC COUNTDOWN TIMER CONTROL REGISTERS)
- Timer Value 1 Register (0Bh) (see PERIODIC COUNTDOWN TIMER CONTROL REGISTERS)
- Timer Status 0 Register (0Ch) (see PERIODIC COUNTDOWN TIMER CONTROL REGISTERS)
- Timer Status 1 shadow Register (0Dh) (see PERIODIC COUNTDOWN TIMER CONTROL REGISTERS)
- TF flag (see STATUS AND CONTROL REGISTERS, 0Eh – Status)
- TRPT bit, TE bit and TD field (see STATUS AND CONTROL REGISTERS, 0Fh – Control 1)
- TIE bit (see STATUS AND CONTROL REGISTERS, 10h – Control 2)
- CTIE bit (see STATUS AND CONTROL REGISTERS, 12h – Clock Interrupt Mask)

For selecting Countdown Timer Signal for CLKOUT pin (CLKOE = 1 and FD = 110):

- CLKOE bit and FD field (see EEPROM CLKOUT REGISTER, 35h – EEPROM Clkout)

Prior to entering any timer settings for the Periodic Countdown Timer Interrupt, it is recommended to write a 0 to the TIE and TE bits to prevent inadvertent interrupts on $\overline{\text{INT}}$ pin. When writing 1 to the RESET bit or writing a value to the Seconds register affects the length of a current countdown period (see RESET BIT FUNCTION). When the Periodic Countdown Timer Interrupt function is not used, one Timer Value register (0Ah) can be used as RAM byte. The Timer Clock Frequency selection field TD is used to set the countdown period (source clock) for the Periodic Countdown Timer Interrupt function (four settings are possible).

Procedure to start the Periodic Countdown Timer Interrupt function and the Automatic Clock output function:

1. Initialize bits TE, TIE and TF to 0. In that order, to prevent inadvertent interrupts on $\overline{\text{INT}}$ pin.
2. Set TRPT bit to 1 if periodic countdown is needed (Repeat Mode).
3. Choose the Timer Clock Frequency and write the corresponding value in the TD field.
4. Choose the Countdown Period based on the Timer Clock Frequency, and write the corresponding Timer Value to the registers Timer Value 0 (0Ah) and Timer Value 1 (0Bh). See following table.
5. Set the TIE bit to 1 if you want to get a hardware interrupt on $\overline{\text{INT}}$ pin.
6. Set CTIE bit to 1 to enable clock output when a timer interrupt occurs. See also CLOCK OUTPUT SCHEME.
7. Set the TIE and CLKOE bits to 1 and the FD field to 110 if you want to get the timer signal on CLKOUT.
8. Set the TE bit from 0 to 1 to start the Periodic Countdown Timer. The countdown starts at the rising edge of the SCL signal after Bit 0 of the Address 0Fh is transferred. See subsequent Figure that shows the start timing.

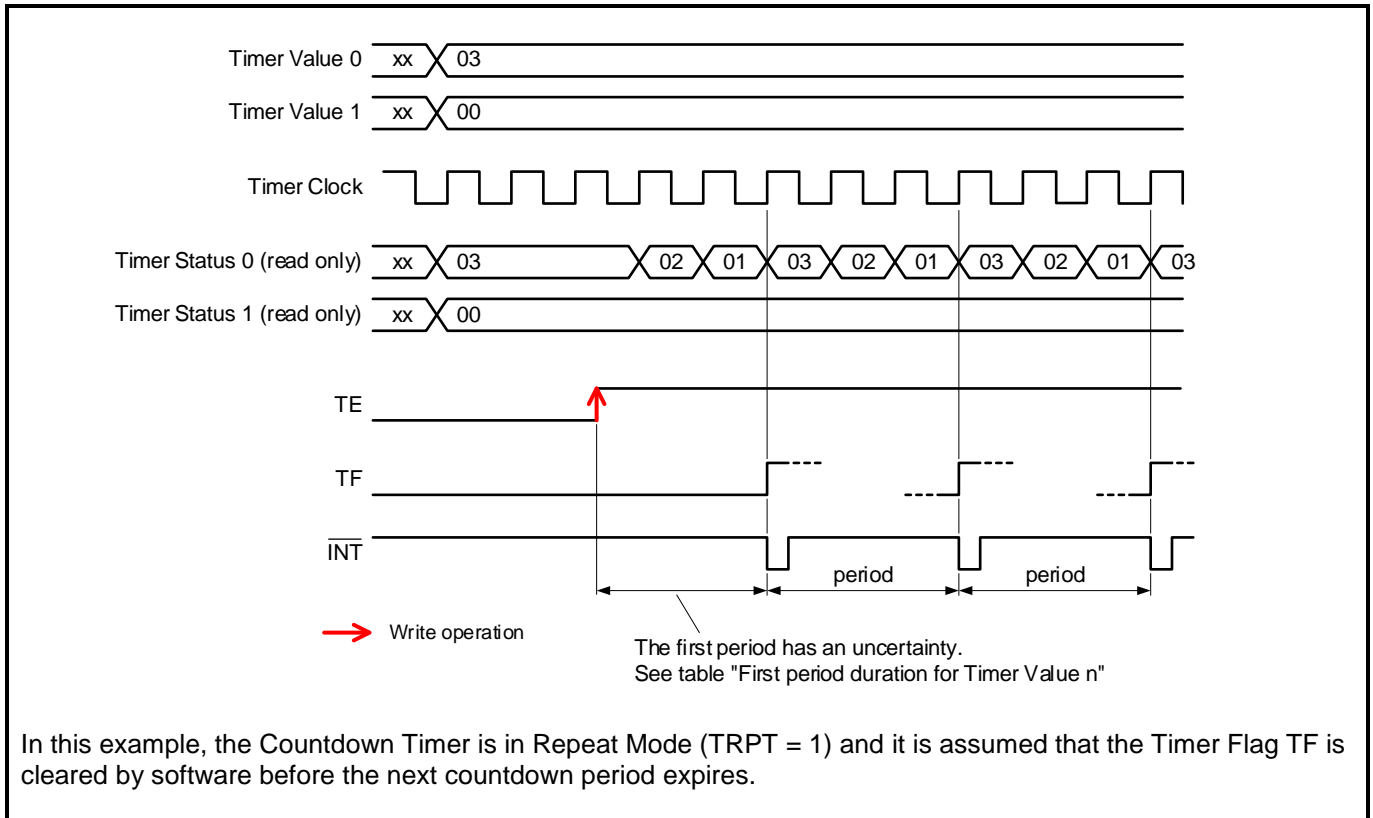
Countdown Period in seconds:

$$\text{Countdown Period} = \frac{\text{Timer Value}}{\text{Timer Clock Frequency}}$$

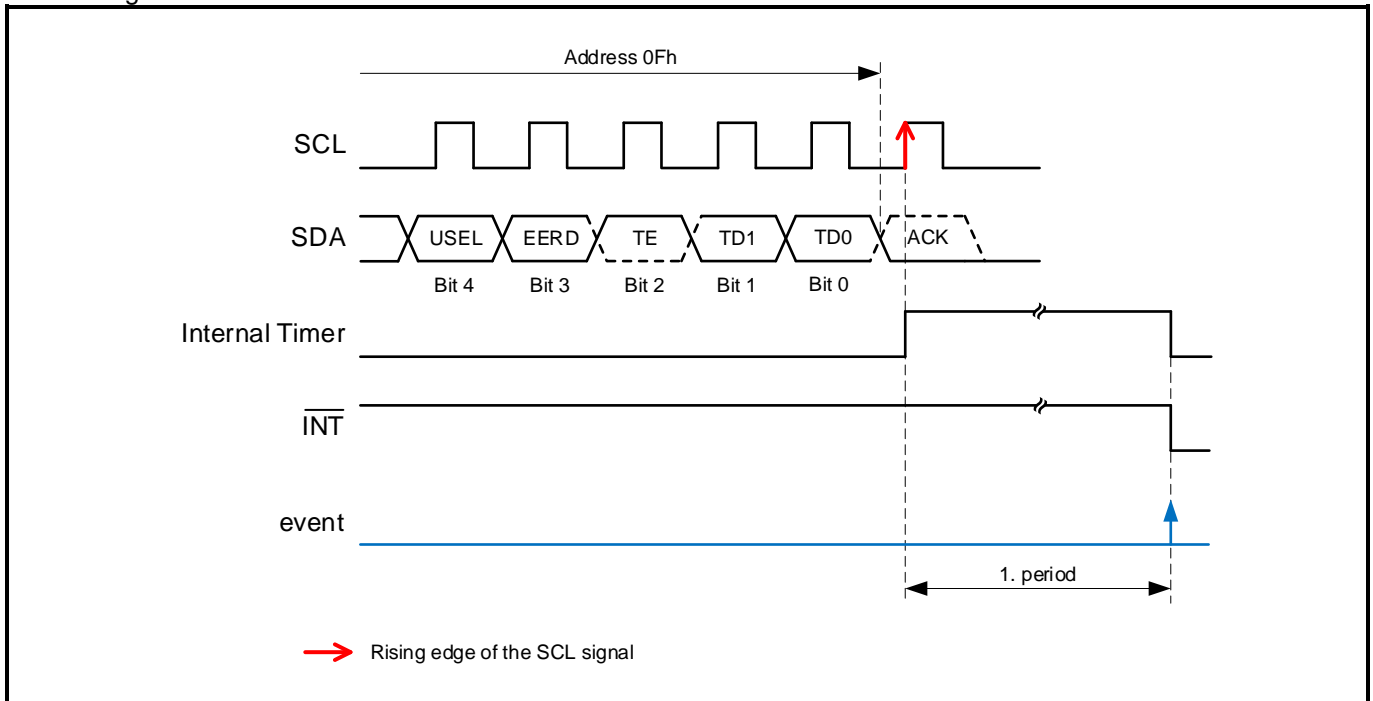
Countdown Period:

| Timer Value (0Ah and 0Bh) | Countdown Period | | | |
|------------------------------|-------------------|-----------------|----------------|-------------------|
| | TD = 00 (4096 Hz) | TD = 01 (64 Hz) | TD = 10 (1 Hz) | TD = 11 (1/60 Hz) |
| 0 | - | - | - | - |
| 1 | 244.14 μ s | 15.625 ms | 1 s | 1 min |
| 2 | 488.28 μ s | 31.25 ms | 2 s | 2 min |
| : | : | : | : | : |
| 41 | 10.010 ms | 640.63 ms | 41 s | 41 min |
| 205 | 50.049 ms | 3.203 s | 205 s | 205 min |
| 410 | 100.10 ms | 6.406 s | 410 s | 410 min |
| 2048 | 500.00 ms | 32.000 s | 2048 s | 2048 min |
| : | : | : | : | : |
| 4095 (FFFh) | 0.9998 s | 63.984 s | 4095 s | 4095 min |

General countdown timer behavior:



Start timing of the Periodic Countdown Timer:



4.8.3.FIRST PERIOD DURATION

When the TF flag is set, it indicates that an interrupt signal on $\overline{\text{INT}}$ is generated if this mode is enabled. See Section INTERRUPT OUTPUT for details on how the interrupt can be controlled.

When starting the timer for the first time, the first period has an uncertainty. The uncertainty arises because of the activation instruction of the interface clock, which is not synchronous to the Timer Clock Frequency. Subsequent timer periods do not have such deviation. The amount of deviation for the first timer period depends on the chosen Timer Clock Frequency, see following Table.

First period duration for Timer Value $n^{(1)}$:

| TD value | Timer Clock Frequency | First period duration | | Subsequent periods duration |
|----------|-----------------------|------------------------------|---|------------------------------|
| | | Minimum Period | Maximum Period | |
| 00 | 4096 Hz | $n \times 244 \mu\text{s}$ | $(n + 1) \times 244 \mu\text{s}$ | $n \times 244 \mu\text{s}$ |
| 01 | 64 Hz | $n \times 15.625 \text{ ms}$ | $(n + 1) \times 15.625 \text{ ms}$ | $n \times 15.625 \text{ ms}$ |
| 10 | 1 Hz | $n \times 1 \text{ s}$ | $n \times 1 \text{ s} + 15.625 \text{ ms}$ | $n \times 1 \text{ s}$ |
| 11 | 1/60 Hz | $n \times 60 \text{ s}$ | $n \times 60 \text{ s} + 15.625 \text{ ms}$ | $n \times 60 \text{ s}$ |

⁽¹⁾ Timer Values n from 1 to 4095 are valid. When the Timer Value is set to 0, the countdown timer does not start.

At the end of every countdown, the timer sets the Periodic Countdown Timer Flag (bit TF in Status Register). The TF flag can only be cleared by command. When enabled, a pulse is generated at the interrupt pin $\overline{\text{INT}}$.

When reading the Timer Value (Timer Value 0 and Timer Value 1), the preset value is returned and not the actual value. The actual value of the Periodic Countdown Timer can be read in the registers Timer Status 0 and Timer Status 1.

4.8.4.SINGLE MODE (TRPT = 0)

If TRPT bit is set to 0 (default), Single Mode is selected. In Single Mode the countdown timer will stop after reaching 0 and bit TE will be cleared automatically. The TF flag retains 1 until it is cleared to 0 by software.

Hint: An ongoing countdown can be stopped by writing 0 to the TE bit. No interrupt will be executed. The Timer Status 0 and Timer Status 1 registers store the last updated value.

4.8.5.REPEAT MODE (TRPT = 1)

If TRPT bit is set to 1, Repeat Mode is selected. In Repeat Mode the countdown timer is in the periodic countdown mode where it will be automatically reloaded with the Timer Value from the Timer Value 0 and Timer Value 1 registers when reaching 0. This will repeat until TE is cleared to 0. When a 0 is written to the TE bit, the Timer Status 0 and Timer Status 1 registers store the last updated value. The TF flag retains 1 until it is cleared to 0 by software.

Caution: Changing only TRPT from 1 to 0 during countdown to stop the function will automatically reload the countdown timer with the preset Timer Value immediately because TE in the same register is still 1. The last countdown period will therefore be longer as intended but will stop correctly after reaching 0 and bit TE will be cleared automatically.

Caution: A running countdown should not be stopped by writing 0 to the Timer Value because RV-3028-C7 outputs 64 Hz when the countdown value reaches 0.

Write as usual 0 to the TE bit to stop the function.

4.9. PERIODIC TIME UPDATE INTERRUPT FUNCTION

The Periodic Time Update Interrupt function generates an interrupt event periodically at the One-Second or the One-Minute update time, according to the selected timer source with bit USEL.

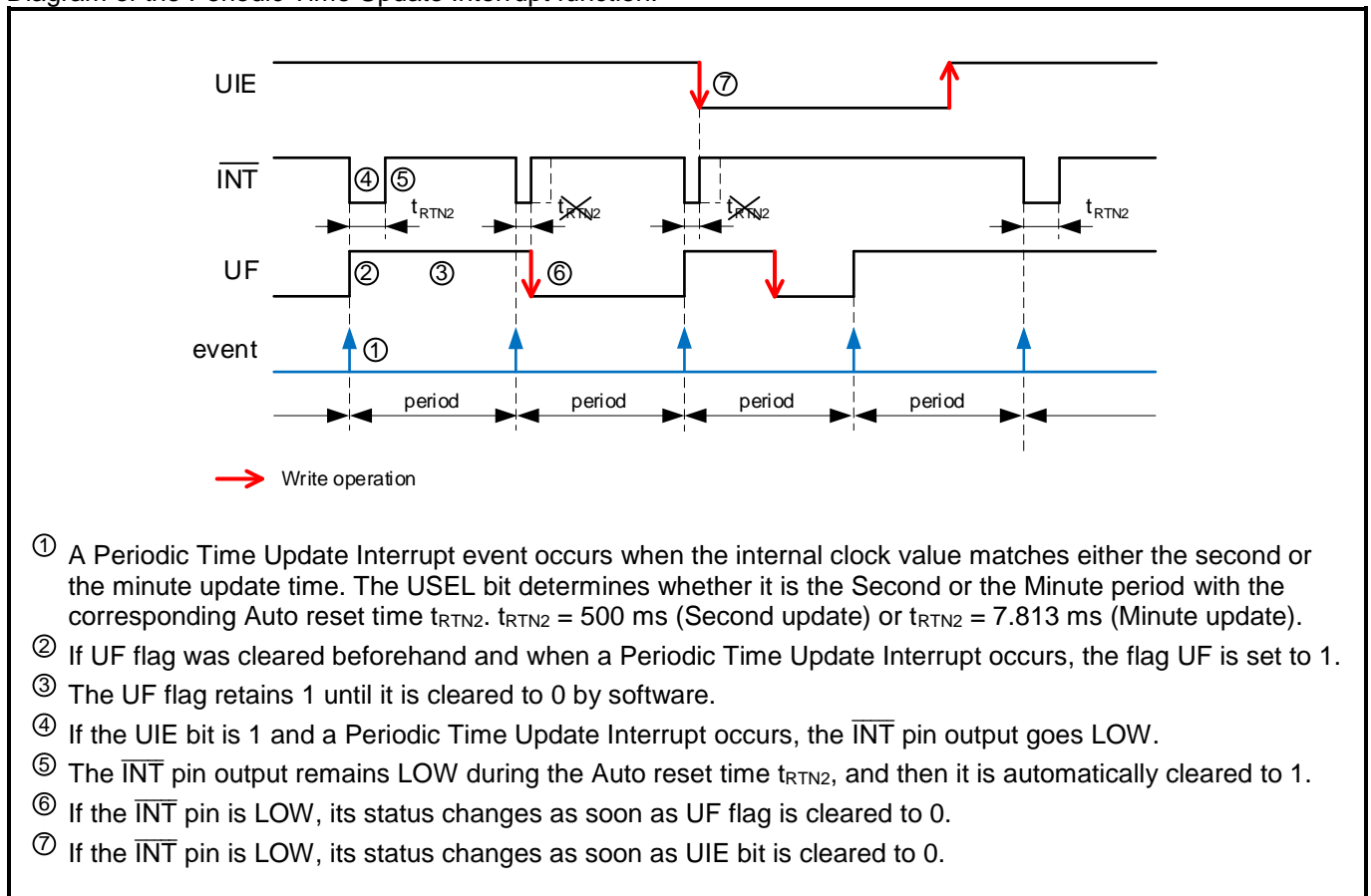
When an interrupt event is generated, the $\overline{\text{INT}}$ pin goes to the low level and the UF flag is set to 1 to indicate that an event has occurred. The output on $\overline{\text{INT}}$ pin is only effective if UIE bit in Control 2 register is set to 1. The low-level output signal on the $\overline{\text{INT}}$ pin is automatically cleared after the Auto reset time t_{RTN2} or it is cancelled when UF flag is cleared to 0.

- When USEL = 0 (Second update), $t_{\text{RTN2}} = 500 \text{ ms}$
- When USEL = 1 (Minute update), $t_{\text{RTN2}} = 7.813 \text{ ms}$

When bit UIE is set to 1, the internal update interrupt pulse (UI) can be used to enable the clock output on CLKOUT pin automatically, if CUIE and CLKIE bits are set to 1 and CLKOE bit is cleared to 0 and a frequency is selected in the FD field (see CLOCK OUTPUT SCHEME).

4.9.1. PERIODIC TIME UPDATE DIAGRAM

Diagram of the Periodic Time Update Interrupt function:



4.9.2.USE OF THE PERIODIC TIME UPDATE INTERRUPT

The following bits are related to the Periodic Time Update Interrupt and Automatic Clock output function:

- UF flag (see STATUS AND CONTROL REGISTER, 0Eh – Status)
- USEL bit (see STATUS AND CONTROL REGISTER, 0Fh – Control 1)
- UIE bit (see STATUS AND CONTROL REGISTER, 10h – Control 2)
- CUIE bit (see STATUS AND CONTROL REGISTERS, 12h – Clock Interrupt Mask)

Prior to entering any other settings, it is recommended to write a 0 to the UIE bit to prevent inadvertent interrupts on $\overline{\text{INT}}$ pin. The Periodic Time Update Interrupt function cannot be fully stopped, but by writing a 0 in the UIE bit, it prevents the occurrence of a hardware interrupt on the $\overline{\text{INT}}$ pin.

When writing 1 to the RESET bit or when writing to the Seconds register affects the length of a current update period (see RESET BIT FUNCTION).

Procedure to use the Periodic Time Update Interrupt and Automatic Clock output function:

1. Initialize bits UIE and UF to 0.
2. Choose the timer source clock and write the corresponding value in the USEL bit.
3. Set the UIE bit to 1 if you want to get a hardware interrupt on $\overline{\text{INT}}$ pin.
4. Set CUIE bit to 1 to enable clock output when a time update interrupt occurs. See also CLOCK OUTPUT SCHEME.
5. The first interrupt will occur after the next event, either second or minute change.

4.10. ALARM INTERRUPT FUNCTION

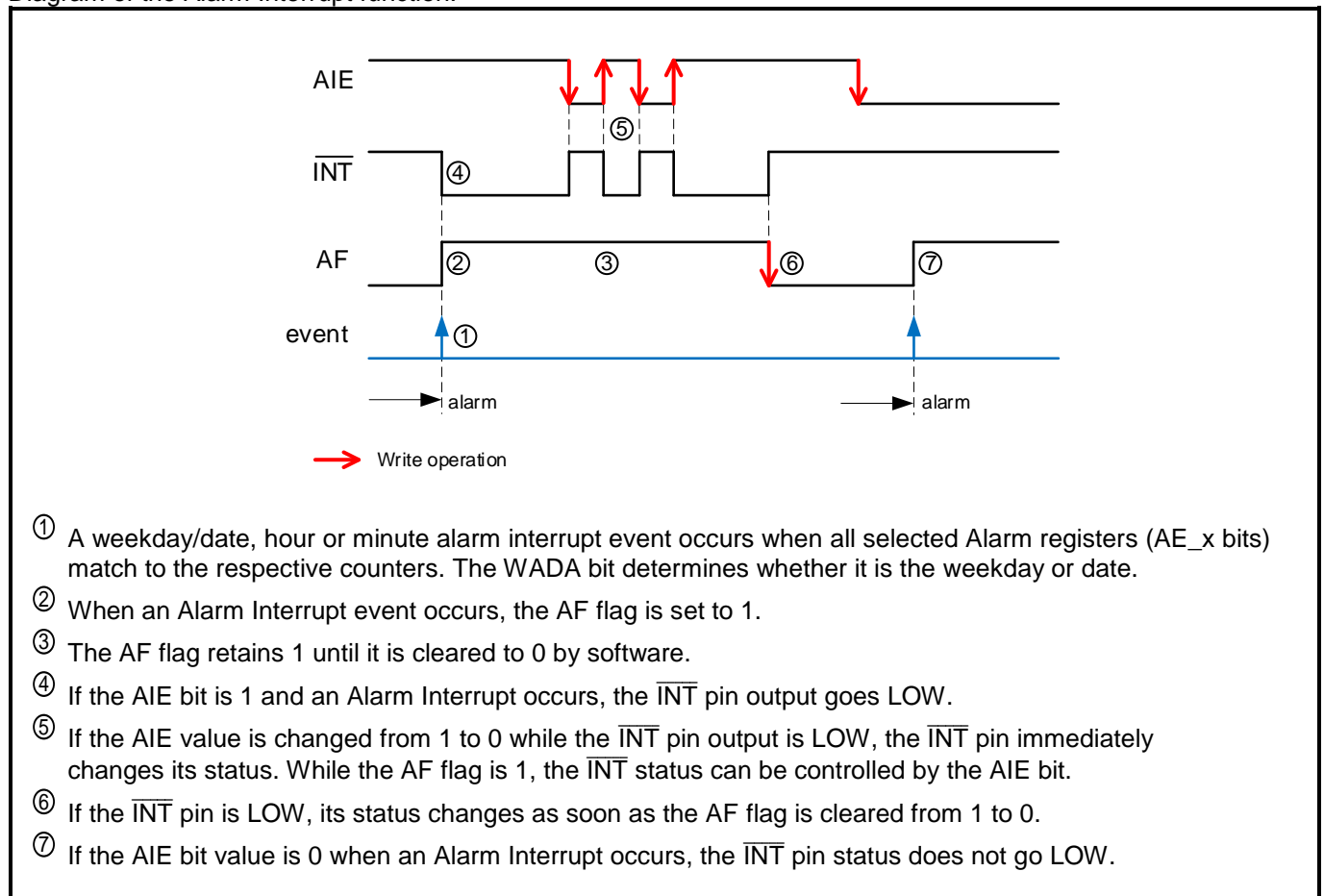
The Alarm Interrupt function generates an interrupt for alarm settings such as weekday/date, hour and minute settings.

When an interrupt event is generated, the $\overline{\text{INT}}$ pin goes to the low level and the AF flag is set to 1 to indicate that an event has occurred. The output on the $\overline{\text{INT}}$ pin is only effective if the AIE bit in the Control 2 register is set to 1.

When bit AIE is set to 1, the internal alarm interrupt signal (AI) can be used to enable the clock output on CLKOUT pin automatically, if CAIE and CLKIE bits are set to 1 and CLKOE bit is cleared to 0 and a frequency is selected in the FD field (see CLOCK OUTPUT SCHEME).

4.10.1. ALARM DIAGRAM

Diagram of the Alarm Interrupt function:



4.10.2. USE OF THE ALARM INTERRUPT

The following registers and bits are related to the Alarm Interrupt and Automatic Clock output function:

- Minutes Register (01h) (see CLOCK REGISTERS)
- Hours Register (02h) (see CLOCK REGISTERS)
- Weekday Register (03h) (see CALENDAR REGISTERS)
- Date Register (04h) (see CALENDAR REGISTERS)
- Minutes Alarm Register and AE_M bit (07h) (see ALARM REGISTERS)
- Hours Alarm Register and AE_H bit (08h) (see ALARM REGISTERS)
- Weekday/Date Alarm Register and AE_WD bit (09h) (see ALARM REGISTERS)
- AF flag (see STATUS AND CONTROL REGISTER, 0Eh – Status)
- WADA bit (see STATUS AND CONTROL REGISTERS, 0Fh – Control 1)
- AIE and 12_24 bits (see STATUS AND CONTROL REGISTERS, 10h – Control 2)
- CAIE bit (see STATUS AND CONTROL REGISTERS, 12h – Clock Interrupt Mask)

Prior to entering any timer settings for the Alarm Interrupt, it is recommended to write a 0 to the AIE bit to prevent inadvertent interrupts on $\overline{\text{INT}}$ pin. When writing 1 to the RESET bit or writing a value to the Seconds register affects the time to the next alarm interrupt (see RESET BIT FUNCTION). When the Alarm Interrupt function is not used, one Byte (07h) of the Alarm registers can be used as RAM byte. In such case, be sure to write a 0 to the AIE bit (if the AIE bit value is 1 and the Alarm register is used as RAM register, $\overline{\text{INT}}$ may change to low level unintentionally).

Procedure to use the Alarm Interrupt and Automatic Clock output function:

1. Initialize bits AIE and AF to 0.
2. Choose weekday alarm or date alarm (weekday/date) by setting the WADA bit. WADA = 0 for weekday alarm or WADA = 1 for date alarm.
3. Write the desired alarm settings in registers 07h to 09h. The three alarm enable bits, AE_M, AE_H and AE_WD, are used to select the corresponding register that has to be taken into account for match or not. See the following table.
4. Set CAIE bit to 1 to enable clock output when an alarm occurs. See also CLOCK OUTPUT SCHEME.
5. Set the AIE bit to 1 if you want to get a hardware interrupt on $\overline{\text{INT}}$ pin.

Alarm Interrupt:

| Alarm enable bits | | | Alarm event |
|-------------------|------|------|--|
| AE_WD | AE_H | AE_M | |
| 0 | 0 | 0 | When minutes, hours and weekday/date match (once per weekday/date) |
| 0 | 0 | 1 | When hours and weekday/date match (once per weekday/date) |
| 0 | 1 | 0 | When minutes and weekday/date match (once per hour per weekday/date) |
| 0 | 1 | 1 | When weekday/date match (once per weekday/date) |
| 1 | 0 | 0 | When hours and minutes match (once per day) |
| 1 | 0 | 1 | When hours match (once per day) |
| 1 | 1 | 0 | When minutes match (once per hour) |
| 1 | 1 | 1 | All disabled – Default value |

AE_x bits (where x is WD, H or M)
 AE_x = 0: Alarm is enabled
 AE_x = 1: Alarm is disabled – Default value

4.11. EXTERNAL EVENT INTERRUPT FUNCTION

The External Event Interrupt and the Time Stamp function are enabled by the control bits TSS, TSE and EIE. With the ET field the EVI input events can be configured either for edge detection, or for level detection with filtering, and with the EHL bit the active edge or level can be configured.

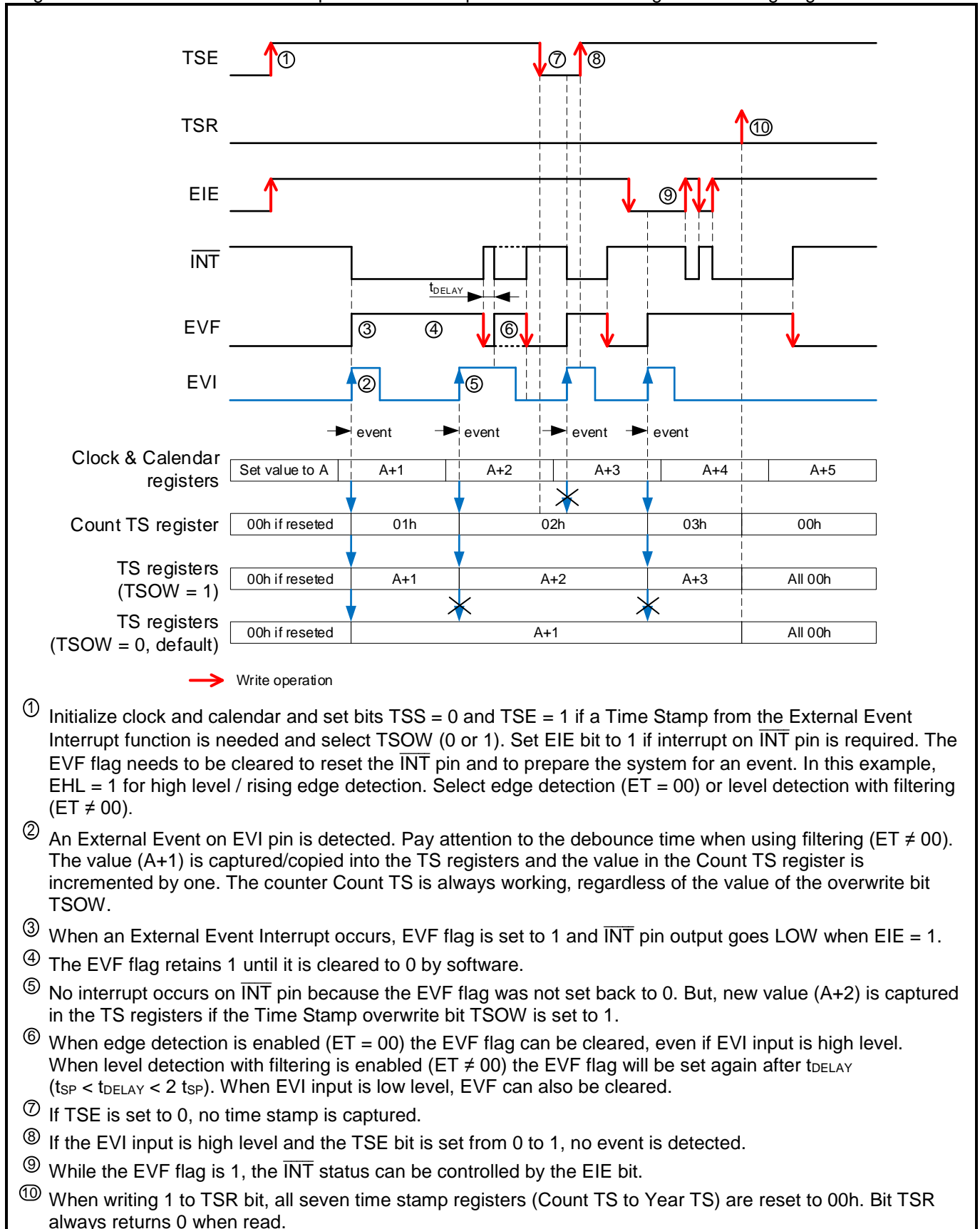
If enabled (TSS = 0, TSE = 1, EIE = 1 and EVF flag was cleared to 0 before) and an External Event on EVI pin is detected, the clock and calendar registers are captured and copied into the Time Stamp registers, the \overline{INT} is issued and the EVF flag is set to 1 to indicate that an external event has occurred.

When bit TSS = 0 and bit EIE = 1, the internal event interrupt signal (EI) can be used to enable the clock output on CLKOUT pin automatically, if CEIE and CLKIE bits are set to 1 and CLKOE bit is cleared to 0 and a frequency is selected in the FD field (see CLOCK OUTPUT SCHEME).

Caution: The EVF flag is also set by an event of the Backup Switchover function when bits TSS and TSE are set to 1.

4.11.1. EXTERNAL EVENT DIAGRAM

Diagram of the External Event Interrupt function. Example with EHL = 1 for high level / rising edge detection:



4.11.2. USE OF THE EXTERNAL EVENT INTERRUPT

The following registers and bits are related to the External Event Interrupt, Time Stamp and Automatic Clock output function:

- Seconds Register (00h) (see CLOCK REGISTERS)
- Minutes Register (01h) (see CLOCK REGISTERS)
- Hours Register (02h) (see CLOCK REGISTERS)
- Date Register (04h) (see CALENDAR REGISTERS)
- Month Register (05h) (see CALENDAR REGISTERS)
- Year Register (06h) (see CALENDAR REGISTERS)
- Count TS Register (14h) (see TIME STAMP REGISTERS)
- Seconds TS (15h) (see TIME STAMP REGISTERS)
- Minutes TS (16h) (see TIME STAMP REGISTERS)
- Hours TS (17h) (see TIME STAMP REGISTERS)
- Date TS (18h) (see TIME STAMP REGISTERS)
- Month TS (19h) (see TIME STAMP REGISTERS)
- Year TS (1A) (see TIME STAMP REGISTERS)
- EVF flag (see STATUS AND CONTROL REGISTERS, 0Eh – Status)
- TSE, EIE and 12_24 bits (see STATUS AND CONTROL REGISTERS, 10h – Control 2)
- CEIE bit (see STATUS AND CONTROL REGISTERS, 12h – Clock Interrupt Mask)
- EHL bit, ET field, TSR bit, TSOW bit and TSS bit (see EVENT CONTROL REGISTER, 13h – Event Control)

Prior to entering any timer settings for the event interrupt, it is recommended to write a 0 to the TSE and EIE bit to prevent inadvertent interrupts on $\overline{\text{INT}}$ pin.

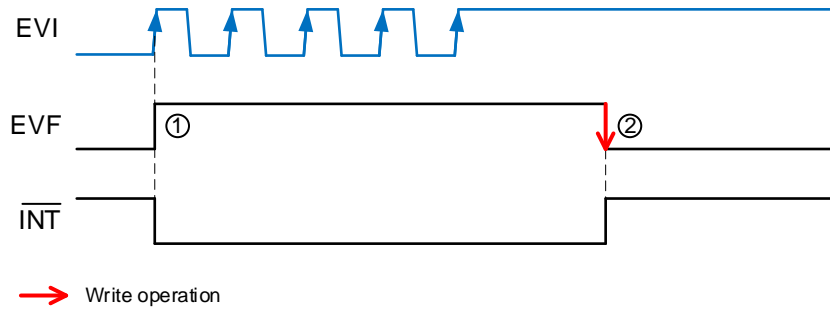
Note that changing TSS bit value from 1 to 0 before clearing TSE and EIE can create unwanted interrupts (according to EHL bit, but regardless of the status of the ET field).

Procedure to use the External Event Interrupt, Time Stamp and Automatic Clock output function:

1. Initialize bits TSE and EIE to 0.
2. Clear flag EVF to 0.
3. Set TSS bit to 0 to select External Event on EVI pin as Time Stamp and Interrupt source.
4. Set EHL bit to 1 or 0 to choose high or low level (or rising or falling edge) detection on pin EVI.
5. Select EDGE DETECTION (ET = 00) or LEVEL DETECTION WITH FILTERING (ET \neq 00).
6. Set TSOW bit to 1 if the last occurred event has to be recorded and TS registers are overwritten.
Hint: The counter Count TS is always working, independent of the settings of the overwrite bit TSOW.
7. Write 1 to TSR bit, to reset all Time Stamp registers to 00h. Bit TSR always returns 0 when read.
8. Set CEIE bit to 1 to enable clock output when external event occurs. See also CLOCK OUTPUT SCHEME.
9. Set TSE bit to 1 if you want to enable the Time Stamp function.
10. Set EIE bit to 1 if you want to get a hardware interrupt on $\overline{\text{INT}}$ pin.

4.11.3. EDGE DETECTION (ET = 00)

Example with rising edge detection and interrupt output:

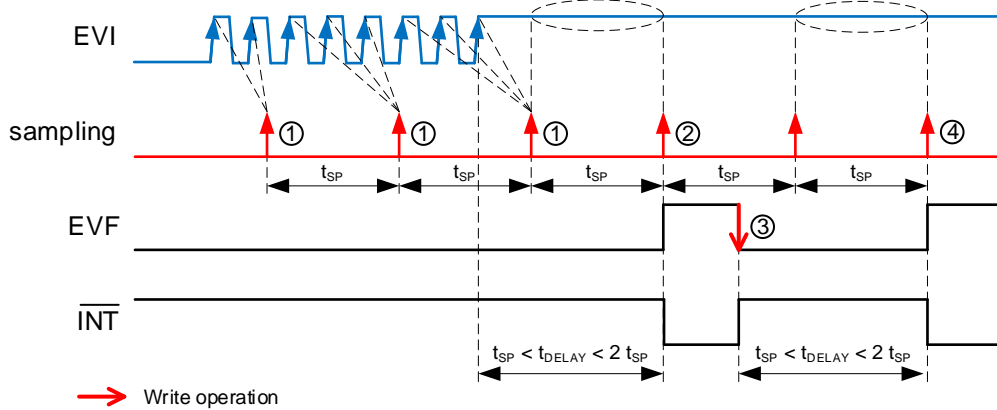


Settings: EHL = 1, ET = 00, TSS = 0, EIE = 1.

- ① When a rising edge on EVI pin is detected, the EVF flag is set to 1 and the $\overline{\text{INT}}$ output pin goes LOW.
- ② If the $\overline{\text{INT}}$ pin is LOW, its status changes as soon as the EVF flag is cleared to 0, even if EVI input is high level.

4.11.4. LEVEL DETECTION WITH FILTERING (ET ≠ 00)

Example with high level detection and interrupt output:



Settings: EHL = 1, ET ≠ 00, TSS = 0, EIE = 1.

Available sampling periods for the digital debounce filtering:

- ET = 01, $t_{SP} = 3.9 \text{ ms}$
- ET = 10, $t_{SP} = 15.6 \text{ ms}$
- ET = 11, $t_{SP} = 125.0 \text{ ms}$

- ① From the previous sampling pulse to this sampling pulse, no stable high level was detected.
- ② If a stable high level on EVI pin during one sampling period is detected, the EVF flag is set to 1 and the $\overline{\text{INT}}$ output pin goes LOW. The delay time t_{DELAY} is between t_{SP} and $2 t_{SP}$.
- ③ If the $\overline{\text{INT}}$ pin is LOW, its status changes as soon as the EVF flag is cleared to 0.
- ④ When the high level on EVI pin remains stable, again, the EVF flag is set to 1 and the $\overline{\text{INT}}$ output pin goes LOW. The delay time t_{DELAY} is again between t_{SP} and $2 t_{SP}$.

4.12. AUTOMATIC BACKUP SWITCHOVER INTERRUPT FUNCTION

The Automatic Backup Switchover Interrupt function generates an interrupt event when the BSM field (EEPROM 37h) is set to 01 (DSM) or 11 (LSM) and a switchover from VDD Power state to VBACKUP Power state occurs.

If enabled (TSS = 1, TSE = 1, BSIE = 1 and BSF flag was cleared to 0 before) and a Backup Switchover is detected, the clock and calendar registers are captured and copied into the Time Stamp registers, the $\overline{\text{INT}}$ is issued and the BSF flag is set to 1 to indicate that a Backup Switchover has occurred.

Similar to the External Event Interrupt Function, clock output on CLKOUT pin can be controlled by the Automatic Backup Switchover Interrupt function. When bits TSS and EIE are set to 1, the internal event interrupt signal (EI) created by the Automatic Backup Switchover function can be used to enable the clock output on CLKOUT pin automatically.

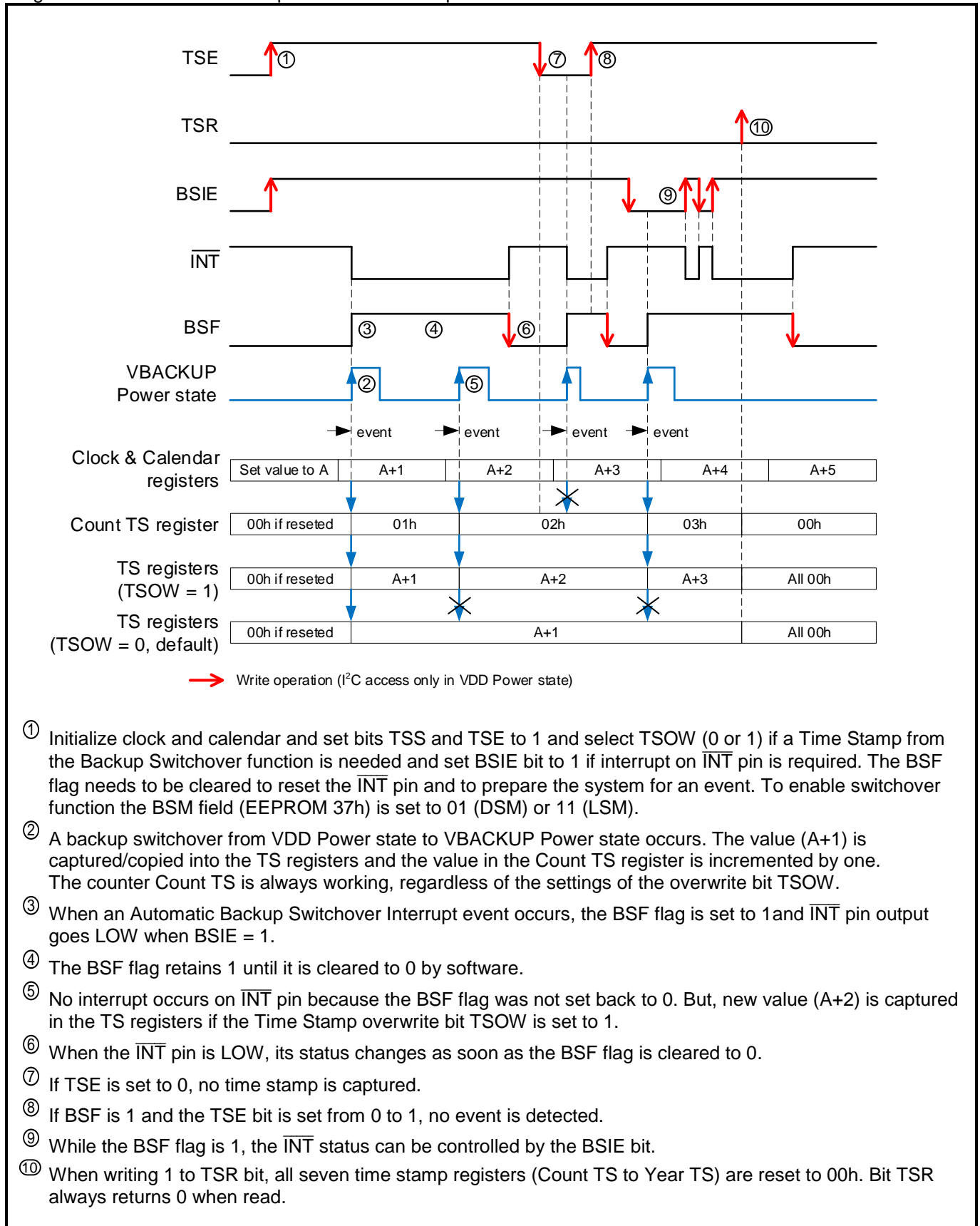
If enabled (TSS, EIE, CEIE, CLKIE are set to 1 and CLKOE is cleared to 0 and a frequency is selected in the FD field), when again in VDD Power state, CLKOUT pin outputs the frequency (see INTERRUPT SCHEME and CLOCK OUTPUT SCHEME).

Note that a debounce logic provides a debounce time t_{DEB} of 122 μs to 183 μs , which will filter V_{DD} oscillation when the backup switchover will switch back from V_{BACKUP} to V_{DD} (see AUTOMATIC BACKUP SWITCHOVER FUNCTION). I²C access is possible in VDD Power state after the debounce time t_{DEB} .

Note that the FEDE bit (EEPROM 37h) should always be set to 1, so that Fast Edge Detection ($\geq 7 \text{ V/ms}$) is enabled (see EEPROM BACKUP REGISTER). FEDE = 1 is the default value on delivery.

4.12.1. AUTOMATIC BACKUP SWITCHOVER DIAGRAM

Diagram of the Automatic Backup Switchover Interrupt function:



4.12.2. USE OF THE AUTOMATIC BACKUP SWITCHOVER INTERRUPT

The following registers and bits are related to the Automatic Backup Switchover Interrupt, Time Stamp and Automatic Clock output function:

- Seconds Register (00h) (see CLOCK REGISTERS)
- Minutes Register (01h) (see CLOCK REGISTERS)
- Hours Register (02h) (see CLOCK REGISTERS)
- Date Register (04h) (see CALENDAR REGISTERS)
- Month Register (05h) (see CALENDAR REGISTERS)
- Year Register (06h) (see CALENDAR REGISTERS)
- Count TS (14h) (see TIME STAMP REGISTERS)
- Seconds TS (15h) (see TIME STAMP REGISTERS)
- Minutes TS (16h) (see TIME STAMP REGISTERS)
- Hours TS (17h) (see TIME STAMP REGISTERS)
- Date TS (18h) (see TIME STAMP REGISTERS)
- Month TS (19h) (see TIME STAMP REGISTERS)
- Year TS (1A) (see TIME STAMP REGISTERS)
- BSF flag (see STATUS AND CONTROL REGISTERS, 0Eh – Status)
- TSE, EIE and 12_24 bits (see STATUS AND CONTROL REGISTERS, 10h – Control 2)
- CEIE bit (see STATUS AND CONTROL REGISTERS, 12h – Clock Interrupt Mask)
- TSR bit, TSOW bit and TSS bit (see EVENT CONTROL REGISTER, 13h – Event Control)
- BSIE bit, FEDE bit and BSM field (see EEPROM BACKUP REGISTER, 37h – EEPROM Backup)

Prior to entering any other settings, it is recommended to write a 0 to the TSE and BSIE bit to prevent inadvertent interrupts on $\overline{\text{INT}}$ pin.

Procedure to use the Automatic Backup Switchover Interrupt, Time Stamp and Automatic Clock output function:

1. Initialize bits TSE and BSIE to 0.
2. Clear flag BSF to 0.
3. Set TSS bit to 1 to select Backup Switchover as Time Stamp and Interrupt source.
4. Set TSOW bit to 1 if the last occurred event has to be recorded and TS registers are overwritten.
Hint: The counter Count TS is always working, independent of the settings of the overwrite bit TSOW.
5. Write 1 to TSR bit, to reset all Time Stamp registers to 00h. Bit TSR always returns 0 when read.
6. Set CEIE bit to 1 to enable clock output when a backup switchover occurs.
Caution: This function is only working with the Automatic Backup Switchover function when bits TSS and TSE are set to 1. See also CLOCK OUTPUT SCHEME.
7. Set TSE bit to 1 if you want to enable the Time Stamp function.
8. The FEDE bit should always be set to 1, so that Fast Edge Detection (≥ 7 V/ms) is enabled.
9. Set the BSIE bit to 1 if you want to get a hardware interrupt on $\overline{\text{INT}}$ pin.
10. Choose the switchover mode (DSM or LSM) and write the corresponding value in the BSM field.

See also EEPROM READ/WRITE CONDITIONS.

4.13. POWER ON RESET INTERRUPT FUNCTION

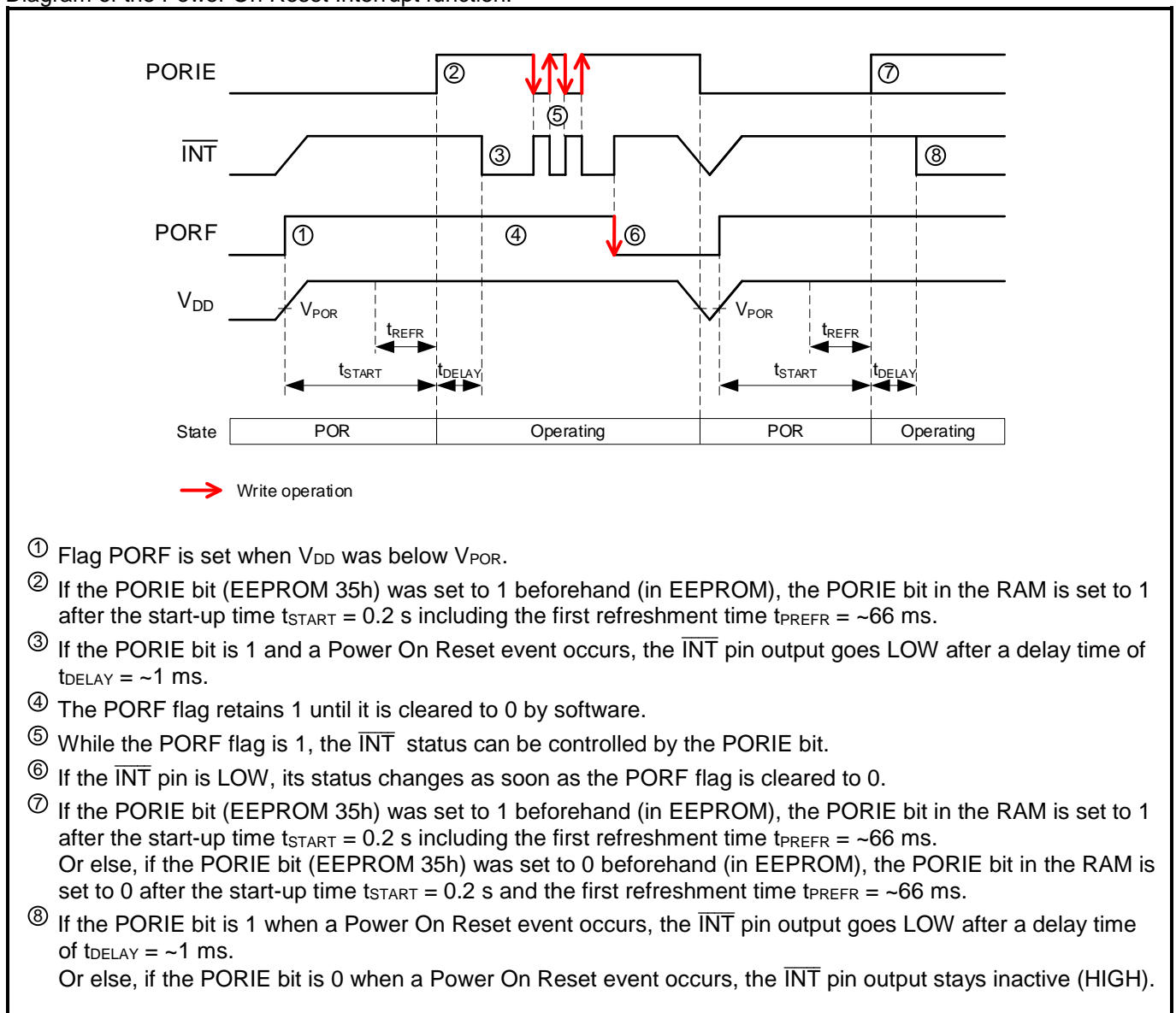
The Power On Reset Interrupt function is enabled by the PORIE bit (EEPROM 35h). The PORIE bit has to be set beforehand in the EEPROM, not in the RAM (see EEPROM READ/WRITE).

When voltage drop below V_{POR} is detected ($V_{DD} < V_{POR}$) the PORF flag is set to 1 to indicate that a Power On Reset has occurred and when the PORIE bit is 1 the \overline{INT} pin goes to low level.

A PORF value of 1 indicates also that the time information is corrupted. The value 1 is retained until a 0 is written by the user.

4.13.1. POWER ON RESET DIAGRAM

Diagram of the Power On Reset Interrupt function:



4.13.2. USE OF THE POWER ON RESET INTERRUPT

The following registers and bits are related to the Power On Reset Interrupt function (including EEPROM handling):

- PORF flag and EEbusy bit (see STATUS AND CONTROL REGISTERS, 0Eh – Status)
- EERD bit (see STATUS AND CONTROL REGISTERS, 0Fh – Control 1)
- EE Address register (25h) (see EEPROM MEMORY CONTROL REGISTERS)
- EE Data register (26h) (see EEPROM MEMORY CONTROL REGISTERS)
- EE Command register (27h) (see EEPROM MEMORY CONTROL REGISTERS)
- PORIE bit (see EEPROM CLKOUT REGISTER, 35h – EEPROM Clkout)

The PORIE bit has to be set beforehand in the EEPROM, not in the RAM (see EEPROM READ/WRITE).

Procedure to use the Power On Reset Interrupt function:

1. In the EEPROM, set the PORIE bit to 1 if you want to get a hardware interrupt on $\overline{\text{INT}}$ pin at the next Power On Reset event. Procedure according to EEPROM READ/WRITE.
2. The first interrupt will occur after the next POR event.

4.14. TIME STAMP FUNCTION

The Time Stamp function is enabled by the control bit TSE. Sources are the External Event Interrupt function (TSS = 0) or the Automatic Backup Switchover Interrupt function (TSS = 1).

If a source is enabled and an event is detected, the Time Stamp (TS) registers are recorded. When the TSOW bit is set to 0 and the EVF flag was cleared to 0 before, only one (the first) event is recorded. When the TSOW bit is set to 1, the last event is recorded (EVF flag does not need to be cleared). The counter Count TS is always working, independent of the settings of the overwrite bit TSOW.

- When writing 1 to TSR bit, all seven time stamp registers (Count TS to Year TS) are reset to 00h. Bit TSR always returns 0 when read.
- Before starting the Time Stamp function, it is recommended to write 0 to the TSE bit and 1 to TSR bit.
- When writing 1 to the RESET bit or when writing to the Seconds register, Time Stamp capture/copy does not occur. Bit RESET always returns 0 when read.
- Note that changing TSS bit value from 1 to 0 before clearing TSE can create unwanted Time Stamp capture/copy from the External Event Interrupt function (according to EHL bit, but regardless of the status of the ET field).

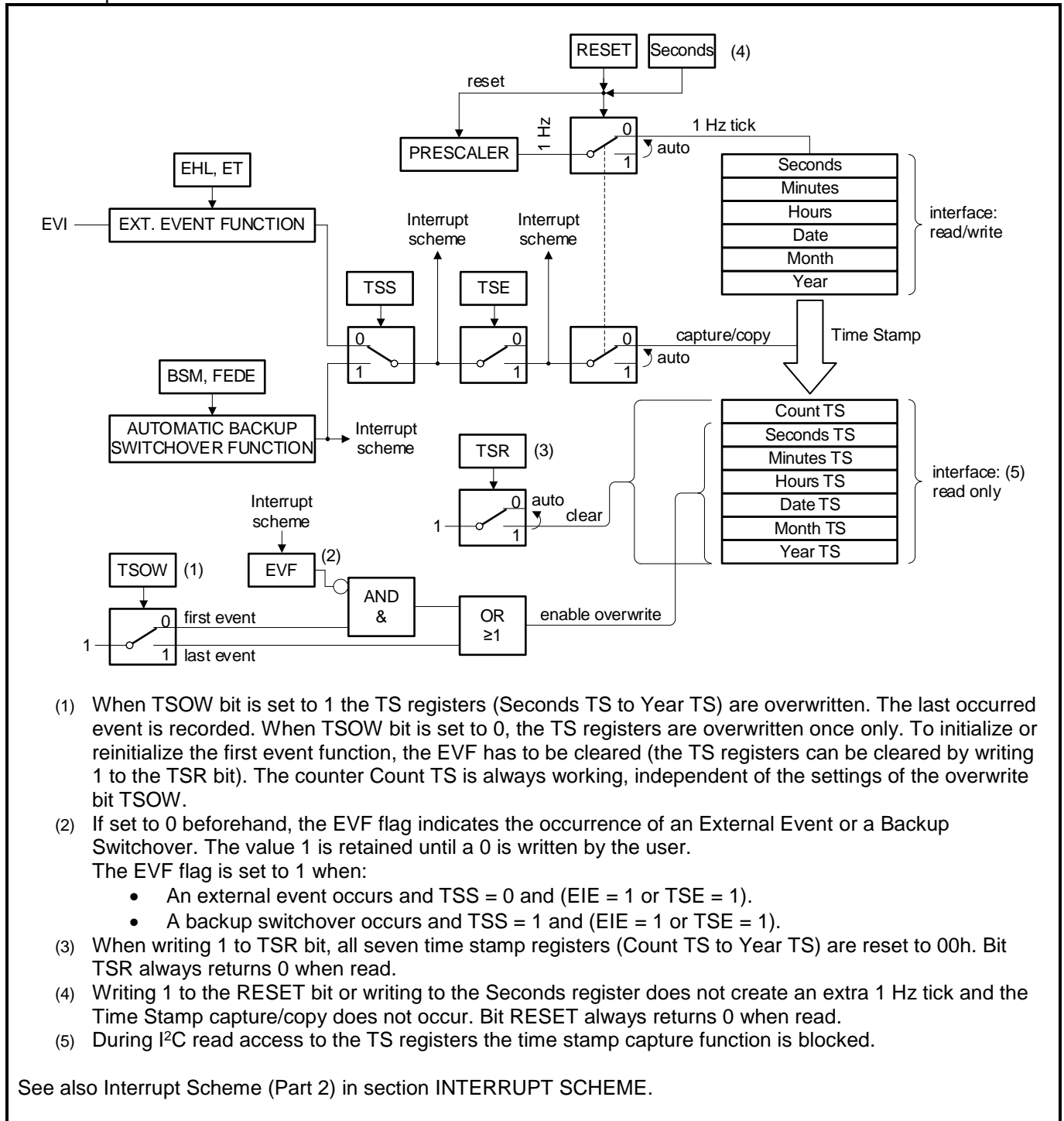
Procedure for using the Time Stamp function:

1. Initialize bits TSE and EIE to 0.
2. Select TSOW (0 or 1), clear EVF and BSF.
3. Write 1 to TSR bit, to reset all Time Stamp registers to 00h. Bit TSR always returns 0 when read.
4. Select the External Event Interrupt function (TSS = 0) or the Automatic Backup Switchover Interrupt function (TSS = 1) as time stamp source and initialize the appropriate function (see EXTERNAL EVENT INTERRUPT FUNCTION or AUTOMATIC BACKUP SWITCHOVER INTERRUPT FUNCTION).
5. Set the TSE bit to 1 to enable the Time Stamp function.

Hint: The $\overline{\text{INT}}$ signal is issued when EIE (RAM) or BSIE (EEPROM 37h) bit is set to 1. The EVF or BSF flag is set to 1 to indicate that a corresponding event has occurred.

Caution: Because the EVF flag is internally used for the identification of a First Event detection it is set by an event from the External Event Interrupt function (TSS = 0, TSE = 1) or by an event of the Backup Switchover Interrupt function (TSS = 1, TSE = 1). See also the following scheme:

Time Stamp scheme:



4.15. FREQUENCY OFFSET CORRECTION

An aging adjustment or accuracy tuning can be done with the EEOffset value. The correction is made purely digital and has only the effect of shifting the time vs. temperature curve vertically up or down. It has no effect on the time vs. temperature characteristics of the final frequency. The EEOffset value contains a two's complement number with a range of +255 to -256 adjustment steps. The minimal correction step (one LSB) is $\pm 1 / (16384 \times 64) = \pm 0.9537$ ppm and the maximum correction range is from +243.2 ppm to -244.1 ppm. The compensation period is 64 seconds. Note that the signed offset value EEOffset corresponds to the correction value of the measured frequency (32.768 kHz). The non-volatile user programmable EEOffset value (factory calibrated time accuracy is ± 1 ppm @ 25°C) can be adjusted by the user. See chapters below.

Caution: Bits 8 to 1 of the EEOffset value are in the register 36h – EEPROM Offset (see EEPROM OFFSET REGISTER). Bit 0 (LSB) of the EEOffset value is in the register 37h – EEPROM Backup (see EEPROM BACKUP REGISTER).

4.15.1. EEOFFSET VALUE DETERMINATION

The EEOffset value is determined by the following process:

1. Select the 32.768 kHz frequency on the CLKOUT pin.
(If another frequency than 32.768 kHz is selected, the EEOffset value has to be set to 0 so that the uncorrected frequency can be measured, and the following calculations have to be adapted.)
2. Measure the frequency F_{meas} at CLKOUT pin in Hz.
3. Compute the offset value required in ppm: $POffset = ((F_{meas} - 32768) / 32768 \times 1'000'000)$
4. Compute the offset value in steps: $Offset = POffset / (1 / (16384 \times 64) \text{ in ppm}) = POffset / (0.9537 \text{ ppm})$
5. If $Offset > 256$, the frequency is too high to be corrected.
6. Else if $1 \leq Offset \leq 256$ (correction is $-1 \geq OffsetCorr. \geq -256$), \rightarrow set $EEOffset = 512 - Offset$
7. Else if $-255 \leq Offset \leq 0$ (correction is $+255 \leq OffsetCorr. \leq 0$), \rightarrow set $EEOffset = - Offset$
8. Else the frequency is too low to be corrected.

Examples:

- If 32768.48 Hz is measured when the 32.768 kHz clock is selected, the offset is +0.48 Hz, which is $+0.48 \text{ Hz} / 32768 \text{ Hz} \times 1'000'000 = +14.648$ ppm. The Offset value in steps is then calculated as follows: $+14.648 \text{ ppm} / 0.9537 \text{ ppm} = +15.36$, the rounded integral part is 15 (the offset correction is -15 steps). The unsigned EEOffset value is then: $512 - 15 = +497$. In binary, $EEOffset = 111110001$.
- If 32767.52 Hz is measured when the 32.768 kHz clock is selected, the offset is -0.48 Hz, which is $-0.48 \text{ Hz} / 32768 \text{ Hz} \times 1'000'000 = -14.648$ ppm. The Offset value in steps is then calculated as follows: $-14.648 \text{ ppm} / 0.9537 \text{ ppm} = -15.36$, the rounded integral part is -15 (the offset correction is +15 steps). The EEOffset value is then: $-(-15) = +15$. In binary, $EEOffset = 000001111$.

4.15.2. VERIFICATION OF THE CORRECTED TIME ACCURACY

The offset correction can be verified by the following process:

1. Enter the calculated EEOffset value (see EEOFFSET VALUE DETERMINATION).
2. Select the 1 Hz frequency on the CLKOUT pin (if another frequency is selected the following calculations have to be adapted).
3. Measure every period during one compensation period of 64 seconds at CLKOUT pin.
4. Calculate the average frequency F_{meas_aver} in Hz.
5. Compute the new achieved offset value in ppm: $POffset = ((F_{meas_aver} - 1) / 1 \times 1'000'000)$

4.16. UNIX TIME COUNTER

The UNIX Time counter is a 32-bit counter, unsigned integer, which rolls over to 00000000h when reaching the value FFFFFFFFh. The 4 bytes are fully readable and writable. The counter source clock is the digitally offset compensated 1 Hz tick.

4.16.1. SETTING THE UNIX TIME

During I²C write access with an access time smaller than 950 ms the UNIX registers (UNIX Time 0 to UNIX Time 3) are blocked. Unlike to the setting of the clock and calendar registers, after I²C STOP condition a possibly memorized 1 Hz tick can be lost.

Advantage of register blocking:

- Prevents faulty writing to the UNIX registers during an I²C write access (no incrementing of UNIX registers during the write access).
- No reading is needed for control. The written data are coherent.

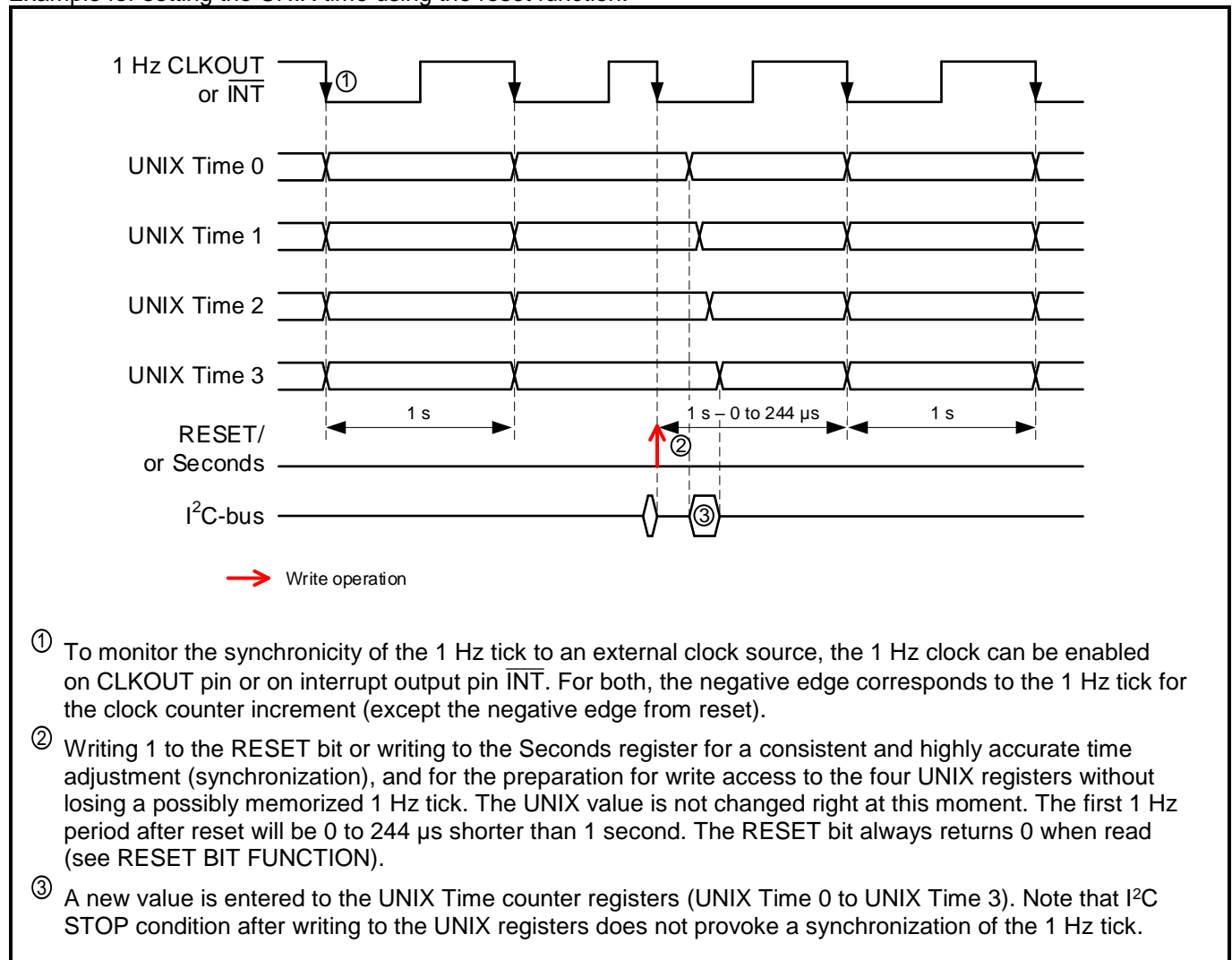
If the I²C write access takes longer than 950 ms the I²C bus interface is reset by the internal bus timeout function. In this case the previous UNIX value is maintained and the UNIX increment (1 Hz tick) continues to operate normally (a pending 1 Hz tick can be lost). Restarting of communications begins with transfer of the START condition again.

Since when writing immediately to the four UNIX registers, a possibly memorized 1 Hz tick can be lost, it is recommended to make a reset of the prescaler before setting the UNIX time (see RESET BIT FUNCTION). The 32-bit UNIX counter value itself does not change during reset. The time between the reset and the I²C STOP after writing the UNIX time should be within 950 ms. See diagram below.

Advantage of this method:

- No 1 Hz tick will be lost during write access to the four UNIX registers.
- Prevents unwanted difference of one second between Seconds register and UNIX time.

Example for setting the UNIX time using the reset function:



4.16.2. READING THE UNIX TIME

During I²C read access with an access time smaller than 950 ms the UNIX registers (UNIX Time 0 to UNIX Time 3) are fully readable but not blocked. Like to the reading of the clock and calendar registers, after I²C STOP condition a possibly memorized 1 Hz tick is realized.

Advantage of the memorized 1 Hz tick:

- After reading, one memorized 1 Hz tick is handled. The UNIX time is updated.

If the I²C read access takes longer than 950 ms the I²C bus interface is reset by the internal bus timeout function. In this case all UNIX data that is read has a value of FFh, the pending 1 Hz tick is realized and the UNIX increment (1 Hz tick) continues to operate normally. Restarting of communications begins with transfer of the START condition again.

Two methods for reading the UNIX time are recommended:

1. Read the four registers (UNIX Time 0 to UNIX Time 3) twice and check for consistent results.
2. Generate 1 Hz interrupt on $\overline{\text{INT}}$ pin with PERIODIC TIME UPDATE INTERRUPT FUNCTION for the MCU, when can be read. The time between the interrupt event and the I²C STOP after reading the UNIX time should be within 950 ms. No second reading needed.

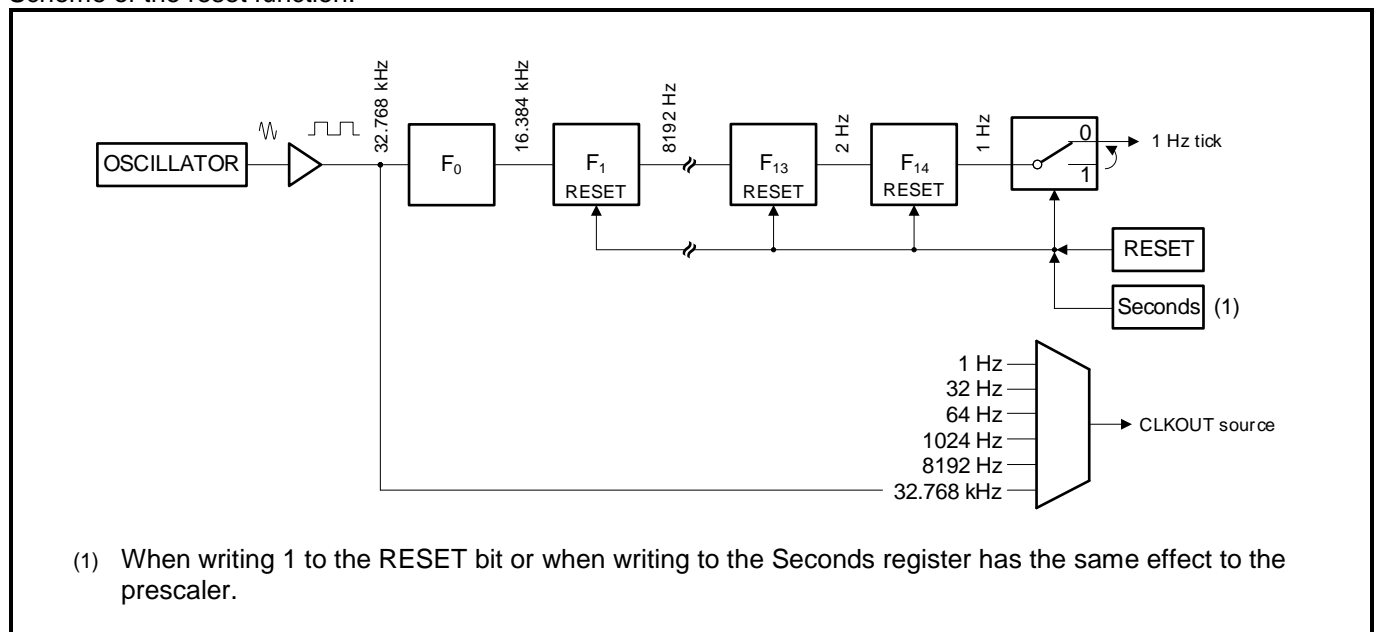
4.17. RESET BIT FUNCTION

The RESET bit is used for a software-based accurate and safe starting of the time circuits (synchronization). Writing to the Seconds register has the same effect.

When writing 1 to the RESET bit or when writing to the Seconds register, the clock prescaler frequencies for 8192 Hz to 1 Hz are reset and an eventual present memorized 1 Hz update is also reset. The RESET bit always returns 0 when read. Because the upper stage of the prescaler is not reset (16.384 kHz) and the I²C interface is asynchronous, the first 1 Hz period after reset will be 0 to 244 μ s shorter than 1 second. Resetting the prescaler will have an influence on the length of current clock period on all subsequent peripherals (clock and calendar, CLKOUT clock, timer clock, update timer clock, UNIX clock, EVI input filter).

Writing 1 to the RESET bit or writing to the Seconds register will not affect the CLKOUT of the 32.768 kHz (see also CLKOUT FREQUENCY SELECTION).

Scheme of the reset function:

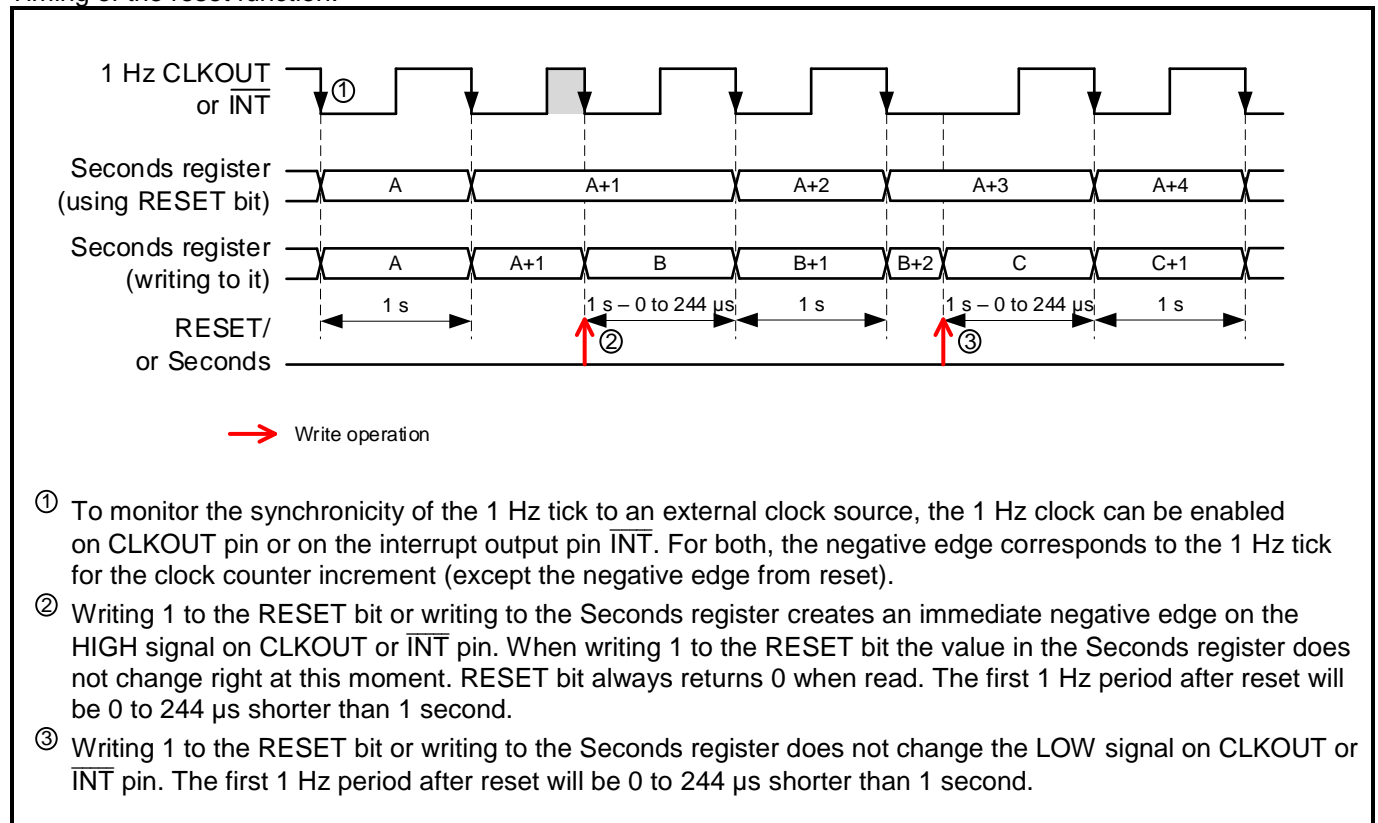


Procedure for setting the clock and calendar values using the RESET bit function:

1. Write the desired clock and calendar values within 950 ms to the registers (seconds, minutes, hours, weekday, date, month and year).
2. Write 1 to the RESET bit or write a value to the Seconds register for a synchronized start of the time circuits (1 Hz tick). The RESET bit always returns 0 when read.

See also sections SETTING THE TIME and SETTING THE UNIX TIME.

Timing of the reset function:



4.18. USER PROGRAMMABLE PASSWORD

After a Power up and the first refreshment of $t_{\text{PREFR}} = \sim 66 \text{ ms}$, the Password PW registers (RAM 21h to 24h) are reset to 00h and the value in EEPWE (EEPROM 30h) and the values in the EEPROM Password EEPW registers (EEPROM 31h to 34h) are copied from the EEPROM to the corresponding RAM mirror.

The first four Password registers (PW), in case of the use of the function (enabled by writing 255 into the EEPROM Password Enable register EEPWE), are used to write the 32-Bit Password necessary to be able to write in all writable registers that have the convention WP (time, control, user RAM, configuration EEPROM and user EEPROM registers). The 32-Bit Password PW is compared to the 32 bits stored in the RAM mirror of the EEPROM Password EEPW (see PASSWORD REGISTERS, EEPROM PASSWORD ENABLE REGISTER and EEPROM PASSWORD REGISTERS).

Caution: The number of possible passwords is $2^{32} \approx 4.3 \times 10^9 = 4.3 \text{ billion}$.

4.18.1. ENABLE/DISABLE WRITE PROTECTION

If the write protection function is enabled by writing 255 in register EEPWE (EEPROM 30h), it remains possible to read all the registers except the EEPROM registers. The EEPROM registers cannot be read because it cannot be written to the EE Address and EE Command registers. If the function is not enabled, read and write are possible for all corresponding registers.

If the write protection function is enabled, it is necessary to first write the correct 32-Bit Password PW (PW = EEPW) before any attempt to write in the RAM registers (Unlock), and to read and write in the EEPROM registers.

Once the user is finished with the write access and subsequently the write protection is still enabled or enabled again (by writing 255 in EEPROM register EEPWE), it is necessary to write an incorrect password (PW \neq EEPW) into the Password registers PW0 to PW3 in order to write-protect (Lock) the registers. See program sequences below and FLOWCHART.

Enable write protection:

1. Initial state: WP-Registers are Not write-protected (EEPWE \neq 255)
(Reference password is stored in the EEPROM Password EEPW)
2. Disable automatic refresh by setting EERD = 1
3. Enable password function by entering EEPWE = 255 (RAM)
4. Enter the correct password PW (PW = EEPW) to unlock write protection
5. Update EEPROM (all Configuration RAM \rightarrow EEPROM) by writing EECMD = 00h followed by 11h
6. Enable automatic refresh by setting EERD = 0
7. Enter an incorrect password PW (PW \neq EEPW) to lock the device
8. Final state: WP-Registers are Write-protected by password (EEPWE = 255)

Disable write protection:

1. Initial state: WP-Registers are Write-protected by password (EEPWE = 255)
(Reference password is stored in the EEPROM Password EEPW)
2. Enter the correct password PW (PW = EEPW) to unlock write protection
3. Disable automatic refresh by setting EERD = 1
4. Disable password function by entering EEPWE \neq 255 (RAM)
5. Update EEPROM (all Configuration RAM \rightarrow EEPROM) by writing EECMD = 00h followed by 11h
6. Enable automatic refresh by setting EERD = 0
7. Final state: WP-Registers are Not write-protected (EEPWE \neq 255)

Hint: The EEPROM values of the reference password in the EEPROM Password EEPW registers can be READ with the Read one EEPROM byte command (EECMD = 00h followed by 22h) when in Unlocked state (registers not write-protected). This option is useful if it is not certain which password is written in the EEPW before the write protection function is enabled. The RAM mirror from the EEPW registers can never be read.

4.18.2. CHANGING PASSWORD

To code a new password, the user has to first enter the current (correct) Password PW (PW = EEPW) into the registers 21h to 24h, if the WP-Registers are write protected, and then write a value not equal to all 1 (value \neq 255) in the EEPWE register (EEPROM 30h) to unlock write protection, and then write the new reference password EEPW into the EEPROM registers 31h to 34h and writing all 1 (value = 255) in the EEPWE register to enable password function. See program sequences below and FLOWCHART.

Change password if password function is enabled (EEPWE = 255):

1. Initial state: WP-Registers are Write-protected by old reference EEPROM Password EEPW
2. Enter old, correct password PW (PW = EEPW) to unlock write protection
3. Disable automatic refresh by setting EERD = 1
4. Disable password function by entering EEPWE \neq 255 (RAM)
5. Define a new reference password in the EEPW in registers (RAM)
6. Enable the password function by entering EEPWE = 255 (RAM)
7. Enter the correct password PW (PW = EEPW) to unlock write protection
8. Update EEPROM (all Configuration RAM \rightarrow EEPROM) by writing EECMD = 00h followed by 11h
9. Enable automatic refresh by setting EERD = 0
10. Enter an incorrect password PW (PW \neq EEPW) to lock the device
11. Final state: WP-Registers are Write-protected by new reference EEPROM Password EEPW

Change password if password function is disabled (EEPWE \neq 255):

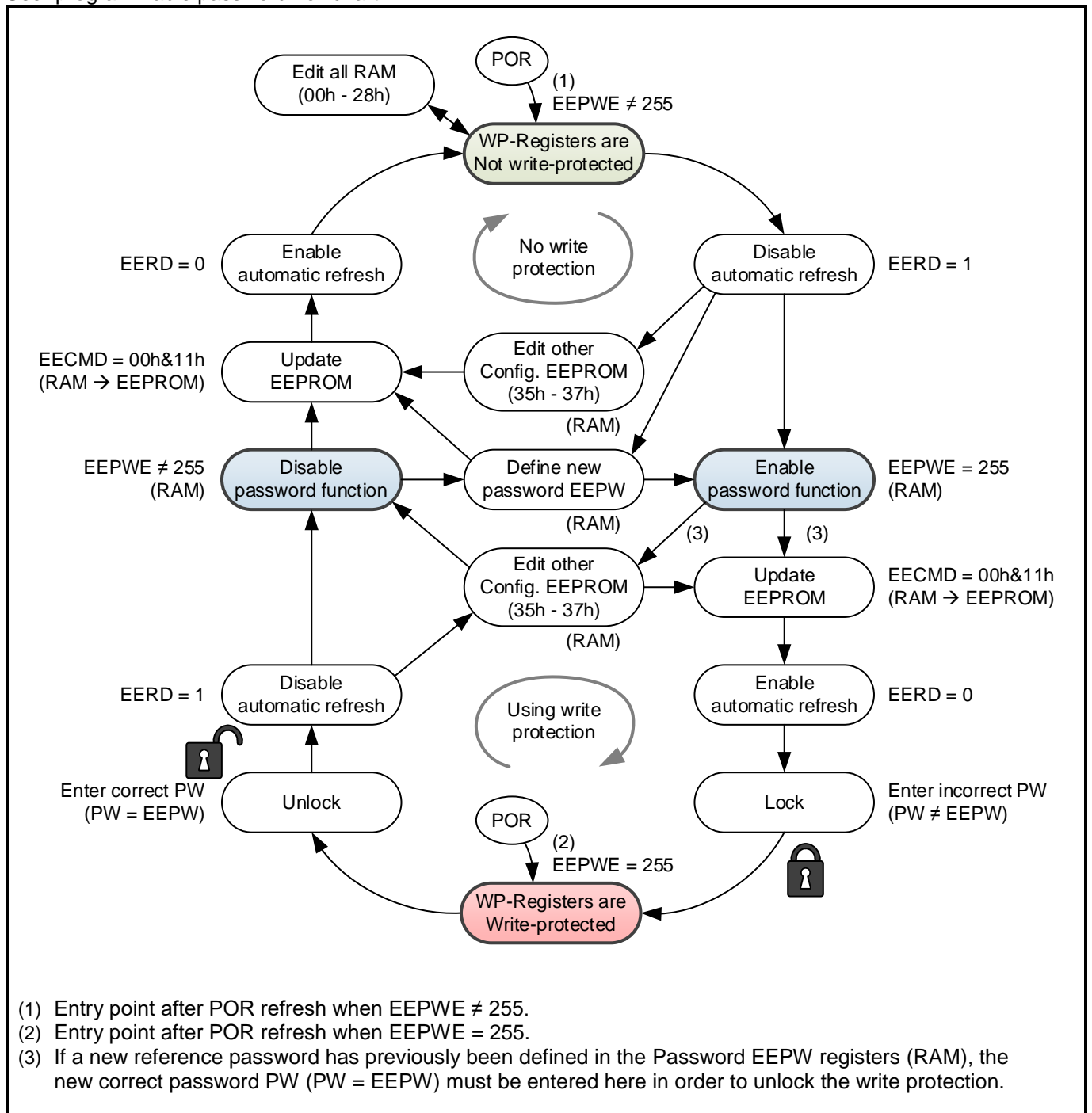
1. Initial state: Old reference password is stored in the EEPROM Password EEPW
2. Disable automatic refresh by setting EERD = 1
3. Define a new reference password in the EEPW registers (RAM)
4. Update EEPROM (all Configuration RAM \rightarrow EEPROM) by writing EECMD = 00h followed by 11h
5. Enable automatic refresh by setting EERD = 0
6. Final state: New reference password is stored in the EEPROM Password EEPW

Note that the EEPROM password EEPW = 00000000h is not a real password, because after POR the password PW is also 00000000h (PW = EEPW) and although the password function is enabled after POR refresh (EEPWE = 255) the PW-Registers are unlocked.

4.18.3. FLOWCHART

The following flowchart describes the programming of the enabling and disabling of the register write protection by user password and the changing of the user password and the other Configuration EEPROM registers (35h – 37h) if write protection is enabled or disabled. In this example the Update EEPROM command (writing EECMD = 00h followed by 11h) is applied to write (store) data from all Configuration RAM mirror bytes (addresses 30h to 37h) into the corresponding Configuration EEPROM bytes. See also USE OF THE CONFIGURATION REGISTERS.

User programmable password flowchart:



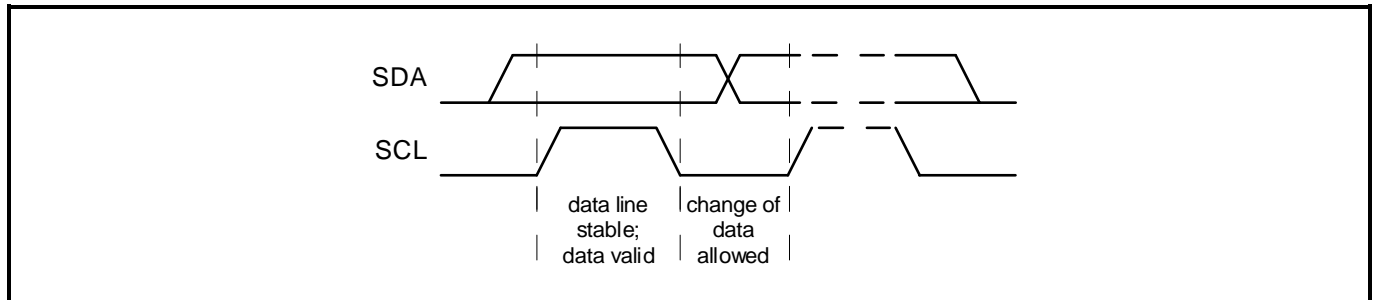
5. I²C INTERFACE

The I²C interface is for bidirectional, two-line communication between different ICs or modules. The RV-3028-C7 is accessed at addresses A4h/A5h, and supports Fast Mode (up to 400 kHz). The I²C interface consists of two lines: one bi-directional data line (SDA) and one clock line (SCL). Both lines are connected to a positive supply via pull-up resistors. Data transfer is initiated only when the interface is not busy.

5.1. BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line remains stable during the HIGH period of the clock pulse, as changes in the data line at this time are interpreted as a control signals. Data changes should be executed during the LOW period of the clock pulse (see Figure below).

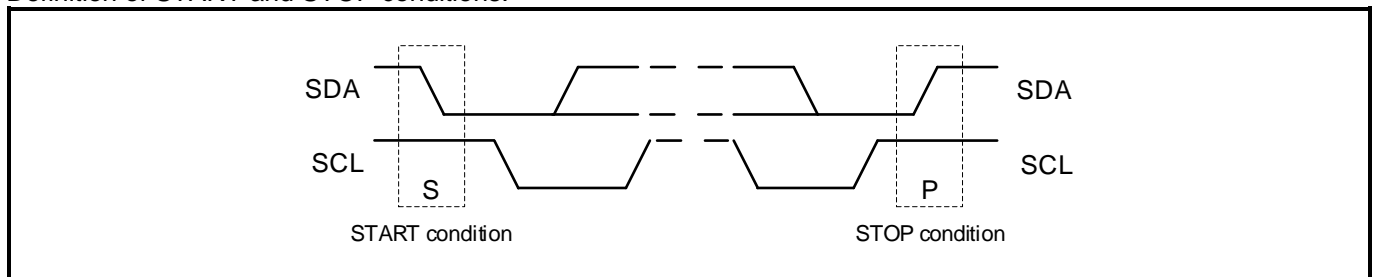
Bit transfer:



5.2. START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the STOP condition (P) (see Figure below).

Definition of START and STOP conditions:



A START condition which occurs after a previous START but before a STOP is called a Repeated START condition, and functions exactly like a normal STOP followed by a normal START.

Caution:

When communicating with the RV-3028-C7 module, the series of operations from transmitting the START condition to transmitting the STOP condition should occur within **950 ms**.

If this series of operations requires **950 ms or longer**, the I²C-bus interface will be automatically cleared and set to standby mode by the bus timeout function of the RV-3028-C7. Note with caution that both write and read operations are invalid for communications that occur during or after this auto clearing operation. When writing: no acknowledge will occur. When reading: FFh will be read.

Restarting of communications begins with transfer of the START condition again.

The I²C auto increment Address Pointer is neither reset by the I²C STOP condition nor by the internal stop forced after timeout.

5.3. DATA VALID

After a START condition, SDA is stable for the duration of the high period of SCL. The data on SDA may be changed during the low period of SCL. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and STOP conditions is not limited (however, the transfer time must be no longer than 950 ms). The information is transmitted byte-wise and each receiver acknowledges with a ninth bit.

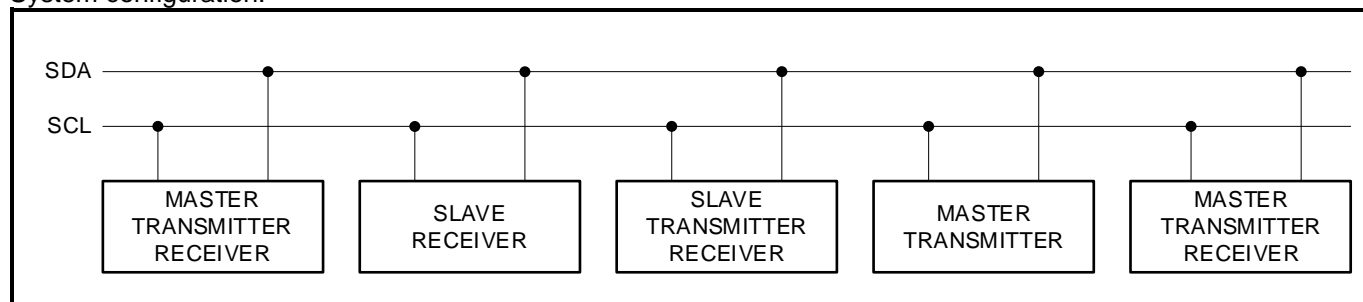
5.4. SYSTEM CONFIGURATION

Since multiple devices can be connected with the I²C-bus, all I²C-bus devices have a fixed and unique device number built-in to allow individual addressing of each device.

The device that controls the I²C-bus is the Master; the devices which are controlled by the Master are the Slaves. A device generating a message is a Transmitter; a device receiving a message is the Receiver. The RV-3028-C7 acts as a Slave-Receiver or Slave-Transmitter.

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the START procedure. The clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

System configuration:

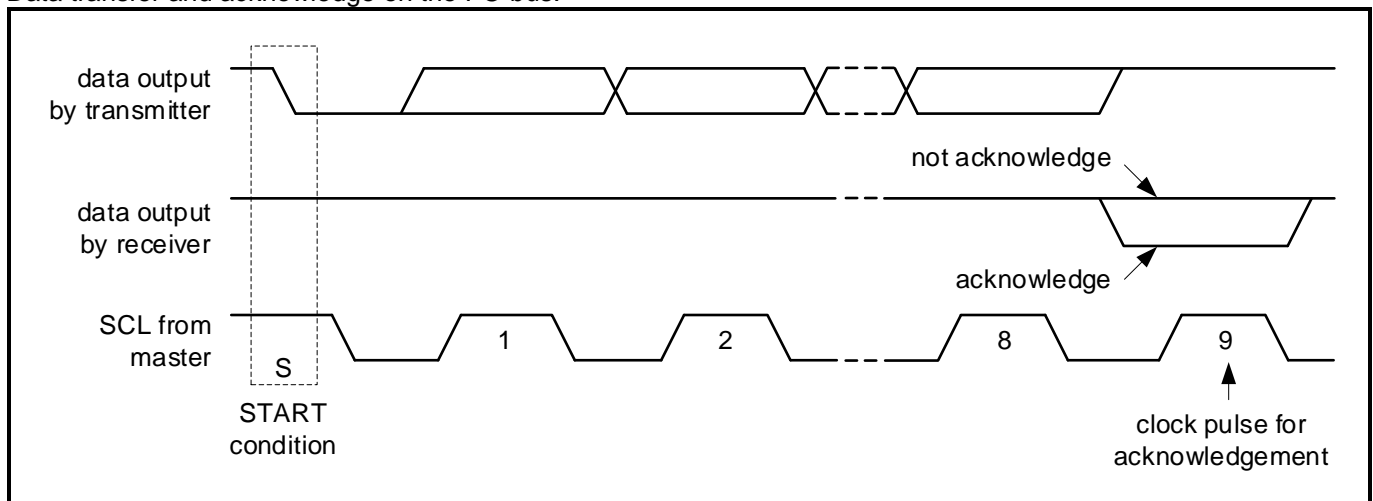


5.5. ACKNOWLEDGE

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited (however, the transfer time must be no longer than 950 ms). Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge cycle after the reception of each byte.
- Also a master receiver must generate an acknowledge cycle after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge cycle on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Data transfer and acknowledge on the I²C-bus:



5.6. SLAVE ADDRESS

On the I²C-bus the 7-bit slave address 1010010b is reserved for the RV-3028-C7. The entire I²C-bus slave address byte is shown in the following table.

| Slave address | | | | | | | R/ \bar{W} | Transfer data |
|---------------|-------|-------|-------|-------|-------|-------|-----------------|---------------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 (R) | A5h (read) |
| | | | | | | | 0 (\bar{W}) | A4h (write) |

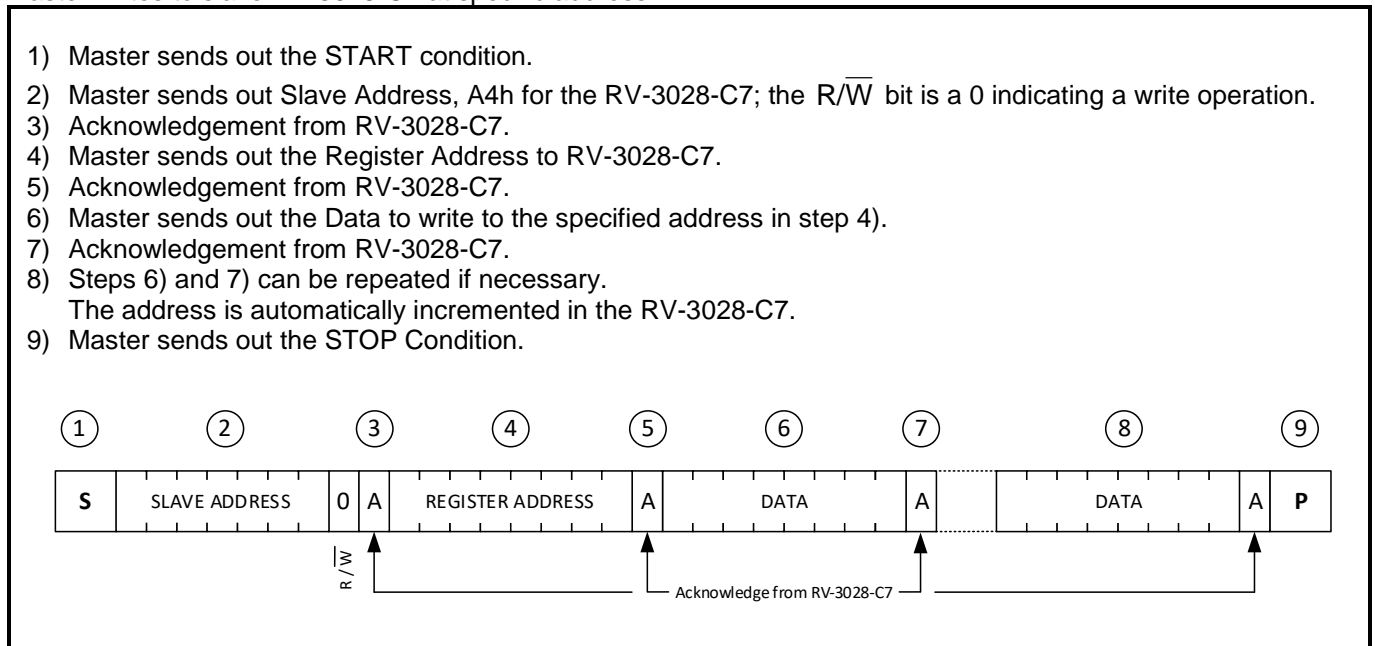
After a START condition, the I²C slave address has to be sent to the RV-3028-C7 device. The R/ \bar{W} bit defines the direction of the following single or multiple byte data transfer. The 7-bit address is transmitted MSB first. If this address is 1010010b, the RV-3028-C7 is selected, the eighth bit indicates a read (R/ \bar{W} = 1) or a write (R/ \bar{W} = 0) operation (results in A5h or A4h) and the RV-3028-C7 supplies the ACK. The RV-3028-C7 ignores all other address values and does not respond with an ACK.

In the write operation, a data transfer is terminated by sending either the STOP condition or the START condition of the next data transfer.

5.7. WRITE OPERATION

Master transmits to Slave-Receiver at specified address. The Register Address is an 8-bit value that defines which register is to be accessed next. After writing one byte, the Register Address is automatically incremented by 1.

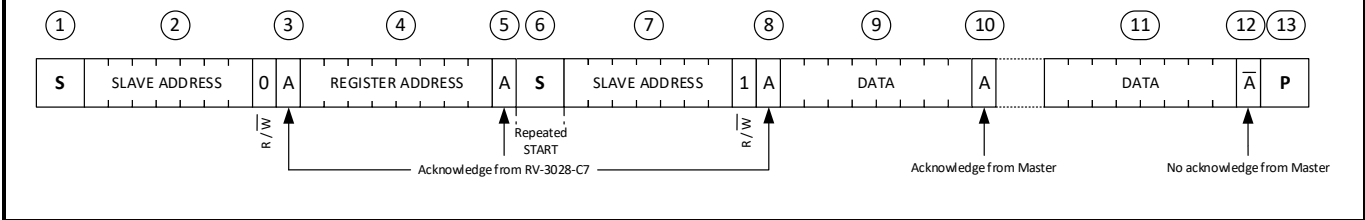
Master writes to slave RV-3028-C7 at specific address:



5.8. READ OPERATION AT SPECIFIC ADDRESS

Master reads data from slave RV-3028-C7 at specific address:

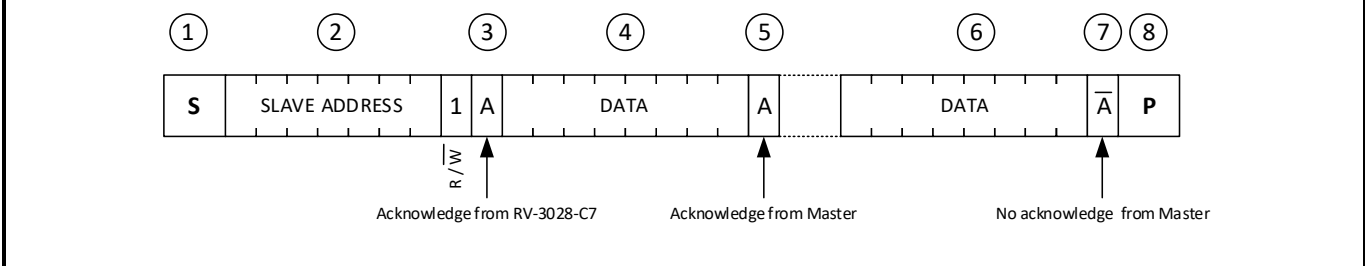
- 1) Master sends out the START condition.
- 2) Master sends out Slave Address, A4h for the RV-3028-C7; the $\overline{R/\overline{W}}$ bit is a 0 indicating a write operation.
- 3) Acknowledgement from RV-3028-C7.
- 4) Master sends out the Register Address to RV-3028-C7.
- 5) Acknowledgement from RV-3028-C7.
- 6) Master sends out the Repeated START condition (or STOP condition followed by START condition)
- 7) Master sends out Slave Address, A5h for the RV-3028-C7; the $\overline{R/\overline{W}}$ bit is a 1 indicating a read operation.
- 8) Acknowledgement from RV-3028-C7.
At this point, the Master becomes a Receiver and the Slave becomes the Transmitter.
- 9) The Slave sends out the Data from the Register Address specified in step 4).
- 10) Acknowledgement from Master.
- 11) Steps 9) and 10) can be repeated if necessary.
The address is automatically incremented in the RV-3028-C7.
- 12) The Master, addressed as Receiver, can stop data transmission by not generating an acknowledge on the last byte that has been sent from the Slave-Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a STOP condition.
- 13) Master sends out the STOP condition.



5.9. READ OPERATION

Master reads data from slave RV-3028-C7 immediately after first byte:

- 1) Master sends out the START condition.
- 2) Master sends out Slave Address, A5h for the RV-3028-C7; the $\overline{R/\overline{W}}$ bit is a 1 indicating a read operation.
- 3) Acknowledgement from RV-3028-C7.
At this point, the Master becomes a Receiver and the Slave becomes the Transmitter.
- 4) The RV-3028-C7 sends out the Data from the last accessed Register Address incremented by 1.
- 5) Acknowledgement from Master.
- 6) Steps 4) and 5) can be repeated if necessary.
The address is automatically incremented in the RV-3028-C7.
- 7) The Master, addressed as Receiver, can stop data transmission by not generating an acknowledge on the last byte that has been sent from the Slave-Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a STOP condition.
- 8) Master sends out the STOP condition.



5.10. I²C-BUS IN SWITCHOVER CONDITION

To save power when the RV-3028-C7 is in VBACKUP Power state the bus I²C-bus interface is automatically disabled (high impedance) and reset. Therefore the communication via I²C interface should be terminated before the supply is switched from V_{DD} to V_{BACKUP}. If the bus communication could not be completed properly, the I²C read/write data integrity is no longer guaranteed.

Note: If the I²C communication has ended in an uncontrolled manner, the I²C-bus interface has to be re-initialized by sending a STOP followed by a START after the device switched back from VBACKUP Power state to VDD Power state.

6. ELECTRICAL SPECIFICATIONS

6.1. ABSOLUTE MAXIMUM RATINGS

The following Table lists the absolute maximum ratings.

Absolute Maximum Ratings according to IEC 60134:

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|--------------------------|----------------------|------|-----|----------------------|------|
| V _{DD} | Power Supply Voltage | | -0.3 | | 6.0 | V |
| V _I | Input voltage | Input Pin | -0.3 | | V _{DD} +0.3 | V |
| V _O | Output voltage | Output Pin | -0.3 | | V _{DD} +0.3 | V |
| I _I | Input current | | -10 | | 10 | mA |
| I _O | Output current | | -10 | | 10 | mA |
| V _{ESD} | ESD Voltage | HBM ⁽¹⁾ | | | ±2000 | V |
| | | CDM ⁽²⁾ | | | ±500 | V |
| I _{LU} | Latch-up Current | Jedec ⁽³⁾ | | | ±100 | mA |
| T _{OPR} | Operating Temperature | | -40 | | 85 | °C |
| T _{STO} | Storage Temperature | | -55 | | 125 | °C |
| T _{PEAK} | Maximum reflow condition | JEDEC J-STD-020C | | | 265 | °C |

⁽¹⁾ HBM: Human Body Model, according to JS-001.

⁽²⁾ CDM: Charged-Device Model, according to JEDEC JS-002-201X.

⁽³⁾ Latch-up testing, according to JESD78., Class I (room temperature), level A (100 mA)

6.2. OPERATING PARAMETERS

For this Table, $T_A = -40$ to $+85^\circ\text{C}$ unless otherwise indicated. $V_{DD} = 1.2$ to 5.5 V, TYP values at 25°C and 3.0 V.

Operating Parameters:

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|-----|------|-----|---------------|
| Supplies | | | | | | |
| V_{DD} | Power Supply Voltage | Time-keeping mode ⁽¹⁾ | 1.1 | | 5.5 | V |
| | | Minimum time-keeping voltage ⁽¹⁾ | | 0.9 | 1.1 | |
| | | I ² C-bus (100 kHz) | 1.2 | | 5.5 | |
| | | I ² C-bus (400 kHz) | 2.0 | | 5.5 | |
| V_{BACKUP} | Backup Supply Voltage | | 1.1 | | 5.5 | V |
| I_{DD} | V_{DD} supply current timekeeping I ² C-bus inactive, CLKOUT disabled, average current | $V_{DD} = 1.1$ V ⁽²⁾ , $T_A = 25^\circ\text{C}$ | | 45 | 60 | nA |
| | | $V_{DD} = 3.0$ V ⁽²⁾ , $T_A = 25^\circ\text{C}$ | | 45 | 60 | |
| | | $V_{DD} = 5.0$ V ⁽²⁾ , $T_A = 25^\circ\text{C}$ | | 45 | 66 | |
| | | $V_{DD} = 1.1$ V ⁽²⁾ , $T_{OPR} = -40$ to $+85^\circ\text{C}$ | | | 300 | |
| | | $V_{DD} = 3.0$ V ⁽²⁾ , $T_{OPR} = -40$ to $+85^\circ\text{C}$ | | | 330 | |
| | | $V_{DD} = 5.0$ V ⁽²⁾ , $T_{OPR} = -40$ to $+85^\circ\text{C}$ | | | 400 | |
| $I_{DD:I2C}$ | V_{DD} supply current during I ² C burst read/write, CLKOUT disabled | $V_{DD} = 1.2$ V, SCL = 100 kHz ⁽³⁾ | | 2 | 15 | μA |
| | | $V_{DD} = 3.0$ V, SCL = 400 kHz ⁽³⁾ | | 5 | 40 | |
| | | $V_{DD} = 5.0$ V, SCL = 400 kHz ⁽³⁾ | | 7 | 60 | |
| $I_{DD:DSM}$ | V_{DD} supply current in Direct Switching Mode I ² C-bus inactive, CLKOUT disabled | $V_{DD} = 3.0$ V, $T_A = 25^\circ\text{C}$, $V_{BACKUP} < V_{DD}$ | | 95 | 150 | nA |
| $I_{DD:LSM}$ | V_{DD} supply current in Level Switching Mode I ² C-bus inactive, CLKOUT disabled | $V_{DD} = 3.0$ V, $T_A = 25^\circ\text{C}$ | | 115 | 180 | |
| $I_{BACKUP:DSM}$ | V_{BACKUP} supply current in Direct Switching Mode | $V_{BACKUP} = 3.0$ V, $T_A = 25^\circ\text{C}$, $V_{DD} < V_{BACKUP}$ | | 95 | 150 | |
| $I_{BACKUP:LSM}$ | V_{BACKUP} supply current in Level Switching Mode | $V_{BACKUP} = 3.0$ V, $T_A = 25^\circ\text{C}$, $V_{DD} < V_{TH:LSM}$ (2.0 V) | | 115 | 180 | |
| $\Delta I_{DD:CK32}$ | Additional V_{DD} supply current ⁽⁴⁾ | $V_{DD} = 3.0$ V, $F_{CLKOUT} = 32.768$ kHz, $C_L = 10$ pF | | 1 | | μA |
| $\Delta I_{DD:CK1024}$ | | $V_{DD} = 3.0$ V, $F_{CLKOUT} = 1024$ Hz, $C_L = 10$ pF | | 30 | | nA |
| $\Delta I_{DD:CK1}$ | | $V_{DD} = 3.0$ V, $F_{CLKOUT} = 1$ Hz, $C_L = 10$ pF | | 0.03 | | |
| <p>(1) Clocks operating and RAM registers retained.</p> <p>(2) All inputs and outputs are at 0 V or V_{DD}.</p> <p>(3) 2.2 kΩ pull-up resistors on SCL/SDA, excluding external peripherals and pull-up resistor current. All other inputs (besides SDA and SCL) are at 0 V or V_{DD}. Test conditions: Continuous burst read/write, 55h data pattern, 25 μs between each data byte, 20 pF load on each bus pin.</p> <p>(4) When CLKOUT is enabled the additional V_{DD} supply current ΔI_{DD} can be calculated as follows: $\Delta I_{DD} = C_L \times V_{DD} \times f_{OUT}$, e.g. $\Delta I_{DD} = 10$ pF \times 3.0 V \times 32'768 Hz = 980 nA \approx 1 μA</p> | | | | | | |

For this Table, $T_A = -40$ to $+85^\circ\text{C}$ unless otherwise indicated. $V_{DD} = 1.2$ to 5.5 V, TYP values at 25°C and 3.0 V.

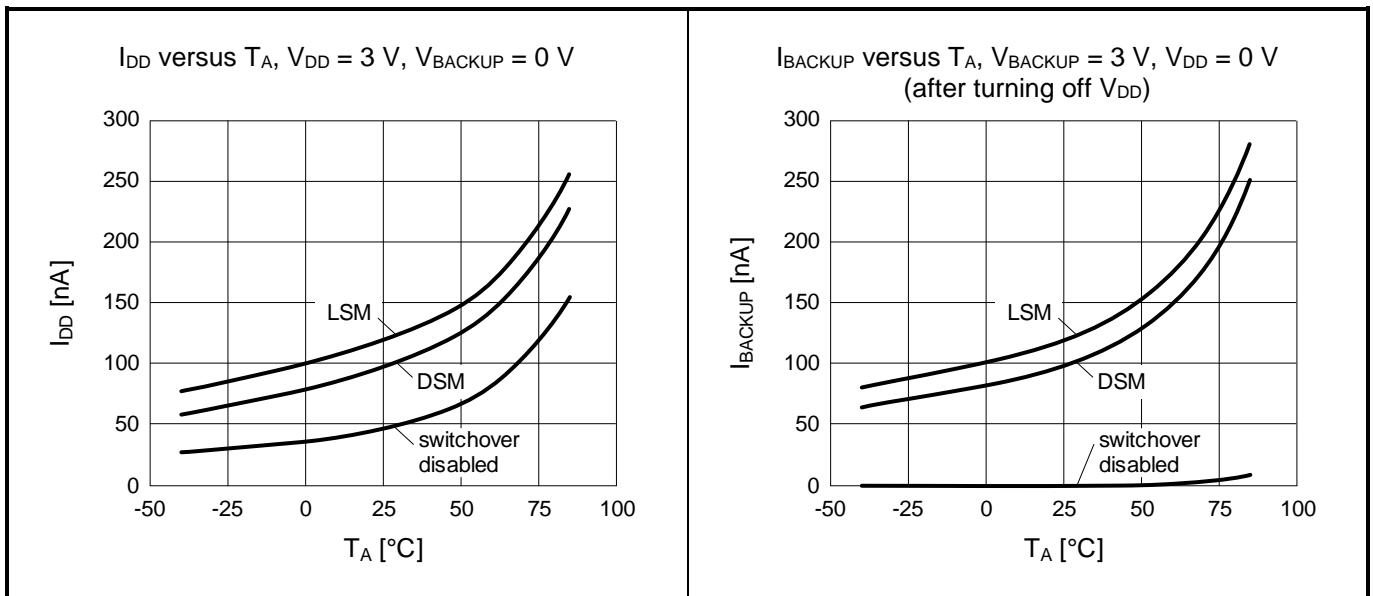
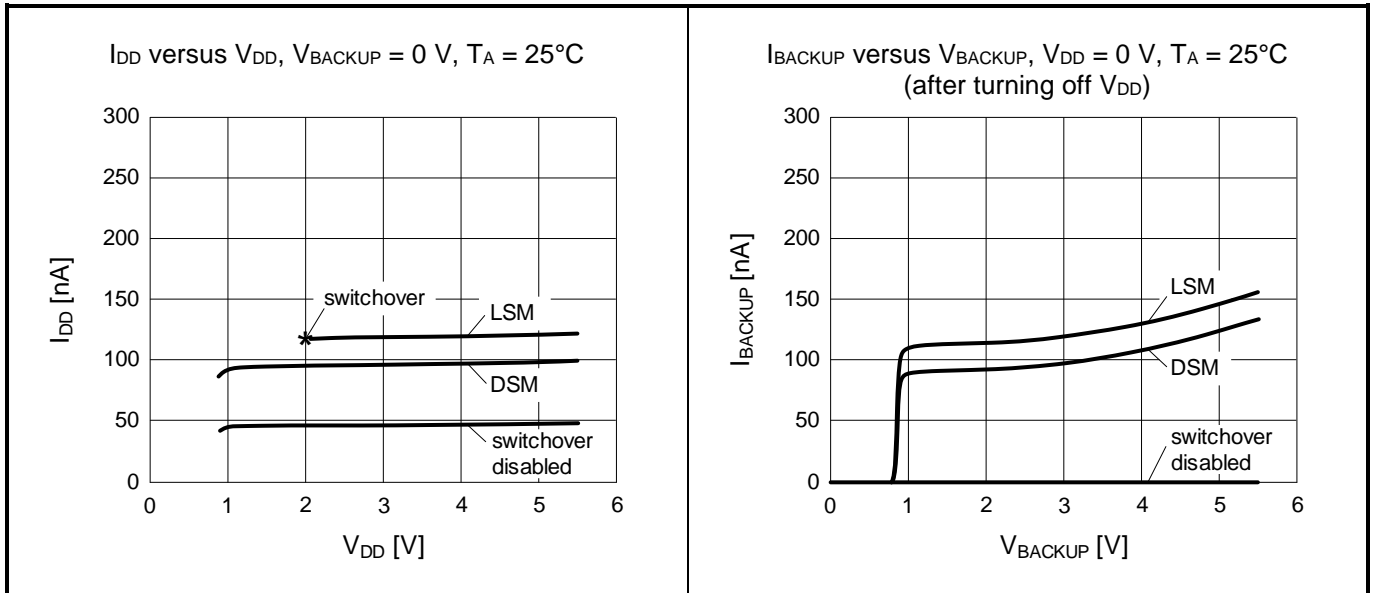
Operating Parameters (continued):

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|---|--|--------------|------|--------------|---------------|
| Inputs | | | | | | |
| V_{IH} | HIGH level input voltage | $V_{DD} = 1.1$ V to 5.5 V Pins: SCL, SDA, EVI | $0.8 V_{DD}$ | | | V |
| V_{IL} | LOW level input voltage | | | | $0.2 V_{DD}$ | V |
| I_{LEAK} | Input leakage current | $V_{SS} \leq V_I \leq V_{DD}$ | -0.5 | | 0.5 | μA |
| C_I | Input capacitance | $V_{DD} = 3.0$ V, $T_A = 25^\circ\text{C}$ $f = 1$ MHz | | | 7 | pF |
| Outputs | | | | | | |
| $V_{OH:CLK}$ | HIGH level output voltage CLKOUT | $V_{DD} = 1.1$ V, $I_{OH} = -0.1$ mA | 1.0 | | | V |
| | | $V_{DD} = 3.0$ V, $I_{OH} = -1.0$ mA | 2.7 | | | |
| | | $V_{DD} = 5.0$ V, $I_{OH} = -1.0$ mA | 4.5 | | | |
| $V_{OL:CLK}$ | LOW level output voltage CLKOUT | $V_{DD} = 1.1$ V, $I_{OL} = 0.1$ mA | | | 0.1 | V |
| | | $V_{DD} = 3.0$ V, $I_{OL} = 1.0$ mA | | | 0.3 | |
| | | $V_{DD} = 5.0$ V, $I_{OL} = 1.0$ mA | | | 0.5 | |
| V_{OL} | LOW level output voltage Pins: SDA, INT | $V_{DD} = 1.2$ V, $I_{OL} = 0.5$ mA | | | 0.4 | V |
| | | $V_{DD} = 3.0$ V, $I_{OL} = 3.0$ mA | | | 0.4 | |
| | | $V_{DD} = 5.0$ V, $I_{OL} = 3.0$ mA | | | 0.3 | |
| I_{OLEAK} | Output leakage current | $V_O = V_{DD}$ or V_{SS} | -0.5 | | 0.5 | μA |
| C_{OUT} | Output capacitance | $V_{DD} = 3.0$ V, $T_A = 25^\circ\text{C}$ $f = 1$ MHz | | | 7 | pF |
| Power On Reset | | | | | | |
| V_{POR} | POR detection threshold | | 0.75 | 0.8 | 0.85 | V |
| Trickle charger | | | | | | |
| TCR 3 k Ω | Current limiting resistor | $V_{DD} = 5.0$ V, $V_{BACKUP} = 3.0$ V, including internal schottky diode | 2 | 3 | 4 | k Ω |
| TCR 5 k Ω | | | 4.5 | 5.5 | 6.25 | |
| TCR 9 k Ω | | | 7.5 | 9.3 | 11.6 | |
| TCR 15 k Ω | | | 12.5 | 15.5 | 17.4 | |
| V_F | Schottky diode voltage drop | | | 0.25 | | V |
| Switchover | | | | | | |
| $V_{HYST:DSM}$ | Switchover hysteresis in Direct Switching Mode | V_{DD} with respect to $V_{BACKUP} = 3.0$ V, V_{DD} slew rate = ± 1 V/ms $T_{OPR} = -40$ to $+85^\circ\text{C}$ | | 60 | | mV |
| $V_{TH:LSM}$ | Backup switchover threshold voltage in Level Switching Mode | V_{DD} falls below $V_{TH:LSM}$ | 1.8 | 2.0 | 2.2 | V |
| $V_{HYST:LSM}$ | Switchover hysteresis in Level Switching Mode | V_{DD} with respect to $V_{BACKUP} = 3.0$ V, V_{DD} slew rate = ± 1 V/ms $T_{OPR} = -40$ to $+85^\circ\text{C}$ | | 100 | | mV |
| EEPROM Characteristics | | | | | | |
| $V_{DD:READ}$ | V_{DD} read voltage | V_{DD} Power state | 1.1 | | | V |
| $V_{DD:WRITE}$ | V_{DD} write voltage | | 1.5 | | | |
| t_{PREFR} | POR refresh time | At power up | | 66 | | ms |
| t_{AREFR} | Automatic refresh time | Each 24 hours, EERD = 0 | | 3.5 | | |
| t_{UPDATE} | Update time | EECMD = 11h | | 63 | | |
| t_{REFR} | Refresh time | EECMD = 12h | | 3.5 | | |
| t_{WRITE} | Write to one EEPROM byte time | EECMD = 21h | 4 | 16 | 30 | |
| t_{READ} | Read one EEPROM byte time | EECMD = 22h | | 1.4 | | |
| n_{CYCLE} | Write cycle endurance ⁽¹⁾ | $V_{DD} = 3.0$ V, $T_A = 25^\circ\text{C}$ | 10'000 | | | cycles |
| | | $V_{DD} = 5.5$ V, $T_A = 85^\circ\text{C}$ | 100 | | | |
| t_{RET} | Data retention time ⁽¹⁾ | $T_A = 55^\circ\text{C}$ | 10 | | | years |

⁽¹⁾ Guaranteed by indirect testing.

6.2.1.TYPICAL CHARACTERISTICS

Typical characteristics for Direct Switching Mode (DSM), Level Switching Mode (LSM) and switchover disabled:
 For these diagrams, I²C-bus inactive, CLKOUT disabled.



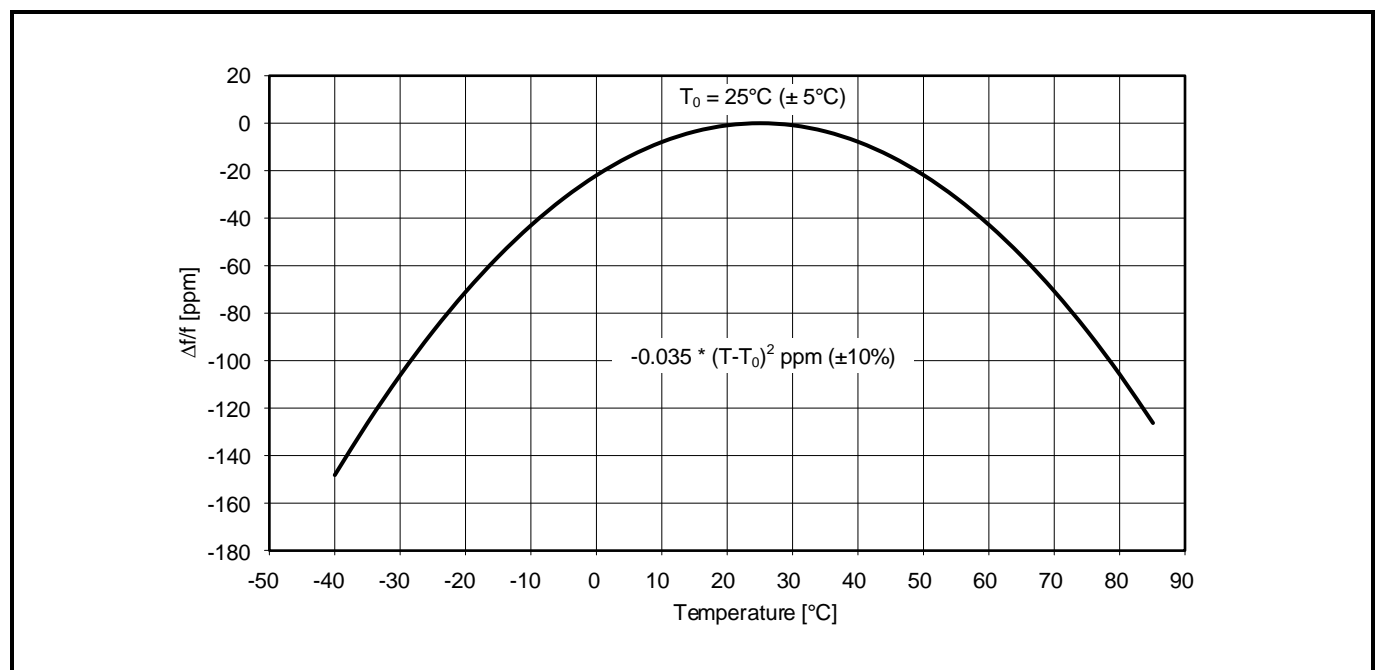
6.3. OSCILLATOR PARAMETERS

For this Table, $T_A = -40$ to $+85^\circ\text{C}$ unless otherwise indicated. $V_{DD} = 1.2$ to 5.5 V, TYP values at 25°C and 3.0 V.

Oscillator Parameters:

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|--|--|-------------|-------------------|------------------|
| Xtal General | | | | | | |
| F | Crystal Frequency | | | 32.768 | | kHz |
| t_{START} | Oscillator start-up time at $V_{DD} = 3.0$ V | $T_A = 25^\circ\text{C}$ | | 0.2 | 1 | s |
| V_{START} | Oscillator start-up voltage | | 1.3 | | 3 | V |
| $\Delta f/V$ | Frequency vs. voltage characteristics | $V_{DD} = 1.1$ V to 5.5 V $T_A = 25^\circ\text{C}$ | | 0.5 | 1 | ppm/V |
| V_{DDR} | V_{DD} rising slew rate | $V_{DD} = 1.1$ V to 3.6 V | | | 2.5 | V/ms |
| | | $V_{DD} = 3.6$ V to 5.5 V | | | 3.8 | |
| V_{DDF} | V_{DD} falling slew rate | $V_{DD} = 5.5$ V to 1.1 V | | | 2.2 | |
| δ_{CLKOUT} | CLKOUT duty cycle | $V_{DD} = 1.1$ V to 5.5 V $F_{CLKOUT} = 32.768$ kHz | | 50 \pm 10 | | % |
| Xtal Frequency Characteristics | | | | | | |
| $\Delta F/F$ | Frequency accuracy | $T_A = 25^\circ\text{C}$ | | | ± 5 | ppm |
| $\Delta F/F_{TOPR}$ | Frequency vs. temperature characteristics | $T_{OPR} = -40$ to $+85^\circ\text{C}$ $V_{DD} = 3.0$ V | $-0.035 \text{ ppm}/^\circ\text{C}^2 (T_{OPR} - T_0)^2 \pm 10\%$ | | | ppm |
| T_0 | Turnover temperature | | $+25 \pm 5$ | | | $^\circ\text{C}$ |
| $\Delta F/F$ | Aging first year max. | $T_A = 25^\circ\text{C}$, $V_{DD} = 3.0$ V | | | ± 3 | ppm |
| Xtal Frequency Offset Correction | | | | | | |
| $\Delta t/t$ | EEOffset correction: Min. corr. step (LSB) and Max. corr. range | $T_A = -40$ to $+85^\circ\text{C}$ | ± 0.954 | | +243.2/ -244.1 | ppm |
| $\Delta t/t$ | EEOffset. Achievable time accuracy. | Calibrated at an initial temperature and voltage | -0.48 | | +0.48 | ppm |
| $\Delta t/t$ | EEOffset. Factory Calibrated time accuracy. | Calibrated at $T_A = 25^\circ\text{C}$, $V_{DD} = 3.0$ V | | ± 1 | | ppm |

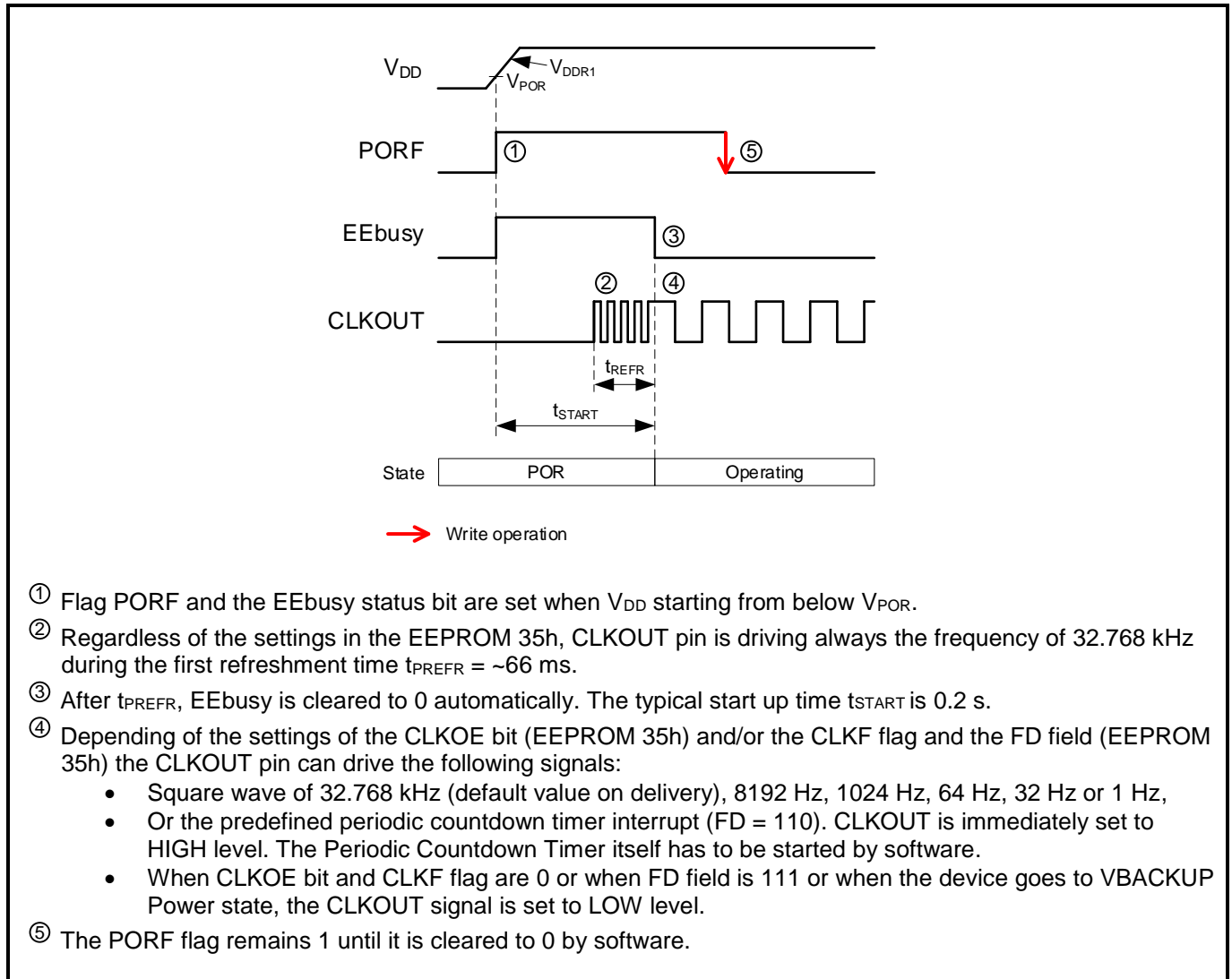
6.3.1.XTAL FREQUENCY VS. TEMPERATURE CHARACTERISTICS



6.4. POWER ON AC ELECTRICAL CHARACTERISTICS

The following Figure describes the power on AC electrical characteristics for the CLKOUT pin. The clock output signal on CLKOUT pin is primarily controlled by the CLKOE bit (EEPROM 35h), the CLKF flag and the FD field (EEPROM 35h). See also CLOCK OUTPUT SCHEME and USE OF THE CONFIGURATION REGISTERS.

Power On AC Electrical Characteristics:



For this Table, $T_A = -40$ to $+85^\circ\text{C}$ and $V_{DD} = 1.2$ to 5.5 V, TYP values at 25°C and 3.0 V.

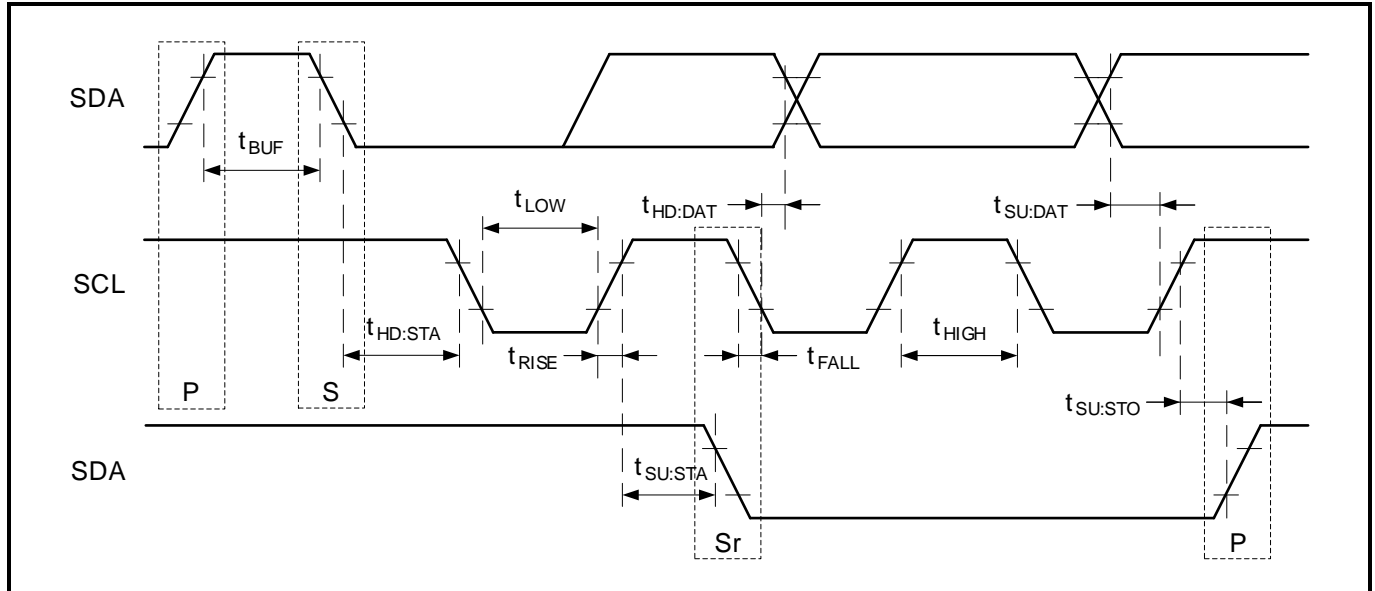
Power On AC Electrical Parameters:

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------|---|--------------------------|-----|-----|-----|------|
| V_{DDR1} | V_{DD} rising slew rate at initial power on reset (POR) | | 0.1 | | 1 | V/ms |
| t_{START} | Oscillator start-up time at $V_{DD} = 3.0$ V | $T_A = 25^\circ\text{C}$ | | 0.2 | 1 | s |
| V_{START} | Oscillator start-up voltage | | 1.3 | | 3 | |
| t_{PREFR} | First refreshment time | | | 66 | | ms |

6.5. I²C-BUS CHARACTERISTICS

The following Figure and Table describe the I²C AC electrical parameters.

I²C AC Parameter Definitions:



For the following Table, $T_A = -40$ to $+85^{\circ}\text{C}$.

I²C AC Electrical Parameters:

| SYMBOL | PARAMETER | $V_{DD} \geq 1.2\text{ V}$ | | $V_{DD} \geq 2.0\text{ V}$ | | UNIT |
|--------------|---|----------------------------|------|----------------------------|-----|---------------|
| | | MIN | MAX | MIN | MAX | |
| f_{SCL} | SCL input clock frequency | 0 | 100 | 0 | 400 | kHz |
| t_{LOW} | Low period of SCL clock | 4.7 | | 1.3 | | μs |
| t_{HIGH} | High period of SCL clock | 4.0 | | 0.6 | | μs |
| t_{RISE} | Rise time of SDA and SCL | | 1000 | | 300 | ns |
| t_{FALL} | Fall time of SDA and SCL | | 300 | | 300 | ns |
| $t_{HD:STA}$ | START condition hold time | 4.0 | | 0.6 | | μs |
| $t_{SU:STA}$ | START condition setup time | 4.7 | | 0.6 | | μs |
| $t_{SU:DAT}$ | SDA setup time | 250 | | 100 | | ns |
| $t_{HD:DAT}$ | SDA hold time | 0 | | 0 | | μs |
| $t_{SU:STO}$ | STOP condition setup time | 4.0 | | 0.6 | | μs |
| t_{BUF} | Bus free time before a new transmission | 4.7 | | 1.3 | | μs |

S = Start condition, Sr = Repeated Start condition, P = Stop condition

Caution:

When accessing the RV-3028-C7, all communication from transmitting the Start condition to transmitting the Stop condition after access should be completed within 950 ms.

If such communication requires 950 ms or longer, the I²C-bus interface is reset by the internal bus timeout function.

7. TYPICAL APPLICATION CIRCUITS

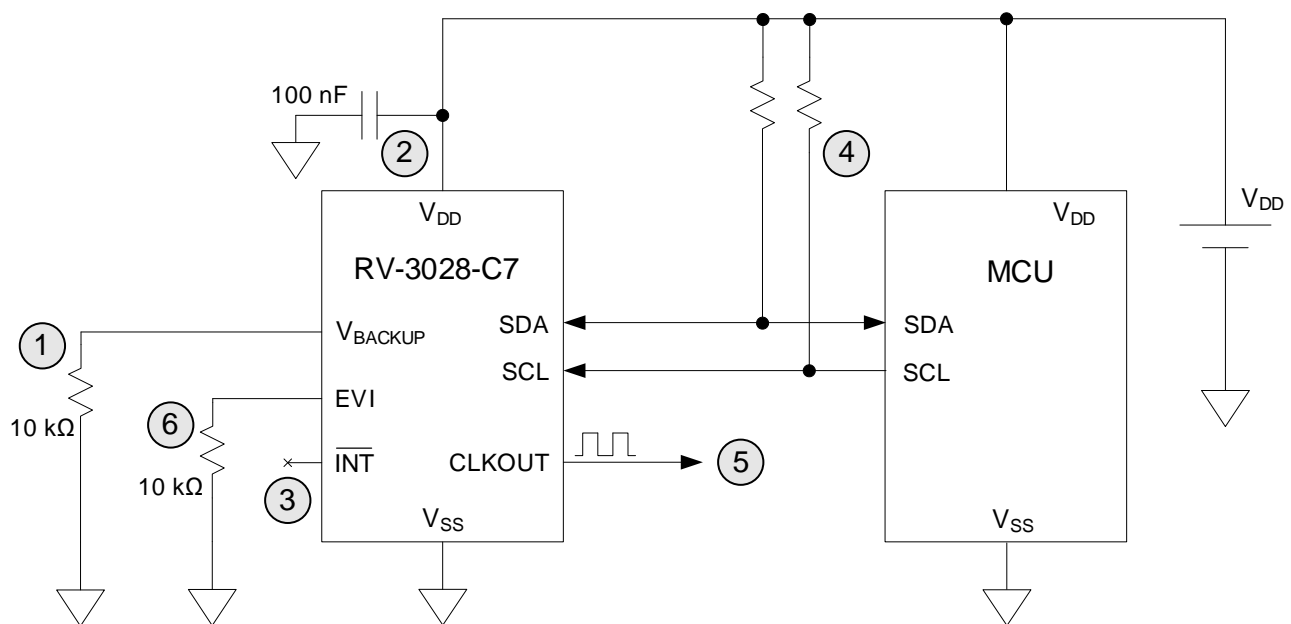
7.1. NO BACKUP SOURCE / EVENT INPUT NOT USED

Application Key Points:

- No V_{BACKUP} source
- Lowest current consumption (45 nA typ.)
- CLKOUT settings stored in EEPROM for permanent configuration

Register Configuration:

| | | | | | | | | | | | |
|----|--|-------|---|---|---|---|----|---|---|--|---|
| 0. | RTC with default configuration on delivery (bits in black) | | | | | | | | | | |
| 1. | Register 35h | CLKOE | | | | | FD | | | | CLKOE → CLKOUT to be set FD → Frequency to be selected |
| | | X | 1 | 0 | 0 | 0 | X | X | X | | |
| 2. | CLKOUT settings (35h) to be stored in EEPROM using procedure of 4.6.3. | | | | | | | | | | |



- Backup Switchover functionality is disabled by default. Do not leave V_{BACKUP} power supply pin floating. Connection to V_{SS} through a 10 kΩ resistor keeps functional test possible.
- 100 nF decoupling capacitor close to the device.
- Interrupts are disabled by default. $\overline{\text{INT}}$ pin is an open-drain output, which can be left open when not used.
- I²C lines SCL, SDA are open-drain and require pull-up resistors to V_{DD} .
- CLKOUT with a frequency of 32.768 kHz (*) is enabled by default (default value on delivery). If not used, disable CLKOUT to minimize current consumption (CLKOE = 0 and CLKF = 0, or FD = 111).
- External Events functionality is disabled by default. Do not leave EVI input pin floating. Connection to V_{SS} through a resistor keeps functional test possible.

(*) CLKOUT offers the selectable frequencies 32.768 kHz (default), 8192 Hz, 1024 Hz, 64 Hz, 32 Hz or 1 Hz, or the predefined periodic countdown Timer Interrupt for application use.

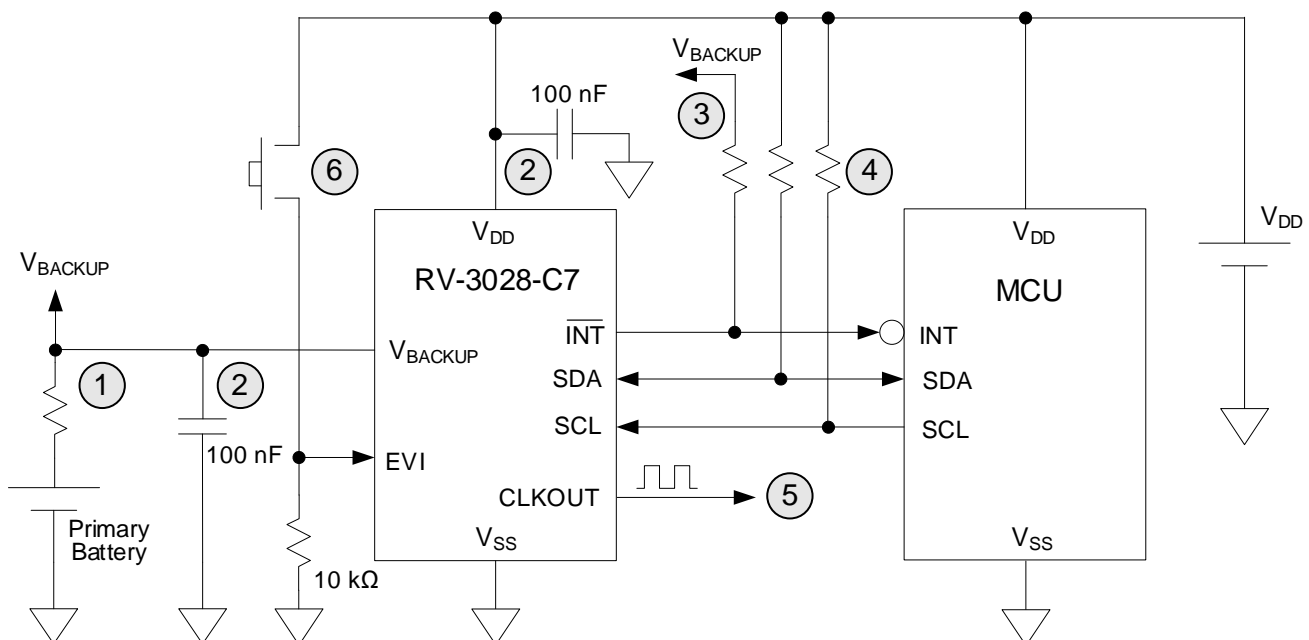
7.2. NON-RECHARGEABLE BACKUP SOURCE / EVENT INPUT USED (ACTIVE HIGH)

Application Key Points:

- Trickle charger disabled to avoid dangerous charging current into the backup source
- LSM Backup Switchover Mode to avoid non-desired backup switching ($V_{TH:LSM} = 2.0\text{ V}$)
- Power Management settings have to be stored in EEPROM for permanent configuration
- Rising edge or high-level voltage applied to the EVI input triggers an interrupt

Register Configuration:

| 0. RTC with default configuration on delivery (bits in black) | | | | | | | | | | |
|---|--------------|-----|-----|----|---|---|---|---|---------------------------|--------------------------------|
| 1. | Register 10h | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | EIE → Event interrupt enabled |
| | Register 13h | EHL | | ET | | | | | | EHL → Event-high detection |
| | | 0 | 1 | X | X | 0 | 0 | 0 | 0 | ET → Event filtering to be set |
| Register 37h | TCE | | BSM | | | | | | | TCE → Trickle charger disabled |
| | 0/1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | BSM → LSM switchover mode | |
| 2. Switchover settings (37h) to be stored in EEPROM using procedure of 4.6.3. | | | | | | | | | | |



- ① Insert a protection resistor of 100 – 1000 Ω to prevent damage in case of soldering issues causing short between supply pins.
- ② 100 nF decoupling ceramic capacitor close to the device for V_{DD} and V_{BACKUP} .
- ③ The \overline{INT} signal also works when the device operates on V_{BACKUP} supply voltage. In that case, it is possible to tie the \overline{INT} signal pull-up resistor to V_{BACKUP} .
- ④ I²C lines SCL, SDA are open-drain and require pull-up resistors to V_{DD} .
- ⑤ CLKOUT is disabled in V_{BACKUP} Power state. If not used in V_{DD} Power state, disable CLKOUT to minimize current consumption (CLKOE = 0 and CLKF = 0, or FD = 111).
- ⑥ EVI input set to detect rising edge or high-level of tamper detection signal; The EVI input is never floating thanks to the 10 k Ω to V_{SS} .

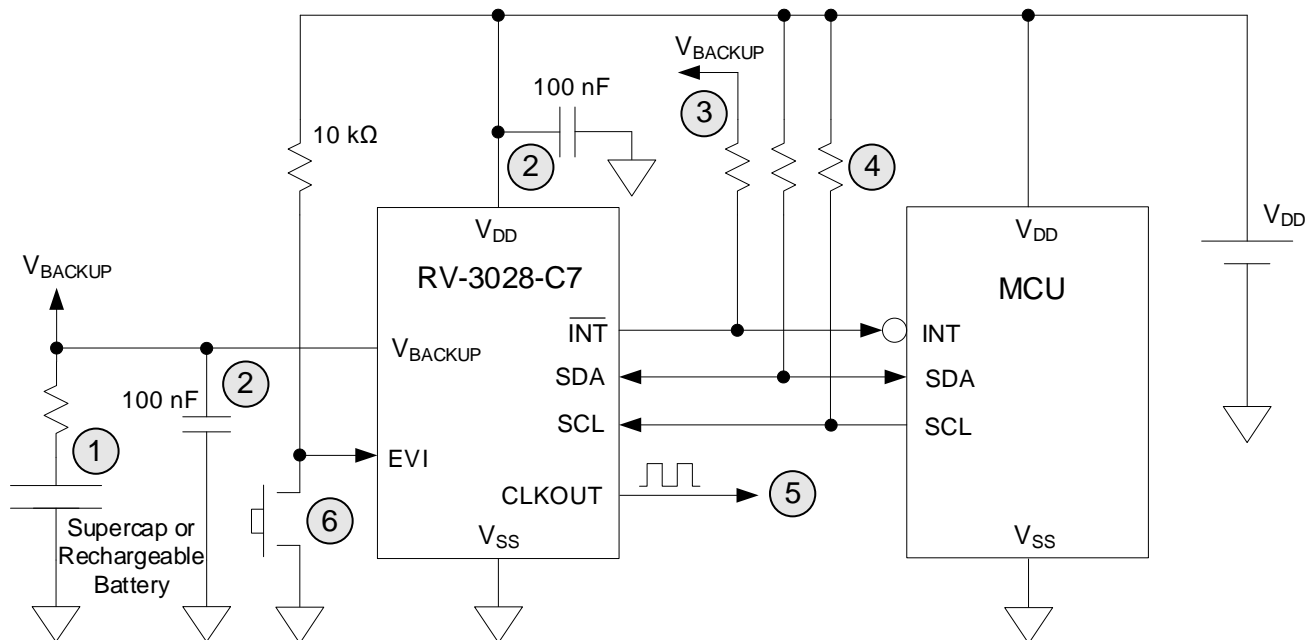
7.3. RECHARGEABLE BACKUP SOURCE / EVENT INPUT USED (ACTIVE LOW)

Application Key Points:

- MLCC, Supercap or Rechargeable Battery as secondary V_{BACKUP} source
- DSM Backup Switchover Mode for capacitors (or LSM for rechargeable battery)
- Backup source charged through the trickle charger
- Power Management settings have to be stored in EEPROM for permanent configuration

Register Configuration:

| | | | | | | | | | | |
|----|--|-----|----------|----------|---|----------|---|----------|---|--|
| 0. | RTC with default configuration on delivery (bits in black) | | | | | | | | | |
| 1. | Register 10h | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | EIE → Event interrupt enabled |
| | Register 13h | 0 | EHL 0 | ET X | X | 0 | 0 | 0 | 0 | EHL → Event-low detection ET → Event filtering to be set |
| | Register 37h | 0/1 | 0 | TCE 1 | 1 | BSM 0 | 1 | TCR X | X | TCE → Trickle charger enabled BSM → DSM switchover mode TCR → Trickle resistor to be set |
| 2. | Switchover settings (37h) to be stored in EEPROM using procedure of 4.6.3. | | | | | | | | | |



- ① Low-cost MLCC (*) ceramic capacitor, supercapacitor (e.g. 1 farad) or secondary battery LMR (respect manufacturer specifications for constant charging voltage).
When Lithium Battery is used, it is recommended to insert a protection resistor of 100 – 1000 Ω. to limit battery current and to prevent damage in case of soldering issues causing short between supply pins.
- ② 100 nF decoupling ceramic capacitor close to the device for V_{DD} and V_{BACKUP} .
- ③ The \overline{INT} signal also works when the device operates on V_{BACKUP} supply voltage.
In that case, it is possible to tie the \overline{INT} signal pull-up resistor to V_{BACKUP} .
- ④ I²C lines SCL, SDA are open-drain and require pull-up resistors to V_{DD} .
- ⑤ CLKOUT is disabled in V_{BACKUP} Power state. If not used in V_{DD} Power state, disable CLKOUT to minimize current consumption (CLKOE = 0 and CLKF = 0, or FD = 111).
- ⑥ EVI input set to detect falling edge or low-level of tamper detection signal;
The EVI input is never floating thanks to the 10 kΩ to V_{DD} .

(*) Note, that low-cost MLCCs are normally used for short time keeping (minutes) and the more expensive supercapacitors for a longer backup time (days - weeks).

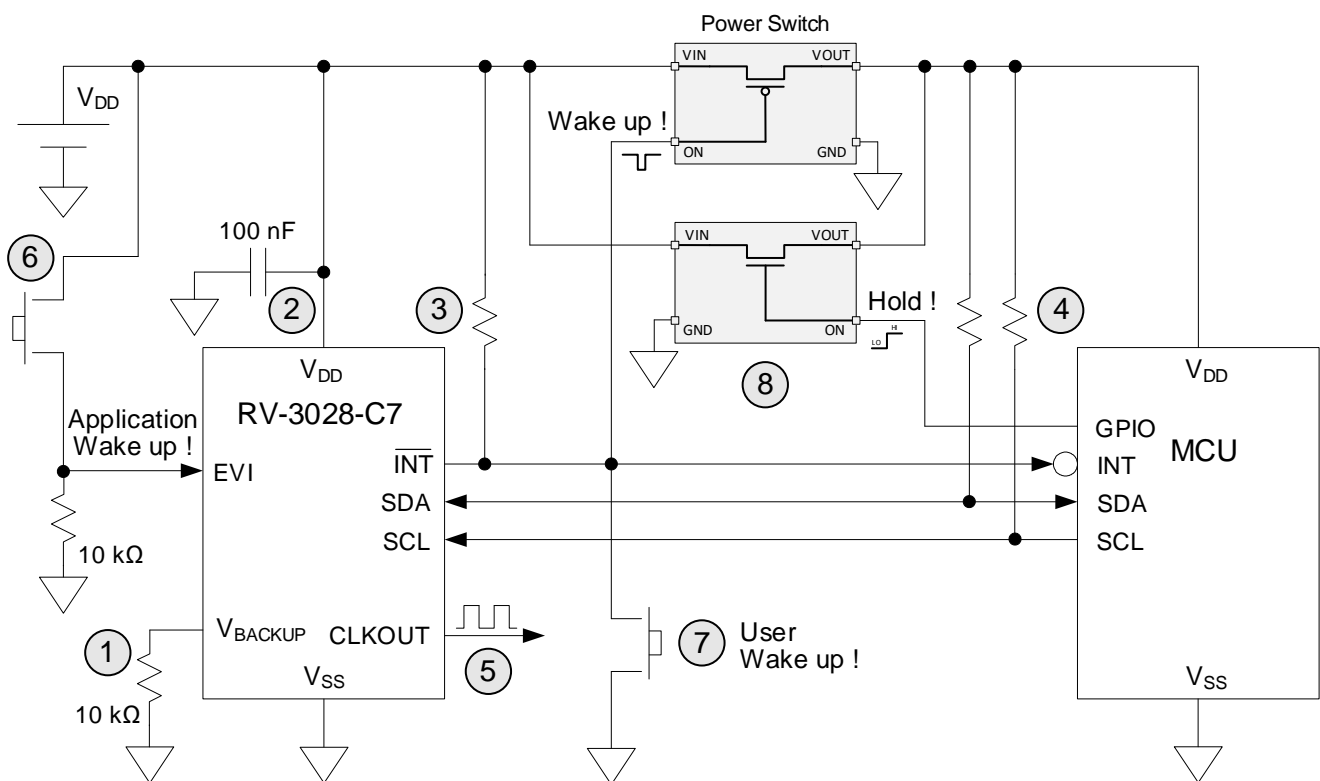
7.4. NO BACKUP SOURCE / EVENT INPUT USED (“WAKE-UP” & “POWER SWITCH”)

Application Key Points:

- No V_{BACKUP} source and lowest current consumption (45 nA typ.)
- External Event enabled allowing RTC to fire “wake-up” interrupt acting on load switch
- MCU most of the time in idle mode is awoken by RTC’s interrupt through the upper load switch
- MCU holds supply voltage until its task is finished and cuts off its own supply voltage

Register Configuration:

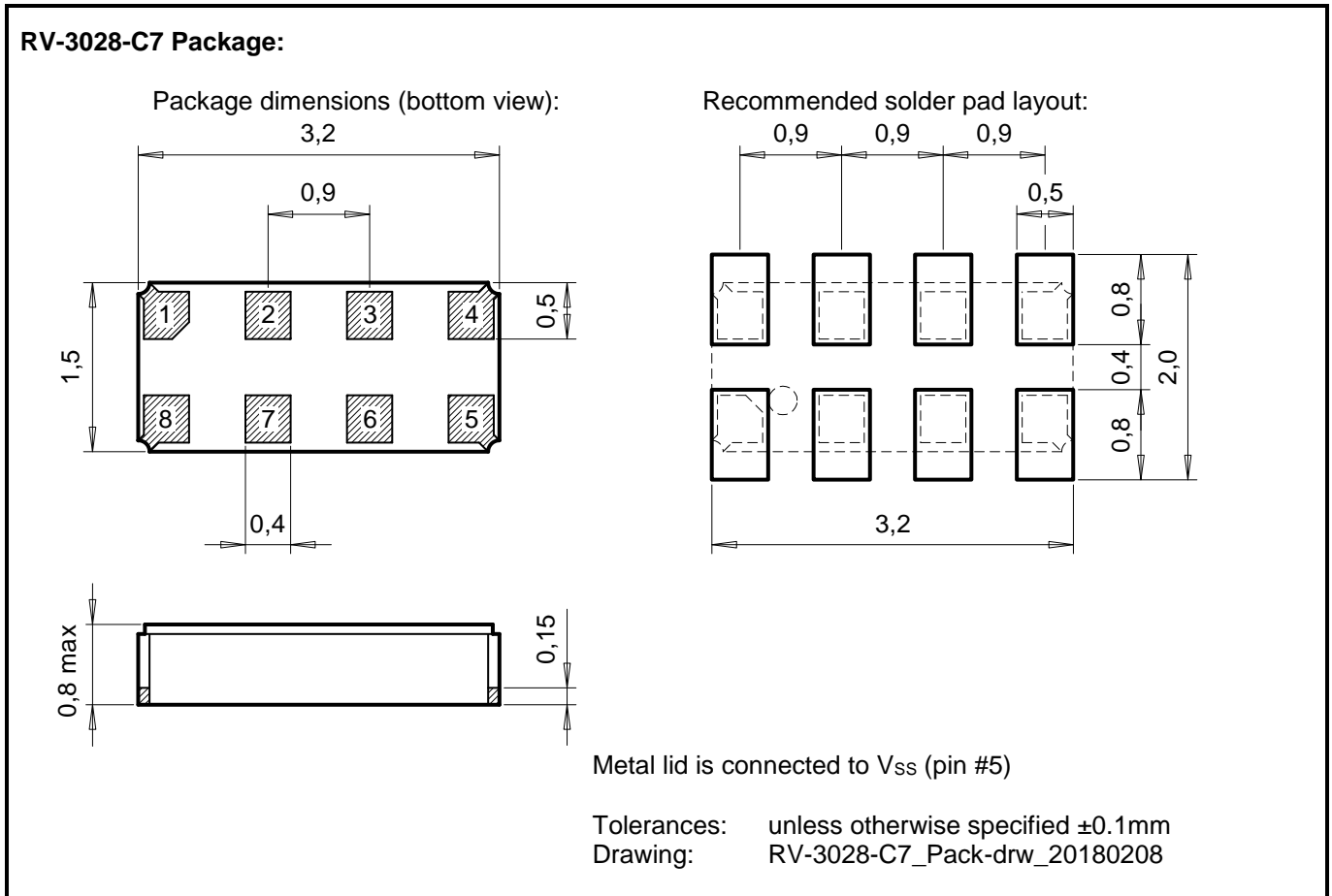
| | | | | | | | | | | |
|----|--|---|----------|---------|---|---|---|---|---|--|
| 0. | RTC with default configuration on delivery (bits in black) | | | | | | | | | |
| 1. | Register 10h | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | EIE → Event interrupt enabled |
| | Register 13h | 0 | EHL 1 | ET X | X | 0 | 0 | 0 | 0 | EHL → Event-high detection ET → Event filtering to be set |



- Backup Switchover functionality is disabled by default. Do not leave V_{BACKUP} power supply pin floating. Connection to V_{SS} through a 10 kΩ resistor keeps functional test possible.
- 100 nF decoupling capacitor close to the device.
- \overline{INT} pin is an open-drain output and requires a pull-up resistor.
- I²C lines SCL, SDA are open-drain and require pull-up resistors to V_{DD} .
- Disable CLKOUT to minimize current consumption (CLKOE = 0 and CLKF = 0, or FD = 111).
- EVI input set to detect rising edge or high-level of tamper detection signal; can be used as an Application Wake-Up signal. The EVI Input is never floating thanks to the 10 kΩ to V_{SS} .
- User or Manual Wake-Up, always available; e.g for initial system power-on to configure RTC and system.
- MCU Power Retention via GPIO = High maintains MCU Power to complete I²C Interface communication with the RTC. MCU cuts-off it's own supply voltage by set GPIO = Low at the very end of its task.

8. PACKAGE

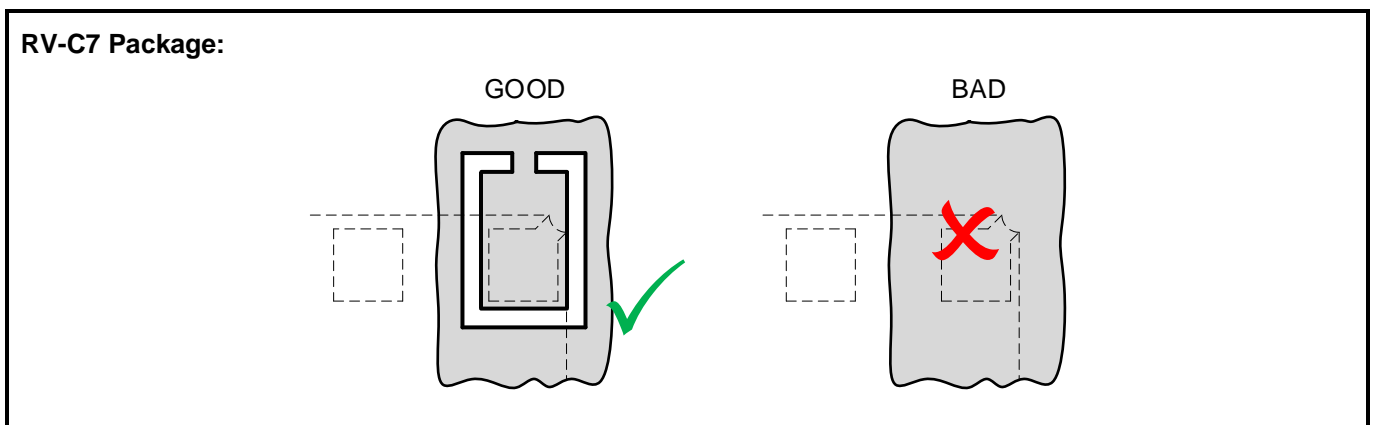
8.1. DIMENSIONS AND SOLDER PAD LAYOUT



All dimensions in mm typical.

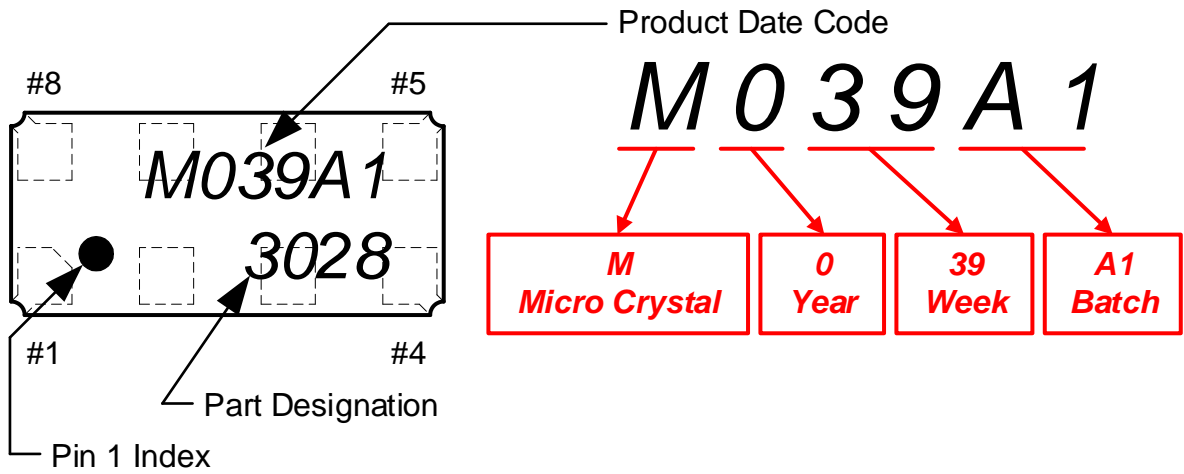
8.1.1. RECOMMENDED THERMAL RELIEF

When connecting a pad to a copper plane, thermal relief is recommended.



8.2. MARKING AND PIN #1 INDEX

Laser marking RV-3028-C7 Package: (top view)

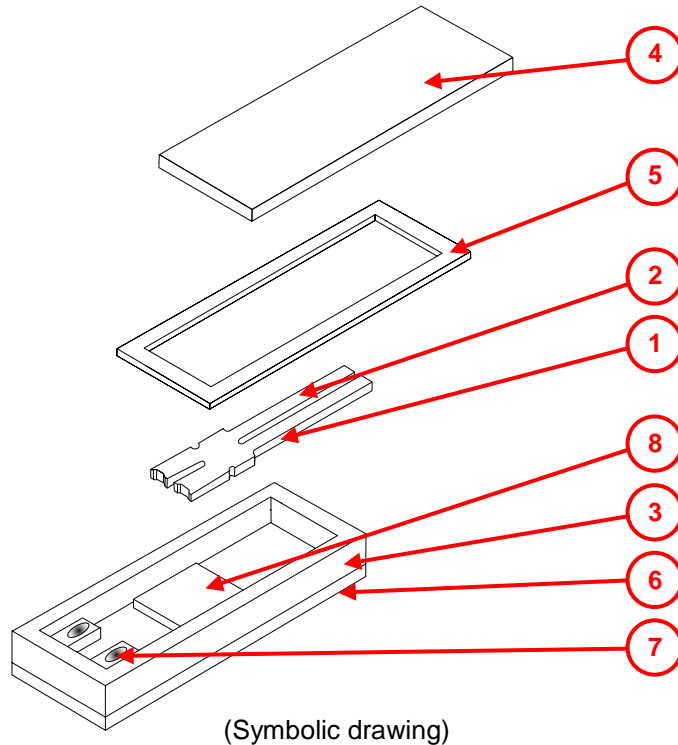


9. MATERIAL COMPOSITION DECLARATION & ENVIRONMENTAL INFORMATION

9.1. HOMOGENOUS MATERIAL COMPOSITION DECLARATION

Homogenous material information according to IPC-1752 standard

Material Composition RV-3028-C7:



| No. | Item Component Name | Sub Item Material Name | Material Weight | | Substance Element | CAS Number | Comment |
|-------------|---------------------|---------------------------------|-----------------|-------|-------------------------------------|---|-------------------------------------|
| | | | (mg) | (%) | | | |
| 1 | Resonator | Quartz Crystal | 0.13 | 100% | SiO ₂ | 14808-60-7 | |
| 2 | Electrodes | Cr+Au | 0.01 | 6% | Cr | Cr: 7440-47-3 | |
| | | | | 94% | Au | Au: 7440-57-5 | |
| 3 | Housing | Ceramic | 6.90 | 100% | Al ₂ O ₃ | 1344-28-1 | |
| 4 | Metal Lid | Kovar Lid | 2.67 | 95% | Fe53Ni29Co18 | Fe: 7439-89-6 Ni: 7440-02-0 Co: 7440-48-4 | Metal Lid (Kovar) |
| | | | | 4.95% | Ni | Ni: 7440-02-0 | Nickel plating |
| | | | | 0.05% | Au | Au: 7440-57-5 | Gold plating |
| 5 | Seal | Solder Preform | 0.54 | 80% | Au80 / Sn20 | Au: 7440-57-5 | |
| | | | | 20% | | Sn | Sn: 7440-31-5 |
| 6 | Terminations | Internal and external terminals | 0.38 | 80% | Mo | Mo: 7439-98-7 | Molybdenum |
| | | | | 15% | Ni | Ni: 7440-02-0 | Nickel plating |
| | | | | 5% | Au 0.5 micron | Au: 7440-57-5 | Gold plating |
| 7 | Conductive adhesive | Silver filled Silicone glue | 0.09 | 88% | Ag | Ag: 7440-22-4 | |
| | | | | 12% | Siloxanes and silicones | 68083-19-2 | di-Me, vinyl group-terminated |
| | | | | 0% | Distillates, petroleum hydrotreated | 64742-47-8 | Does not appear in finished product |
| 8 | CMOS IC | Silicon Gold bumps | 0.64 | 90% | Si | Si: 7440-21-3 | |
| | | | | 10% | Au | Au: 7440-57-5 | |
| Unit weight | | | 11.4 | | | | |

9.2. MATERIAL ANALYSIS & TEST RESULTS

Homogenous material information according to IPC-1752 standard

| No. | Item Component Name | Sub Item Material Name | RoHS | | | | | | Halogens | | | | Phthalates | | | |
|-----|---------------------|-----------------------------|------|----|----|--------|-----|------|----------|----|----|----|------------|-----|------|------|
| | | | Pb | Cd | Hg | Cr(VI) | PBB | PBDE | F | Cl | Br | - | BBP | DBP | DEHP | DIBP |
| 1 | Resonator | Quartz Crystal | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd |
| 2 | Electrodes | Cr+Au | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd |
| 3 | Housing | Ceramic | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd |
| 4 | Metal Lid | Kovar Lid & Plating | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd |
| 5 | Seal | Solder Preform | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd |
| 6 | Terminations | Int. & ext. terminals | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd |
| 7 | Conductive adhesive | Silver filled Silicone glue | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd |
| 8 | CMOS IC | Silicon & Gold bumps | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd | nd |
| | MDL [ppm] | Method Detection Limit | 2 | | | 8 | 5 | 50 | | | | 50 | | | | |

nd (not detected) = below "Method Detection Limit" (MDL)

Test methods:

RoHS

- Pb, Cd
- Hg
- Cr(VI)
- PBB / PBDE

Test method with reference to:

- IEC 62321-5:2013
- IEC 62321-4:2013 + AMD1:2017
- IEC 62321-7-2:2017
- IEC 62321-6:2015

MDL: 2 ppm

MDL: 2 ppm

MDL: 8 ppm

MDL: 5 ppm

Halogens

Test method with reference to BS EN 14582:2016

MDL: 50 ppm

Phthalates

Test method with reference to IEC 62321-8:2017

MDL: 50 ppm

9.3. RECYCLING MATERIAL INFORMATION

Recycling material information according to IPC-1752 standard.

Element weight is accumulated and referenced to the unit weight of 11.4 mg.

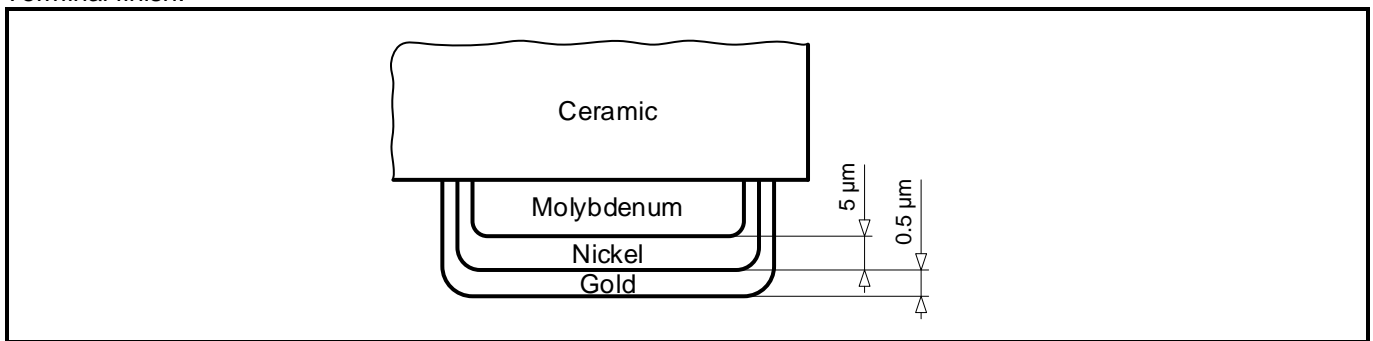
| Item Material Name | No. | Item Component Name | Material Weight | | Substance Element | CAS Number | Comment |
|-------------------------|-----------------------|--|-----------------|-------|--|---|--|
| | | | (mg) | (%) | | | |
| Quartz Crystal | 1 | Resonator | 0.13 | 1.14 | SiO ₂ | 14808-60-7 | |
| Chromium | 2 | Electrodes | 0.0006 | 0.005 | Cr | Cr: 7440-47-3 | |
| Ceramic | 3 | Housing | 6.90 | 60.74 | Al ₂ O ₃ | 1344-28-1 | |
| Gold | 2 4 5 6 8 | Electrodes Metal Lid Seal Terminations CMOS IC | 0.53 | 4.63 | Au | Au: 7440-57-5 | |
| Tin | 5 | Seal | 0.11 | 0.95 | Sn | Sn: 7440-31-5 | |
| Nickel | 4 6 | Metal Lid Terminations | 0.19 | 1.67 | Ni | Ni: 7440-02-0 | |
| Molybdenum | 6 | Terminations | 0.3 | 2.68 | Mo | Mo: 7439-98-7 | |
| Kovar | 4 | Metal Lid | 2.53 | 22.33 | Fe ₅₃ Ni ₂₉ Co ₁₈ | Fe: 7439-89-6 Ni: 7440-02-0 Co: 7440-48-4 | |
| Silver | 7a | Conductive adhesive | 0.079 | 0.7 | Ag | Ag: 7440-22-4 | |
| Siloxanes and silicones | 7b | Conductive adhesive | 0.011 | 0.10 | Siloxanes and silicones | 68083-19-2 | di-Me, vinyl group-terminated |
| Distillates | 7c | Conductive adhesive | 0 | 0 | Distillates | 64742-47-8 | hydrotreated petroleum, does not appear in finished products |
| Silicon | 8 | CMOS IC | 0.58 | 5.07 | Si | Si: 7440-21-3 | |
| Unit weight (total) | | | 11.4 | 100 | | | |

9.4. ENVIRONMENTAL PROPERTIES & ABSOLUTE MAXIMUM RATINGS

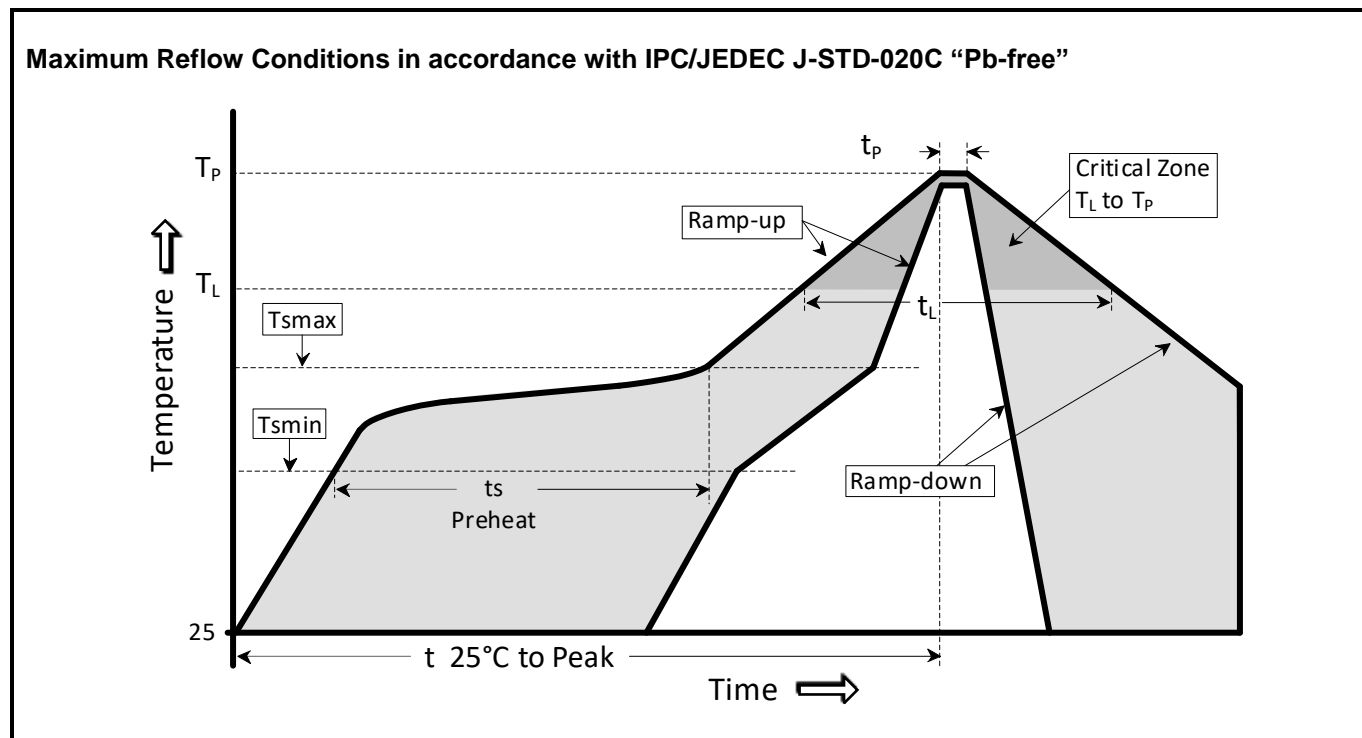
| Package | Description |
|-------------------------------|---|
| SON-8 (DFN-8) ceramic package | Small Outline Non-leaded (SON), hermetically sealed ceramic package with metal lid. |

| Parameter | Directive | Conditions | Value |
|----------------------------------|----------------------|-----------------------|----------------------|
| Product weight (total) | | | 11.4 mg |
| Storage temperature | | Store as bare product | -55 to +125°C |
| Moisture sensitivity level (MSL) | IPC/JEDEC J-STD-020D | | MSL1 |
| FIT / MTBF | | | available on request |

Terminal finish:



10. SOLDERING INFORMATION



| Temperature Profile | Symbol | Condition | Unit |
|-------------------------------------|-------------------------|------------------|--------|
| Average ramp-up rate | (T_{Smax} to T_P) | 3°C / second max | °C / s |
| Ramp down Rate | T_{cool} | 6°C / second max | °C / s |
| Time 25°C to Peak Temperature | $T_{to-peak}$ | 8 minutes max | min |
| Preheat | | | |
| Temperature min | T_{Smin} | 150 | °C |
| Temperature max | T_{Smax} | 200 | °C |
| Time T_{Smin} to T_{Smax} | t_s | 60 – 180 | sec |
| Soldering above liquidus | | | |
| Temperature liquidus | T_L | 217 | °C |
| Time above liquidus | t_L | 60 – 150 | sec |
| Peak temperature | | | |
| Peak Temperature | T_p | 260 | °C |
| Time within 5°C of peak temperature | t_p | 20 – 40 | sec |

11. HANDLING PRECAUTIONS FOR MODULES WITH EMBEDDED CRYSTALS

The built-in tuning-fork crystal consists of pure Silicon Dioxide in crystalline form. The cavity inside the package is evacuated and hermetically sealed in order for the crystal blank to function undisturbed from air molecules, humidity and other influences.

Shock and vibration:

Keep the crystal / module from being exposed to **excessive mechanical shock and vibration**. Micro Crystal guarantees that the crystal / module will bear a mechanical shock of 5000 g / 0.3 ms.

The following special situations may generate either shock or vibration:

Multiple PCB panels - Usually at the end of the pick & place process the single PCBs are cut out with a router. These machines sometimes generate vibrations on the PCB that have a fundamental or harmonic frequency close to 32.768 kHz. This might cause breakage of crystal blanks due to resonance. Router speed should be adjusted to avoid resonant vibration.

Ultrasonic cleaning - Avoid cleaning processes using ultrasonic energy. These processes can damage the crystals due to the mechanical resonance frequencies of the crystal blank.

Overheating, rework high temperature exposure:

Avoid overheating the package. The package is sealed with a seal ring consisting of 80% Gold and 20% Tin. The eutectic melting temperature of this alloy is at 280°C. Heating the seal ring up to >280°C will cause melting of the metal seal which then, due to the vacuum, is sucked into the cavity forming an air duct. This happens when using hot-air-gun set at temperatures >280°C.

Use the following methods for rework:

- Use a hot-air-gun set at 270°C.
- Use 2 temperature controlled soldering irons, set at 270°C, with special-tips to contact all solder-joints from both sides of the package at the same time, remove part with tweezers when pad solder is liquid.

13. COMPLIANCE INFORMATION

Micro Crystal confirms that the standard product Real-Time Clock Module RV-3028-C7 is compliant with “EU RoHS Directive” and “EU REACH Directives”.

Please find the actual Certificate of Conformance for Environmental Regulations on our website:

[CoC Environment RV-Series.pdf](#)

14. DOCUMENT REVISION HISTORY

| Date | Revision # | Revision Details |
|----------------|------------|---|
| August 2018 | 1.0 | First release |
| August 2019 | 1.1 | Corrected typos and added sections |
| March 2021 | 1.2 | Corrected and added specifications and drawings Added new disclaimer |
| September 2021 | 1.3 | Improved password description, 3.12., 3.15.3., 4.18. Removed note about I ² C interface re-initialization, 4.2. Added "to any RTC register", 4.5., 4.5.1. and 4.5.2. Corrected "V _{BAT} " to "V _{BACKUP} ", 4.6.8. Clarified text about I ² C read/write data integrity and I ² C re-initialization, 5.10. Removed EEOffset calibrated Δt/t MAX value (±2 ppm), 6.3. Removed older application circuit, 7.1. Added four new application circuits, 7.1., 7.2., 7.3. and 7.4. Adapted limit values and methods in accordance with the latest standards, 9.2. Corrected package designation to SON-8 (DFN-8), 9.4. Corrected text to "hot-air-gun set at temperatures >280°C.", 11. |
| November 2021 | 1.4 | Corrected location of designation "+ AMD1:2017", 9.2. |

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