Arria V GT FPGA Development Board

Reference Manual

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Additional Information

1. Overview

This document describes the hardware features of the Arria® V GT FPGA development board, including the detailed pin-out and component reference information required to create custom FPGA designs that interface with all components of the board.

General Description

The Arria V GT FPGA development board provides a hardware platform for developing and prototyping low-power, high-performance, and logic-intensive designs using Altera's Arria V GT FPGA device. The board provides a wide range of peripherals and memory interfaces to facilitate the development of Arria V GT FPGA designs.

Two high-speed mezzanine card (HSMC) connectors are available to add additional functionality via a variety of HSMCs available from Altera® and various partners.

To see a list of the latest HSMCs available or to download a copy of the HSMC specification, refer to the Development Board Daughtercards page of the Altera website.

Design advancements and innovations, such as the PCI Express hard IP implementation and programmable power technology ensure that designs implemented in the Arria V GT FPGAs operate faster, with lower power, and have a faster time to market than previous FPGA families.

For more information on the following topics, refer to the respective documents:

- Arria V device family, refer to the *Arria V Device Handbook*.
- PCI Express MegaCore function, refer to the *PCI Express Compiler User Guide*.
- HSMC Specification, refer to the *High Speed Mezzanine Card (HSMC) Specification*.

Board Component Blocks

The development board features the following major component blocks:

- Two Arria V GT FPGA 5AGTFD7K3F40I3N in the 1517-pin FineLine BGA (FBGA) package
  - 504K LEs
  - 190,240 adaptive logic modules (ALMs)
  - 24,140 Kbit (Kb) M10K on-die memory
  - 2,906 Kb MLAB memory
  - 36 transceivers
  - 16 phase locked loops (PLLs)
  - 2,312 18x18 multipliers
  - 1.15-V core voltage
- MAX® II CPLD EPM2210GF324 System Controller in the 324-pin FBGA package
- FPGA configuration circuitry
  - MAX II CPLD EPM570GM100 and flash fast passive parallel (FPP) configuration
  - On-board USB-Blaster™ II for use with the Quartus® II Programmer
- Clocking circuitry
  - Nine on-board oscillators
    - One 50-MHz oscillator
    - Two 125-MHz oscillators
    - Clock buffer with six outputs sourced by SMA or programmable oscillator with a default frequency of 100-MHz
    - One programmable oscillator with a default frequency of 148.5-MHz
    - Four programmable oscillators with four outputs each of various default frequencies
    - Clock buffer with two outputs sourced by one of the above four programmable oscillators with one output to the FPGA reference clock and Bull's Eye® SMA
  - SMA connectors for external LVPECL clock input
- Power supply
  - 14-V – 20-V DC input
  - PCI Express edge connector power
  - 12-V PCI Express ATX supply
  - On-board power measurement circuitry

- Mechanical
  - PCI Express long form factor (4.376″ x 10.45″)
  - PCI Express chassis or bench-top operation

Dual FPGA

The development board includes two Arria V GT FPGAs that connect to other components on the board to provide a better transceiver and bandwidth design solution.

FPGA 1

The first FPGA device (FPGA 1) connects to the following components:

- Communication ports
  - One PCI Express x8 edge connector
  - One universal HSMC expansion port (port A)
  - One USB 2.0 connector
  - One gigabit Ethernet port
  - Chip-to-Chip (C2C) bridge with 29 LVDS inputs and 29 LVDS outputs, and x8 transceivers
  - Two small form factor pluggable plus (SFP+) channels
  - One SMA 10 Gbps transceiver channel
  - Three Bull's Eye 10 Gbps transceiver channels
- Memory
  - 1152-Mbyte (MB) DDR3 SDRAM with a 72-bit data bus
  - 72-Mbit (Mb) QDRII+ SRAM
  - 1-Gbit (Gb) synchronous flash with a 16-bit data bus

- General user I/O
  - LEDs and displays
    - Eight dual color user LEDs
    - Two-line character LCD display
    - Three configuration select LEDs
    - One configuration done LED
    - Two HSMC interface transmit/receive (TX/RX) LEDs
    - Three PCI Express LEDs
    - Five Ethernet LEDs
  - Push buttons
    - One CPU reset push button
    - One Max II CPLD EPM2210 System Controller configuration reset push button
    - One load image push button (to program the FPGA from flash memory)
    - One image select push button (select an image to load from flash memory)
    - Three general user push buttons
  - Eight user control DIP switches

FPGA 2

The second FPGA device (FPGA 2) connects to the following components:

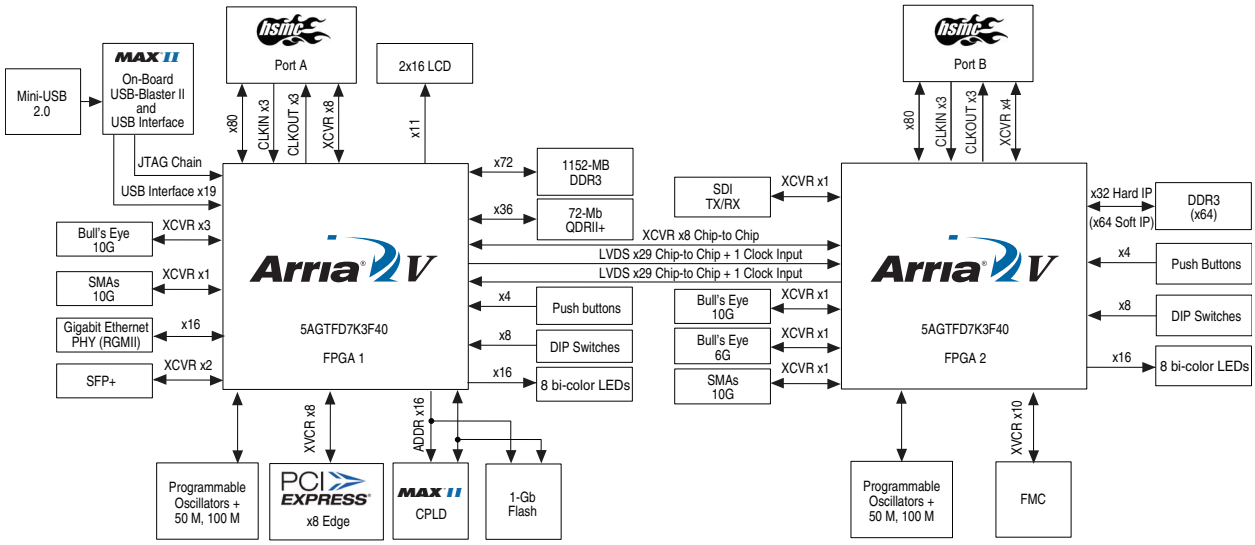
- Communication ports
  - One universal HSMC expansion port (port B)
  - One FMC port
  - C2C bridge with 29 LVDS inputs and 29 LVDS outputs, and x8 transceivers
  - One serial digital interface (SDI) channel
  - One SMA 10 Gbps transceiver channel
  - One Bull's Eye 6 Gbps transceiver channel
  - One Bull's Eye 10 Gbps transceiver channel
- Memory
  - 1024-MB DDR3 SDRAM with a 64-bit data bus (soft controller)
  - 512-MB DDR3 SDRAM with a 32-bit data bus (hard IP controller)

- General user I/O
  - LEDs and displays
    - Eight dual color user LEDs
    - Two HSMC interface transmit/receive (TX/RX) LEDs
  - Push buttons
    - One CPU reset push button
    - Three general user push buttons
  - Eight user control DIP switches

Development Board Block Diagram

Figure 1–1 shows a block diagram of the Arria V GT FPGA development board.

Figure 1–1. Arria V GT FPGA Development Board Block Diagram



Handling the Board

When handling the board, it is important to observe the following static discharge precaution:

CAUTION

Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

2. Board Components

Introduction

This chapter introduces the major components on the Arria V GT FPGA development board. Figure 2–1 illustrates the component locations and Table 2–1 provides a brief description of all component features of the board.

A complete set of schematics, a physical layout database, and GERBER files for the development board reside in the Arria V GT FPGA development kit documents directory.

For information about powering up the board and installing the demonstration software, refer to the *Arria V GT FPGA Development Kit User Guide*.

This chapter consists of the following sections:

Board Overview

This section provides an overview of the Arria V GT FPGA development board, including an annotated board image and component descriptions. Figure 2–1 shows an overview of the available components.

Figure 2–1. Overview of the Arria V GT FPGA Development Board Features

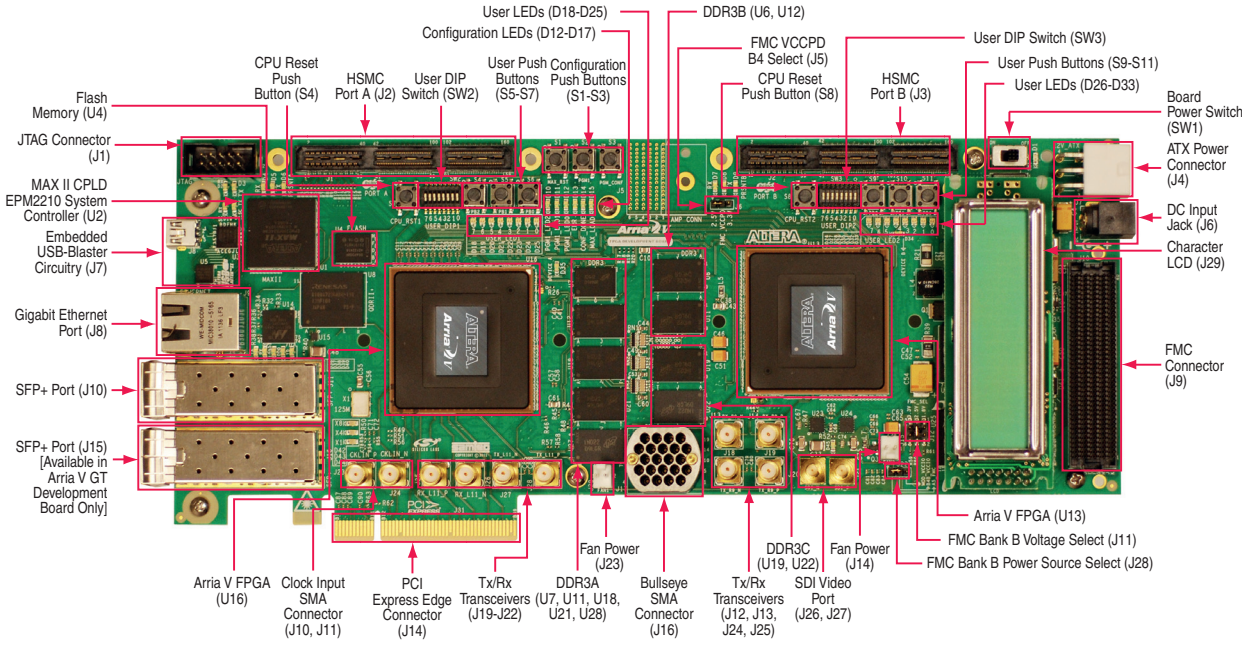


Table 2–1 describes the components and lists their corresponding board references.

Table 2–1. Arria V GT FPGA Development Board Components (Part 1 of 4)

Board Reference	Type	Description
Featured Devices		
U13, U16	FPGA	Two Arria V GT FPGA, 5AGTFD7K3F40I3N, 1517-pin FBGA.
U2	CPLD	MAX II CPLD, EPM2210GF324, 324-pin μBGA.
Configuration, Status, and Setup Elements		
J1	JTAG connector	Disables the on-board USB-Blaster II (for use with external USB-Blasters).
J7	On-Board USB-Blaster II	Mini-USB 2.0 connector for programming and debugging the FPGA.
SW5	Board settings DIP switch	Controls the MAX II CPLD EPM2210 System Controller functions such as clock enable, SMA clock input control, and which image to load from flash memory at power-up. This switch is located on the bottom of the board.
SW6	JTAG chain DIP switch	Enables and disables devices in the JTAG chain. This switch is located on the bottom of the board.

Table 2–1. Arria V GT FPGA Development Board Components (Part 2 of 4)

Board Reference	Type	Description
SW7	PCI Express DIP switch	Controls the PCI Express lane width by connecting prsnt pins together on the PCI Express edge connector. This switch is located on the bottom of the board.
SW8	FPGA 1 mode select DIP switch	Sets the Arria V MSEL[4,2,1] pins. This switch is located on the bottom of the board.
SW4	FPGA 2 mode select DIP switch	Sets the Arria V MSEL[4,2,1] pins. This switch is located on the bottom of the board.
S2	Image select push button	Toggles the configuration LEDs which selects the program image that loads from flash memory to the FPGA.
S3	Program configuration push button	Configures the FPGA from flash memory image based on the program LEDs.
D1	Power LED	Illuminates when 5.0-V power is present.
D2, D3	JTAG Tx/Rx LEDs	Indicate the transmit or receive activity of the JTAG chain. The Tx and Rx LEDs blink when the link is in use and active. The LEDs are off when not in use and on when in use or idle.
D4, D5	HSMC port A LEDs	You can configure these LEDs to indicate transmit or receive activity.
D6	HSMC port A present LED	Illuminates when a daughtercard is plugged into the HSMC port A.
D7, D8	HSMC port B LEDs	You can configure these LEDs to indicate transmit or receive activity.
D9	HSMC port B present LED	Illuminates when a daughtercard is plugged into the HSMC port B.
D10, D11	System Console Tx/Rx LEDs	Indicate the transmit or receive activity of the System Console USB interface. The Tx and Rx LEDs blink when the link is in use and active. The LEDs are off when not in use and on when in use or idle.
D12, D13, D14	Configuration LEDs	Illuminates to show the LED sequence that determines which flash memory image loads to the FPGA when you press the PGM1_SEL push button.
D15	Error LED	Illuminates when the FPGA configuration from flash memory fails.
D16	Configuration done LED	Illuminates when the FPGA is configured.
D17	Load LED	Illuminates when the MAX II CPLD EPM2210 System Controller is actively configuring the FPGA.
D36, D37, D38, D39, D40	Ethernet LEDs	Shows the connection speed as well as transmit or receive activity.
D42, D43, D44	PCI Express link LEDs	You can configure these LEDs to display the PCI Express link width (x1, x4, x8).
Clock Circuitry		
U48	Si5338 programmable oscillator	Programmable oscillator with default frequencies of CLK0=125 MHz, CLK1=100 MHz, CLK2=625 MHz, CLK3=125 MHz at I^2C address 71 HEX. The frequency is programmable using the clock GUI with the default MAX II CPLD EPM2210 System Controller design programmed into the MAX II EPM2210.
U53	Si5338 programmable oscillator	Programmable oscillator with default frequencies of CLK0=625 MHz, CLK1=156.25 MHz, CLK2=125 MHz, CLK3=125 MHz at I^2C address 70 HEX. The frequency is programmable using the clock GUI with the default MAX II CPLD EPM2210 System Controller design programmed into the MAX II EPM2210.

Table 2–1. Arria V GT FPGA Development Board Components (Part 3 of 4)

Board Reference	Type	Description
U52	Si5338 programmable oscillator	Programmable oscillator with default frequencies of CLK0=125 MHz, CLK1=100 MHz, CLK2=156.25 MHz, CLK3=125 MHz at I^2C address 73 HEX. The frequency is programmable using the clock GUI with the default MAX II CPLD EPM2210 System Controller design programmed into the MAX II EPM2210.
U34	Si5338 programmable oscillator	Programmable oscillator with default frequencies of CLK0=625 MHz, CLK1=100 MHz, CLK2=625 MHz, CLK3=125 MHz at I^2C address 72 HEX. The frequency is programmable using the clock GUI with the default MAX II CPLD EPM2210 System Controller design programmed into the MAX II EPM2210.
X1	125 MHz oscillator	125.000 MHz crystal oscillator for general purpose logic to FPGA 1.
X4	125 MHz oscillator	125.000 MHz crystal oscillator for general purpose logic to FPGA 2.
X2	Si571 programmable Oscillator (148.5 MHz default)	Programmable oscillator for SDI or REFCLK0RP/N with default frequencies at I^2C address 55 HEX. The frequency is programmable using the clock GUI with the default MAX II EPM2210 System Controller design programmed into the MAX II EPM2210.
X7, or J17 and J18 to U56 buffer	Programmable oscillator (100 MHz default)	Programmable oscillator with a default frequency of 100.00 MHz. The frequency is programmable using the clock GUI with the default MAX II CPLD EPM2210 System Controller design programmed into the MAX II EPM2210. Multiplex with `CLKIN_SMA_P/N` based on `CLK_SEL` switch value.
X6 to U51 1:3 zero delay clock buffer	50 MHz oscillator	50.000 MHz crystal oscillator for general purpose logic. Three outputs connect to the FPGA 1, FPGA 2, and MAX II devices.
J17, J18	Clock input SMAs	Drive LVPECL-compatible clock inputs into the clock multiplexer buffer (U56).
General User Input/Output		
SW2	FPGA 1 user DIP switch	Octal user DIP switches. When the switch is ON, a logic 0 is selected.
SW3	FPGA 2 user DIP switch	Octal user DIP switches. When the switch is ON, a logic 0 is selected.
S1	MAX II reset push button	Resets the MAX II CPLD EPM2210 System Controller.
S4	FPGA 1 CPU reset push button	Resets the FPGA 1 logic.
S8	FPGA 2 CPU reset push button	Resets the FPGA 2 logic.
S5–S7	FPGA 1 general user push buttons	Three user push buttons. Driven low when pressed.
S9–S11	FPGA 2 general user push buttons	Three user push buttons. Driven low when pressed.
D18–D25	FPGA 1 user LEDs	Eight bi-color user LEDs. Illuminates when driven low.
D26–D33	FPGA 2 user LEDs	Eight bi-color user LEDs. Illuminates when driven low.
D35	FPGA 1 LED	LED indicator for FPGA 1.
D32	FPGA 2 LED	LED indicator for FPGA 2.
Memory Devices		
U4	Flash x16 memory	Synchronous burst mode flash device that provides a 16-bit 125-MB non-volatile memory port.

Table 2–1. Arria V GT FPGA Development Board Components (Part 4 of 4)

Board Reference	Type	Description
U8	QDRII+ memory	9-MB QDRII+ SRAM with a 36-bit data bus. The device has a separate 36-bit read and 36-bit write port with DDR signalling at up to 400 MHz.
U7, U11, U18, U21, U28	DDR3A memory	DDR3 SDRAM interface on FPGA 1. This 1152-MB DDR3 x72-bit data bus consists of four x16 devices and one x8 device with a single address or command bus.
U6, U12, U19, U22	DDR3B/C memory	DDR3 SDRAM interface on FPGA 2. There are two interface options: ■ Option 1: 512-MB interface with a 32-bit data bus. This DDR3 x32-bit data bus consists of two x16 devices with a single shared address. ■ Option 2: 1024-MB interface with a 64-bit data bus. This DDR3 x64-bit data bus consists of four x16 devices with a single shared address.
Communication Ports		
J30	PCI Express edge connector	Gold-plated edge fingers connector for up to ×8 signaling in Gen1 and x4 Gen2 modes.
J2	HSMC port A	Provides four transceiver channels and 80 CMOS or 17 LVDS channels per the HSMC specification.
J3	HSMC port B	Provides four transceiver channels and 80 CMOS or 17 LVDS channels per the HSMC specification.
J7	Mini-USB type-AB connector	USB interface for programming the FPGA through on-board USB-Blaster II JTAG via a type-AB Mini-USB cable.
J8	Gigabit Ethernet	RJ-45 connector which provides a 10/100/1000 Ethernet connection via a Marvell 88E1111 PHY and the FPGA-based Altera Triple Speed Ethernet MegaCore function in RGMII mode.
Display Ports		
J29	Character LCD connector	Connector which interfaces to the provided 16 character × 2 line LCD module along with two standoffs at MTH7 and MTH8.
Power Supply		
J6	DC input jack	Accepts a 19-V DC power supply. Do not use this input jack while the board is plugged into a PCI Express slot.
J4	ATX power connector	PCI Express auxiliary power source option.
J30	PCI Express edge connector	Interfaces to a PCI Express root port such as an appropriate PC motherboard.
SW1	Power switch	Switch to power on or off the board when power is supplied from the DC input jack.

Featured Device: Arria V GT FPGA

The Arria V GT FPGA development board features two Arria V GT FPGA 5AGTFD7K3F40I3N device (U13 and U16) in a 1517-pin FBGA package.

For more information about Arria V device family, refer to the *Arria V Device Handbook*.

Table 2–2 describes the features of the Arria V GT FPGA 5AGTFD7K3F40I3N device.

Table 2–2. Arria V GT FPGA Features

ALMs	Equivalent LEs	M10K RAM Blocks	Total RAM Kbits	18-bit × 18-bit Multipliers	PLLs	Transceivers	Package Type
190,240	504,000	24,140	27,046	2,312	16	36	1517-pin FBGA

I/O Resources

Figure 2–2 illustrates the bank organization and I/O count for the Arria V GT FPGA 5AGTFD7K3F40I3N device in the 1517-pin FBGA package.

Figure 2–2. Arria V GT FPGA Device I/O Bank Diagrams

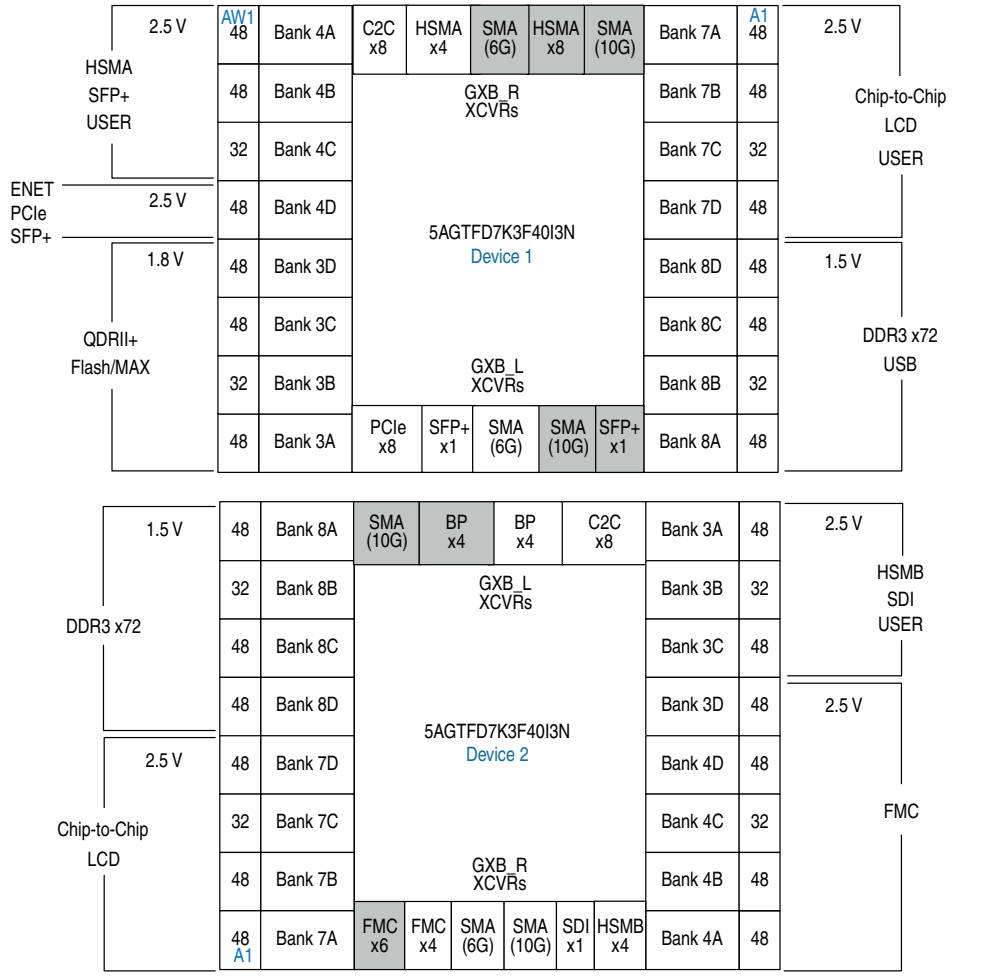


Table 2–3 lists the Arria V GT FPGA 1 pin count and usage by function on the development board. Clocks are listed under special pins as it uses dedicated I/O pins.

Table 2–3. Arria V GT FPGA 1 Pin Count and Usage

Function	I/O Standard	I/O Count	Special Pins
DDR3 ×72 interface	1.5-V SSTL	125	1 differential ×9 differential DQS
QDRII+ ×36 interface	1.8-V HSTL	103	1 differential ×36 differential DQS
MAX II System Controller	1.8-V CMOS	8	—
Flash	1.8-V CMOS	49	—
PCI Express	2.5-V CMOS	10	1 reference clock
HSMC port A	2.5-V CMOS + LVDS	84	1 reference clock
Gigabit Ethernet	2.5-V CMOS + LVDS	16	—
On-Board USB-Blaster II	1.5-V/2.5-V CMOS	19	—
SFP+	2.5-V CMOS	16	2 reference clocks
Chip-to-chip bridge	2.5-V	120	2 reference clocks
Buttons	2.5-V CMOS	3	—
Switches	2.5-V CMOS	4	—
LCD	2.5-V CMOS	11	—
LEDs	2.5-V CMOS	16	—
Clocks or Oscillators	1.8-V CMOS + LVDS	10	5 differential clocks, 1 single-ended
Total I/O Used:		625	
Transceivers			
SMA or Bull's Eye	—	16	—
HSMC port A	—	32	—
PCI Express	—	32	—
Chip-to-chip bridge	—	32	—
SFP+	—	8	—
Total Transceiver Used:		120	

Table 2–4 lists the Arria V GT FPGA 2 pin count and usage by function on the development board. Clocks are listed under special pins as it uses dedicated I/O pins.

Table 2–4. Arria V GT FPGA 2 Pin Count and Usage (Part 1 of 2)

Function	I/O Standard	I/O Count	Special Pins
DDR3 ×64 device	1.5-V SSTL	156	1 differential ×9 differential DQS
HSMC port B	2.5-V CMOS + LVDS	84	1 reference clock
FMC	2.5-V	178	1 reference clock
SDI	2.5-V CMOS	8	1 reference clock
Chip-to-chip bridge	2.5-V	120	1 reference clock
Buttons	2.5-V CMOS	4	—
Switches	2.5-V CMOS	8	—
LEDs	2.5-V CMOS	16	—

Table 2–4. Arria V GT FPGA 2 Pin Count and Usage (Part 2 of 2)

Function	I/O Standard	I/O Count	Special Pins
Clocks or Oscillators	1.8-V CMOS + LVDS	10	5 differential clocks, 1 single-ended
Total I/O Used:		584	
Transceivers			
SMAs or Bull's Eye	—	12	—
HSMC port B	—	16	—
FMC	—	40	—
Chip-to-chip bridge	—	32	—
Total Transceivers:		116	

MAX II CPLD EPM2210 System Controller

The board utilizes the EPM2210 System Controller, an Altera MAX II CPLD, for the following purposes:

- FPGA configuration from flash
- Power consumption monitoring
- Virtual JTAG interface for PC-based GUI
- Control registers for clocks
- Control registers for remote system update

Figure 2–3 illustrates the MAX II CPLD EPM2210 System Controller's functionality and external circuit connections as a block diagram.

Figure 2–3. MAX II CPLD EPM2210 System Controller Block Diagram

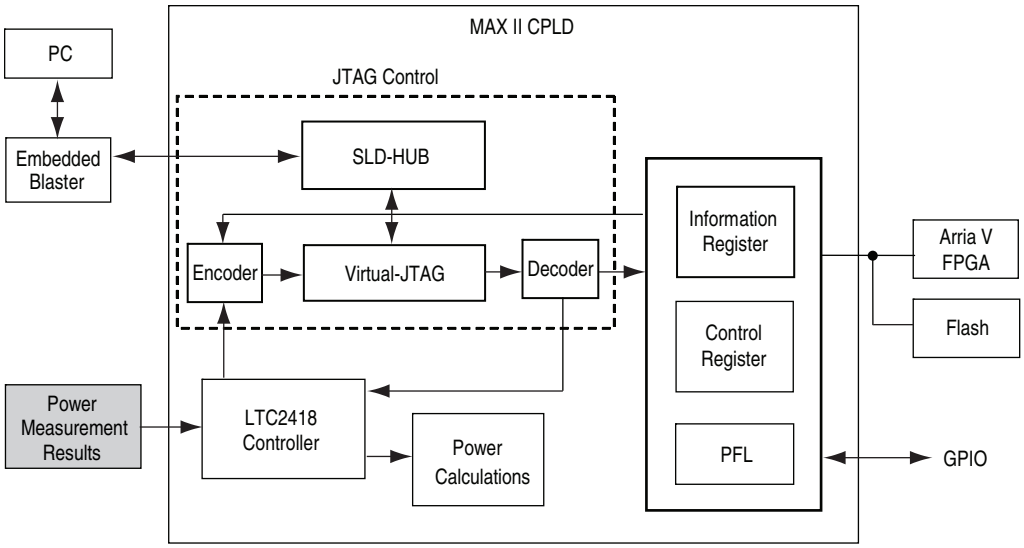


Table 2–5 lists the I/O signals present on the MAX II CPLD EPM2210 System Controller. The signal names and functions are relative to the MAX II device (U2).

Table 2–5. MAX II CPLD EPM2210 System Controller Device Pin-Out (Part 1 of 5)

Schematic Signal Name	MAX II CPLD Pin Number	I/O Standard	Description
CLK125A_EN	B13	2.5-V	125 MHz oscillator enable
CLK125B_EN	D7	2.5-V	125 MHz oscillator enable
CLK50_EN	D11	2.5-V	50 MHz oscillator enable
CLK_CONFIG	K6	2.5-V	100 MHz configuration clock input
CLK_ENABLE	B5	2.5-V	DIP switch for clock oscillator enable
CLK_SEL	E7	2.5-V	DIP switch for clock select—SMA or oscillator
CLKIN_MAX_50	K13	2.5-V	50 MHz clock input
CLOCK_SCL	C14	2.5-V	Programmable oscillator I^2C clock
CLOCK_SDA	L4	2.5-V	Programmable oscillator I^2C data
CPU1_RESETN	B8	2.5-V	FPGA 1 reset push button
CPU2_RESETN	E6	2.5-V	FPGA 2 reset push button
DEVICE1_LED	D13	2.5-V	FPGA 1 configuration done LED
DEVICE2_LED	C15	2.5-V	FPGA 2 configuration done LED
EXTRA_SIG0	B10	2.5-V	Reserved for future use.
EXTRA_SIG1	F16	1.8-V	Reserved for future use.
EXTRA_SIG2	J16	1.8-V	Reserved for future use.
FACTORY_USER1	A5	2.5-V	Load factory or user design at power-up
FACTORY_USER2	C4	2.5-V	Load factory or user design at power-up
FACTORY_REQUEST	B9	2.5-V	On-Board USB-Blaster II request to send FACTORY command
FACTORY_STATUS	F10	2.5-V	On-Board USB-Blaster II FACTORY command status
FLASH_ACCESSN	B12	1.8-V	FM bus flash memory access indication
FLASH_ADVN	G15	1.8-V	FM bus flash memory address valid
FLASH_CEN	E16	1.8-V	FM bus flash memory chip enable
FLASH_CLK	E17	1.8-V	FM bus flash memory clock
FLASH_OEN	F14	1.8-V	FM bus flash memory output enable
FLASH_RDYBSYN	D18	1.8-V	FM bus flash memory ready
FLASH_RESETN	F13	1.8-V	FM bus flash memory reset
FLASH_WEN	D17	1.8-V	FM bus flash memory write enable
FM_A0	T17	1.8-V	FM bus address
FM_A1	R15	1.8-V	FM bus address
FM_A2	T16	1.8-V	FM bus address
FM_A3	F15	1.8-V	FM bus address
FM_A4	R16	1.8-V	FM bus address
FM_A5	P15	1.8-V	FM bus address
FM_A6	R17	1.8-V	FM bus address
FM_A7	P14	1.8-V	FM bus address

Table 2–5. MAX II CPLD EPM2210 System Controller Device Pin-Out (Part 2 of 5)

Schematic Signal Name	MAX II CPLD Pin Number	I/O Standard	Description
FM_A8	R18	1.8-V	FM bus address
FM_A9	N15	1.8-V	FM bus address
FM_A10	P16	1.8-V	FM bus address
FM_A11	N14	1.8-V	FM bus address
FM_A12	P18	1.8-V	FM bus address
FM_A13	M15	1.8-V	FM bus address
FM_A14	N16	1.8-V	FM bus address
FM_A15	P17	1.8-V	FM bus address
FM_A16	N13	1.8-V	FM bus address
FM_A17	M14	1.8-V	FM bus address
FM_A18	N17	1.8-V	FM bus address
FM_A19	M13	1.8-V	FM bus address
FM_A20	N18	1.8-V	FM bus address
FM_A21	M12	1.8-V	FM bus address
FM_A22	M16	1.8-V	FM bus address
FM_A23	K14	1.8-V	FM bus address
FM_A24	K18	1.8-V	FM bus address
FM_A25	K15	1.8-V	FM bus address
FM_A26	H17	1.8-V	FM bus address
FM_D0	L16	1.8-V	FM data bus
FM_D1	M18	1.8-V	FM data bus
FM_D2	L14	1.8-V	FM data bus
FM_D3	L17	1.8-V	FM data bus
FM_D4	L13	1.8-V	FM data bus
FM_D5	L18	1.8-V	FM data bus
FM_D6	M17	1.8-V	FM data bus
FM_D7	L15	1.8-V	FM data bus
FM_D8	K16	1.8-V	FM data bus
FM_D9	K17	1.8-V	FM data bus
FM_D10	D15	1.8-V	FM data bus
FM_D11	C17	1.8-V	FM data bus
FM_D12	E15	1.8-V	FM data bus
FM_D13	C16	1.8-V	FM data bus
FM_D14	D16	1.8-V	FM data bus
FM_D15	E14	1.8-V	FM data bus
FMC_C2M_PG	P6	2.5-V	FMC card to module power good
FMC_M2C_PG	T4	2.5-V	FMC module to card power good
FMC_PRSNT	U3	2.5-V	FMC module present
FMC_SCL	R5	2.5-V	FMC module clock

Table 2–5. MAX II CPLD EPM2210 System Controller Device Pin-Out (Part 3 of 5)

Schematic Signal Name	MAX II CPLD Pin Number	I/O Standard	Description
FMC_SDA	V2	2.5-V	FMC module data
FPGA1_CEN	L1	2.5-V	FPGA 1 chip enable
FPGA1_CEON	F11	2.5-V	FPGA 1 chip output enable
FPGA1_CONF_DONE	M4	2.5-V	FPGA 1 configuration done
FPGA1_CONFIG_D0	D1	2.5-V	FPGA configuration data
FPGA1_CONFIG_D1	D3	2.5-V	FPGA configuration data
FPGA1_CONFIG_D2	E2	2.5-V	FPGA configuration data
FPGA1_CONFIG_D3	D4	2.5-V	FPGA configuration data
FPGA1_CONFIG_D4	E1	2.5-V	FPGA configuration data
FPGA1_CONFIG_D5	E3	2.5-V	FPGA configuration data
FPGA1_CONFIG_D6	F3	2.5-V	FPGA configuration data
FPGA1_CONFIG_D7	E4	2.5-V	FPGA configuration data
FPGA1_CONFIG_D8	F2	2.5-V	FPGA configuration data
FPGA1_CONFIG_D9	E5	2.5-V	FPGA configuration data
FPGA1_CONFIG_D10	F1	2.5-V	FPGA configuration data
FPGA1_CONFIG_D11	F4	2.5-V	FPGA configuration data
FPGA1_CONFIG_D12	G3	2.5-V	FPGA configuration data
FPGA1_CONFIG_D13	F5	2.5-V	FPGA configuration data
FPGA1_CONFIG_D14	G2	2.5-V	FPGA configuration data
FPGA1_CONFIG_D15	F6	2.5-V	FPGA configuration data
FPGA1_CVP_CONFDONE	M1	2.5-V	FPGA 1 configuration via protocol done
FPGA1_MSEL0	F8	2.5-V	FPGA 1 mode select 0
FPGA1_MSEL1	A6	2.5-V	FPGA 1 mode select 1
FPGA1_MSEL2	E8	2.5-V	FPGA 1 mode select 2
FPGA1_MSEL3	B7	2.5-V	FPGA 1 mode select 3
FPGA1_MSEL4	D8	2.5-V	FPGA 1 mode select 4
FPGA1_NCONFIG	M5	2.5-V	FPGA 1 configuration active
FPGA1_NSTATUS	N1	2.5-V	FPGA 1 configuration ready
FPGA1_PR_DONE	K4	2.5-V	FPGA 1 partial reconfiguration done
FPGA1_PR_ERROR	L5	2.5-V	FPGA 1 partial reconfiguration error
FPGA1_PR_READY	L6	2.5-V	FPGA 1 partial reconfiguration ready
FPGA1_PR_REQUEST	L2	2.5-V	FPGA 1 partial reconfiguration request
FPGA2_CEN	K5	2.5-V	FPGA 2 chip enable
FPGA2_CEON	C11	2.5-V	FPGA 2 chip output enable
FPGA2_CONF_DONE	M3	2.5-V	FPGA 2 configuration done
FPGA2_CVP_CONFDONE	B18	2.5-V	FPGA 2 configuration via protocol done
FPGA2_MSEL0	U5	2.5-V	FPGA 2 mode select 0
FPGA2_MSEL1	R7	2.5-V	FPGA 2 mode select 1
FPGA2_MSEL2	V5	2.5-V	FPGA 2 mode select 2

Table 2–5. MAX II CPLD EPM2210 System Controller Device Pin-Out (Part 4 of 5)

Schematic Signal Name	MAX II CPLD Pin Number	I/O Standard	Description
FPGA2_MSEL3	T7	2.5-V	FPGA 2 mode select 3
FPGA2_MSEL4	U6	2.5-V	FPGA 2 mode select 4
FPGA2_NCONFIG	M2	2.5-V	FPGA 2 configuration active
FPGA2_NSTATUS	M6	2.5-V	FPGA 2 configuration ready
FPGA2_PR_DONE	B16	2.5-V	FPGA 2 partial reconfiguration done
FPGA2_PR_ERROR	D14	2.5-V	FPGA 2 partial reconfiguration error
FPGA2_PR_READY	A17	2.5-V	FPGA 2 partial reconfiguration ready
FPGA2_PR_REQUEST	E13	2.5-V	FPGA 2 partial reconfiguration request
FPGA_DCLK	N2	2.5-V	FPGA configuration clock
HSMA_PRSNTN	A14	2.5-V	HSMC port A present
HSMB_PRSNTN	E11	2.5-V	HSMC port B present
INIT_DONE1	T6	2.5-V	FPGA initialization done
INIT_DONE2	V4	2.5-V	FPGA initialization done
JTAG_EPM2210_TDI	M7	2.5-V	MAX II CPLD on-board JTAG chain data in
JTAG_BLASTER_TDI	N6	2.5-V	MAX II CPLD on-board JTAG chain data out
JTAG_TCK	R4	2.5-V	JTAG chain clock
JTAG_TMS	P5	2.5-V	JTAG mode select
M570_CLOCK	A10	1.8-V	25-MHz clock to the on-board USB-Blaster II for sending FACTORY command
M570_PCIE_JTAG_EN	D9	1.8-V	Low signal to disable the on-board USB-Blaster II when the PCI Express acts as a master to the JTAG chain.
MAX_BEN0	B11	2.5-V	FM bus MAX II byte enable 0
MAX_BEN1	C10	2.5-V	FM bus MAX II byte enable 1
MAX_BEN2	A11	2.5-V	FM bus MAX II byte enable 2
MAX_BEN3	C9	2.5-V	FM bus MAX II byte enable 3
MAX_CLK	J18	1.8-V	FM bus MAX II clock
MAX_CSN	J17	1.8-V	FM bus MAX II chip select
MAX_OEN	J15	1.8-V	FM bus MAX II output enable
MAX_WEN	J14	1.8-V	FM bus MAX II write enable
MAX_CONF_DONE1	B3	2.5-V	FPGA configuration done LED
MAX_CTL0	E10	2.5-V	FPGA 1 to MAX II option
MAX_CTL1	A12	2.5-V	FPGA 1 to MAX II option
MAX_CTL2	D10	2.5-V	FPGA 1 to MAX II option
MAX_ERROR1	C7	2.5-V	FPGA 1 configuration error LED
MAX_LOAD1	B6	2.5-V	FPGA 1 configuration active LED
MAX_RESETN	E18	1.8-V	MAX II reset push button
OVERTEMP1	B14	2.5-V	FPGA 1 fan RPM control
OVERTEMP2	C12	2.5-V	FPGA 2 fan RPM control
PGM1_CONFIG	B4	2.5-V	Load the flash memory image identified by the PGM LEDs

Table 2–5. MAX II CPLD EPM2210 System Controller Device Pin-Out (Part 5 of 5)

Schematic Signal Name	MAX II CPLD Pin Number	I/O Standard	Description
PGM1_LED0	A4	2.5-V	Flash memory PGM select indicator 0
PGM1_LED1	F7	2.5-V	Flash memory PGM select indicator 1
PGM1_LED2	C5	2.5-V	Flash memory PGM select indicator 2
PGM1_SEL	D6	2.5-V	Toggles the PGM_LED[0:2] LED sequence
PHASE0	P8	2.5-V	LTM4601 phase control
SDI_A_RX_BYPASS	A8	2.5-V	SDI equalization bypass
SDI_A_RX_EN	E9	2.5-V	SDI receive enable
SDI_A_TX_EN	F9	2.5-V	SDI transmit enable
SENSE_CS0N	F12	2.5-V	Power monitor chip select
SENSE_CS1N	B15	2.5-V	Power monitor chip select
SENSE_SCK	E12	2.5-V	Power monitor SPI clock
SENSE_SDI	A15	2.5-V	Power monitor SPI data in
SENSE_SDO	D12	2.5-V	Power monitor SPI data out
SI570_EN	A13	2.5-V	Si570 programmable oscillator enable
SI571_EN	C13	2.5-V	Si571 programmable VCXO enable
USB_CFG0	H14	1.8-V	On-board USB-Blaster II data
USB_CFG1	H13	1.8-V	On-board USB-Blaster II data
USB_CFG2	G13	1.8-V	On-board USB-Blaster II data
USB_CFG3	F17	1.8-V	On-board USB-Blaster II data
USB_CFG4	G12	1.8-V	On-board USB-Blaster II data
USB_CFG5	F18	1.8-V	On-board USB-Blaster II data
USB_CFG6	H16	1.8-V	On-board USB-Blaster II data
USB_CFG7	G16	1.8-V	On-board USB-Blaster II data
USB_CFG8	H15	1.8-V	On-board USB-Blaster II data
USB_CFG9	G17	1.8-V	On-board USB-Blaster II data
USB_CFG10	G14	1.8-V	On-board USB-Blaster II data
USB_CFG11	G18	1.8-V	On-board USB-Blaster II data
USB_CLK	J6	2.5-V	On-board USB-Blaster II clock
VCCINT_SCL	R3	2.5-V	LTC3880 serial clock
VCCINT_SDA	R2	2.5-V	LTC3880 serial data

Configuration, Status, and Setup Elements

This section describes the board's configuration, status, and setup elements.

Configuration

This section describes the FPGA, flash memory, and MAX II CPLD EPM2210 System Controller device programming methods supported by the Arria V GT FPGA development board.

The Arria V GT FPGA development board supports the following three configuration methods:

- On-board USB-Blaster II is the default method for configuring the FPGA at any time using the Quartus II Programmer in JTAG mode with the supplied USB cable.
- External USB-Blaster for configuring the FPGA using an external USB-Blaster that connects to the JTAG programming header (J1).
- Flash memory download for configuring the FPGA using stored images from the flash memory on either power-up or pressing the program configuration push button, `PGM1_CONFIG` (S3).

FPGA Programming over On-Board USB-Blaster II

This configuration method implements a USB Type-AB connector (J7), a FTDI USB 2.0 PHY device (U5), and an Altera MAX II CPLD (U2) to allow the FPGA configuration using a USB cable that connects directly between the USB port on the board and a USB port of a PC running the Quartus II software.

The on-board USB-Blaster II in the MAX II CPLD EPM570GM100 normally masters the JTAG chain. To prevent contention between the JTAG masters, the on-board USB-Blaster II is automatically disabled when you connect an external USB-Blaster to the JTAG chain through the JTAG connector.

If the USB-Blaster II is detected but no hardware is found in the chain, try reducing the clock frequency of the JTAG chain using these commands:

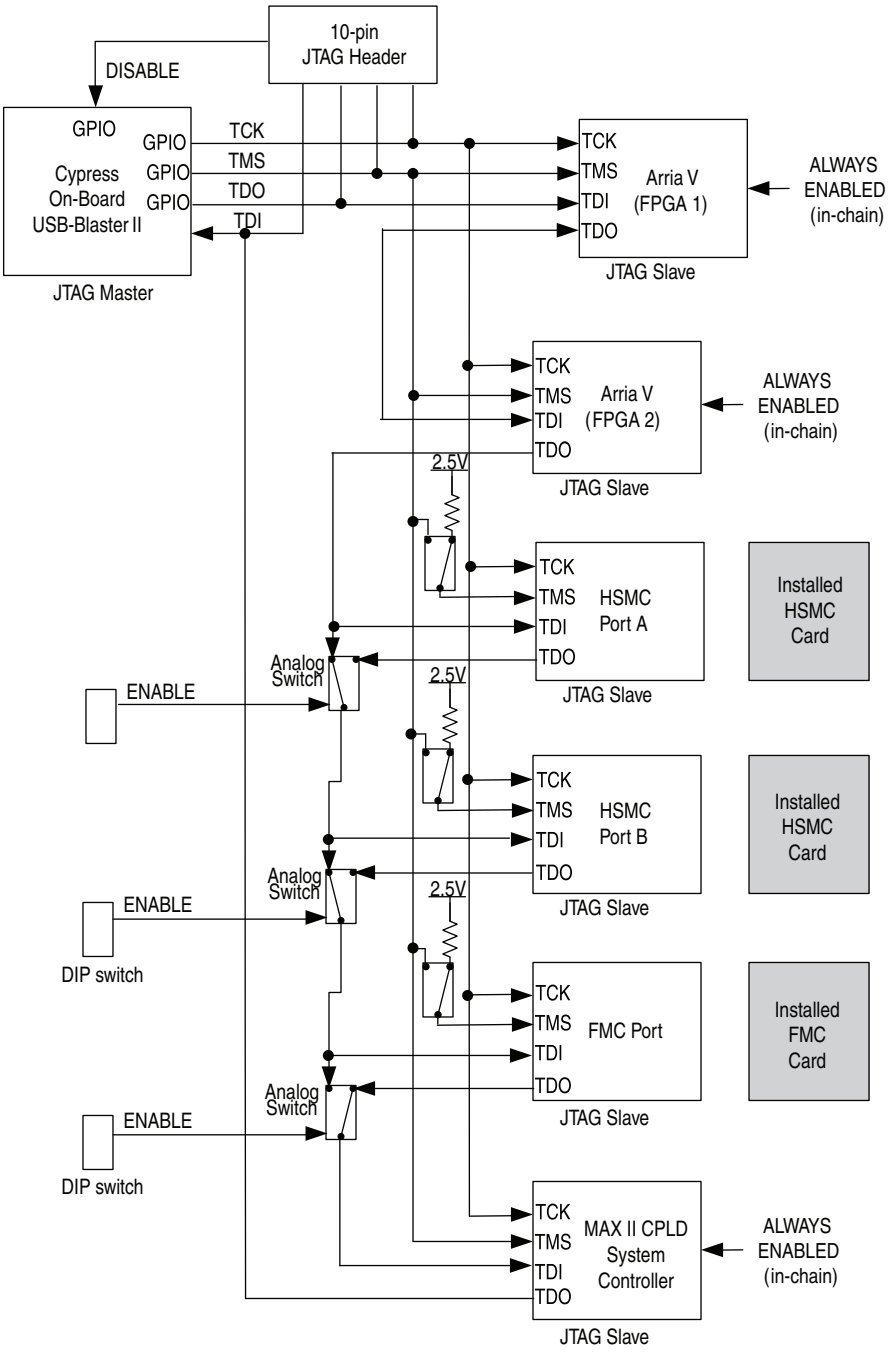
- To check the current setting: `jtagconfig --getparam <cable-no> JtagClock`
- To set a new setting (example clock frequency = 16 M): `jtagconfig --setparam <cable-no> JtagClock 16M`

The USB-Blaster II needs to be 16 M or slower in this case. Only 6 M, 16 M, and 24 M clock frequency options are available. Insert a value of 1 for the `<cable-no>` if this is the only JTAG cable you attach to the board.

Installing daughtercards such as HSMC or FMC can affect performance and requires a lower speed.

Figure 2–4 illustrates the JTAG chain.

Figure 2–4. JTAG Chain



Each jumper shown in Figure 2–4 is located in the JTAG chain DIP switch (SW6) on the back of the board. To connect a device or interface in the chain, you must set the corresponding switch from the JTAG chain DIP switch (SW6). The interface in the JTAG chain depends on the switch settings but the FPGAs and MAX II devices are always in the JTAG chain.

Flash Memory Programming

Flash memory programming is possible through a variety of methods.

The default method is to use the factory design—Board Update Portal (BUP). This design is an embedded webserver, which serves the BUP web page. The web page allows you to select new FPGA designs including hardware, software, or both in an industry-standard S-Record File (**.flash**) and write the design to the user hardware page (page 1) of the flash memory over the network.

The secondary method is to use the pre-built parallel flash loader (PFL) design included in the development kit. The development board implements the Altera PFL megafunction for flash memory programming. The PFL megafunction is a block of logic that is programmed into an Altera programmable logic device (FPGA or CPLD). The PFL functions as a utility for writing to a compatible flash memory device. This pre-built design contains the PFL megafunction that allows you to write either page 0, page 1, or other areas of flash memory over the USB interface using the Quartus II software. This method is used to restore the development board to its factory default settings.

Other methods to program the flash memory can be used as well, including the Nios® II processor.

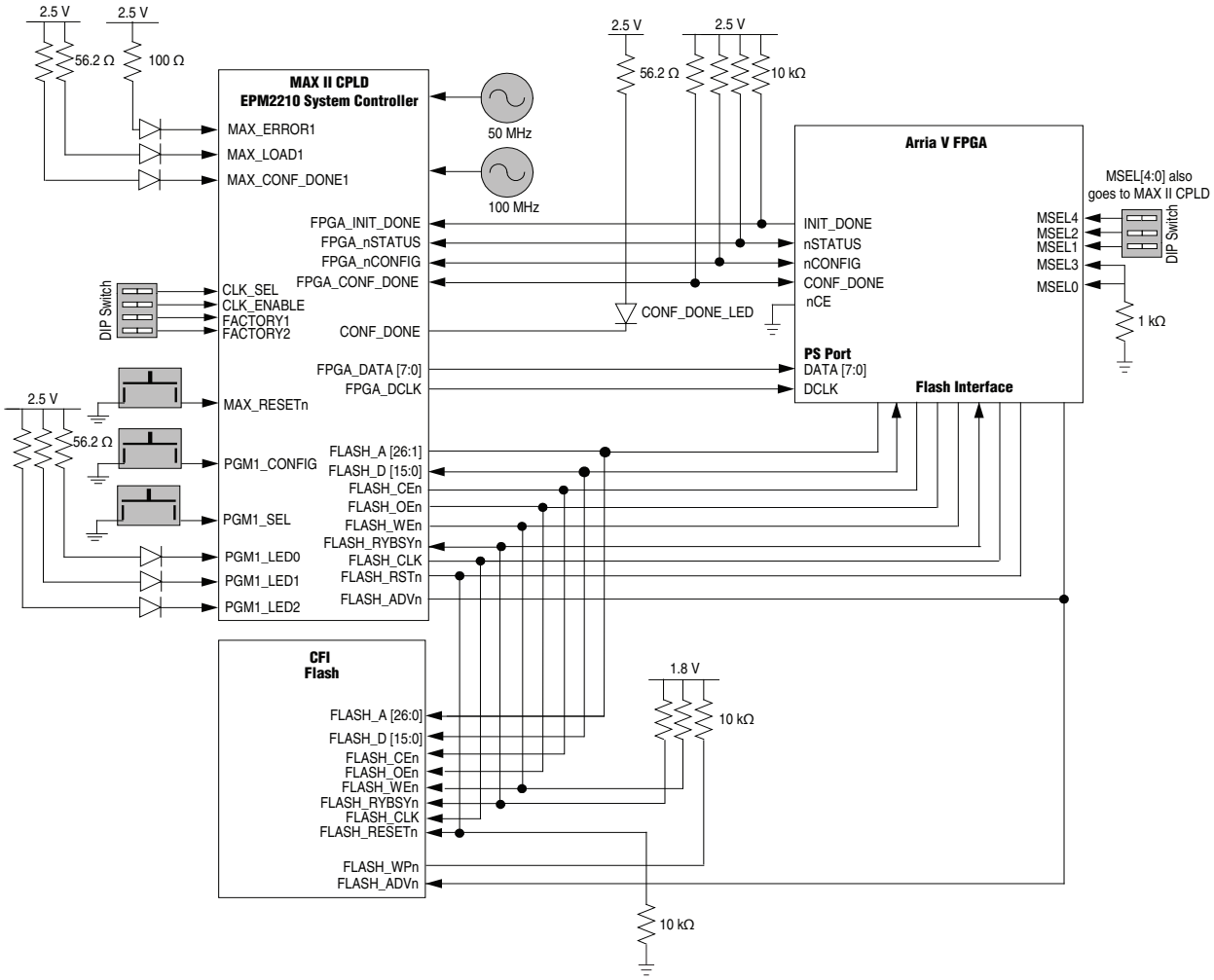
For more information on the Nios II processor, refer to the Nios II Processor page of the Altera website.

FPGA Programming from Flash Memory

On either power-up or by pressing the program configuration push button, `PGM1_CONFIG` (S3), the MAX II CPLD EPM2210 System Controller's PFL configures the FPGA from the flash memory when the `PGM1_LED[2:0]` are ON. The PFL megafunction reads 16-bit data from the flash memory and converts it to fast passive parallel (FPP) format. This 8-bit data is then written to the FPGA's dedicated configuration pins during configuration.

Figure 2–5 shows the PFL configuration.

Figure 2–5. PFL Configuration



For information on the flash memory map storage, refer to the *Arria V GT FPGA Development Kit User Guide*.

There are two pages reserved for the FPGA configuration data. The factory hardware page—page 0—loads upon power-up when the `Factory1` DIP switch (SW5.3) is set to '1'. Otherwise, the user hardware page 1 loads. Pressing the `PGM1_CONFIG` push button (S3) loads the FPGA with a hardware page based on which `PGM1_LED[2:0]` LED (D12, D13, D14) illuminates.

Table 2–6 defines the hardware page that loads when you press the PGM1_CONFIG push button (S3).

Table 2–6. PGM1_LED Settings

PGM1_LED0	PGM1_LED1	PGM1_LED2	Design
ON	OFF	OFF	Factory hardware
OFF	ON	OFF	User design 1
OFF	OFF	ON	User design 2

FPGA Programming over External USB-Blaster

The JTAG programming header provides another method for configuring the FPGA using an external USB-Blaster device with the Quartus II Programmer running on a PC. The external USB-Blaster connects to the board through the JTAG connector (J5). Both FPGAs and the MAX II devices are always in the JTAG chain.

For more information on the following topics, refer to the respective documents:

- Board Update Portal and PFL design, refer to the *Arria V GT FPGA Development Kit User Guide*.
- PFL megafunction, refer to *Parallel Flash Loader Megafunction User Guide.*

Status Elements

The development board includes status LEDs. This section describes the status elements.

Table 2–7 lists the LED board references, names, and functional descriptions.

Table 2–7. Board-Specific LEDs (Part 1 of 2)

Board Reference	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
D1	Power	—	5.0-V	Blue LED. Illuminates when 5.0 V power is active.
D16	MAX_CONF_DONE1	—	2.5-V	Green LED. Illuminates when the MAX II CPLD EPM2210 System Controller is successfully configured. Driven by the MAX II CPLD EPM2210 System Controller.
D17	MAX_LOAD1	—	2.5-V	Green LED. Illuminates when the MAX II CPLD EPM2210 System Controller is actively configuring the FPGA. Driven by the MAX II CPLD EPM2210 System Controller wire-OR'd with the on-board USB-Blaster II CPLD.
D15	MAX_ERROR1	—	2.5-V	Red LED. Illuminates when the MAX II CPLD EPM2210 System Controller fails to configure the FPGA. Driven by the MAX II CPLD EPM2210 System Controller.
D12, D13, D14	PGM1_LED[2:0]	—	2.5-V	Green LEDs. Illuminates to indicate which hardware page loads from flash memory when you press the PGM1_SEL push button or when you power-on the board.

Table 2–7. Board-Specific LEDs (Part 2 of 2)

Board Reference	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
D34	DEVICE1_LED	—	2.5-V	Green LED. Illuminates when FPGA 1 is successfully configured. Driven by the MAX II CPLD EPM2210 System Controller.
D35	DEVICE2_LED	—	2.5-V	Green LED. Illuminates when FPGA 2 is successfully configured. Driven by the MAX II CPLD EPM2210 System Controller.
D36	ENET_LED_TX	—	2.5-V	Green LED. Illuminates to indicate Ethernet PHY transmit activity. Driven by the Marvell 88E1111 PHY.
D37	ENET_LED_RX	—	2.5-V	Green LED. Illuminates to indicate Ethernet PHY receive activity. Driven by the Marvell 88E1111 PHY.
D40	ENET_LED_LINK10	—	2.5-V	Green LED. Illuminates to indicate Ethernet linked at 10 Mbps connection speed. Driven by the Marvell 88E1111 PHY.
D38	ENET_LED_LINK100	—	2.5-V	Green LED. Illuminates to indicate Ethernet linked at 100 Mbps connection speed. Driven by the Marvell 88E1111 PHY.
D39	ENET_LED_LINK1000	AN17	2.5-V	Green LED. Illuminates to indicate Ethernet linked at 1000 Mbps connection speed. Driven by the Marvell 88E1111 PHY.
D4	HSMA_RX_LED	AT15	2.5-V	Green LED. Illuminates to indicate HSMA port A receive data activity.
D5	HSMA_TX_LED	AH14	2.5-V	Green LED. Illuminates to indicate HSMA port A transmit data activity.
D6	HSMA_PRSNTn	AW15	3.3-V	Green LED. Illuminates when HSMC port A has a board or cable plugged-in such that pin 160 becomes grounded. Driven by the add-in card.
D7	HSMB_RX_LED	AG26	2.5-V	Green LED. Illuminates to indicate HSMA port B receive data activity.
D8	HSMB_TX_LED	AM28	2.5-V	Green LED. Illuminates to indicate HSMA port B transmit data activity.
D9	HSMB_PRSNTn	AT24	3.3-V	Green LED. Illuminates when HSMC port B has a board or cable plugged-in such that pin 160 becomes grounded. Driven by the add-in card.
D44	PCIE_LED_X1	AC18	2.5-V	Yellow LED. Configure this LED to display the PCI Express link width x1.
D43	PCIE_LED_X4	AD17	2.5-V	Yellow LED. Configure this LED to display the PCI Express link width x4.
D42	PCIE_LED_X8	AT16	2.5-V	Yellow LED. Configure this LED to display the PCI Express link width x8.

Setup Elements

The development board includes several different kinds of setup elements. This section describes the following setup elements:

- Board settings DIP switch
- JTAG chain header switch
- PCI Express control DIP switch
- CPU reset push button
- MAX II reset push button
- Configuration push button
- Image select push button

For more information about the default settings of the DIP switches, refer to the *Arria V GT FPGA Development Kit User Guide*.

Board Settings DIP Switch

The board settings DIP switch (SW5) controls various features specific to the board and the MAX II CPLD EPM2210 System Controller logic design. Table 2–8 lists the switch controls and descriptions.

Table 2–8. Board Settings DIP Switch Controls

Switch	Schematic Signal Name	Description
1	CLK_SEL	ON : 100 MHz clock select OFF : SMA input clock select
2	CLK_ENABLE	ON : Enable on-board oscillators OFF : Disable on-board oscillators
3	FACTORY_USER1	ON : Load the factory design from flash for Arria V FPGA 1 at power up OFF : Load the user design from flash at power up
4	FACTORY_USER2	Unused

JTAG Settings DIP Switch

The JTAG settings DIP switch (SW6) either remove or include devices in the active JTAG chain. However, the Arria V GT FPGAs and MAX II CPLD EPM2210 System Controller are always in the JTAG chain. Table 2–9 lists the switch controls and its descriptions.

Table 2–9. JTAG Chain Header Switch Controls (Part 1 of 2)

Switch	Schematic Signal Name	Description
1	HSMA_JTAG_EN	ON : Bypass HSMA OFF : HSMA in-chain
2	HSMB_JTAG_EN	ON : Bypass HSMB OFF : HSMB in-chain

Table 2–9. JTAG Chain Header Switch Controls (Part 2 of 2)

Switch	Schematic Signal Name	Description
3	FMC_JTAG_EN	ON : Bypass FMC connector OFF : FMC connector in-chain
4	NC	Unused

PCI Express Control DIP Switch

The PCI Express control DIP switch (SW7) is provided to enable or disable different configurations. Table 2–10 lists the switch controls and descriptions.

Table 2–10. PCI Express Control DIP Switch Controls

Switch	Schematic Signal Name	Description
1	PCIE_PRSNT2n_x1	ON : Enable x1 presence detect OFF : Disable x1 presence detect
2	PCIE_PRSNT2n_x4	ON : Enable x4 presence detect OFF : Disable x4 presence detect
3	PCIE_PRSNT2n_x8	ON : Enable x8 presence detect OFF : Disable x8 presence detect
4	NC	Unused

CPU Reset Push Button

Each Arria V GT FPGA has a CPU reset push button, CPU1_RESETn (S4) for FPGA 1 and CPU2_RESETn (S8) for FPGA 2. Both these push buttons are inputs to the Arria V GT FPGA DEV_CLRn pin and are open-drain I/Os from the MAX II CPLD System Controller. The push button is the default reset for both the FPGA and CPLD logic. The MAX II System Controller also drives these push button during POR.

You must enable the CPU_RESETn signal within the Quartus II software for this reset function to work. Otherwise, the CPU_RESETn acts as a regular I/O pin. When you enable the signal in the Quartus II software, and then pull high on the board, every register within the FPGA resets to a low signal.

MAX II Reset Push Button

The MAX II reset push button, MAX_RESETn, is an input to the MAX II CPLD System Controller. This push button is the default reset for the CPLD logic.

Configuration Push Button

The configuration push button, PGM1_CONFIG (S3), is an input to the MAX II CPLD EPM2210 System Controller. The push button forces a reconfiguration of the FPGA from flash memory. The location in the flash memory is based on the settings of the PGM1_LED[2:0], which is controlled by the image select push button, PGM1_SEL (S2). Valid settings include PGM1_LED0, PGM1_LED1, or PGM1_LED2 on the three pages in flash memory reserved for FPGA designs.

Image Select Push Button

The program select push button, PGM1_SEL (S2), is an input to the MAX II CPLD System Controller. The push button toggles the PGM1_LED[2:0] sequence that selects which location in the flash memory is used to configure the FPGA. Refer to Table 2–6 for the PGM1_LED[2:0] sequence definitions.

Clock Circuitry

This section describes the board's clock inputs and outputs.

On-Board Oscillators

The development board includes fixed and programmable oscillators with a frequency of 50-MHz, 100-MHz, 125-MHz, 148.5-MHz, 156.25-MHz, and 625-MHz.

Figure 2–6 shows the default frequencies of all external clocks going to the Arria V GT FPGA development board.

Figure 2–6. Arria V GT FPGA Development Board Clocks

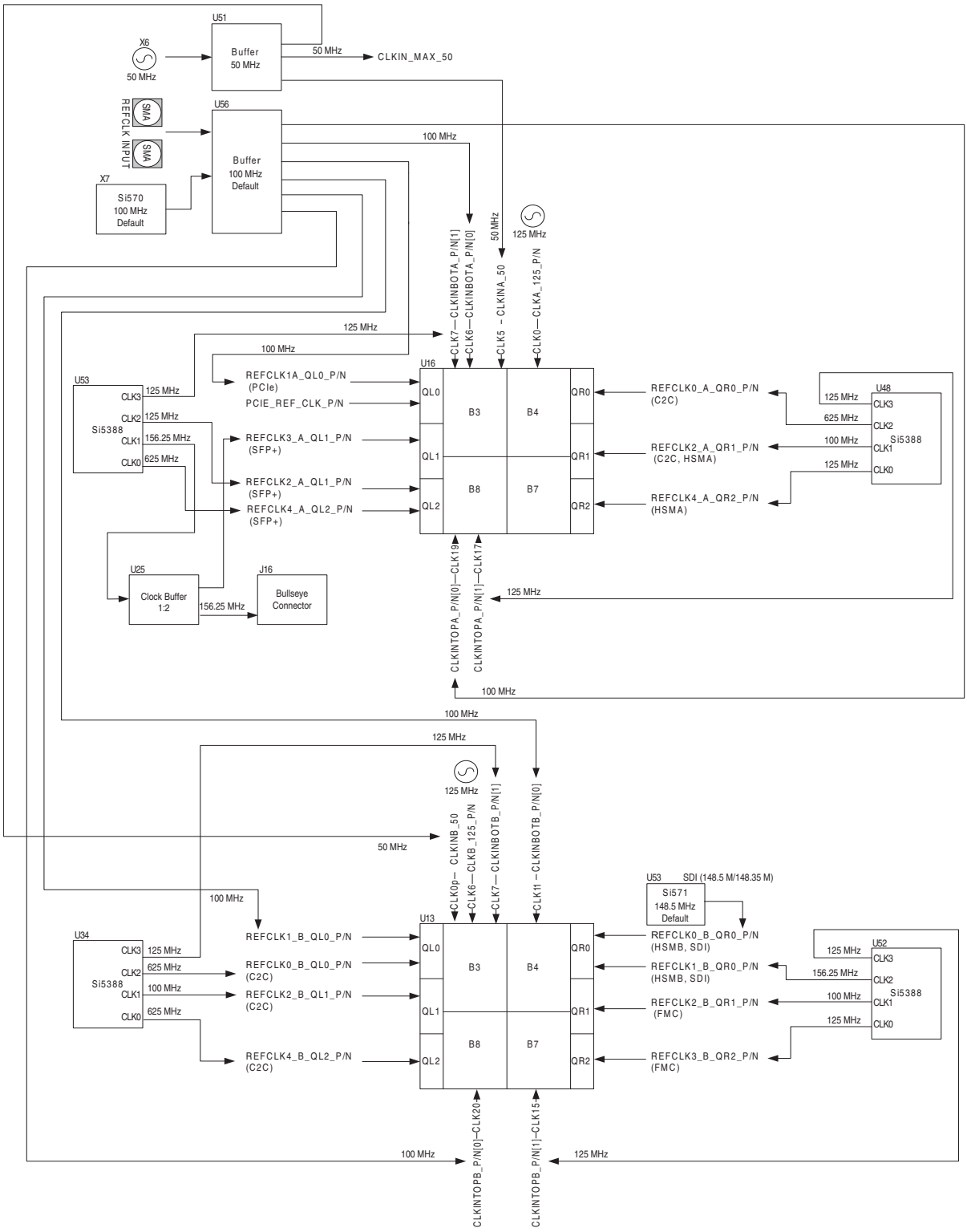


Table 2–11 lists the oscillators, its I/O standard, and voltages required for the development board.

Table 2–11. On-Board Oscillators

Source	Schematic Signal Name	Frequency	I/O Standard	Arria V GT FPGA Pin Number	Application
X6 to U51 1:3 clock buffer	CLKIN_MAX_50	50.000 MHz	1.8-V	—	Nios II and MAX II CPLD
	CLKINA_50		1.8-V	AF21	
	CLKINB_50		1.8-V	AP34	
X3	CLK_CONFIG	100.000 MHz	2.5-V CMOS	—	Fast FPGA configuration
X7 to U56 1:6 clock buffer	REFCLK1_A_QL0_P	100.000 MHz	LVDS (fanout buffer)	AE31	PCI Express host/dual-XTL
	REFCLK1_A_QL0_N			AE32	
	CLKINBOTA_P0			AD20	Bottom edge FPGA 1 – QDRII+
	CLKINBOTA_N0			AC21	
	CLKINTOPA_P0			C20	Top edge FPGA 1 – DDR3
	CLKINTOPA_N0			D20	
	CLKINBOTB_P0			AK7	Bottom edge FPGA 2
	CLKINBOTB_N0			AJ7	
	CLKINTOPB_P0			C34	Top edge FPGA 2 – DDR3
	CLKINTOPB_N0			D34	
X1	CLKA_125_P	125.000 MHz	LVDS	AP34	Fixed clock at 125 MHz for FPGA 1 bank 3A
	CLKA_125_N		LVDS	AN34	
X4	CLKB_125_P	125.000 MHz	LVDS	AD20	Fixed clock at 125 MHz for FPGA 1 bank 3D
	CLKB_125_N		LVDS	AC21	
X2	REFCLK0_QR0_P	148.500 MHz	LVDS	—	HD-SDI video
	REFCLK0_QL2_N		LVDS	—	
U53	REFCLK4_A_QL2_P	625.000 MHz	LVDS	W31	SFP+
	REFCLK4_A_QL2_N		LVDS	W32	
	REFCLK3_A_BUF_P	156.250 MHz	LVDS	—	SFP+, Bull's Eye connector, 1:2 clock to REFCLK3 on FPGA 1,
	REFCLK3_A_BUF_N		LVDS	—	
	REFCLK2_A_QL1_P	125.000 MHz	LVDS	U31	
	REFCLK2_A_QL1_N		LVDS	U32	
	CLKINBOTA_P1	125.000 MHz	LVDS	AL20	Bottom edge FPGA 1 – memory
	CLKINBOTA_N1		LVDS	AK20	
U48	REFCLK4_A_QR2_P	125.000 MHz	LVDS	T9	HSMC port A, C2C
	REFCLK4_A_QR2_N		LVDS	T8	
	REFCLK2_A_QR1_P	100.000 MHz	LVDS	AB9	
	REFCLK2_A_QR1_N		LVDS	AB8	
	REFCLK0_A_QR0_P	625.000 MHz	LVDS	AF8	C2C
	REFCLK0_A_QR0_N		LVDS	AF7	
	CLKINTOPA_P1	125.000 MHz	LVDS	A22	Top edge FPGA 1 – memory
	CLKINTOPA_N1		LVDS	A21	

Table 2–11. On-Board Oscillators

Source	Schematic Signal Name	Frequency	I/O Standard	Arria V GT FPGA Pin Number	Application
U34	REFCLK4_B_QL2_P	625.000 MHz	LVDS	U31	C2C
	REFCLK4_B_QL2_N		LVDS	U32	
	REFCLK2_B_QL1_P	100.000 MHz	LVDS	AC31	C2C
	REFCLK2_B_QL1_N		LVDS	AC32	
	REFCLK0_B_QL0_P	625.000 MHz	LVDS	AG32	C2C
	REFCLK0_B_QL0_N		LVDS	AG33	
	CLKINBOTB_P1	125.000 MHz	LVDS	AL20	Bottom edge FPGA 2 – memory
	CLKINBOTB_N1		LVDS	AK20	
U52	REFCLK3_B_QR2_P	125.000 MHz	LVDS	T9	FMC
	REFCLK3_B_QR2_N		LVDS	T8	
	REFCLK2_B_QR1_P	100.000 MHz	LVDS	Y9	FMC
	REFCLK2_B_QR1_N		LVDS	Y8	
	REFCLK1_B_QR0_P	156.250 MHz	LVDS	AD9	HSMC port B, SDI
	REFCLK1_B_QR0_N		LVDS	AD8	
	CLKINTOPB_P1	125.000 MHz	LVDS	H6	Top edge FPGA 2
	CLKINTOPB_N1		LVDS	J6	

Off-Board Clock Input/Output

The development board has input and output clocks which can be driven onto the board. The output clocks can be programmed to different levels and I/O standards according to the FPGA device's specification.

Table 2–12 lists the clock inputs for the development board.

Table 2–12. Off-Board Clock Inputs

Source	Schematic Signal Name	I/O Standard	Arria V GT FPGA Pin Number	Description
SMA	CLKIN_SMA_P	LVPECL	—	Input to LVDS fan-out buffer (drives one REFCLK, one clock on the top edge and one on the bottom edge of each FPGA)
	CLKIN_SMA_N	LVPECL	—	
HSMC	HSMA_CLK_IN0	2.5-V	AT7	Single-ended input from the installed HSMC cable or board.
HSMC	HSMA_CLK_IN_P1	LVDS/2.5-V	AW4	LVDS input from the installed HSMC cable or board. Can also support 2x LVTTL inputs.
	HSMA_CLK_IN_N1	LVDS/LVTTL	AV4	
HSMC	HSMA_CLK_IN_P2	LVDS/LVTTL	AR6	LVDS input from the installed HSMC cable or board. Can also support 2x LVTTL inputs.
	HSMA_CLK_IN_N2	LVDS/LVTTL	AP6	
HSMC	HSMB_CLK_IN0	2.5-V	AR6	Single-ended input from the installed HSMC cable or board.
HSMC	HSMB_CLK_IN_P1	LVDS/LVTTL	AM33	LVDS input from the installed HSMC cable or board. Can also support 2x LVTTL inputs.
	HSMB_CLK_IN_N1	LVDS/LVTTL	AL33	

Table 2–12. Off-Board Clock Inputs

Source	Schematic Signal Name	I/O Standard	Arria V GT FPGA Pin Number	Description
HSMC	HSMB_CLK_IN_P2	LVDS/LVTTL	AU32	LVDS input from the installed HSMC cable or board. Can also support 2x LVTTL inputs.
	HSMB_CLK_IN_N2	LVDS/LVTTL	AT32	
PCI Express Edge	PCIE_REFCLK_P	LVDS/LVTTL	AG32	LVDS input from the PCI Express edge connector.
	PCIE_REFCLK_N	HCSL	AG33	
FMC	FMC_REFCLK_P0	LVDS	AB9	LVDS input from the FMC board (drives two REFCLKs on FPGA 2)
	FMC_REFCLK_P1	LVDS	V9	
	FMC_REFCLK_N0	LVDS	AB8	
	FMC_REFCLK_N1	LVDS	V8	
	FMC_CLK_M2C_P0	LVDS	AV19	LVDS input from the FMC board.
	FMC_CLK_M2C_P1	LVDS	AF21	
	FMC_CLK_M2C_N0	LVDS	AU19	
	FMC_CLK_M2C_N0	LVDS	AE21	

Table 2–13 lists the clock outputs for the development board.

Table 2–13. Off-Board Clock Outputs

Source	Schematic Signal Name	I/O Standard	Arria V GT FPGA Pin Number	Description
HSMC	HSMA_CLK_OUT0	2.5V CMOS	AL14	FPGA CMOS output (or GPIO)
HSMC	HSMA_CLK_OUT_P1	LVDS/2.5V CMOS	AU13	LVDS output. Can also support 2x CMOS outputs.
	HSMA_CLK_OUT_N1	LVDS/2.5V CMOS	AT13	
HSMC	HSMA_CLK_OUT_P2	LVDS/2.5V CMOS	AM7	LVDS output. Can also support 2x CMOS outputs.
	HSMA_CLK_OUT_N2	LVDS/2.5V CMOS	AL7	
HSMC	HSMB_CLK_OUT0	2.5V CMOS	AJ33	FPGA CMOS output (or GPIO)
HSMC	HSMB_CLK_OUT_P1	LVDS/2.5V CMOS	AM33	LVDS output. Can also support 2x CMOS outputs.
	HSMB_CLK_OUT_N1	LVDS/2.5V CMOS	AL34	
HSMC	HSMB_CLK_OUT_P2	LVDS/2.5V CMOS	AU32	LVDS output. Can also support 2x CMOS outputs.
	HSMB_CLK_OUT_N2	LVDS/2.5V CMOS	AD26	

General User Input/Output

This section describes the user I/O interface to the FPGA, including the push buttons, DIP switches, status LEDs, character LCD, and SDI video output/input port.

User-Defined Push Buttons

The development board includes three user-defined push buttons for each FPGA device. For information on the system and safe reset push buttons, refer to "Setup Elements" on page 2–20.

Board references S5, S6, and S7 are push buttons that allow you to interact with the Arria V GT FPGA 1 while S9, S10, and S11 are for use with the Arria V GT FPGA 2. When you press and hold down the button, the device pin is set to logic 0; when you release the button, the device pin is set to logic 1. There are no board-specific functions for these general user push buttons.

Table 2–14 lists the user-defined push button schematic signal names and their corresponding Arria V GT FPGA device pin numbers.

Table 2–14. User-Defined Push Button Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
S6	USER1_PB0	U16.T19	2.5-V	User-defined push buttons for FPGA 1.
S5	USER1_PB1	U16.R19	2.5-V	
S4	USER1_PB2	U16.F18	2.5-V	
S11	USER2_PB0	U13.D6	2.5-V	User-defined push buttons for FPGA 2.
S10	USER2_PB1	U13.C6	2.5-V	
S9	USER2_PB2	U13.K7	2.5-V	

User-Defined DIP Switches

Board references SW2 and SW3 are two sets of eight-pin DIP switches. There are no board-specific functions for these switches. Each of the Arria V GT FPGA have a set of user-defined DIP switch. When the switch is in the OFF position, a logic 1 is selected. When the switch is in the ON position, a logic 0 is selected.

Table 2–15 lists the user-defined DIP switch schematic signal names and their corresponding Arria V GT FPGA pin numbers.

Table 2–15. User-defined DIP Switch Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
SW2.1	USER1_DIPSW0	P18	2.5-V	User-defined DIP switch that connects to FPGA 1.
SW2.2	USER1_DIPSW1	N18	2.5-V	
SW2.3	USER1_DIPSW2	C16	2.5-V	
SW2.4	USER1_DIPSW3	B16	2.5-V	
SW2.5	USER1_DIPSW4	G17	2.5-V	
SW2.6	USER1_DIPSW5	F17	2.5-V	
SW2.7	USER1_DIPSW6	D17	2.5-V	
SW2.8	USER1_DIPSW7	C17	2.5-V	
SW3.1	USER2_DIPSW0	C8	2.5-V	User-defined DIP switch that connects to FPGA 2.
SW3.2	USER2_DIPSW1	D8	2.5-V	
SW3.3	USER2_DIPSW2	E7	2.5-V	
SW3.4	USER2_DIPSW3	E6	2.5-V	
SW3.5	USER2_DIPSW4	G8	2.5-V	
SW3.6	USER2_DIPSW5	F8	2.5-V	
SW3.7	USER2_DIPSW6	D15	2.5-V	
SW3.8	USER2_DIPSW7	G11	2.5-V	

User-Defined LEDs

The development board includes general and user-defined LEDs. This section describes all user-defined LEDs. For information on board specific or status LEDs, refer to "Status Elements" on page 2–18.

General User-Defined LEDs

Board references D18 through D25 and D26 through D33 are two sets of eight pairs user-defined LEDs. Each of the Arria V GT FPGA have a set of user-defined LEDs. The LEDs illuminate when a logic 0 is driven, and turns off when a logic 1 is driven. There are no board-specific functions for these LEDs.

Table 2–16 lists the user-defined LED schematic signal names and their corresponding Arria V GT FPGA pin numbers.

Table 2–16. User-Defined LED Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
D25	USER1_LED_G0	U16.C15	2.5-V	User-defined LEDs for FPGA 1.
	USER1_LED_R0	U16.AL15	2.5-V	
D24	USER1_LED_G1	U16.R18	2.5-V	
	USER1_LED_R1	U16.AC15	2.5-V	
D23	USER1_LED_G2	U16.F11	2.5-V	
	USER1_LED_R2	U16.AD14	2.5-V	
D22	USER1_LED_G3	U16.AP11	2.5-V	
	USER1_LED_R3	U16.AN8	2.5-V	
D21	USER1_LED_G4	U16.AU14	2.5-V	
	USER1_LED_R4	U16.AP8	2.5-V	
D20	USER1_LED_G5	U16.AE16	2.5-V	
	USER1_LED_R5	U16.AK14	2.5-V	
D19	USER1_LED_G6	U16.AF15	2.5-V	
	USER1_LED_R6	U16.AG14	2.5-V	
D18	USER1_LED_G7	U16.AK15	2.5-V	
	USER1_LED_R7	U16.AH15	2.5-V	
D33	USER2_LED_G0	U13.M19	2.5-V	User-defined LEDs for FPGA 2.
	USER2_LED_R0	U13.N20	2.5-V	
D32	USER2_LED_G1	U13.L19	2.5-V	
	USER2_LED_R1	U13.C15	2.5-V	
D31	USER2_LED_G2	U13.K19	2.5-V	
	USER2_LED_R2	U13.AL28	2.5-V	
D30	USER2_LED_G3	U13.J19	2.5-V	
	USER2_LED_R3	U13.F11	2.5-V	
D29	USER2_LED_G4	U13.K20	2.5-V	
	USER2_LED_R4	U13.AJ31	2.5-V	
D28	USER2_LED_G5	U13.J20	2.5-V	
	USER2_LED_R5	U13.AN34	2.5-V	
D27	USER2_LED_G6	U13.T20	2.5-V	
	USER2_LED_R6	U13.AJ34	2.5-V	
D26	USER2_LED_G7	U13.R20	2.5-V	
	USER2_LED_R7	U13.AK33	2.5-V	

HSMC User-Defined LEDs

Each HSMC port has two LEDs located nearby. There are no board-specific functions for the HSMC LEDs. The LEDs are labeled TX and RX, and are intended to display data flow to and from the connected HSMC daughtercards. The LEDs are driven by the Arria V GT FPGA.

Table 2–17 lists the HSMC user-defined LED schematic signal names and their corresponding Arria V GT FPGA pin numbers.

Table 2–17. HSMC User-Defined LED Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
D5	HSMA_TX_LED	U16.AH14	2.5-V	User-defined LEDs. Labeled TX for HSMC port A.
D4	HSMA_RX_LED	U16.AT15	2.5-V	User-defined LEDs. Labeled RX for HSMC port A.
D8	HSMB_TX_LED	U13.AM28	2.5-V	User-defined LEDs. Labeled TX for HSMC port B.
D7	HSMB_RX_LED	U13.AG26	2.5-V	User-defined LEDs. Labeled RX for HSMC port B.

LCD

The development board includes a single 14-pin 0.1" pitch dual-row header that interfaces to a 16 character × 2 line Lumex LCD display. The LCD has a 14-pin receptacle that mounts directly to the board's 14-pin header, so it can be easily removed for access to components under the display. You can also use the header for debugging or other purposes.

Table 2–18 summarizes the LCD pin assignments. The signal names and directions are relative to the Arria V GT FPGA.

Table 2–18. LCD Pin Assignments, Schematic Signal Names, and Functions

Board Reference (J30)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
7	LCD1_DATA0	N20	2.5-V	LCD data bus
8	LCD1_DATA1	R20	2.5-V	LCD data bus
9	LCD1_DATA2	T20	2.5-V	LCD data bus
10	LCD1_DATA3	J20	2.5-V	LCD data bus
11	LCD1_DATA4	K20	2.5-V	LCD data bus
12	LCD1_DATA5	J19	2.5-V	LCD data bus
13	LCD1_DATA6	K19	2.5-V	LCD data bus
14	LCD1_DATA7	L19	2.5-V	LCD data bus
4	LCD1_D_Cn	M19	2.5-V	LCD data or command select
5	LCD1_WEn	M20	2.5-V	LCD write enable
6	LCD1_CSn	E18	2.5-V	LCD chip select

Table 2–19 lists the LCD pin definitions, and is an excerpt from Lumex data sheet.

Table 2–19. LCD Pin Definitions and Functions

Pin Number	Symbol	Level	Function	
1	V_{DD}	—	Power supply	5 V
2	V_{SS}	—		GND (0 V)
3	V_0	—		For LCD drive
4	RS	H/L	Register select signal H: Data input L: Instruction input	
5	R/W	H/L	H: Data read (module to MPU) L: Data write (MPU to module)	
6	E	H, H to L	Enable	
7–14	DB0–DB7	H/L	Data bus—software selectable 4-bit or 8-bit mode	

For more information such as timing, character maps, interface guidelines, and other related documentation, visit www.lumex.com.

SDI Video Output/Input

The SDI video port consists of a LMH0303SQx cable driver and a LMH0384SQ cable equalizer. The PHY devices from National Semiconductor interface to single-ended 75-Ω SMB connectors.

The cable driver supports operation at 270 Mbit standard definition (SD), 1.5 Gbit high definition (HD), and 3.0 Gbit dual-link HD modes. Control signals are allowed for SD and HD modes selections, as well as device enable. The device can be clocked by the 148.5 MHz voltage-controlled crystal oscillator (VCXO) and matched to incoming signals within 50 ppm using the UP and DN voltage control lines to the VCXO.

Table 2–20 lists the supported output standards for the SD and HD input.

Table 2–20. Supported Output Standards for SD and HD Input

SD_HD Input	Supported Output Standards	Rise TIme
0	SMPTE 424M, SMPTE 292M	Faster
1	SMPTE 259M	Slower

For more information about the application circuit of the LMH0303SQx cable driver, refer to the cable driver data sheet at www.national.com.

Table 2–21 summarizes the SDI video output interface pin assignments, signal names, and functions.

Table 2–21. SDI Video Output Interface Pin Assignments, Schematic Signal Names, and Functions

Board Reference (U24)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
1	SDI_A_TX_P	AH3	1.4-V PCML	SDI video input P
2	SDI_A_TX_N	AH4	1.4-V PCML	SDI video input N
4	SDI_A_TX_RSET	—	3.3-V	Device reset pull up register
6	SDI_A_TX_EN	AK31	2.5-V	Device enable
10	SDI_A_TX_SD_HDN	M20	2.5-V	High definition select
11	SDI_A_TXDRV_N	—	3.3-V	SDI video output from cable driver N
12	SDI_A_TXDRV_P	—	3.3-V	SDI video output from cable driver P

The cable equalizer supports operation at 270 Mbit SD, 1.5 Gbit HD, and 3.0 Gbit dual-link HD modes. Control signals are allowed for bypassing or disabling the device, as well as a carrier detect or auto-mute signal interface.

Table 2–22 lists the cable equalizer lengths.

Table 2–22. SDI Cable Equalizer Lengths

Data Rate (Mbps)	Cable Type	Maximum Cable Length (m)
270	Belden 1694A	400
1485		140
2970		120

Figure 2–7 is an excerpt from the LMH0384SQ cable equalizer data sheet that shows the SDI cable equalizer. On this development board, the output is a single-ended output, with the negative channel driving a load local to the board.

Figure 2–7. SDI Cable Equalizer

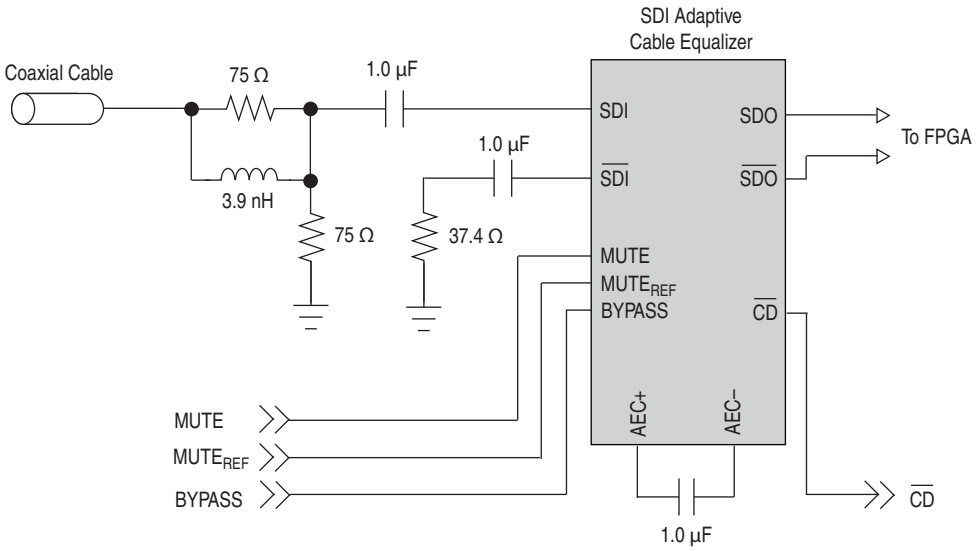


Table 2–23 summarizes the SDI video input interface pin assignments, signal names, and functions.

Table 2–23. SDI Video Input Interface Pin Assignments, Schematic Signal Names, and Functions

Board Reference (U23)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
2	SDI_A_EQIN_P1	—	3.3-V	SDI video cable equalizer input P
3	SDI_A_EQIN_N1	—	3.3-V	SDI video cable equalizer input N
7	SDI_A_RX_BYPASS	P19	2.5-V	Equalizer bypass enable
11	SDI_A_RX_P	AJ1	1.4-V PCML	SDI video output P
10	SDI_A_RX_N	AJ2	1.4-V PCML	SDI video output N
14	SDI_A_RX_EN	AK34	2.5-V	Device enable
15	SDI_A_RX_CDN	—	3.3-V	SDI video cable equalizer input carrier detect output to LED

Components and Interfaces

This section describes the development board's communication ports and interface cards relative to the Arria V GT FPGA. The development board supports the following communication ports:

- PCI Express
- 10/100/1000 Ethernet
- HSMC
- SFP+ modules
- FMC connector
- Bull's Eye connector

PCI Express

The Arria V GT FPGA development board is designed to fit entirely into a PC motherboard with a ×8 PCI Express slot that can accommodate a full height long form factor add-in card. This interface uses the Arria V GT FPGA's PCI Express hard IP block, saving logic resources for the user logic application. The PCI express edge connector has a presence detect feature to allow the motherboard to determine if a card is installed.

For more information on using the PCI Express hard IP block, refer to the *PCI Express Compiler User Guide*.

The PCI Express interface supports auto-negotiating channel width from ×1 to ×4 to ×8 by using Altera's PCIe MegaCore IP. You can also configure this board to a ×1, ×4, or ×8 interface through a DIP switch that connects the PRSNTn pins for each bus width.

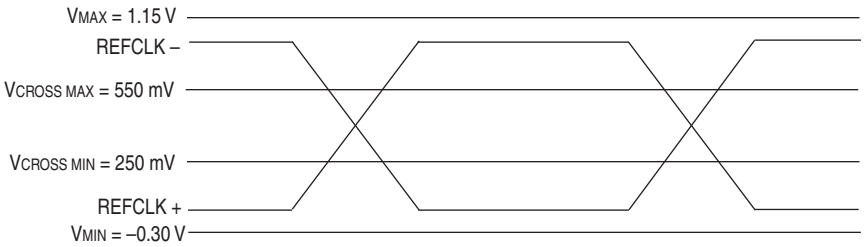
The PCI Express edge connector has a connection speed of 2.5 Gbps/lane for a maximum of 20 Gbps full-duplex (Gen1) or 5.0 Gbps/lane for a maximum of 40 Gbps full-duplex (Gen2).

The power for the board can be sourced entirely from the PCI Express edge connector when installed into a PC motherboard. Although the board can also be powered by a laptop power supply for use on a lab bench, Altera recommends that you do not power up from both supplies at the same time. Ideal diode power sharing devices have been designed into this board to prevent damages or back-current from one supply to the other.

The PCIE_REFCLK_P signal is a 100 MHz differential input that is driven from the PC motherboard on to this board through the edge connector. This signal connects directly to a Arria V GT FPGA REFCLK input pin pair using DC coupling. This clock is terminated on the motherboard and therefore, no on-board termination is required. This clock can have spread-spectrum properties that change its period between 9.847 ps to 10.203 ps. The I/O standard is High-Speed Current Steering Logic (HCSL).

Figure 2–8 shows the PCI Express reference clock levels.

Figure 2–8. PCI Express Reference Clock Levels



The JTAG and SMB are optional signals in the PCI Express specification. Therefore, the JTAG signal loopback from PCI Express TDI to PCI Express TDO and are not used on this board. The SMB signals are wired to the Arria V GT FPGA but are not required for normal operation.

Table 2–24 summarizes the PCI Express pin assignments. The signal names and directions are relative to the Arria V GT FPGA.

Table 2–24. PCI Express Pin Assignments, Schematic Signal Names, and Functions

Board Reference (J4)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
A5	PCIE_JTAG_TCK	—	1.4-V PCML	JTAG chain clock
A6	PCIE_JTAG_TDI	—	1.4-V PCML	JTAG chain data in
A7	PCIE_JTAG_TDO	—	1.4-V PCML	JTAG chain data out
A8	PCIE_JTAG_TMS	—	1.4-V PCML	JTAG chain mode select
A11	PCIE_PERSTN	N9	1.4-V PCML	Presence detect DIP switch
A1	PCIE_PRSNT1N	—	1.4-V PCML	Presence detect DIP switch
B17	PCIE_PRSNT2N_X1	—	1.4-V PCML	Presence detect DIP switch
B31	PCIE_PRSNT2N_X4	—	1.4-V PCML	Presence detect DIP switch
B48	PCIE_PRSNT2N_X8	—	1.4-V PCML	Presence detect DIP switch
A14	PCIE_REFCLK_N	AG33	1.4-V PCML	Motherboard reference clock
A13	PCIE_REFCLK_P	AG32	1.4-V PCML	Motherboard reference clock
B15	PCIE_RX_N0	AW36	1.4-V PCML	Receive bus

Table 2–24. PCI Express Pin Assignments, Schematic Signal Names, and Functions

Board Reference (J4)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
B20	PCIE_RX_N1	AT38	1.4-V PCML	Receive bus
B24	PCIE_RX_N2	AP38	1.4-V PCML	Receive bus
B28	PCIE_RX_N3	AM38	1.4-V PCML	Receive bus
B34	PCIE_RX_N4	AH38	1.4-V PCML	Receive bus
B38	PCIE_RX_N5	AF38	1.4-V PCML	Receive bus
B42	PCIE_RX_N6	AD38	1.4-V PCML	Receive bus
B46	PCIE_RX_N7	AB38	1.4-V PCML	Receive bus
B14	PCIE_RX_P0	AW37	1.4-V PCML	Receive bus
B19	PCIE_RX_P1	AT39	1.4-V PCML	Receive bus
B23	PCIE_RX_P2	AP39	1.4-V PCML	Receive bus
B27	PCIE_RX_P3	AM39	1.4-V PCML	Receive bus
B33	PCIE_RX_P4	AH39	1.4-V PCML	Receive bus
B37	PCIE_RX_P5	AF39	1.4-V PCML	Receive bus
B41	PCIE_RX_P6	AD39	1.4-V PCML	Receive bus
B45	PCIE_RX_P7	AB39	1.4-V PCML	Receive bus
B5	PCIE_SMBCLK	AV18	1.4-V PCML	SMB clock
B6	PCIE_SMBDAT	AM16	1.4-V PCML	SMB data
A17	PCIE_TX_CN0	AU36	1.4-V PCML	Transmit bus
A22	PCIE_TX_CN1	AR36	1.4-V PCML	Transmit bus
A26	PCIE_TX_CN2	AN36	1.4-V PCML	Transmit bus
A30	PCIE_TX_CN3	AL36	1.4-V PCML	Transmit bus
A36	PCIE_TX_CN4	AG36	1.4-V PCML	Transmit bus
A40	PCIE_TX_CN5	AE36	1.4-V PCML	Transmit bus
A44	PCIE_TX_CN6	AC36	1.4-V PCML	Transmit bus
A48	PCIE_TX_CN7	AA36	1.4-V PCML	Transmit bus
A16	PCIE_TX_CP0	AU37	1.4-V PCML	Transmit bus
A21	PCIE_TX_CP1	AR37	1.4-V PCML	Transmit bus
A25	PCIE_TX_CP2	AN37	1.4-V PCML	Transmit bus
A29	PCIE_TX_CP3	AL37	1.4-V PCML	Transmit bus
A35	PCIE_TX_CP4	AG37	1.4-V PCML	Transmit bus
A39	PCIE_TX_CP5	AE37	1.4-V PCML	Transmit bus
A43	PCIE_TX_CP6	AC37	1.4-V PCML	Transmit bus
A47	PCIE_TX_CP7	AA37	1.4-V PCML	Transmit bus
B11	PCIE_WAKEN_R	AL16	1.4-V PCML	Wake signal

10/100/1000 Ethernet

This development board supports 10/100/1000 base-T Ethernet using an external Marvell 88E1111 PHY and Altera Triple-Speed Ethernet MegaCore MAC function. The PHY-to-MAC interface employs RGMII using the Arria V GT FPGA LVDS pins in Soft-CDR mode at 1.25 Gbps transmit and receive. In 10-Mb or 100-Mb mode, the RGMII interface still runs at 1.25 GHz but the packet data is repeated 10 or 100 times. The MAC function must be provided in the FPGA for typical networking applications.

The Marvell 88E1111 PHY uses 2.5-V and 1.0-V power rails and requires a 25 MHz reference clock driven from a dedicated oscillator. The PHY interfaces to a HALO HFJ11-1G02E model RJ45 with internal magnetics that can be used for driving copper lines with Ethernet traffic.

Figure 2–9 shows the RGMII interface between the FPGA (MAC) and Marvell 88E1111 PHY.

Figure 2–9. RGMII Interface between FPGA (MAC) and Marvell 88E1111 PHY

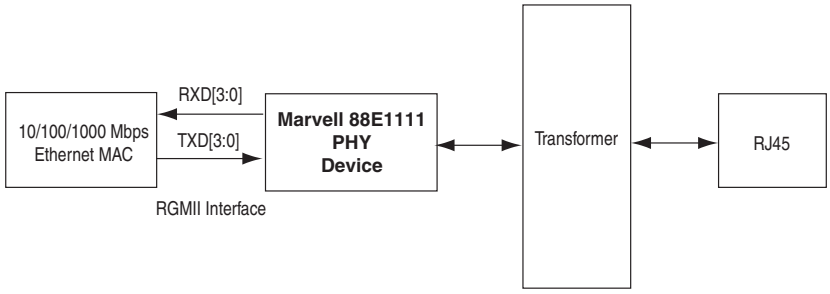


Table 2–25 lists the Ethernet PHY interface pin assignments.

Table 2–25. Ethernet PHY Pin Assignments, Signal Names and Functions (Part 1 of 2)

Board Reference (U14)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
8	ENET_GTX_CLK	AN16	2.5-V CMOS	RGMII transmit clock
23	ENET_INTN	AP16	2.5-V CMOS	Management bus interrupt
60	ENET_LED_DUPLEX	—	2.5-V CMOS	Duplex link LED
70	ENET_LED_DUPLEX	—	2.5-V CMOS	Duplex link LED
76	ENET_LED_LINK10	—	2.5-V CMOS	10-Mb link LED
74	ENET_LED_LINK100	—	2.5-V CMOS	100-Mb link LED
73	ENET_LED_LINK1000	AN17	2.5-V CMOS	1000-Mb link LED
58	ENET_LED_RX	—	2.5-V CMOS	RX data active LED
69	ENET_LED_RX	—	2.5-V CMOS	RX data active LED
68	ENET_LED_TX	—	2.5-V CMOS	TX data active LED
25	ENET_MDC	AJ18	2.5-V CMOS	Management bus data clock
24	ENET_MDIO	AL17	2.5-V CMOS	Management bus data
28	ENET_RESETN	AK17	2.5-V CMOS	Device reset

Table 2–25. Ethernet PHY Pin Assignments, Signal Names and Functions (Part 2 of 2)

Board Reference (U14)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
30	ENET_RSET	—	2.5-V CMOS	Bias voltage for the Ethernet PHY. This pin connects to ground through a 4.99-KΩ resistor.
2	ENET_RX_CLK	AK7	2.5-V CMOS	RGMII receive clock
95	ENET_RX_D0	AU17	2.5-V CMOS	RGMII receive data
92	ENET_RX_D1	AT17	2.5-V CMOS	RGMII receive data
93	ENET_RX_D2	AW16	2.5-V CMOS	RGMII receive data
91	ENET_RX_D3	AH18	2.5-V CMOS	RGMII receive data
94	ENET_RX_DV	AW17	2.5-V CMOS	RGMII receive data valid
75	ENET_RX_N	AK19	2.5-V CMOS	RGMII receive channel
77	ENET_RX_P	AL19	2.5-V CMOS	RGMII receive channel
11	ENET_TX_D0	AT19	2.5-V CMOS	RGMII transmit data
12	ENET_TX_D1	AU18	2.5-V CMOS	RGMII transmit data
14	ENET_TX_D2	AH19	2.5-V CMOS	RGMII transmit data
16	ENET_TX_D3	AG19	2.5-V CMOS	RGMII transmit data
9	ENET_TX_EN	AP19	2.5-V CMOS	RGMII transmit enable
81	ENET_TX_N	AE19	2.5-V CMOS	RGMII transmit channel
82	ENET_TX_P	AF19	2.5-V CMOS	RGMII transmit channel
55	ENET_XTAL_25MHZ	—	2.5-V CMOS	25-MHz clock
29	MDI_P0	—	2.5-V CMOS	Media dependent interface 0
31	MDI_N0	—	2.5-V CMOS	Media dependent interface 0
33	MDI_P1	—	2.5-V CMOS	Media dependent interface 1
34	MDI_N1	—	2.5-V CMOS	Media dependent interface 1
39	MDI_P2	—	2.5-V CMOS	Media dependent interface 2
41	MDI_N2	—	2.5-V CMOS	Media dependent interface 2
42	MDI_P3	—	2.5-V CMOS	Media dependent interface 3
43	MDI_N3	—	2.5-V CMOS	Media dependent interface 3

HSMC

The development board contains two HSMC interfaces—port A on device 1 and port B on device 2. HSMC port A and port B interfaces support both single-ended and differential signaling. This physical interface provides eight channels of 6.5536 Gbps-capable transceivers for the GT version of this board. The HSMC interface also supports a full SPI4.2 interface (17 LVDS channels), three input and output clocks, JTAG and SMB signals, as well as power for compatible HSMC cards. The LVDS channels can be used for CMOS signaling as well as LVDS.

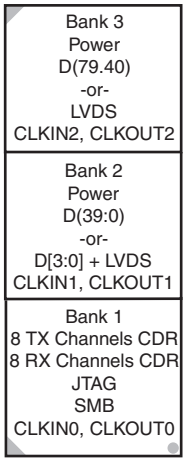
The HSMC is an Altera-developed open specification, which allows you to expand the functionality of the development board through the addition of daughtercards (HSMCs).

For more information about the HSMC specification such as signaling standards, signal integrity, compatible connectors, and mechanical information, refer to the *High Speed Mezzanine Card (HSMC) Specification* manual.

The HSMC connector has a total of 172 pins, including 120 signal pins, 39 power pins, and 13 ground pins. The ground pins are located between the two rows of signal and power pins, acting both as a shield and a reference. The HSMC host connector is based on the 0.5 mm-pitch QSH/QTH family of high-speed, board-to-board connectors from Samtec. There are three banks in this connector. Bank 1 has every third pin removed as done in the QSH-DP/QTH-DP series. Bank 2 and bank 3 have all the pins populated as done in the QSH/QTH series.

Figure 2–10 shows the bank arrangement of signals with respect to the Samtec connector's three banks.

Figure 2–10. HSMC Signal and Bank Diagram



The HSMC interface has programmable bi-directional I/O pins that can be used as 2.5-V LVCMOS, which is 3.3-V LVTTL-compatible. These pins can also be used as various differential I/O standards including, but not limited to, LVDS, mini-LVDS, and RSDS with up to 17 full-duplex channels.

As noted in the *High Speed Mezzanine Card (HSMC) Specification* manual, LVDS and single-ended I/O standards are only guaranteed to function when mixed according to either the generic single-ended pin-out or generic differential pin-out.

Table 2–26 lists the HSMC port A interface pin assignments, signal names, and functions.

Table 2–26. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 5)

Board Reference (J1)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
1	HSMA_TX_P7	D3	1.5-V PCML	Transceiver TX bit 7
2	HSMA_RX_P7	E1	1.5-V PCML	Transceiver RX bit 7
3	HSMA_TX_N7	D4	1.5-V PCML	Transceiver TX bit 7n

Table 2–26. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 5)

Board Reference (J1)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
4	HSMA_RX_N7	E2	1.5-V PCML	Transceiver RX bit 7n
5	HSMA_TX_P6	H3	1.5-V PCML	Transceiver TX bit 6
6	HSMA_RX_P6	J1	1.5-V PCML	Transceiver RX bit 6
7	HSMA_TX_N6	H4	1.5-V PCML	Transceiver TX bit 6n
8	HSMA_RX_N6	J2	1.5-V PCML	Transceiver RX bit 6n
9	HSMA_TX_P5	K3	1.5-V PCML	Transceiver TX bit 5
10	HSMA_RX_P5	L1	1.5-V PCML	Transceiver RX bit 5
11	HSMA_TX_N5	K4	1.5-V PCML	Transceiver TX bit 5n
12	HSMA_RX_N5	L2	1.5-V PCML	Transceiver RX bit 5n
13	HSMA_TX_P4	M3	1.5-V PCML	Transceiver TX bit 4
14	HSMA_RX_P4	N1	1.5-V PCML	Transceiver RX bit 4
15	HSMA_TX_N4	M4	1.5-V PCML	Transceiver TX bit 4n
16	HSMA_RX_N4	N2	1.5-V PCML	Transceiver RX bit 4n
17	HSMA_TX_P3	AH3	1.5-V PCML	Transceiver TX bit 3
18	HSMA_RX_P3	AJ1	1.5-V PCML	Transceiver RX bit 3
19	HSMA_TX_N3	AH4	1.5-V PCML	Transceiver TX bit 3n
20	HSMA_RX_N3	AJ2	1.5-V PCML	Transceiver RX bit 3n
21	HSMA_TX_P2	V3	1.5-V PCML	Transceiver TX bit 2
22	HSMA_RX_P2	W1	1.5-V PCML	Transceiver RX bit 2
23	HSMA_TX_N2	V4	1.5-V PCML	Transceiver TX bit 2n
24	HSMA_RX_N2	W2	1.5-V PCML	Transceiver RX bit 2n
25	HSMA_TX_P1	T3	1.5-V PCML	Transceiver TX bit 1
26	HSMA_RX_P1	U1	1.5-V PCML	Transceiver RX bit 1
27	HSMA_TX_N1	T4	1.5-V PCML	Transceiver TX bit 1n
28	HSMA_RX_N1	U2	1.5-V PCML	Transceiver RX bit 1n
29	HSMA_TX_P0	P3	1.5-V PCML	Transceiver TX bit 0
30	HSMA_RX_P0	R1	1.5-V PCML	Transceiver RX bit 0
31	HSMA_TX_N0	P4	1.5-V PCML	Transceiver TX bit 0n
32	HSMA_RX_N0	R2	1.5-V PCML	Transceiver RX bit 0n
33	HSMA_SDA	AT14	2.5-V CMOS	Management serial data
34	HSMA_SCL	AU15	2.5-V CMOS	Management serial clock
35	JTAG_TCK	AV34	2.5-V CMOS	JTAG clock signal
36	HSMA_JTAG_TMS	—	2.5-V CMOS	JTAG mode select signal
37	HSMA_JTAG_TDO	—	2.5-V CMOS	JTAG data output
38	AVB_JTAG_TDO	AT34	2.5-V CMOS	JTAG data output
39	HSMA_CLK_OUT0	AL14	LVDS or 2.5-V	Dedicated CMOS clock out
40	HSMA_CLK_IN0	AT7	LVDS or 2.5-V	Dedicated CMOS clock in
41	HSMA_D0	AG16	2.5-V CMOS	Dedicated CMOS I/O bit 0

Table 2–26. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 5)

Board Reference (J1)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
42	HSMA_D1	AH16	2.5-V CMOS	Dedicated CMOS I/O bit 1
43	HSMA_D2	AV13	2.5-V CMOS	Dedicated CMOS I/O bit 2
44	HSMA_D3	AW13	2.5-V CMOS	Dedicated CMOS I/O bit 3
47	HSMA_TX_D_P0	AV6	LVDS or 2.5-V	LVDS TX bit 0 or CMOS bit 4
48	HSMA_RX_D_P0	AW12	LVDS or 2.5-V	LVDS RX bit 0 or CMOS bit 5
49	HSMA_TX_D_N0	AV7	LVDS or 2.5-V	LVDS TX bit 0n or CMOS bit 6
50	HSMA_RX_D_N0	AV12	LVDS or 2.5-V	LVDS RX bit 0n or CMOS bit 7
53	HSMA_TX_D_P1	AU6	LVDS or 2.5-V	LVDS TX bit 1 or CMOS bit 8
54	HSMA_RX_D_P1	AR18	LVDS or 2.5-V	LVDS RX bit 1 or CMOS bit 9
55	HSMA_TX_D_N1	AT6	LVDS or 2.5-V	LVDS TX bit 1n or CMOS bit 10
56	HSMA_RX_D_N1	AP18	LVDS or 2.5-V	LVDS RX bit 1n or CMOS bit 11
59	HSMA_TX_D_P2	AU9	LVDS or 2.5-V	LVDS TX bit 2 or CMOS bit 12
60	HSMA_RX_D_P2	AU8	LVDS or 2.5-V	LVDS RX bit 2 or CMOS bit 13
61	HSMA_TX_D_N2	AT9	LVDS or 2.5-V	LVDS TX bit 2n or CMOS bit 14
62	HSMA_RX_D_N2	AU7	LVDS or 2.5-V	LVDS RX bit 2n or CMOS bit 15
65	HSMA_TX_D_P3	AV10	LVDS or 2.5-V	LVDS TX bit 3 or CMOS bit 16
66	HSMA_RX_D_P3	AW8	LVDS or 2.5-V	LVDS RX bit 3 or CMOS bit 17
67	HSMA_TX_D_N3	AU10	LVDS or 2.5-V	LVDS TX bit 3n or CMOS bit 18
68	HSMA_RX_D_N3	AW7	LVDS or 2.5-V	LVDS RX bit 3n or CMOS bit 19
71	HSMA_TX_D_P4	AU12	LVDS or 2.5-V	LVDS TX bit 4 or CMOS bit 20
72	HSMA_RX_D_P4	AW9	LVDS or 2.5-V	LVDS RX bit 4 or CMOS bit 21
73	HSMA_TX_D_N4	AT12	LVDS or 2.5-V	LVDS TX bit 4n or CMOS bit 22
74	HSMA_RX_D_N4	AV9	LVDS or 2.5-V	LVDS RX bit 4n or CMOS bit 23
77	HSMA_TX_D_P5	AP9	LVDS or 2.5-V	LVDS TX bit 5 or CMOS bit 24
78	HSMA_RX_D_P5	AU11	LVDS or 2.5-V	LVDS RX bit 5 or CMOS bit 25
79	HSMA_TX_D_N5	AN9	LVDS or 2.5-V	LVDS TX bit 5n or CMOS bit 26
80	HSMA_RX_D_N5	AT11	LVDS or 2.5-V	LVDS RX bit 5n or CMOS bit 27
83	HSMA_TX_D_P6	AP12	LVDS or 2.5-V	LVDS TX bit 6 or CMOS bit 28
84	HSMA_RX_D_P6	AR9	LVDS or 2.5-V	LVDS RX bit 6 or CMOS bit 29
85	HSMA_TX_D_N6	AN12	LVDS or 2.5-V	LVDS TX bit 6n or CMOS bit 30
86	HSMA_RX_D_N6	AT8	LVDS or 2.5-V	LVDS RX bit 6n or CMOS bit 31
89	HSMA_TX_D_P7	AM9	LVDS or 2.5-V	LVDS TX bit 7 or CMOS bit 32
90	HSMA_RX_D_P7	AW5	LVDS or 2.5-V	LVDS RX bit 7 or CMOS bit 33
91	HSMA_TX_D_N7	AL9	LVDS or 2.5-V	LVDS TX bit 7n or CMOS bit 34
92	HSMA_RX_D_N7	AW6	LVDS or 2.5-V	LVDS RX bit 7n or CMOS bit 35
95	HSMA_CLK_OUT_P1	AU13	LVDS or 2.5-V	LVDS or CMOS clock out 1 or CMOS bit 36
96	HSMA_CLK_IN_P1	AW4	LVDS or 2.5-V	LVDS or CMOS clock in 1 or CMOS bit 37
97	HSMA_CLK_OUT_N1	AT13	LVDS or 2.5-V	LVDS or CMOS clock out 1 or CMOS bit 38

Table 2–26. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 5)

Board Reference (J1)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
98	HSMA_CLK_IN_N1	AV4	LVDS or 2.5-V	LVDS or CMOS clock in 1 or CMOS bit 39
101	HSMA_TX_D_P8	AL8	LVDS or 2.5-V	LVDS TX bit 8 or CMOS bit 40
102	HSMA_RX_D_P8	AW11	LVDS or 2.5-V	LVDS RX bit 8 or CMOS bit 41
103	HSMA_TX_D_N8	AK8	LVDS or 2.5-V	LVDS TX bit 8n or CMOS bit 42
104	HSMA_RX_D_N8	AW10	LVDS or 2.5-V	LVDS RX bit 8n or CMOS bit 43
107	HSMA_TX_D_P9	AK10	LVDS or 2.5-V	LVDS TX bit 9 or CMOS bit 44
108	HSMA_RX_D_P9	AR10	LVDS or 2.5-V	LVDS RX bit 9 or CMOS bit 45
109	HSMA_TX_D_N9	AK9	LVDS or 2.5-V	LVDS TX bit 9n or CMOS bit 46
110	HSMA_RX_D_N9	AP10	LVDS or 2.5-V	LVDS RX bit 9n or CMOS bit 47
113	HSMA_TX_D_P10	AL11	LVDS or 2.5-V	LVDS TX bit 10 or CMOS bit 48
114	HSMA_RX_D_P10	AM10	LVDS or 2.5-V	LVDS RX bit 10 or CMOS bit 49
115	HSMA_TX_D_N10	AK11	LVDS or 2.5-V	LVDS TX bit 10n or CMOS bit 50
116	HSMA_RX_D_N10	AL10	LVDS or 2.5-V	LVDS RX bit 10n or CMOS bit 51
119	HSMA_TX_D_P11	AL12	LVDS or 2.5-V	LVDS TX bit 11 or CMOS bit 52
120	HSMA_RX_D_P11	AJ13	LVDS or 2.5-V	LVDS RX bit 11 or CMOS bit 53
121	HSMA_TX_D_N11	AK12	LVDS or 2.5-V	LVDS TX bit 11n or CMOS bit 54
122	HSMA_RX_D_N11	AH13	LVDS or 2.5-V	LVDS RX bit 11n or CMOS bit 55
125	HSMA_TX_D_P12	AM13	LVDS or 2.5-V	LVDS TX bit 12 or CMOS bit 56
126	HSMA_RX_D_P12	AH11	LVDS or 2.5-V	LVDS RX bit 12 or CMOS bit 57
127	HSMA_TX_D_N12	AL13	LVDS or 2.5-V	LVDS TX bit 12n or CMOS bit 58
128	HSMA_RX_D_N12	AG11	LVDS or 2.5-V	LVDS RX bit 12n or CMOS bit 59
131	HSMA_TX_D_P13	AE12	LVDS or 2.5-V	LVDS TX bit 13 or CMOS bit 60
132	HSMA_RX_D_P13	AG12	LVDS or 2.5-V	LVDS RX bit 13 or CMOS bit 61
133	HSMA_TX_D_N13	AD12	LVDS or 2.5-V	LVDS TX bit 13n or CMOS bit 62
134	HSMA_RX_D_N13	AF12	LVDS or 2.5-V	LVDS RX bit 13n or CMOS bit 63
137	HSMA_TX_D_P14	AD11	LVDS or 2.5-V	LVDS TX bit 14 or CMOS bit 64
138	HSMA_RX_D_P14	AD13	LVDS or 2.5-V	LVDS RX bit 14 or CMOS bit 65
139	HSMA_TX_D_N14	AC12	LVDS or 2.5-V	LVDS TX bit 14n or CMOS bit 66
140	HSMA_RX_D_N14	AC13	LVDS or 2.5-V	LVDS RX bit 14n or CMOS bit 67
143	HSMA_TX_D_P15	AR13	LVDS or 2.5-V	LVDS TX bit 15 or CMOS bit 68
144	HSMA_RX_D_P15	AE13	LVDS or 2.5-V	LVDS RX bit 15 or CMOS bit 69
145	HSMA_TX_D_N15	AP13	LVDS or 2.5-V	LVDS TX bit 15n or CMOS bit 70
146	HSMA_RX_D_N15	AE14	LVDS or 2.5-V	LVDS RX bit 15n or CMOS bit 71
149	HSMA_TX_D_P16	AJ12	LVDS or 2.5-V	LVDS TX bit 16 or CMOS bit 72
150	HSMA_RX_D_P16	AG13	LVDS or 2.5-V	LVDS RX bit 16 or CMOS bit 73
151	HSMA_TX_D_N16	AH12	LVDS or 2.5-V	LVDS TX bit 16n or CMOS bit 74
152	HSMA_RX_D_N16	AF13	LVDS or 2.5-V	LVDS RX bit 16n or CMOS bit 75
155	HSMA_CLK_OUT_P2	AM7	LVDS or 2.5-V	LVDS or CMOS clock out 2 or CMOS bit 76

Table 2–26. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 5 of 5)

Board Reference (J1)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
156	HSMA_CLK_IN_P2	AR6	LVDS or 2.5-V	LVDS or CMOS clock in 2 or CMOS bit 77
157	HSMA_CLK_OUT_N2	AL7	LVDS or 2.5-V	LVDS or CMOS clock out 2 or CMOS bit 78
158	HSMA_CLK_IN_N2	AP6	LVDS or 2.5-V	LVDS or CMOS clock in 2 or CMOS bit 79
160	HSMA_PSNTN	AW15	2.5-V CMOS	HSMC port A presence detect

Table 2–27 lists the HSMC port B interface pin assignments, signal names, and functions.

Table 2–27. HSMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 4)

Board Reference (J2)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
17	HSMB_TX_P3	AT3	1.5-V PCML	Transceiver TX bit 3
18	HSMB_RX_P3	AU1	1.5-V PCML	Transceiver RX bit 3
19	HSMB_TX_N3	AT4	1.5-V PCML	Transceiver TX bit 3n
20	HSMB_RX_N3	AU2	1.5-V PCML	Transceiver RX bit 3n
21	HSMB_TX_P2	AP3	1.5-V PCML	Transceiver TX bit 2
22	HSMB_RX_P2	AR1	1.5-V PCML	Transceiver RX bit 2
23	HSMB_TX_N2	AP4	1.5-V PCML	Transceiver TX bit 2n
24	HSMB_RX_N2	AR2	1.5-V PCML	Transceiver RX bit 2n
25	HSMB_TX_P1	AM3	1.5-V PCML	Transceiver TX bit 1
26	HSMB_RX_P1	AN1	1.5-V PCML	Transceiver RX bit 1
27	HSMB_TX_N1	AM4	1.5-V PCML	Transceiver TX bit 1n
28	HSMB_RX_N1	AN2	1.5-V PCML	Transceiver RX bit 1n
29	HSMB_TX_P0	AK3	1.5-V PCML	Transceiver TX bit 0
30	HSMB_RX_P0	AL1	1.5-V PCML	Transceiver RX bit 0
31	HSMB_TX_N0	AK4	1.5-V PCML	Transceiver TX bit 0n
32	HSMB_RX_N0	AL2	1.5-V PCML	Transceiver RX bit 0n
33	HSMB_SDA	AG25	2.5-V CMOS	Management serial data
34	HSMB_SCL	AH26	2.5-V CMOS	Management serial clock
35	JTAG_TCK	AV34	2.5-V CMOS	JTAG clock signal
36	HSMB_JTAG_TMS	—	2.5-V CMOS	JTAG mode select signal
37	HSMB_JTAG_TDO	—	2.5-V CMOS	JTAG data output
38	HSMB_JTAG_TDI	—	2.5-V CMOS	JTAG data input
39	HSMB_CLK_OUT0	AJ33	LVDS or 2.5-V	Dedicated CMOS clock out
40	HSMB_CLK_IN0	AR6	LVDS or 2.5-V	Dedicated CMOS clock in
41	HSMB_D0	AW25	2.5-V CMOS	Dedicated CMOS I/O bit 0
42	HSMB_D1	AW26	2.5-V CMOS	Dedicated CMOS I/O bit 1
43	HSMB_D2	AV25	2.5-V CMOS	Dedicated CMOS I/O bit 2
44	HSMB_D3	AV24	2.5-V CMOS	Dedicated CMOS I/O bit 3

Table 2–27. HSMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 4)

Board Reference (J2)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
47	HSMB_TX_D_P0	AC29	LVDS or 2.5-V	LVDS TX bit 0 or CMOS bit 4
48	HSMB_RX_D_P0	AC25	LVDS or 2.5-V	LVDS RX bit 0 or CMOS bit 5
49	HSMB_TX_D_N0	AB29	LVDS or 2.5-V	LVDS TX bit 0n or CMOS bit 6
50	HSMB_RX_D_N0	AB25	LVDS or 2.5-V	LVDS RX bit 0n or CMOS bit 7
53	HSMB_TX_D_P1	AE28	LVDS or 2.5-V	LVDS TX bit 1 or CMOS bit 8
54	HSMB_RX_D_P1	AF25	LVDS or 2.5-V	LVDS RX bit 1 or CMOS bit 9
55	HSMB_TX_D_N1	AD28	LVDS or 2.5-V	LVDS TX bit 1n or CMOS bit 10
56	HSMB_RX_D_N1	AE25	LVDS or 2.5-V	LVDS RX bit 1n or CMOS bit 11
59	HSMB_TX_D_P2	AE29	LVDS or 2.5-V	LVDS TX bit 2 or CMOS bit 12
60	HSMB_RX_D_P2	AD27	LVDS or 2.5-V	LVDS RX bit 2 or CMOS bit 13
61	HSMB_TX_D_N2	AD29	LVDS or 2.5-V	LVDS TX bit 2n or CMOS bit 14
62	HSMB_RX_D_N2	AC27	LVDS or 2.5-V	LVDS RX bit 2n or CMOS bit 15
65	HSMB_TX_D_P3	AK27	LVDS or 2.5-V	LVDS TX bit 3 or CMOS bit 16
66	HSMB_RX_D_P3	AB28	LVDS or 2.5-V	LVDS RX bit 3 or CMOS bit 17
67	HSMB_TX_D_N3	AJ27	LVDS or 2.5-V	LVDS TX bit 3n or CMOS bit 18
68	HSMB_RX_D_N3	AB27	LVDS or 2.5-V	LVDS RX bit 3n or CMOS bit 19
71	HSMB_TX_D_P4	AL29	LVDS or 2.5-V	LVDS TX bit 4 or CMOS bit 20
72	HSMB_RX_D_P4	AJ28	LVDS or 2.5-V	LVDS RX bit 4 or CMOS bit 21
73	HSMB_TX_D_N4	AK29	LVDS or 2.5-V	LVDS TX bit 4n or CMOS bit 22
74	HSMB_RX_D_N4	AH28	LVDS or 2.5-V	LVDS RX bit 4n or CMOS bit 23
77	HSMB_TX_D_P5	AL30	LVDS or 2.5-V	LVDS TX bit 5 or CMOS bit 24
78	HSMB_RX_D_P5	AG28	LVDS or 2.5-V	LVDS RX bit 5 or CMOS bit 25
79	HSMB_TX_D_N5	AK30	LVDS or 2.5-V	LVDS TX bit 5n or CMOS bit 26
80	HSMB_RX_D_N5	AF28	LVDS or 2.5-V	LVDS RX bit 5n or CMOS bit 27
83	HSMB_TX_D_P6	AL32	LVDS or 2.5-V	LVDS TX bit 6 or CMOS bit 28
84	HSMB_RX_D_P6	AH30	LVDS or 2.5-V	LVDS RX bit 6 or CMOS bit 29
85	HSMB_TX_D_N6	AK32	LVDS or 2.5-V	LVDS TX bit 6n or CMOS bit 30
86	HSMB_RX_D_N6	AG30	LVDS or 2.5-V	LVDS RX bit 6n or CMOS bit 31
89	HSMB_TX_D_P7	AM31	LVDS or 2.5-V	LVDS TX bit 7 or CMOS bit 32
90	HSMB_RX_D_P7	AP29	LVDS or 2.5-V	LVDS RX bit 7 or CMOS bit 33
91	HSMB_TX_D_N7	AL31	LVDS or 2.5-V	LVDS TX bit 7n or CMOS bit 34
92	HSMB_RX_D_N7	AN29	LVDS or 2.5-V	LVDS RX bit 7n or CMOS bit 35
95	HSMB_CLK_OUT_P1	AM34	LVDS or 2.5-V	LVDS or CMOS clock out 1 or CMOS bit 36
96	HSMB_CLK_IN_P1	AM33	LVDS or 2.5-V	LVDS or CMOS clock in 1 or CMOS bit 37
97	HSMB_CLK_OUT_N1	AL34	LVDS or 2.5-V	LVDS or CMOS clock out 1 or CMOS bit 38
98	HSMB_CLK_IN_N1	AL33	LVDS or 2.5-V	LVDS or CMOS clock in 1 or CMOS bit 39
101	HSMB_TX_D_P8	AN27	LVDS or 2.5-V	LVDS TX bit 8 or CMOS bit 40
102	HSMB_RX_D_P8	AU29	LVDS or 2.5-V	LVDS RX bit 8 or CMOS bit 41

Table 2–27. HSMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 4)

Board Reference (J2)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
103	HSMB_TX_D_N8	AM27	LVDS or 2.5-V	LVDS TX bit 8n or CMOS bit 42
104	HSMB_RX_D_N8	AT29	LVDS or 2.5-V	LVDS RX bit 8n or CMOS bit 43
107	HSMB_TX_D_P9	AP30	LVDS or 2.5-V	LVDS TX bit 9 or CMOS bit 44
108	HSMB_RX_D_P9	AW31	LVDS or 2.5-V	LVDS RX bit 9 or CMOS bit 45
109	HSMB_TX_D_N9	AN30	LVDS or 2.5-V	LVDS TX bit 9n or CMOS bit 46
110	HSMB_RX_D_N9	AW30	LVDS or 2.5-V	LVDS RX bit 9n or CMOS bit 47
113	HSMB_TX_D_P10	AR28	LVDS or 2.5-V	LVDS TX bit 10 or CMOS bit 48
114	HSMB_RX_D_P10	AW28	LVDS or 2.5-V	LVDS RX bit 10 or CMOS bit 49
115	HSMB_TX_D_N10	AP28	LVDS or 2.5-V	LVDS TX bit 10n or CMOS bit 50
116	HSMB_RX_D_N10	AW29	LVDS or 2.5-V	LVDS RX bit 10n or CMOS bit 51
119	HSMB_TX_D_P11	AV30	LVDS or 2.5-V	LVDS TX bit 11 or CMOS bit 52
120	HSMB_RX_D_P11	AU27	LVDS or 2.5-V	LVDS RX bit 11 or CMOS bit 53
121	HSMB_TX_D_N11	AU30	LVDS or 2.5-V	LVDS TX bit 11n or CMOS bit 54
122	HSMB_RX_D_N11	AT27	LVDS or 2.5-V	LVDS RX bit 11n or CMOS bit 55
125	HSMB_TX_D_P12	AV31	LVDS or 2.5-V	LVDS TX bit 12 or CMOS bit 56
126	HSMB_RX_D_P12	AW27	LVDS or 2.5-V	LVDS RX bit 12 or CMOS bit 57
127	HSMB_TX_D_N12	AU31	LVDS or 2.5-V	LVDS TX bit 12n or CMOS bit 58
128	HSMB_RX_D_N12	AV27	LVDS or 2.5-V	LVDS RX bit 12n or CMOS bit 59
131	HSMB_TX_D_P13	AR27	LVDS or 2.5-V	LVDS TX bit 13 or CMOS bit 60
132	HSMB_RX_D_P13	AW32	LVDS or 2.5-V	LVDS RX bit 13 or CMOS bit 61
133	HSMB_TX_D_N13	AP27	LVDS or 2.5-V	LVDS TX bit 13n or CMOS bit 62
134	HSMB_RX_D_N13	AW33	LVDS or 2.5-V	LVDS RX bit 13n or CMOS bit 63
137	HSMB_TX_D_P14	AP31	LVDS or 2.5-V	LVDS TX bit 14 or CMOS bit 64
138	HSMB_RX_D_P14	AT31	LVDS or 2.5-V	LVDS RX bit 14 or CMOS bit 65
139	HSMB_TX_D_N14	AN31	LVDS or 2.5-V	LVDS TX bit 14n or CMOS bit 66
140	HSMB_RX_D_N14	AR31	LVDS or 2.5-V	LVDS RX bit 14n or CMOS bit 67
143	HSMB_TX_D_P15	AP32	LVDS or 2.5-V	LVDS TX bit 15 or CMOS bit 68
144	HSMB_RX_D_P15	AV28	LVDS or 2.5-V	LVDS RX bit 15 or CMOS bit 69
145	HSMB_TX_D_N15	AN32	LVDS or 2.5-V	LVDS TX bit 15n or CMOS bit 70
146	HSMB_RX_D_N15	AU28	LVDS or 2.5-V	LVDS RX bit 15n or CMOS bit 71
149	HSMB_TX_D_P16	AP33	LVDS or 2.5-V	LVDS TX bit 16 or CMOS bit 72
150	HSMB_RX_D_P16	AT30	LVDS or 2.5-V	LVDS RX bit 16 or CMOS bit 73
151	HSMB_TX_D_N16	AN33	LVDS or 2.5-V	LVDS TX bit 16n or CMOS bit 74
152	HSMB_RX_D_N16	AR30	LVDS or 2.5-V	LVDS RX bit 16n or CMOS bit 75
155	HSMB_CLK_OUT_P2	AE26	LVDS or 2.5-V	LVDS or CMOS clock out 2 or CMOS bit 76
156	HSMB_CLK_IN_P2	AU32	LVDS or 2.5-V	LVDS or CMOS clock in 2 or CMOS bit 77
157	HSMB_CLK_OUT_N2	AD26	LVDS or 2.5-V	LVDS or CMOS clock out 2 or CMOS bit 78

Table 2–27. HSMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 4)

Board Reference (J2)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
158	HSMB_CLK_IN_N2	AT32	LVDS or 2.5-V	LVDS or CMOS clock in 2 or CMOS bit 79
160	HSMB_PRSNTN	AT24	2.5-V CMOS	HSMC port B presence detect

SFP+ Modules

The development board include two SFP+ modules that use transceiver channels from the FPGA. These modules takes in serial data from the FPGA and transform them into optical signals. Both SFP+ ports are active and include the SFP+ cage assembly only when the Arria V GT FPGA device is installed.

☞ The Arria V GX FPGA development board includes only one SFP+ cage assembly for the SFP+ port used by the device.

Table 2–28 list the SFP+ modules interface pin assignments, signal names, and functions.

Table 2–28. SFP+ Modules Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 2)

Board Reference	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
SFP+ Module (J10)				
6	SFP_MOD_ABS1	AK16	3.3-V LVTTL	Module present indicator
8	SFP_OP_RX_LOS1	AN19	3.3-V LVTTL	Signal present indicator
2	SFP_OP_TX_FLT1	AG17	3.3-V LVTTL	Transmitter fault indicator
12	SFP_RX_N1	Y38	3.3-V LVTTL	Receiver data
13	SFP_RX_P1	Y39	3.3-V LVTTL	Receiver data
5	SFP_SCL1	AL18	3.3-V LVTTL	Serial 2-wire clock
4	SFP_SDA1	AC16	3.3-V LVTTL	Serial 2-wire data
3	SFP_TX_DIS1	AN15	3.3-V LVTTL	Drive low to disable transmitter
19	SFP_TX_N1	W36	3.3-V LVTTL	Transmitter data
18	SFP_TX_P1	W37	3.3-V LVTTL	Transmitter data
7	SFP_TX_RS01	AN14	3.3-V LVTTL	Reserved
9	SFP_TX_RS11	AE15	3.3-V LVTTL	Reserved
SFP+ Module (J15)				
6	SFP_MOD_ABS2	AT16	3.3-V LVTTL	Module present indicator
8	SFP_OP_RX_LOS2	AH17	3.3-V LVTTL	Signal present indicator
2	SFP_OP_TX_FLT2	AM18	3.3-V LVTTL	Transmitter fault indicator
12	SFP_RX_N2	K38	3.3-V LVTTL	Receiver data
13	SFP_RX_P2	K39	3.3-V LVTTL	Receiver data
5	SFP_SCL2	AD16	3.3-V LVTTL	Serial 2-wire clock
4	SFP_SDA2	AP15	3.3-V LVTTL	Serial 2-wire data
3	SFP_TX_DIS2	AD15	3.3-V LVTTL	Drive low to disable transmitter

Table 2–28. SFP+ Modules Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 2)

Board Reference	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
19	SFP_TX_N2	J36	3.3-V LVTTL	Transmitter data
18	SFP_TX_P2	J37	3.3-V LVTTL	Transmitter data
7	SFP_TX_RS02	AP14	3.3-V LVTTL	Reserved
9	SFP_TX_RS12	AN7	3.3-V LVTTL	Reserved

FMC Connector

The development board contains a high pin count (HPC) FPGA mezzanine card (FMC) connector that functions with a quadrature amplitude modulation (QAM) digital-to-analog converter (DAC) FMC module or daughter card. This pinout satisfies a QAM DAC that requires 58 LVDS data output pairs, one LVDS input clock pair, and three low-voltage differential signaling (LVDS) control pairs from the Arria V. These pins also have the option to be used as single-ended I/O pins. The VCCIO supply for the FMC A banks in the low pin count (LPC) and HPC provide a variable voltage of 1.5 V, 1.8 V, 2.5 V (default), or 3.3 V. The VCCIO supply for the FMC B bank in the HPC provides a variable voltage from 1.2 V to 3.3 V, which can be supplied by the FMC module. However, for the sake of device safety concerns, a jumper is available for you to connect this bank to the same VCCIO used for the FMC A banks. This allows the VCCIO pins on the FPGA to be tied to a known power. The VCCIO pins also allows you the option to perform a manual check for the module's input voltage before connecting to the FPGA. This is to ensure that the module does not exceed the power supply maximum voltage rating.

Table 2–29 lists the FMC connector pin assignments, signal names, and functions.

Table 2–29. FMC Connector Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 7)

Board Reference (J10)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
D1	FMC_C2M_PG	—	2.5-V CMOS	Power good output
K4	FMC_CLK_BIDIR_P2	AE23	2.5-V CMOS	Clock input or output 2
K5	FMC_CLK_BIDIR_N2	AD22	2.5-V CMOS	Clock input or output 2
J2	FMC_CLK_BIDIR_P3	AU22	2.5-V CMOS	Clock input or output 3
J3	FMC_CLK_BIDIR_N3	AT22	2.5-V CMOS	Clock input or output 3
B1	FMC_CLK_DIR	AW21	2.5-V CMOS	Clock direction select for FMC_CLK_BIDIR
H4	FMC_CLK_M2C_P0	AV19	2.5-V CMOS	Clock input 0
H5	FMC_CLK_M2C_N0	AU19	2.5-V CMOS	Clock input 0
G2	FMC_CLK_M2C_P1	AF21	2.5-V CMOS	Clock input 1
G3	FMC_CLK_M2C_N1	AE21	2.5-V CMOS	Clock input 1
C3	FMC_DP_C2M_N0	AD4	2.5-V CMOS	Transmit channel
A23	FMC_DP_C2M_N1	Y4	2.5-V CMOS	Transmit channel
A27	FMC_DP_C2M_N2	T4	2.5-V CMOS	Transmit channel
A31	FMC_DP_C2M_N3	P4	2.5-V CMOS	Transmit channel
A35	FMC_DP_C2M_N4	H4	2.5-V CMOS	Transmit channel

Table 2–29. FMC Connector Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 7)

Board Reference (J10)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
A39	FMC_DP_C2M_N5	M4	2.5-V CMOS	Transmit channel (available in Arria V GT FPGA device)
B37	FMC_DP_C2M_N6	K4	2.5-V CMOS	Transmit channel (available in Arria V GT FPGA device)
B33	FMC_DP_C2M_N7	F4	2.5-V CMOS	Transmit channel (available in Arria V GT FPGA device)
B29	FMC_DP_C2M_N8	D4	2.5-V CMOS	Transmit channel (available in Arria V GT FPGA device)
B25	FMC_DP_C2M_N9	B4	2.5-V CMOS	Transmit channel (available in Arria V GT FPGA device)
C2	FMC_DP_C2M_P0	AD3	2.5-V CMOS	Transmit channel
A22	FMC_DP_C2M_P1	Y3	2.5-V CMOS	Transmit channel
A26	FMC_DP_C2M_P2	T3	2.5-V CMOS	Transmit channel
A30	FMC_DP_C2M_P3	P3	2.5-V CMOS	Transmit channel
A34	FMC_DP_C2M_P4	H3	2.5-V CMOS	Transmit channel
A38	FMC_DP_C2M_P5	M3	2.5-V CMOS	Transmit channel (available in Arria V GT FPGA device)
B36	FMC_DP_C2M_P6	K3	2.5-V CMOS	Transmit channel (available in Arria V GT FPGA device)
B32	FMC_DP_C2M_P7	F3	2.5-V CMOS	Transmit channel (available in Arria V GT FPGA device)
B28	FMC_DP_C2M_P8	D3	2.5-V CMOS	Transmit channel (available in Arria V GT FPGA device)
B24	FMC_DP_C2M_P9	B3	2.5-V CMOS	Transmit channel (available in Arria V GT FPGA device)
C7	FMC_DP_M2C_N0	AE2	2.5-V CMOS	Transmit channel
A3	FMC_DP_M2C_N1	AA2	2.5-V CMOS	Transmit channel
A7	FMC_DP_M2C_N2	U2	2.5-V CMOS	Transmit channel
A11	FMC_DP_M2C_N3	R2	2.5-V CMOS	Transmit channel
A15	FMC_DP_M2C_N4	J2	2.5-V CMOS	Transmit channel
A19	FMC_DP_M2C_N5	N2	2.5-V CMOS	Transmit channel (available in Arria V GT FPGA device)
B17	FMC_DP_M2C_N6	L2	2.5-V CMOS	Transmit channel (available in Arria V GT FPGA device)
B13	FMC_DP_M2C_N7	G2	2.5-V CMOS	Transmit channel (available in Arria V GT FPGA device)
B9	FMC_DP_M2C_N8	E2	2.5-V CMOS	Transmit channel (available in Arria V GT FPGA device)
B5	FMC_DP_M2C_N9	C2	2.5-V CMOS	Transmit channel (available in Arria V GT FPGA device)
C6	FMC_DP_M2C_P0	AE1	2.5-V CMOS	Transmit channel
A2	FMC_DP_M2C_P1	AA1	2.5-V CMOS	Transmit channel
A6	FMC_DP_M2C_P2	U1	2.5-V CMOS	Transmit channel
A10	FMC_DP_M2C_P3	R1	2.5-V CMOS	Transmit channel
A14	FMC_DP_M2C_P4	J1	2.5-V CMOS	Transmit channel
A18	FMC_DP_M2C_P5	N1	2.5-V CMOS	Transmit channel (available in Arria V GT FPGA device)
B16	FMC_DP_M2C_P6	L1	2.5-V CMOS	Transmit channel (available in Arria V GT FPGA device)
B12	FMC_DP_M2C_P7	G1	2.5-V CMOS	Transmit channel (available in Arria V GT FPGA device)
B8	FMC_DP_M2C_P8	E1	2.5-V CMOS	Transmit channel (available in Arria V GT FPGA device)
B4	FMC_DP_M2C_P9	C1	2.5-V CMOS	Transmit channel (available in Arria V GT FPGA device)
D4	FMC_GBTCLK_M2C_P0	AB9	2.5-V CMOS	Transceiver reference clock 0
D5	FMC_GBTCLK_M2C_N0	AB8	2.5-V CMOS	Transceiver reference clock 0
B20	FMC_GBTCLK_M2C_P1	—	2.5-V CMOS	Transceiver reference clock 1

Table 2–29. FMC Connector Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 7)

Board Reference (J10)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
B21	FMC_GBTCLK_M2C_N1	—	2.5-V CMOS	Transceiver reference clock 1
F5	FMC_HA_N0	AG16	2.5-V CMOS	FMC data bus HPC bank A
E3	FMC_HA_N1	AE17	2.5-V CMOS	FMC data bus HPC bank A
K8	FMC_HA_N2	AU16	2.5-V CMOS	FMC data bus HPC bank A
J7	FMC_HA_N3	AN17	2.5-V CMOS	FMC data bus HPC bank A
F8	FMC_HA_N4	AK9	2.5-V CMOS	FMC data bus HPC bank A
E7	FMC_HA_N5	AK11	2.5-V CMOS	FMC data bus HPC bank A
K11	FMC_HA_N6	K8	2.5-V CMOS	FMC data bus HPC bank A
J10	FMC_HA_N7	AG14	2.5-V CMOS	FMC data bus HPC bank A
F11	FMC_HA_N8	AC19	2.5-V CMOS	FMC data bus HPC bank A
E10	FMC_HA_N9	AL7	2.5-V CMOS	FMC data bus HPC bank A
K14	FMC_HA_N10	G6	2.5-V CMOS	FMC data bus HPC bank A
J13	FMC_HA_N11	AD17	2.5-V CMOS	FMC data bus HPC bank A
F14	FMC_HA_N12	AH18	2.5-V CMOS	FMC data bus HPC bank A
E13	FMC_HA_N13	AE19	2.5-V CMOS	FMC data bus HPC bank A
J16	FMC_HA_N14	AC15	2.5-V CMOS	FMC data bus HPC bank A
F17	FMC_HA_N15	AG20	2.5-V CMOS	FMC data bus HPC bank A
E16	FMC_HA_N16	AK17	2.5-V CMOS	FMC data bus HPC bank A
K17	FMC_HA_N17	AR25	2.5-V CMOS	FMC data bus HPC bank A
J19	FMC_HA_N18	AN20	2.5-V CMOS	FMC data bus HPC bank A
F20	FMC_HA_N19	AN19	2.5-V CMOS	FMC data bus HPC bank A
E19	FMC_HA_N20	AM21	2.5-V CMOS	FMC data bus HPC bank A
K20	FMC_HA_N21	AN23	2.5-V CMOS	FMC data bus HPC bank A
J22	FMC_HA_N22	AN22	2.5-V CMOS	FMC data bus HPC bank A
K23	FMC_HA_N23	AN24	2.5-V CMOS	FMC data bus HPC bank A
F4	FMC_HA_P0	AH16	2.5-V CMOS	FMC data bus HPC bank A
E2	FMC_HA_P1	AF16	2.5-V CMOS	FMC data bus HPC bank A
K7	FMC_HA_P2	AV16	2.5-V CMOS	FMC data bus HPC bank A
J6	FMC_HA_P3	AP17	2.5-V CMOS	FMC data bus HPC bank A
F7	FMC_HA_P4	AK10	2.5-V CMOS	FMC data bus HPC bank A
E6	FMC_HA_P5	AL11	2.5-V CMOS	FMC data bus HPC bank A
K10	FMC_HA_P6	J8	2.5-V CMOS	FMC data bus HPC bank A
J9	FMC_HA_P7	AH14	2.5-V CMOS	FMC data bus HPC bank A
F10	FMC_HA_P8	AD19	2.5-V CMOS	FMC data bus HPC bank A
E9	FMC_HA_P9	AM7	2.5-V CMOS	FMC data bus HPC bank A
K13	FMC_HA_P10	F6	2.5-V CMOS	FMC data bus HPC bank A
J12	FMC_HA_P11	AC18	2.5-V CMOS	FMC data bus HPC bank A
F13	FMC_HA_P12	AJ18	2.5-V CMOS	FMC data bus HPC bank A

Table 2–29. FMC Connector Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 7)

Board Reference (J10)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
E12	FMC_HA_P13	AF19	2.5-V CMOS	FMC data bus HPC bank A
J15	FMC_HA_P14	AD14	2.5-V CMOS	FMC data bus HPC bank A
F16	FMC_HA_P15	AH20	2.5-V CMOS	FMC data bus HPC bank A
E15	FMC_HA_P16	AL17	2.5-V CMOS	FMC data bus HPC bank A
K16	FMC_HA_P17	AT25	2.5-V CMOS	FMC data bus HPC bank A
J18	FMC_HA_P18	AP20	2.5-V CMOS	FMC data bus HPC bank A
F19	FMC_HA_P19	AP19	2.5-V CMOS	FMC data bus HPC bank A
E18	FMC_HA_P20	AN21	2.5-V CMOS	FMC data bus HPC bank A
K19	FMC_HA_P21	AP23	2.5-V CMOS	FMC data bus HPC bank A
J21	FMC_HA_P22	AP22	2.5-V CMOS	FMC data bus HPC bank A
K22	FMC_HA_P23	AP24	2.5-V CMOS	FMC data bus HPC bank A
K26	FMC_HB_N0	AH13	2.5-V CMOS	FMC data bus HPC bank B
J25	FMC_HB_N1	AV12	2.5-V CMOS	FMC data bus HPC bank B
F23	FMC_HB_N2	AT11	2.5-V CMOS	FMC data bus HPC bank B
E22	FMC_HB_N3	AW10	2.5-V CMOS	FMC data bus HPC bank B
F26	FMC_HB_N4	AF13	2.5-V CMOS	FMC data bus HPC bank B
E25	FMC_HB_N5	AE14	2.5-V CMOS	FMC data bus HPC bank B
K29	FMC_HB_N6	AF12	2.5-V CMOS	FMC data bus HPC bank B
J28	FMC_HB_N7	AG11	2.5-V CMOS	FMC data bus HPC bank B
F29	FMC_HB_N8	AP10	2.5-V CMOS	FMC data bus HPC bank B
E28	FMC_HB_N9	AL10	2.5-V CMOS	FMC data bus HPC bank B
K32	FMC_HB_N10	AC13	2.5-V CMOS	FMC data bus HPC bank B
J31	FMC_HB_N11	AV9	2.5-V CMOS	FMC data bus HPC bank B
F32	FMC_HB_N12	AU10	2.5-V CMOS	FMC data bus HPC bank B
E31	FMC_HB_N13	AT9	2.5-V CMOS	FMC data bus HPC bank B
K35	FMC_HB_N14	AP13	2.5-V CMOS	FMC data bus HPC bank B
J34	FMC_HB_N15	AH12	2.5-V CMOS	FMC data bus HPC bank B
F35	FMC_HB_N16	AN12	2.5-V CMOS	FMC data bus HPC bank B
K38	FMC_HB_N17	AC12	2.5-V CMOS	FMC data bus HPC bank B
J37	FMC_HB_N18	AD12	2.5-V CMOS	FMC data bus HPC bank B
E34	FMC_HB_N19	AT12	2.5-V CMOS	FMC data bus HPC bank B
F38	FMC_HB_N20	AK12	2.5-V CMOS	FMC data bus HPC bank B
E37	FMC_HB_N21	AL13	2.5-V CMOS	FMC data bus HPC bank B
K25	FMC_HB_P0	AJ13	2.5-V CMOS	FMC data bus HPC bank B
J24	FMC_HB_P1	AW12	2.5-V CMOS	FMC data bus HPC bank B
F22	FMC_HB_P2	AU11	2.5-V CMOS	FMC data bus HPC bank B
E21	FMC_HB_P3	AW11	2.5-V CMOS	FMC data bus HPC bank B
F25	FMC_HB_P4	AG13	2.5-V CMOS	FMC data bus HPC bank B

Table 2–29. FMC Connector Pin Assignments, Schematic Signal Names, and Functions (Part 5 of 7)

Board Reference (J10)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
E24	FMC_HB_P5	AE13	2.5-V CMOS	FMC data bus HPC bank B
K28	FMC_HB_P6	AG12	2.5-V CMOS	FMC data bus HPC bank B
J27	FMC_HB_P7	AH11	2.5-V CMOS	FMC data bus HPC bank B
F28	FMC_HB_P8	AR10	2.5-V CMOS	FMC data bus HPC bank B
E27	FMC_HB_P9	AM10	2.5-V CMOS	FMC data bus HPC bank B
K31	FMC_HB_P10	AD13	2.5-V CMOS	FMC data bus HPC bank B
J30	FMC_HB_P11	AW9	2.5-V CMOS	FMC data bus HPC bank B
F31	FMC_HB_P12	AV10	2.5-V CMOS	FMC data bus HPC bank B
E30	FMC_HB_P13	AU9	2.5-V CMOS	FMC data bus HPC bank B
K34	FMC_HB_P14	AR13	2.5-V CMOS	FMC data bus HPC bank B
J33	FMC_HB_P15	AJ12	2.5-V CMOS	FMC data bus HPC bank B
F34	FMC_HB_P16	AP12	2.5-V CMOS	FMC data bus HPC bank B
K37	FMC_HB_P17	AD11	2.5-V CMOS	FMC data bus HPC bank B
J36	FMC_HB_P18	AE12	2.5-V CMOS	FMC data bus HPC bank B
E33	FMC_HB_P19	AU12	2.5-V CMOS	FMC data bus HPC bank B
F37	FMC_HB_P20	AL12	2.5-V CMOS	FMC data bus HPC bank B
E36	FMC_HB_P21	AM13	2.5-V CMOS	FMC data bus HPC bank B
D30	FMC_JTAG_TDI	—	2.5-V CMOS	JTAG data in
D31	FMC_JTAG_TDO	—	2.5-V CMOS	JTAG data out
D33	FMC_JTAG_TMS	—	2.5-V CMOS	JTAG mode select
G7	FMC_LA_N0	AN16	2.5-V CMOS	FMC data bus LPC bank A
D9	FMC_LA_N1	AV13	2.5-V CMOS	FMC data bus LPC bank A
H8	FMC_LA_N2	AT15	2.5-V CMOS	FMC data bus LPC bank A
G10	FMC_LA_N3	AW14	2.5-V CMOS	FMC data bus LPC bank A
H11	FMC_LA_N4	AK8	2.5-V CMOS	FMC data bus LPC bank A
D12	FMC_LA_N5	AN7	2.5-V CMOS	FMC data bus LPC bank A
C11	FMC_LA_N6	AL9	2.5-V CMOS	FMC data bus LPC bank A
H14	FMC_LA_N7	AU6	2.5-V CMOS	FMC data bus LPC bank A
G13	FMC_LA_N8	AN9	2.5-V CMOS	FMC data bus LPC bank A
D15	FMC_LA_N9	AG17	2.5-V CMOS	FMC data bus LPC bank A
C15	FMC_LA_N10	AV7	2.5-V CMOS	FMC data bus LPC bank A
H17	FMC_LA_N11	AK15	2.5-V CMOS	FMC data bus LPC bank A
G16	FMC_LA_N12	AJ16	2.5-V CMOS	FMC data bus LPC bank A
D18	FMC_LA_N13	AK14	2.5-V CMOS	FMC data bus LPC bank A
C19	FMC_LA_N14	AT13	2.5-V CMOS	FMC data bus LPC bank A
H20	FMC_LA_N15	AL16	2.5-V CMOS	FMC data bus LPC bank A
G19	FMC_LA_N16	AK24	2.5-V CMOS	FMC data bus LPC bank A
D21	FMC_LA_N17	AN15	2.5-V CMOS	FMC data bus LPC bank A

Table 2–29. FMC Connector Pin Assignments, Schematic Signal Names, and Functions (Part 6 of 7)

Board Reference (J10)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
C23	FMC_LA_N18	AC16	2.5-V CMOS	FMC data bus LPC bank A
H23	FMC_LA_N19	AV22	2.5-V CMOS	FMC data bus LPC bank A
G22	FMC_LA_N20	AR16	2.5-V CMOS	FMC data bus LPC bank A
H26	FMC_LA_N21	AG22	2.5-V CMOS	FMC data bus LPC bank A
G25	FMC_LA_N22	AD21	2.5-V CMOS	FMC data bus LPC bank A
D24	FMC_LA_N23	AV18	2.5-V CMOS	FMC data bus LPC bank A
H29	FMC_LA_N24	AJ25	2.5-V CMOS	FMC data bus LPC bank A
G28	FMC_LA_N25	AK23	2.5-V CMOS	FMC data bus LPC bank A
D27	FMC_LA_N26	AK22	2.5-V CMOS	FMC data bus LPC bank A
C27	FMC_LA_N27	AG23	2.5-V CMOS	FMC data bus LPC bank A
H32	FMC_LA_N28	AG24	2.5-V CMOS	FMC data bus LPC bank A
G31	FMC_LA_N29	AN26	2.5-V CMOS	FMC data bus LPC bank A
H35	FMC_LA_N30	AE27	2.5-V CMOS	FMC data bus LPC bank A
G34	FMC_LA_N31	AG27	2.5-V CMOS	FMC data bus LPC bank A
H38	FMC_LA_N32	AD23	2.5-V CMOS	FMC data bus LPC bank A
G37	FMC_LA_N33	AC24	2.5-V CMOS	FMC data bus LPC bank A
G6	FMC_LA_P0	AP16	2.5-V CMOS	FMC data bus LPC bank A
D8	FMC_LA_P1	AW13	2.5-V CMOS	FMC data bus LPC bank A
H7	FMC_LA_P2	AU15	2.5-V CMOS	FMC data bus LPC bank A
G9	FMC_LA_P3	AW15	2.5-V CMOS	FMC data bus LPC bank A
H10	FMC_LA_P4	AL8	2.5-V CMOS	FMC data bus LPC bank A
D11	FMC_LA_P5	AP7	2.5-V CMOS	FMC data bus LPC bank A
C10	FMC_LA_P6	AM9	2.5-V CMOS	FMC data bus LPC bank A
H13	FMC_LA_P7	AT6	2.5-V CMOS	FMC data bus LPC bank A
G12	FMC_LA_P8	AP9	2.5-V CMOS	FMC data bus LPC bank A
D14	FMC_LA_P9	AH17	2.5-V CMOS	FMC data bus LPC bank A
C14	FMC_LA_P10	AV6	2.5-V CMOS	FMC data bus LPC bank A
H16	FMC_LA_P11	AL15	2.5-V CMOS	FMC data bus LPC bank A
G15	FMC_LA_P12	AK16	2.5-V CMOS	FMC data bus LPC bank A
D17	FMC_LA_P13	AL14	2.5-V CMOS	FMC data bus LPC bank A
C18	FMC_LA_P14	AU13	2.5-V CMOS	FMC data bus LPC bank A
H19	FMC_LA_P15	AM16	2.5-V CMOS	FMC data bus LPC bank A
G18	FMC_LA_P16	AL24	2.5-V CMOS	FMC data bus LPC bank A
D20	FMC_LA_P17	AP15	2.5-V CMOS	FMC data bus LPC bank A
C22	FMC_LA_P18	AD16	2.5-V CMOS	FMC data bus LPC bank A
H22	FMC_LA_P19	AW22	2.5-V CMOS	FMC data bus LPC bank A
G21	FMC_LA_P20	AT16	2.5-V CMOS	FMC data bus LPC bank A
H25	FMC_LA_P21	AH22	2.5-V CMOS	FMC data bus LPC bank A

Table 2–29. FMC Connector Pin Assignments, Schematic Signal Names, and Functions (Part 7 of 7)

Board Reference (J10)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
G24	FMC_LA_P22	AC22	2.5-V CMOS	FMC data bus LPC bank A
D23	FMC_LA_P23	AW18	2.5-V CMOS	FMC data bus LPC bank A
H28	FMC_LA_P24	AK25	2.5-V CMOS	FMC data bus LPC bank A
G27	FMC_LA_P25	AL23	2.5-V CMOS	FMC data bus LPC bank A
D26	FMC_LA_P26	AL22	2.5-V CMOS	FMC data bus LPC bank A
C26	FMC_LA_P27	AH23	2.5-V CMOS	FMC data bus LPC bank A
H31	FMC_LA_P28	AH24	2.5-V CMOS	FMC data bus LPC bank A
G30	FMC_LA_P29	AP26	2.5-V CMOS	FMC data bus LPC bank A
H34	FMC_LA_P30	AF27	2.5-V CMOS	FMC data bus LPC bank A
G33	FMC_LA_P31	AH27	2.5-V CMOS	FMC data bus LPC bank A
H37	FMC_LA_P32	AD24	2.5-V CMOS	FMC data bus LPC bank A
G36	FMC_LA_P33	AD25	2.5-V CMOS	FMC data bus LPC bank A
F1	FMC_M2C_PG	—	2.5-V CMOS	Power good input
H2	FMC_PRSNT	—	2.5-V CMOS	FMC module present
C30	FMC_SCL	—	2.5-V CMOS	Management serial clock line
C31	FMC_SDA	—	2.5-V CMOS	Management serial data line

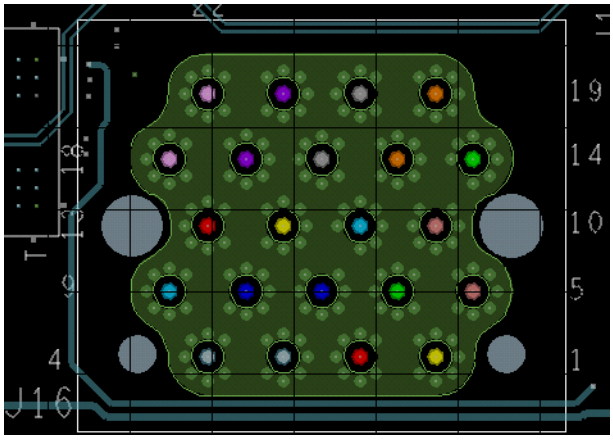
Bull's Eye Connector

The development board comes with Samtec's Bull's Eye system, which includes four SMA cables along with the insertion tool to insert the cables into the connector.

The Bull's Eye high-density RF interconnect system allows many channels to be compacted into a small area on a printed circuit board at a comparable performance to SMA connectors. The cables allow you to monitor only two differential signals at a time. You can move the cables from one channel to another using the tool included with this board.

Figure 2–11 shows a diagram of the color coded Bull's Eye connections. Follow the color code to make loopback connections. For example, connect purple to purple (pins 17 to 21) for RX to TX loopback. The only pins not connected are pins 3 and 4.

Figure 2–11. Bull's Eye Connections



You can order more cables from www.samtec.com and these cable systems can be reused on other boards.

For specific instructions on how to install the connector to the board and insert the cables into the connector, refer to Samtec's web page regarding this system.

Table 2–30 lists the Bull's eye connector pin assignments, signal names, and functions.

Table 2–30. Bull's Eye Connector Pin Assignments, Schematic Signal Names, and Functions

Board Reference (J16)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
4	BULLSEYE_SMA_CLKN	—	LVDS or 2.5-V	Clock buffer
3	BULLSEYE_SMA_CLKP	—	LVDS or 2.5-V	Clock buffer
21	SMA_A_10G_RX_N0	G2	LVDS or 2.5-V	Transceiver channel
2	SMA_A_10G_RX_N1	H38	LVDS or 2.5-V	Transceiver channel
22	SMA_A_10G_RX_P0	G1	LVDS or 2.5-V	Transceiver channel
1	SMA_A_10G_RX_P1	H39	LVDS or 2.5-V	Transceiver channel
7	SMA_A_6G_RX_N2	C2	LVDS or 2.5-V	Transceiver channel
11	SMA_A_6G_RX_P2	C1	LVDS or 2.5-V	Transceiver channel
13	SMA_A_TX_L15_N	G36	LVDS or 2.5-V	Transceiver channel
12	SMA_A_TX_L15_P	G37	LVDS or 2.5-V	Transceiver channel
17	SMA_A_TX_R16_N	F4	LVDS or 2.5-V	Transceiver channel
18	SMA_A_TX_R16_P	F3	LVDS or 2.5-V	Transceiver channel
8	SMA_A_TX_R17_N	B4	LVDS or 2.5-V	Transceiver channel
9	SMA_A_TX_R17_P	B3	LVDS or 2.5-V	Transceiver channel
15	SMA_B_10G_RX_N1	H38	LVDS or 2.5-V	Transceiver channel

Table 2–30. Bull's Eye Connector Pin Assignments, Schematic Signal Names, and Functions

Board Reference (J16)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
16	SMA_B_10G_RX_P1	H39	LVDS or 2.5-V	Transceiver channel
5	SMA_B_6G_RX_N0	AC2	LVDS or 2.5-V	Transceiver channel
6	SMA_B_6G_RX_P0	AC1	LVDS or 2.5-V	Transceiver channel
19	SMA_B_TX_L15_N	G36	LVDS or 2.5-V	Transceiver channel
20	SMA_B_TX_L15_P	G37	LVDS or 2.5-V	Transceiver channel
10	SMA_B_TX_R6_N	AB4	LVDS or 2.5-V	Transceiver channel
14	SMA_B_TX_R6_P	AB3	LVDS or 2.5-V	Transceiver channel

Memory

This section describes the development board's memory interface support and also their signal names, types, and connectivity relative to the Arria V GT FPGA. The development board has the following memory interfaces:

- DDR3
- QDRII+
- Flash

For more information about the memory interfaces, refer to the following documents:

- *Timing Analysis* section in volume 4 of the External Memory Interface Handbook.
- *DDR, DDR2, and DDR3 SDRAM Design Tutorials* section in volume 6 of the External Memory Interface Handbook.

DDR3

DDR3A for FPGA 1

The development board supports a 16Mx72x8 bank DDR3 SDRAM interface on FPGA 1 for very high-speed sequential memory access. The 72-bit data bus consists of four x16 devices and one x8 device with a single address or command bus. This interface connects to the vertical I/O banks on the top edge of the FPGA and utilizes the memory soft controller.

This memory interface is designed to run at a target frequency of 667 MHz for a maximum theoretical bandwidth of over 115.2 Gbps. The minimum frequency for this device is 667 MHz. The target Micron device is rated at 800 MHz with a CAS latency of 11.

Table 2–31 lists the DDR3A (x72 soft controller) pin assignments, signal names, and functions. The signal names and types are relative to the Arria V GT FPGA in terms of I/O setting and direction.

Table 2–31. DDR3A Devices Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 5)

Board Reference	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
DDR3A (U11, U18, U21, U28)				
N3	DDR3A_A0	M34	1.5-V SSTL Class I	Address bus
P7	DDR3A_A1	H25	1.5-V SSTL Class I	Address bus
P3	DDR3A_A2	F32	1.5-V SSTL Class I	Address bus
N2	DDR3A_A3	P28	1.5-V SSTL Class I	Address bus
P8	DDR3A_A4	L24	1.5-V SSTL Class I	Address bus
P2	DDR3A_A5	G32	1.5-V SSTL Class I	Address bus
R8	DDR3A_A6	R21	1.5-V SSTL Class I	Address bus
R2	DDR3A_A7	K30	1.5-V SSTL Class I	Address bus
T8	DDR3A_A8	D21	1.5-V SSTL Class I	Address bus
R3	DDR3A_A9	M30	1.5-V SSTL Class I	Address bus
L7	DDR3A_A10	J28	1.5-V SSTL Class I	Address bus
R7	DDR3A_A11	M21	1.5-V SSTL Class I	Address bus
N7	DDR3A_A12	G28	1.5-V SSTL Class I	Address bus
T3	DDR3A_A13	M31	1.5-V SSTL Class I	Address bus
M2	DDR3A_BA0	G30	1.5-V SSTL Class I	Bank address bus
N8	DDR3A_BA1	T24	1.5-V SSTL Class I	Bank address bus
M3	DDR3A_BA2	K34	1.5-V SSTL Class I	Bank address bus
K3	DDR3A_CASN	D32	1.5-V SSTL Class I	Row address select
K9	DDR3A_CKE	K29	1.5-V SSTL Class I	Column address select
K7	DDR3A_CLK_N	F34	1.5-V SSTL Class I	Differential output clock
J7	DDR3A_CLK_P	E34	1.5-V SSTL Class I	Differential output clock
L2	DDR3A_CSN	F31	1.5-V SSTL Class I	Chip select
K1	DDR3A_ODT	E33	1.5-V SSTL Class I	On-die termination enable
J3	DDR3A_RASN	A32	1.5-V SSTL Class I	Row address select
T2	DDR3A_RESETN	J31	1.5-V SSTL Class I	Reset
L3	DDR3A_WEN	G29	1.5-V SSTL Class I	Write enable
DDR3A (U7)				
K3	DDR3A_A0	M34	1.5-V SSTL Class I	Address bus
L7	DDR3A_A1	H25	1.5-V SSTL Class I	Address bus
L3	DDR3A_A2	F32	1.5-V SSTL Class I	Address bus
K2	DDR3A_A3	P28	1.5-V SSTL Class I	Address bus
L8	DDR3A_A4	L24	1.5-V SSTL Class I	Address bus
L2	DDR3A_A5	G32	1.5-V SSTL Class I	Address bus
M8	DDR3A_A6	R21	1.5-V SSTL Class I	Address bus

Table 2–31. DDR3A Devices Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 5)

Board Reference	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
M2	DDR3A_A7	K30	1.5-V SSTL Class I	Address bus
N8	DDR3A_A8	D21	1.5-V SSTL Class I	Address bus
M3	DDR3A_A9	M30	1.5-V SSTL Class I	Address bus
H7	DDR3A_A10	J28	1.5-V SSTL Class I	Address bus
M7	DDR3A_A11	M21	1.5-V SSTL Class I	Address bus
K7	DDR3A_A12	G28	1.5-V SSTL Class I	Address bus
N3	DDR3A_A13	M31	1.5-V SSTL Class I	Address bus
J2	DDR3A_BA0	G30	1.5-V SSTL Class I	Bank address bus
K8	DDR3A_BA1	T24	1.5-V SSTL Class I	Bank address bus
J3	DDR3A_BA2	K34	1.5-V SSTL Class I	Bank address bus
G3	DDR3A_CASN	D32	1.5-V SSTL Class I	Row address select
G9	DDR3A_CKE	K29	1.5-V SSTL Class I	Column address select
G7	DDR3A_CLK_N	F34	1.5-V SSTL Class I	Differential output clock
F7	DDR3A_CLK_P	E34	1.5-V SSTL Class I	Differential output clock
H2	DDR3A_CSN	F31	1.5-V SSTL Class I	Chip select
B7	DDR3A_DM8	P22	1.5-V SSTL Class I	Write mask byte lane
B3	DDR3A_DQ64	B22	1.5-V SSTL Class I	Data bus byte lane
C7	DDR3A_DQ65	L22	1.5-V SSTL Class I	Data bus byte lane
C2	DDR3A_DQ66	C22	1.5-V SSTL Class I	Data bus byte lane
C8	DDR3A_DQ67	N22	1.5-V SSTL Class I	Data bus byte lane
E3	DDR3A_DQ68	E22	1.5-V SSTL Class I	Data bus byte lane
E8	DDR3A_DQ69	J22	1.5-V SSTL Class I	Data bus byte lane
D2	DDR3A_DQ70	A23	1.5-V SSTL Class I	Data bus byte lane
E7	DDR3A_DQ71	F22	1.5-V SSTL Class I	Data bus byte lane
D3	DDR3A_DQS_N8	D23	1.5-V SSTL Class I	Data strobe N byte lane
C3	DDR3A_DQS_P8	C23	1.5-V SSTL Class I	Data strobe P byte lane
G1	DDR3A_ODT	E33	1.5-V SSTL Class I	On-die termination enable
F3	DDR3A_RASN	A32	1.5-V SSTL Class I	Row address select
N2	DDR3A_RESETN	J31	1.5-V SSTL Class I	Reset
H3	DDR3A_WEN	G29	1.5-V SSTL Class I	Write enable
H8	DDR3A_ZQ05	—	1.5-V SSTL Class I	ZQ impedance calibration
DDR3A (U11)				
E7	DDR3A_DM6	M32	1.5-V SSTL Class I	Write mask byte lane
D3	DDR3A_DM7	D31	1.5-V SSTL Class I	Write mask byte lane
E3	DDR3A_DQ48	T26	1.5-V SSTL Class I	Data bus byte lane
F7	DDR3A_DQ49	R24	1.5-V SSTL Class I	Data bus byte lane
F2	DDR3A_DQ50	D25	1.5-V SSTL Class I	Data bus byte lane
F8	DDR3A_DQ51	T25	1.5-V SSTL Class I	Data bus byte lane
H3	DDR3A_DQ52	E25	1.5-V SSTL Class I	Data bus byte lane

Table 2–31. DDR3A Devices Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 5)

Board Reference	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
H8	DDR3A_DQ53	N24	1.5-V SSTL Class I	Data bus byte lane
G2	DDR3A_DQ54	G25	1.5-V SSTL Class I	Data bus byte lane
H7	DDR3A_DQ55	K24	1.5-V SSTL Class I	Data bus byte lane
D7	DDR3A_DQ56	F23	1.5-V SSTL Class I	Data bus byte lane
C3	DDR3A_DQ57	J23	1.5-V SSTL Class I	Data bus byte lane
C8	DDR3A_DQ58	G23	1.5-V SSTL Class I	Data bus byte lane
C2	DDR3A_DQ59	C24	1.5-V SSTL Class I	Data bus byte lane
A7	DDR3A_DQ60	F24	1.5-V SSTL Class I	Data bus byte lane
A2	DDR3A_DQ61	R23	1.5-V SSTL Class I	Data bus byte lane
B8	DDR3A_DQ62	G24	1.5-V SSTL Class I	Data bus byte lane
A3	DDR3A_DQ63	M23	1.5-V SSTL Class I	Data bus byte lane
G3	DDR3A_DQS_N6	B25	1.5-V SSTL Class I	Data strobe N byte lane
B7	DDR3A_DQS_N7	E24	1.5-V SSTL Class I	Data strobe N byte lane
F3	DDR3A_DQS_P6	A25	1.5-V SSTL Class I	Data strobe P byte lane
C7	DDR3A_DQS_P7	D24	1.5-V SSTL Class I	Data strobe P byte lane
L8	DDR3A_ZQ04	—	1.5-V SSTL Class I	ZQ impedance calibration
DDR3A (U18)				
E7	DDR3A_DM4	E27	1.5-V SSTL Class I	Write mask byte lane
D3	DDR3A_DM5	A26	1.5-V SSTL Class I	Write mask byte lane
E3	DDR3A_DQ32	P27	1.5-V SSTL Class I	Data bus byte lane
F7	DDR3A_DQ33	B27	1.5-V SSTL Class I	Data bus byte lane
F2	DDR3A_DQ34	R27	1.5-V SSTL Class I	Data bus byte lane
F8	DDR3A_DQ35	C27	1.5-V SSTL Class I	Data bus byte lane
H3	DDR3A_DQ36	M27	1.5-V SSTL Class I	Data bus byte lane
H8	DDR3A_DQ37	H27	1.5-V SSTL Class I	Data bus byte lane
G2	DDR3A_DQ38	N27	1.5-V SSTL Class I	Data bus byte lane
H7	DDR3A_DQ39	K27	1.5-V SSTL Class I	Data bus byte lane
D7	DDR3A_DQ40	J26	1.5-V SSTL Class I	Data bus byte lane
C3	DDR3A_DQ41	D26	1.5-V SSTL Class I	Data bus byte lane
C8	DDR3A_DQ42	K25	1.5-V SSTL Class I	Data bus byte lane
C2	DDR3A_DQ43	G26	1.5-V SSTL Class I	Data bus byte lane
A7	DDR3A_DQ44	T27	1.5-V SSTL Class I	Data bus byte lane
A2	DDR3A_DQ45	F26	1.5-V SSTL Class I	Data bus byte lane
B8	DDR3A_DQ46	R26	1.5-V SSTL Class I	Data bus byte lane
A3	DDR3A_DQ47	C26	1.5-V SSTL Class I	Data bus byte lane
G3	DDR3A_DQS_N4	T28	1.5-V SSTL Class I	Data strobe N byte lane
B7	DDR3A_DQS_N5	N26	1.5-V SSTL Class I	Data strobe N byte lane
F3	DDR3A_DQS_P4	R28	1.5-V SSTL Class I	Data strobe P byte lane
C7	DDR3A_DQS_P5	M26	1.5-V SSTL Class I	Data strobe P byte lane

Table 2–31. DDR3A Devices Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 5)

Board Reference	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
L8	DDR3A_ZQ03	—	1.5-V SSTL Class I	ZQ impedance calibration
DDR3A (U21)				
E7	DDR3A_DM2	M32	1.5-V SSTL Class I	Write mask byte lane
D3	DDR3A_DM3	D31	1.5-V SSTL Class I	Write mask byte lane
E3	DDR3A_DQ16	D30	1.5-V SSTL Class I	Data bus byte lane
F7	DDR3A_DQ17	C29	1.5-V SSTL Class I	Data bus byte lane
F2	DDR3A_DQ18	R30	1.5-V SSTL Class I	Data bus byte lane
F8	DDR3A_DQ19	A29	1.5-V SSTL Class I	Data bus byte lane
H3	DDR3A_DQ20	L30	1.5-V SSTL Class I	Data bus byte lane
H8	DDR3A_DQ21	A28	1.5-V SSTL Class I	Data bus byte lane
G2	DDR3A_DQ22	J30	1.5-V SSTL Class I	Data bus byte lane
H7	DDR3A_DQ23	B28	1.5-V SSTL Class I	Data bus byte lane
D7	DDR3A_DQ24	J29	1.5-V SSTL Class I	Data bus byte lane
C3	DDR3A_DQ25	C28	1.5-V SSTL Class I	Data bus byte lane
C8	DDR3A_DQ26	L28	1.5-V SSTL Class I	Data bus byte lane
C2	DDR3A_DQ27	F28	1.5-V SSTL Class I	Data bus byte lane
A7	DDR3A_DQ28	N29	1.5-V SSTL Class I	Data bus byte lane
A2	DDR3A_DQ29	D28	1.5-V SSTL Class I	Data bus byte lane
B8	DDR3A_DQ30	M29	1.5-V SSTL Class I	Data bus byte lane
A3	DDR3A_DQ31	M28	1.5-V SSTL Class I	Data bus byte lane
G3	DDR3A_DQS_N2	P30	1.5-V SSTL Class I	Data strobe N byte lane
B7	DDR3A_DQS_N3	T29	1.5-V SSTL Class I	Data strobe N byte lane
F3	DDR3A_DQS_P2	N30	1.5-V SSTL Class I	Data strobe P byte lane
C7	DDR3A_DQS_P3	R29	1.5-V SSTL Class I	Data strobe P byte lane
L8	DDR3A_ZQ01	—	1.5-V SSTL Class I	ZQ impedance calibration
DDR3A (U28)				
E7	DDR3A_DM0	M32	1.5-V SSTL Class I	Write mask byte lane
D3	DDR3A_DM1	D31	1.5-V SSTL Class I	Write mask byte lane
E3	DDR3A_DQ0	N33	1.5-V SSTL Class I	Data bus byte lane
F7	DDR3A_DQ1	N31	1.5-V SSTL Class I	Data bus byte lane
F2	DDR3A_DQ2	N34	1.5-V SSTL Class I	Data bus byte lane
F8	DDR3A_DQ3	L31	1.5-V SSTL Class I	Data bus byte lane
H3	DDR3A_DQ4	N32	1.5-V SSTL Class I	Data bus byte lane
H8	DDR3A_DQ5	J34	1.5-V SSTL Class I	Data bus byte lane
G2	DDR3A_DQ6	P31	1.5-V SSTL Class I	Data bus byte lane
H7	DDR3A_DQ7	J32	1.5-V SSTL Class I	Data bus byte lane
D7	DDR3A_DQ8	A30	1.5-V SSTL Class I	Data bus byte lane
C3	DDR3A_DQ9	C30	1.5-V SSTL Class I	Data bus byte lane
C8	DDR3A_DQ10	B30	1.5-V SSTL Class I	Data bus byte lane

Table 2–31. DDR3A Devices Pin Assignments, Schematic Signal Names, and Functions (Part 5 of 5)

Board Reference	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
C2	DDR3A_DQ11	H31	1.5-V SSTL Class I	Data bus byte lane
A7	DDR3A_DQ12	B31	1.5-V SSTL Class I	Data bus byte lane
A2	DDR3A_DQ13	E31	1.5-V SSTL Class I	Data bus byte lane
B8	DDR3A_DQ14	A31	1.5-V SSTL Class I	Data bus byte lane
A3	DDR3A_DQ15	C31	1.5-V SSTL Class I	Data bus byte lane
G3	DDR3A_DQS_N0	M33	1.5-V SSTL Class I	Data strobe N byte lane
B7	DDR3A_DQS_N1	B33	1.5-V SSTL Class I	Data strobe N byte lane
F3	DDR3A_DQS_P0	L33	1.5-V SSTL Class I	Data strobe P byte lane
C7	DDR3A_DQS_P1	N30	1.5-V SSTL Class I	Data strobe P byte lane
L8	DDR3A_ZQ01	—	1.5-V SSTL Class I	ZQ impedance calibration

DDR3B/C for FPGA 2

The development board supports a 16Mx64x8 bank DDR3 SDRAM interface on FPGA 2 for very high-speed sequential memory access. The 64-bit data bus consists of four x16 devices with a single address or command bus. This interface connects to the vertical I/O banks on the top edge of the FPGA.

This DDR3 SDRAM has two interface options. The first option is a x32 interface using a memory hard controller. The second option is a x64 interface using a memory soft controller.

Table 2–32 lists the DDR3B (x32 hard controller) pin assignments, signal names, and functions. The signal names and types are relative to the Arria V GT FPGA in terms of I/O setting and direction.

Table 2–32. DDR3 x32 Devices Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 3)

Board Reference	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
DDR3B (U6, U12)				
N3	DDR3B_A0	B31	1.5-V SSTL Class I	Address bus
P7	DDR3B_A1	A30	1.5-V SSTL Class I	Address bus
P3	DDR3B_A2	A31	1.5-V SSTL Class I	Address bus
N2	DDR3B_A3	A32	1.5-V SSTL Class I	Address bus
P8	DDR3B_A4	A33	1.5-V SSTL Class I	Address bus
P2	DDR3B_A5	B33	1.5-V SSTL Class I	Address bus
R8	DDR3B_A6	H31	1.5-V SSTL Class I	Address bus
R2	DDR3B_A7	J31	1.5-V SSTL Class I	Address bus
T8	DDR3B_A8	C31	1.5-V SSTL Class I	Address bus
R3	DDR3B_A9	D31	1.5-V SSTL Class I	Address bus
L7	DDR3B_A10	C32	1.5-V SSTL Class I	Address bus
R7	DDR3B_A11	D32	1.5-V SSTL Class I	Address bus
N7	DDR3B_A12	N31	1.5-V SSTL Class I	Address bus

Table 2–32. DDR3 x32 Devices Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 3)

Board Reference	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
T3	DDR3B_A13	P31	1.5-V SSTL Class I	Address bus
M2	DDR3B_BA0	M32	1.5-V SSTL Class I	Bank address bus
N8	DDR3B_BA1	N32	1.5-V SSTL Class I	Bank address bus
M3	DDR3B_BA2	J34	1.5-V SSTL Class I	Bank address bus
K3	DDR3B_CASN	L33	1.5-V SSTL Class I	Row address select
K9	DDR3B_CKE	E31	1.5-V SSTL Class I	Column address select
K7	DDR3B_CLK_N	C30	1.5-V SSTL Class I	Differential output clock
J7	DDR3B_CLK_P	B30	1.5-V SSTL Class I	Differential output clock
L2	DDR3B_CSN	L34	1.5-V SSTL Class I	Chip select
K1	DDR3B_ODT	L31	1.5-V SSTL Class I	On-die termination enable
J3	DDR3B_RASN	K34	1.5-V SSTL Class I	Row address select
T2	DDR3B_RESETN	G30	1.5-V SSTL Class I	Reset
L3	DDR3B_WEN	M33	1.5-V SSTL Class I	Write enable
L8	DDR3B_ZQ2	—	1.5-V SSTL Class I	ZQ impedance calibration
DDR3B (U6)				
E7	DDR3B_DM0	J30	1.5-V SSTL Class I	Write mask byte lane
D3	DDR3B_DM1	J29	1.5-V SSTL Class I	Write mask byte lane
E3	DDR3B_DQ0	B28	1.5-V SSTL Class I	Data bus byte lane
F7	DDR3B_DQ1	C29	1.5-V SSTL Class I	Data bus byte lane
F2	DDR3B_DQ2	R30	1.5-V SSTL Class I	Data bus byte lane
F8	DDR3B_DQ3	A29	1.5-V SSTL Class I	Data bus byte lane
H3	DDR3B_DQ4	A28	1.5-V SSTL Class I	Data bus byte lane
H8	DDR3B_DQ5	L30	1.5-V SSTL Class I	Data bus byte lane
G2	DDR3B_DQ6	D30	1.5-V SSTL Class I	Data bus byte lane
H7	DDR3B_DQ7	D29	1.5-V SSTL Class I	Data bus byte lane
D7	DDR3B_DQ8	L28	1.5-V SSTL Class I	Data bus byte lane
C3	DDR3B_DQ9	M28	1.5-V SSTL Class I	Data bus byte lane
C8	DDR3B_DQ10	H28	1.5-V SSTL Class I	Data bus byte lane
C2	DDR3B_DQ11	C28	1.5-V SSTL Class I	Data bus byte lane
A7	DDR3B_DQ12	D28	1.5-V SSTL Class I	Data bus byte lane
A2	DDR3B_DQ13	F28	1.5-V SSTL Class I	Data bus byte lane
B8	DDR3B_DQ14	M29	1.5-V SSTL Class I	Data bus byte lane
A3	DDR3B_DQ15	N29	1.5-V SSTL Class I	Data bus byte lane
G3	DDR3B_DQS_N0	P30	1.5-V SSTL Class I	Data strobe N byte lane
B7	DDR3B_DQS_N1	T29	1.5-V SSTL Class I	Data strobe N byte lane
F3	DDR3B_DQS_P0	N30	1.5-V SSTL Class I	Data strobe P byte lane
C7	DDR3B_DQS_P1	R29	1.5-V SSTL Class I	Data strobe P byte lane
DDR3B (U12)				
E7	DDR3B_DM2	J30	1.5-V SSTL Class I	Write mask byte lane

Table 2–32. DDR3 x32 Devices Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 3)

Board Reference	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
D3	DDR3B_DM3	J29	1.5-V SSTL Class I	Write mask byte lane
E3	DDR3B_DQ16	P27	1.5-V SSTL Class I	Data bus byte lane
F7	DDR3B_DQ17	R27	1.5-V SSTL Class I	Data bus byte lane
F2	DDR3B_DQ18	H27	1.5-V SSTL Class I	Data bus byte lane
F8	DDR3B_DQ19	B27	1.5-V SSTL Class I	Data bus byte lane
H3	DDR3B_DQ20	C27	1.5-V SSTL Class I	Data bus byte lane
H8	DDR3B_DQ21	E27	1.5-V SSTL Class I	Data bus byte lane
G2	DDR3B_DQ22	M27	1.5-V SSTL Class I	Data bus byte lane
H7	DDR3B_DQ23	N27	1.5-V SSTL Class I	Data bus byte lane
D7	DDR3B_DQ24	C26	1.5-V SSTL Class I	Data bus byte lane
C3	DDR3B_DQ25	D26	1.5-V SSTL Class I	Data bus byte lane
C8	DDR3B_DQ26	K25	1.5-V SSTL Class I	Data bus byte lane
C2	DDR3B_DQ27	R26	1.5-V SSTL Class I	Data bus byte lane
A7	DDR3B_DQ28	T27	1.5-V SSTL Class I	Data bus byte lane
A2	DDR3B_DQ29	A26	1.5-V SSTL Class I	Data bus byte lane
B8	DDR3B_DQ30	F26	1.5-V SSTL Class I	Data bus byte lane
A3	DDR3B_DQ31	G26	1.5-V SSTL Class I	Data bus byte lane
G3	DDR3B_DQS_N2	T28	1.5-V SSTL Class I	Data strobe N byte lane
B7	DDR3B_DQS_N3	N26	1.5-V SSTL Class I	Data strobe N byte lane
F3	DDR3B_DQS_P2	R28	1.5-V SSTL Class I	Data strobe P byte lane
C7	DDR3B_DQS_P3	M26	1.5-V SSTL Class I	Data strobe P byte lane

Table 2–33 lists the DDR3C (x64 soft controller) pin assignments, signal names, and functions. The signal names and types are relative to the Arria V GT FPGA in terms of I/O setting and direction.

Table 2–33. DDR3 x64 Devices Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 3)

Board Reference	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
DDR3C (U19, U22)				
N3	DDR3B_A0	B31	1.5-V SSTL Class I	Address bus
P7	DDR3B_A1	A30	1.5-V SSTL Class I	Address bus
P3	DDR3B_A2	A31	1.5-V SSTL Class I	Address bus
N2	DDR3B_A3	A32	1.5-V SSTL Class I	Address bus
P8	DDR3B_A4	A33	1.5-V SSTL Class I	Address bus
P2	DDR3B_A5	B33	1.5-V SSTL Class I	Address bus
R8	DDR3B_A6	H31	1.5-V SSTL Class I	Address bus
R2	DDR3B_A7	J31	1.5-V SSTL Class I	Address bus
T8	DDR3B_A8	C31	1.5-V SSTL Class I	Address bus
R3	DDR3B_A9	D31	1.5-V SSTL Class I	Address bus

Table 2–33. DDR3 x64 Devices Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 3)

Board Reference	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
L7	DDR3B_A10	C32	1.5-V SSTL Class I	Address bus
R7	DDR3B_A11	D32	1.5-V SSTL Class I	Address bus
N7	DDR3B_A12	N31	1.5-V SSTL Class I	Address bus
T3	DDR3B_A13	P31	1.5-V SSTL Class I	Address bus
M2	DDR3B_BA0	M32	1.5-V SSTL Class I	Bank address bus
N8	DDR3B_BA1	N32	1.5-V SSTL Class I	Bank address bus
M3	DDR3B_BA2	J34	1.5-V SSTL Class I	Bank address bus
K3	DDR3B_CASN	L33	1.5-V SSTL Class I	Row address select
K9	DDR3B_CKE	E31	1.5-V SSTL Class I	Column address select
K7	DDR3B_CLK_N	C30	1.5-V SSTL Class I	Differential output clock
J7	DDR3B_CLK_P	B30	1.5-V SSTL Class I	Differential output clock
L2	DDR3B_CSN	L34	1.5-V SSTL Class I	Chip select
K1	DDR3B_ODT	L31	1.5-V SSTL Class I	On-die termination enable
J3	DDR3B_RASN	K34	1.5-V SSTL Class I	Row address select
T2	DDR3B_RESETN	G30	1.5-V SSTL Class I	Reset
L3	DDR3B_WEN	M33	1.5-V SSTL Class I	Write enable
DDR3C (U19)				
E7	DDR3C_DM0	M21	1.5-V SSTL Class I	Write mask byte lane
D3	DDR3C_DM1	B22	1.5-V SSTL Class I	Write mask byte lane
E3	DDR3C_DQ0	D20	1.5-V SSTL Class I	Data bus byte lane
F7	DDR3C_DQ1	H21	1.5-V SSTL Class I	Data bus byte lane
F2	DDR3C_DQ2	D21	1.5-V SSTL Class I	Data bus byte lane
F8	DDR3C_DQ3	J21	1.5-V SSTL Class I	Data bus byte lane
H3	DDR3C_DQ4	A21	1.5-V SSTL Class I	Data bus byte lane
H8	DDR3C_DQ5	G21	1.5-V SSTL Class I	Data bus byte lane
G2	DDR3C_DQ6	A22	1.5-V SSTL Class I	Data bus byte lane
H7	DDR3C_DQ7	C20	1.5-V SSTL Class I	Data bus byte lane
D7	DDR3C_DQ8	A23	1.5-V SSTL Class I	Data bus byte lane
C3	DDR3C_DQ9	E22	1.5-V SSTL Class I	Data bus byte lane
C8	DDR3C_DQ10	L22	1.5-V SSTL Class I	Data bus byte lane
C2	DDR3C_DQ11	C22	1.5-V SSTL Class I	Data bus byte lane
A7	DDR3C_DQ12	N22	1.5-V SSTL Class I	Data bus byte lane
A2	DDR3C_DQ13	F22	1.5-V SSTL Class I	Data bus byte lane
B8	DDR3C_DQ14	P22	1.5-V SSTL Class I	Data bus byte lane
A3	DDR3C_DQ15	J22	1.5-V SSTL Class I	Data bus byte lane
G3	DDR3C_DQS_N0	B21	1.5-V SSTL Class I	Data strobe N byte lane
B7	DDR3C_DQS_N1	D23	1.5-V SSTL Class I	Data strobe N byte lane
F3	DDR3C_DQS_P0	A20	1.5-V SSTL Class I	Data strobe P byte lane
C7	DDR3C_DQS_P1	C23	1.5-V SSTL Class I	Data strobe P byte lane

Table 2–33. DDR3 x64 Devices Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 3)

Board Reference	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
L8	DDR3B_ZQ4	—	1.5-V SSTL Class I	ZQ impedance calibration
DDR3C (U22)				
E7	DDR3C_DM2	J23	1.5-V SSTL Class I	Write mask byte lane
D3	DDR3C_DM3	D25	1.5-V SSTL Class I	Write mask byte lane
E3	DDR3C_DQ16	C24	1.5-V SSTL Class I	Data bus byte lane
F7	DDR3C_DQ17	M23	1.5-V SSTL Class I	Data bus byte lane
F2	DDR3C_DQ18	B24	1.5-V SSTL Class I	Data bus byte lane
F8	DDR3C_DQ19	R23	1.5-V SSTL Class I	Data bus byte lane
H3	DDR3C_DQ20	G24	1.5-V SSTL Class I	Data bus byte lane
H8	DDR3C_DQ21	G23	1.5-V SSTL Class I	Data bus byte lane
G2	DDR3C_DQ22	F24	1.5-V SSTL Class I	Data bus byte lane
H7	DDR3C_DQ23	F23	1.5-V SSTL Class I	Data bus byte lane
D7	DDR3C_DQ24	R24	1.5-V SSTL Class I	Data bus byte lane
C3	DDR3C_DQ25	G25	1.5-V SSTL Class I	Data bus byte lane
C8	DDR3C_DQ26	T26	1.5-V SSTL Class I	Data bus byte lane
C2	DDR3C_DQ27	E25	1.5-V SSTL Class I	Data bus byte lane
A7	DDR3C_DQ28	N24	1.5-V SSTL Class I	Data bus byte lane
A2	DDR3C_DQ29	K24	1.5-V SSTL Class I	Data bus byte lane
B8	DDR3C_DQ30	T25	1.5-V SSTL Class I	Data bus byte lane
A3	DDR3C_DQ31	P24	1.5-V SSTL Class I	Data bus byte lane
G3	DDR3C_DQS_N2	E24	1.5-V SSTL Class I	Data strobe N byte lane
B7	DDR3C_DQS_N3	B25	1.5-V SSTL Class I	Data strobe N byte lane
F3	DDR3C_DQS_P2	D24	1.5-V SSTL Class I	Data strobe P byte lane
C7	DDR3C_DQS_P3	A25	1.5-V SSTL Class I	Data strobe P byte lane
L8	DDR3B_ZQ3	—	1.5-V SSTL Class I	ZQ impedance calibration

QDRII+

The development board supports a burst-of-4 QDRII+ SRAM memory device for very-high-speed, low-latency memory access. The QDRII+ has a x36 interface, providing device addressing of up to a 36 Mb.

The QDRII+ has separate read and write data ports with DDR signaling at up to 550 MHz. The pinout and footprint is compatible with a burst-of-2 QDRII SSRAM memory device. The FPGA can support up to 400 MHz QDRII data.

Table 2–34 lists the QDRII+ pin assignments, signal names, and functions.

Table 2–34. QDRII+ Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 3)

Board Reference (U8)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
R9	QDRII_A0	AB29	1.8-V HSTL	Address bus
R8	QDRII_A1	AC29	1.8-V HSTL	Address bus
B4	QDRII_A2	AF28	1.8-V HSTL	Address bus
B8	QDRII_A3	AG28	1.8-V HSTL	Address bus
C5	QDRII_A4	AK29	1.8-V HSTL	Address bus
C7	QDRII_A5	AL29	1.8-V HSTL	Address bus
N5	QDRII_A6	AH28	1.8-V HSTL	Address bus
N6	QDRII_A7	AJ28	1.8-V HSTL	Address bus
N7	QDRII_A8	AD28	1.8-V HSTL	Address bus
P4	QDRII_A9	AP28	1.8-V HSTL	Address bus
P5	QDRII_A10	AJ27	1.8-V HSTL	Address bus
P7	QDRII_A11	AP27	1.8-V HSTL	Address bus
P8	QDRII_A12	AM27	1.8-V HSTL	Address bus
R3	QDRII_A13	AG27	1.8-V HSTL	Address bus
R4	QDRII_A14	AE27	1.8-V HSTL	Address bus
R5	QDRII_A15	AC24	1.8-V HSTL	Address bus
R7	QDRII_A16	AD26	1.8-V HSTL	Address bus
A9	QDRII_A17	AN26	1.8-V HSTL	Address bus
A3	QDRII_A18	AJ25	1.8-V HSTL	Address bus
A10	QDRII_A19	AT32	1.8-V HSTL	Address bus
A2	QDRII_A20	AU32	1.8-V HSTL	Address bus
B7	QDRII_BWSN0	AK27	1.8-V HSTL	Write byte write select 0
A7	QDRII_BWSN1	AB25	1.8-V HSTL	Write byte write select 1
A5	QDRII_BWSN2	AM25	1.8-V HSTL	Write byte write select 2
B5	QDRII_BWSN3	AV24	1.8-V HSTL	Write byte write select 3
R6	QDRII_C_N	AG24	1.8-V HSTL	Clock N
P6	QDRII_C_P	AD23	1.8-V HSTL	Clock P
A1	QDRII_CQ_N	AR21	1.8-V HSTL	Echo clock N
A11	QDRII_CQ_P	AT21	1.8-V HSTL	Echo clock P
P10	QDRII_D0	AE28	1.8-V HSTL	Write data bus

Table 2–34. QDRII+ Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 3)

Board Reference (U8)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
N11	QDRII_D1	AB27	1.8-V HSTL	Write data bus
M11	QDRII_D2	AB28	1.8-V HSTL	Write data bus
K10	QDRII_D3	AM28	1.8-V HSTL	Write data bus
J11	QDRII_D4	AC27	1.8-V HSTL	Write data bus
G11	QDRII_D5	AD27	1.8-V HSTL	Write data bus
E10	QDRII_D6	AR28	1.8-V HSTL	Write data bus
D11	QDRII_D7	AU28	1.8-V HSTL	Write data bus
C11	QDRII_D8	AV28	1.8-V HSTL	Write data bus
N10	QDRII_D9	AW29	1.8-V HSTL	Write data bus
M9	QDRII_D10	AW28	1.8-V HSTL	Write data bus
L9	QDRII_D11	AR27	1.8-V HSTL	Write data bus
J9	QDRII_D12	AT27	1.8-V HSTL	Write data bus
G10	QDRII_D13	AU27	1.8-V HSTL	Write data bus
F9	QDRII_D14	AN27	1.8-V HSTL	Write data bus
D10	QDRII_D15	AV27	1.8-V HSTL	Write data bus
C9	QDRII_D16	AW27	1.8-V HSTL	Write data bus
B9	QDRII_D17	AH27	1.8-V HSTL	Write data bus
B3	QDRII_D18	AC25	1.8-V HSTL	Write data bus
C3	QDRII_D19	AF27	1.8-V HSTL	Write data bus
D2	QDRII_D20	AD25	1.8-V HSTL	Write data bus
F3	QDRII_D21	AG26	1.8-V HSTL	Write data bus
G2	QDRII_D22	AH26	1.8-V HSTL	Write data bus
J3	QDRII_D23	AE26	1.8-V HSTL	Write data bus
L3	QDRII_D24	AG25	1.8-V HSTL	Write data bus
M3	QDRII_D25	AH25	1.8-V HSTL	Write data bus
N2	QDRII_D26	AP26	1.8-V HSTL	Write data bus
C1	QDRII_D27	AN25	1.8-V HSTL	Write data bus
D1	QDRII_D28	AK25	1.8-V HSTL	Write data bus
E2	QDRII_D29	AT26	1.8-V HSTL	Write data bus
G1	QDRII_D30	AU26	1.8-V HSTL	Write data bus
J1	QDRII_D31	AT25	1.8-V HSTL	Write data bus
K2	QDRII_D32	AW25	1.8-V HSTL	Write data bus
M1	QDRII_D33	AW26	1.8-V HSTL	Write data bus
N1	QDRII_D34	AL26	1.8-V HSTL	Write data bus
P2	QDRII_D35	AV25	1.8-V HSTL	Write data bus
H1	QDRII_DOFFN	AN24	1.8-V HSTL	DLL enable
A6	QDRII_K_N	AE25	1.8-V HSTL	Write clock N
B6	QDRII_K_P	AF25	1.8-V HSTL	Write clock P
P11	QDRII_Q0	AD24	1.8-V HSTL	Read data bus

Table 2–34. QDRII+ Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 3)

Board Reference (U8)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
M10	QDRII_Q1	AT24	1.8-V HSTL	Read data bus
L11	QDRII_Q2	AU24	1.8-V HSTL	Read data bus
K11	QDRII_Q3	AL24	1.8-V HSTL	Read data bus
J10	QDRII_Q4	AE24	1.8-V HSTL	Read data bus
F11	QDRII_Q5	AF24	1.8-V HSTL	Read data bus
E11	QDRII_Q6	AH24	1.8-V HSTL	Read data bus
C10	QDRII_Q7	AW23	1.8-V HSTL	Read data bus
B11	QDRII_Q8	AW24	1.8-V HSTL	Read data bus
P9	QDRII_Q9	AP24	1.8-V HSTL	Read data bus
N9	QDRII_Q10	AT23	1.8-V HSTL	Read data bus
L10	QDRII_Q11	AU23	1.8-V HSTL	Read data bus
K9	QDRII_Q12	AP23	1.8-V HSTL	Read data bus
G9	QDRII_Q13	AD22	1.8-V HSTL	Read data bus
F10	QDRII_Q14	AE23	1.8-V HSTL	Read data bus
E9	QDRII_Q15	AL23	1.8-V HSTL	Read data bus
D9	QDRII_Q16	AT22	1.8-V HSTL	Read data bus
B10	QDRII_Q17	AU22	1.8-V HSTL	Read data bus
B2	QDRII_Q18	AW22	1.8-V HSTL	Read data bus
D3	QDRII_Q19	AV21	1.8-V HSTL	Read data bus
E3	QDRII_Q20	AW21	1.8-V HSTL	Read data bus
F2	QDRII_Q21	AH23	1.8-V HSTL	Read data bus
G3	QDRII_Q22	AE22	1.8-V HSTL	Read data bus
K3	QDRII_Q23	AF22	1.8-V HSTL	Read data bus
L2	QDRII_Q24	AP22	1.8-V HSTL	Read data bus
N3	QDRII_Q25	AW19	1.8-V HSTL	Read data bus
P3	QDRII_Q26	AW20	1.8-V HSTL	Read data bus
B1	QDRII_Q27	AH22	1.8-V HSTL	Read data bus
C2	QDRII_Q28	AT20	1.8-V HSTL	Read data bus
E1	QDRII_Q29	AU20	1.8-V HSTL	Read data bus
F1	QDRII_Q30	AK21	1.8-V HSTL	Read data bus
J2	QDRII_Q31	AU19	1.8-V HSTL	Read data bus
K1	QDRII_Q32	AV19	1.8-V HSTL	Read data bus
L1	QDRII_Q33	AN21	1.8-V HSTL	Read data bus
M2	QDRII_Q34	AE21	1.8-V HSTL	Read data bus
P1	QDRII_Q35	AG21	1.8-V HSTL	Read data bus
A8	QDRII_RPSN	AR25	1.8-V HSTL	Read port select
A4	QDRII_WPSN	AK24	1.8-V HSTL	Write port select

Flash

The development board supports a 1 Gb CFI-compatible synchronous flash device for non-volatile storage of FPGA configuration data, board information, test application data, and user code space. This device is part of the shared FM bus that connects to the flash memory and MAX II CPLD EPM2210 System Controller.

This 16-bit data memory interface can sustain burst read operations at up to 52 MHz for a throughput of 832 Mbps. The write performance is 270 µs for a single word while the erase time is 800 ms for a 128 K main block.

Table 2–35 lists the flash pin assignments, signal names, and functions. The signal names and types are relative to the Arria V GT FPGA in terms of I/O setting and direction.

Table 2–35. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 2)

Board Reference (U4)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
F6	FLASH_ADVN	AK30	1.8-V	Address valid
B4	FLASH_CEN	AU30	1.8-V	Chip enable
E6	FLASH_CLK	AL31	1.8-V	Clock
F8	FLASH_OEN	AN30	1.8-V	Output enable
F7	FLASH_RDYBSYN	AK32	1.8-V	Ready
D4	FLASH_RESETN	AL34	1.8-V	Reset
G8	FLASH_WEN	AN32	1.8-V	Write enable
C6	FLASH_WPN	—	1.8-V	Write protect
A1	FM_A1	AT30	1.8-V	Address bus
B1	FM_A2	AL30	1.8-V	Address bus
C1	FM_A3	AP32	1.8-V	Address bus
D1	FM_A4	AM34	1.8-V	Address bus
D2	FM_A5	AJ33	1.8-V	Address bus
A2	FM_A6	AK33	1.8-V	Address bus
C2	FM_A7	AW33	1.8-V	Address bus
A3	FM_A8	AH30	1.8-V	Address bus
B3	FM_A9	AR30	1.8-V	Address bus
C3	FM_A10	AP33	1.8-V	Address bus
D3	FM_A11	AM31	1.8-V	Address bus
C4	FM_A12	AP31	1.8-V	Address bus
A5	FM_A13	AR31	1.8-V	Address bus
B5	FM_A14	AT31	1.8-V	Address bus
C5	FM_A15	AE29	1.8-V	Address bus
D7	FM_A16	AG30	1.8-V	Address bus
D8	FM_A17	AV31	1.8-V	Address bus
A7	FM_A18	AW30	1.8-V	Address bus
B7	FM_A19	AW31	1.8-V	Address bus
C7	FM_A20	AV30	1.8-V	Address bus

Table 2–35. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 2)

Board Reference (U4)	Schematic Signal Name	Arria V GT FPGA Pin Number	I/O Standard	Description
C8	FM_A21	AT29	1.8-V	Address bus
A8	FM_A22	AU29	1.8-V	Address bus
G1	FM_A23	AP30	1.8-V	Address bus
H8	FM_A24	AN29	1.8-V	Address bus
B6	FM_A25	AL32	1.8-V	Address bus
B8	FM_A26	AK31	1.8-V	Address bus
F2	FM_D0	AC22	1.8-V	Data bus
E2	FM_D1	AH20	1.8-V	Data bus
G3	FM_D2	AG22	1.8-V	Data bus
E4	FM_D3	AN20	1.8-V	Data bus
E5	FM_D4	AP20	1.8-V	Data bus
G5	FM_D5	AV22	1.8-V	Data bus
G6	FM_D6	AG23	1.8-V	Data bus
H7	FM_D7	AN22	1.8-V	Data bus
E1	FM_D8	AH21	1.8-V	Data bus
E3	FM_D9	AD21	1.8-V	Data bus
F3	FM_D10	AN23	1.8-V	Data bus
F4	FM_D11	AM21	1.8-V	Data bus
F5	FM_D12	AL22	1.8-V	Data bus
H5	FM_D13	AG20	1.8-V	Data bus
G7	FM_D14	AK22	1.8-V	Data bus
E7	FM_D15	AK23	1.8-V	Data bus

Power Supply

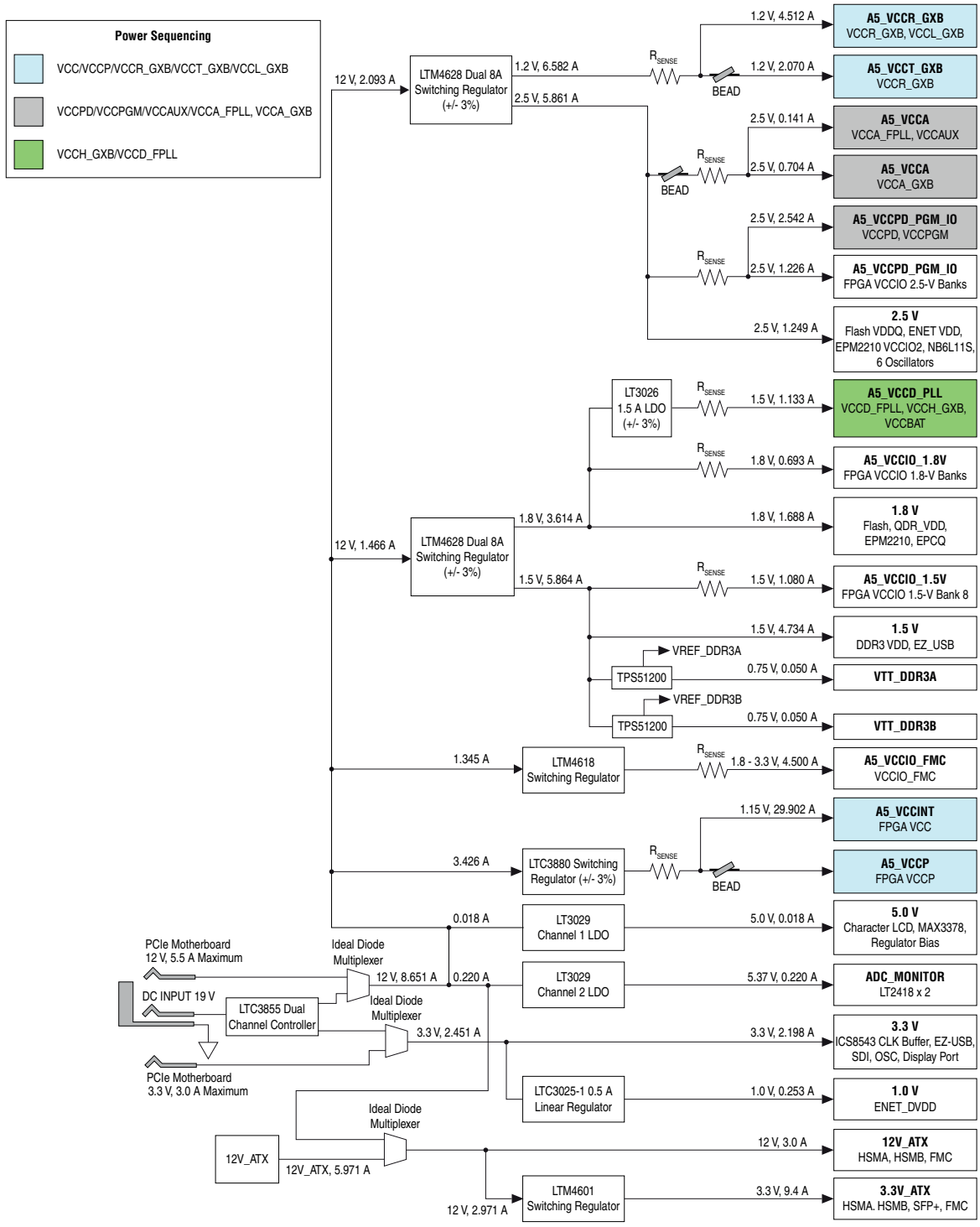
A laptop style DC power input provides power to the development board. The input voltage must be in the range of 14 V to 20 V. The DC voltage is then stepped down to various power rails used by the board components and installed into the HSMC connectors.

An on-board multi-channel analog-to-digital converter (ADC) measures both the voltage and current for several specific board rails. The power utilization is displayed on a graphical user interface (GUI) that can graph power consumption versus time.

Power Distribution System

Figure 2–12 shows the power distribution system on the development board. Regulator efficiencies and sharing are reflected in the currents shown, which are conservative absolute maximum levels.

Figure 2–12. Power Distribution System



Power Measurement

There are 16 power supply rails that have on-board voltage, current, and wattage sense capabilities using 24-bit differential ADC devices. Precision sense resistors split the ADC devices and rails from the primary supply plane for the ADC to measure voltage and current. A SPI bus connects these ADC devices to the MAX II CPLD EPM2210 System Controller as well as the Arria V GT FPGA.

Figure 2–13 shows the block diagram for the power measurement circuitry.

Figure 2–13. Power Measurement Circuit

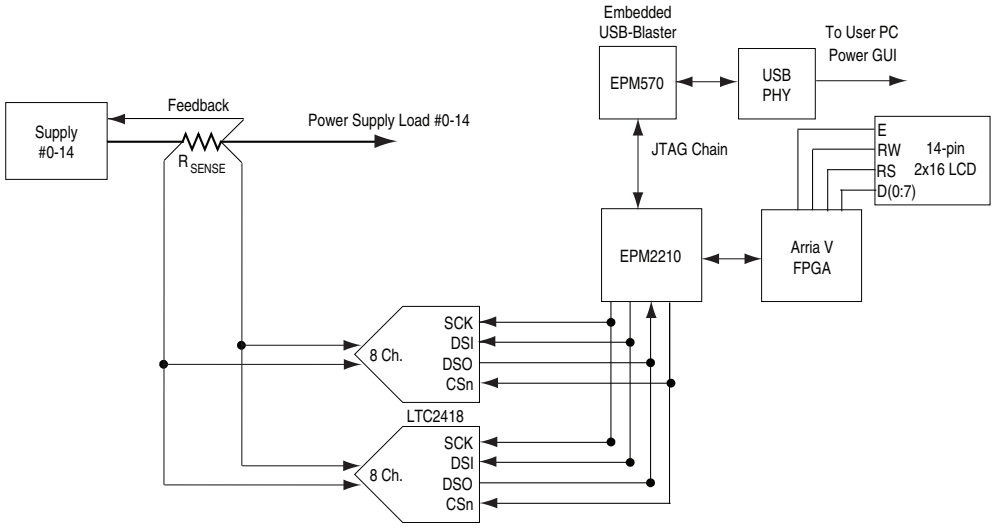


Table 2–36 lists the targeted rails. The schematic signal name column specifies the name of the rail being measured while the device pin column specifies the devices attached to the rail. If no subnet is named, the power is the total output power for that voltage.

Table 2–36. Power Measurement Rails (Part 1 of 3)

Switch	Schematic Signal Name	GUI Name	Voltage	Device Pin	Description
1	A5A_VCCR_VCCL_GXB	A5A_XCVR_GXB	1.2V	VCCR_GXB, VCCL_GXB	XCVR analog receive and clock network
	A5A_VCCT_GXB		1.2V	VCCT_GXB	XCVR transmitter power
2	A5A_VCCA_2.5V	A5A_VCCA	2.5V	VCCA_FPLL	PLL analog power
			2.5V	VCC_AUX, VCCA_GXB	Auxiliary

Table 2–36. Power Measurement Rails (Part 2 of 3)

Switch	Schematic Signal Name	GUI Name	Voltage	Device Pin	Description
3	A5A_VCCPD_PGM_IO_2.5V	A5A_VCCPD/PGM	2.5 V	VCCPD	I/O pre-drivers
			2.5 V	VCCPGM	Configuration I/O
			2.5 V	VCCIO_4A, VCCIO_4B, VCCIO_4C, VCCIO_4D, VCCIO_7A, VCCIO_7B, VCCIO_7C, VCCIO_7D	VCC I/O banks 4 and 7
4	A5A_VCCINT	A5A_VCCINT	1.15 V	VCC, VCCP	FPGA core and periphery power
5	A5A_VCCIO_1.5V	A5A_VCCIO_1.5V	1.5 V	VCCIO_8A, VCCIO_8B, VCCIO_8C, VCCIO_8D	VCCIO bank 8 (DDR3A)
6	A5A_VCCD_PLL_1.5V	A5A_VCCD_PLL	1.5 V	VCCD_FPLL	PLL digital power
			1.5 V	VCCH_GXB	XCVR block level transmit buffers
7	A5A_VCCIO_1.8V	A5A_VCCIO_1.8V	1.8 V	VCCIO_3A, VCCIO_3B, VCCIO_3C, VCCIO_3D	VCC I/O bank 3 (QDRII+)
8	A5B_VCCR_VCCL_GXB	A5B_XCVR_GXB	1.2 V	VCCR_GXB, VCCL_GXB	XCVR analog receive and clock network
	A5B_VCCT_GXB		1.2 V	VCCT_GXB	XCVR transmitter power
9	A5B_VCCA_2.5V	A5B_VCCA	2.5 V	VCCA_FPLL	PLL analog power
			2.5 V	VCC_AUX	Auxiliary
10	A5B_VCCPD_PGM_IO_2.5V	A5B_VCCPD/PGM	2.5 V	VCCPD	I/O pre-drivers
			2.5 V	VCCPGM	Configuration I/O
			2.5 V	VCCIO_3A, VCCIO_3B, VCCIO_7A, VCCIO_7B, VCCIO_7C, VCCIO_7D	VCC I/O banks 3A, 3B and 7
11	A5B_VCCINT	A5B_VCCINT	1.15 V	VCC, VCCP	FPGA core and periphery power
12	A5B_VCCIO_1.5V	A5B_VCCIO_1.5V	1.5 V	VCCIO_8A, VCCIO_8B, VCCIO_8C, VCCIO_8D	VCCIO bank 8 (DDR3A)

Table 2–36. Power Measurement Rails (Part 3 of 3)

Switch	Schematic Signal Name	GUI Name	Voltage	Device Pin	Description
13	A5B_VCCD_PLL_1.5V	A5B_VCCD_PLL	1.5 V	VCCD_FPLL	PLL digital power
			1.5 V	VCCH_GXB	XCVR block level transmit buffers
14	A5_VCCIO_FMC	A5_VCCIO_FMC	1.5 V/ 1.8 V/ 2.5 V/ 3.3 V	VCCIO_3C, VCCIO_3D, VCCIO_4A, VCCIO_4C, VCCIO_4D	I/O supply bank (FMC port)

Statement of China-RoHS Compliance

Table 2–37 lists hazardous substances included with the kit.

Table 2–37. Table of Hazardous Substances' Name and Concentration ***Notes*** *(1)*, *(2)*

Part Name	Lead (Pb)	Cadmium (Cd)	Hexavalent Chromium (Cr6+)	Mercury (Hg)	Polybrominated biphenyls (PBB)	Polybrominated diphenyl Ethers (PBDE)
Arria V development board	X*	0	0	0	0	0
12 V power supply	0	0	0	0	0	0
Type A-B USB cable	0	0	0	0	0	0
User guide	0	0	0	0	0	0

Notes to Table 2–37:

(1) 0 indicates that the concentration of the hazardous substance in all homogeneous materials in the parts is below the relevant threshold of the SJ/T11363-2006 standard.

(2) X* indicates that the concentration of the hazardous substance of at least one of all homogeneous materials in the parts is above the relevant threshold of the SJ/T11363-2006 standard, but it is exempted by EU RoHS.

3. Board Components Reference

This chapter lists the component reference and manufacturing information of all the components on the Arria V GT FPGA FPGA development board.

Table 3–1. Component Reference and Manufacturing Information (Part 1 of 2)

Board Reference	Component	Manufacturer	Manufacturing Part Number	Manufacturer Website
U13, U16	FPGAs, Arria V GT F1517, 504K LEs, lead free	Altera Corporation	5AGTFD7K3F40I3N	www.altera.com
U2	IC - MAX II CPLD EPM2210 324FBGA -3 LF 1.8V VCCINT	Altera Corporation	EPM2210GF324	www.altera.com
D2–D12, D14–D17, D34–D40, D45	Green LEDs	Lumex Inc.	SML-LXT0805GW-TR	www.lumex.com
D42, D43, D44	Yellow LEDs	Lumex Inc.	SML-LXT0805YW-TR	www.lumex.com
D18–D33	Bi color Red/Green LEDs	Lite-On	LTST-C195KGJRKT	www.lite-on.com
D13	Red LED	Lumex Inc.	SML-LXT0805IW-TR	www.lumex.com
D1	Blue LED	Lumex Inc.	SML-LX0805USBC-TR	www.lumex.com
SW5–SW7	Four-position DIP switches	C&K Components/ ITT Industries	TDA04H0SB1	www.ittcannon.com
S1, S4, S8	Reset push buttons	Dawning Precision Co.	TS-A02SA-2-S100	www.dawning2.com.tw
S3	Configuration push button	Dawning Precision Co.	TS-A02SA-2-S100	www.dawning2.com.tw
S2	Image select push button	Dawning Precision Co.	TS-A02SA-2-S100	www.dawning2.com.tw
X1, X4	125.000-MHz LVDS saw clock oscillator	Epson	EG-2121CA 125.0000M-LGPNL3	www.eea.epson.com
X5	25-MHz oscillator	Epson	SG-310SDF 25.0000M-B3	www.eea.epson.com
Y3	24-MHz crystal oscillator	Epson	FA-128 24.0000MB-W	www.eea.epson.com
Y1, Y2, Y4, Y5	25-MHz crystal oscillator	Epson	FA-128 25.0000MB-C	www.eea.epson.com
X6	50-MHz oscillator	ECS Inc.	ECS-3518-500-B-xx	www.ecsxtal.com
U34, U48, U53, U52	Quad output programmable clock generator	Silicon Labs Inc.	Si5338A-A01316-GM, Si5338A-A01317-GM, Si5338A-A01318-GM, Si5338A-A01319-GM	www.silabs.com
X7	100-MHz single output programmable oscillator	Silicon Labs Inc.	570FAB000433DG	www.silabs.com
X2	148.5-MHz single output programmable VCXO	Silicon Labs Inc.	571FDB000159DG	www.silabs.com

Table 3–1. Component Reference and Manufacturing Information (Part 2 of 2)

Board Reference	Component	Manufacturer	Manufacturing Part Number	Manufacturer Website
X7	100 MHz crystal oscillator	ECS Inc.	ECS-3525-1000-B-TR	www.ecsxtal.com
S4–S6, S9–S11	User-defined push button	Dawning Precision Co.	TS-A02SA-2-S100	www.dawning2.com.tw
SW2, SW3	User-defined eight-position DIP switch	C&K Components/ ITT Industries	TDA08H0SB1	www.ittcannon.com
D18–D25, D26–D33	User-defined bi-color red and green LEDs	Lite-On	LTST-C195GEKT	www.us.liteon.com/opto.index.html
D4, D5, D7, D8	HSMC Green LEDs	Lumex Inc.	SML-LXT0805GW-TR	www.lumex.com
J30	2×7 pin, 100 mil, vertical header LCD socket strip	Samtec	TSM-107-01-G-DV	www.samtec.com
	2×16 character display, 5×8 dot matrix	Lumex Inc.	LCM-S01602DSR/C	www.lumex.com
U24	3-Gbps HD/SD SDI cable driver with cable detect	National Semiconductor	LMH0303SQx	www.national.com
U23	3-Gbps HD/SD SDI adaptive cable equalizer	National Semiconductor	LMH0384SQ	www.national.com
J4	PCI Express 4.20-mm pitch header, 13 A per pin, dual row, right angle, with PCB mounting flanges.	Molex	50-34-8571	www.molex.com
U14	Ethernet PHY BASE-T device	Marvell Semiconductor	88E1111-B2-CAA1C000	www.marvell.com
J8	RJ-45 connector, 10/100/1000 Mbps	Wurth Elektronik	7499111001A	www.we-online.com
J1, J2	HSMC, custom version of QSH-DP family high-speed socket.	Samtec	ASP-122953-01	www.samtec.com
B2	SFP+ right-angle, press-fit cage	Molex	74754-0101	www.molex.com
J10, J15	SFP+ right-angle, 20-pin SMT connector	Samtec	MECT-110-01-M-D-RA1	www.samtec.com
J10	FMC pitch socket array assembly connector	Samtec	ASP-134486-01	www.samtec.com
J16	Bull's Eye test point receptacle	Samtec	BAR-J-22	www.samtec.com
	Four CCA-25M cable assemblies		BE25S-01SP1-01.0-02-0152	
	Insertion/Extraction tool		CAT-EX-SCC-01	
U6, U11, U12, U18, U19, U21, U22, U28	32M×16×8, 2 Gb, DDR3 memory	Micron	MT41J128M16HA-125:D	www.micron.com
U7	16M×8×8, 1 Gb, DDR3 memory	Micron	MT41J128M8JP-125:G	www.micron.com
U8	QDRII+ SRAM 72-Mb 4-word burst 2M×36, 533 MHz	Renesas Technology Corp.	R1QDA7236ABG_19IB0	www.am.renesas.com
U4	1-Gb synchronous flash	Numonyx	PC28F512P30BF	www.numonyx.com
U29, U31	8-channel differential 24-bit ADC	Linear Technology	LTC2418CGN#PBF	www.linear.com

This chapter provides additional information about the document and Altera.

Document Revision History

The following table lists the revision history for this document.

Date	Version	Changes
December 2014	1.2	Corrected FPGA pin numbers for user-defined LEDs for FPGA 1. Table 2–16.
May 2013	1.1	Revised the FPGA core voltage to 1.15 V in Figure 2–12 and Table 2–36.
November 2012	1.0	Initial release.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact (1)	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Nontechnical support (general)	Email	nacomp@altera.com
(software licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.
italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>***.pof** file.

Visual Cue	Meaning
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
“Subheading Title”	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, “Typographic Conventions.”
`Courier type`	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. The suffix `n` denotes an active-low signal. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
↵	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	The question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	The multimedia icon directs you to a related multimedia presentation.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.
	The feedback icon allows you to submit feedback to Altera about the document. Methods for collecting feedback vary as appropriate for each document.