User's Guide

LMZ315x0 Power Module Evaluation Module User's Guide

ABSTRACT

The LMZ315x0 EVM is designed as an easy-to-use platform that facilitates evaluation of the features and performance of the SIMPLE SWITCHER® power module. The LMZ31520 and LMZ31530 devices provide output currents of 20 A and 30 A, respectively. This guide provides information on the correct usage of the EVM and an explanation of the various test points found on the board.

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Trademarks

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1 Description

The EVM features a LMZ31520 (20 A) or LMZ31530 (30 A), synchronous buck SIMPLE SWITCHER power module configured for operation with typical 5-V and 12-V input bus applications. The output voltage can be set to one of six popular values by using a configuration jumper. In similar fashion, the switching frequency can be set to one of four values with a jumper. The full 20-A/30-A rated output current can be supplied by the EVM. Input and output capacitors are included on the board to accommodate the entire range of input and output voltages. Monitoring test points are provided to allow the following:

- Measurement of efficiency
- Power dissipation
- Input ripple
- Output ripple
- Line and load regulation
- Transient response

Control test points are provided for use of the PWRGD and Inhibit features of the power module along with a selector for Eco-Mode or FCCM. The EVM uses a recommended PCB layout that maximizes thermal performance and minimizes output ripple and noise.

2 Getting Started

Figure 2-1 highlights the user interface items associated with the EVM. The polarized *PVin Power* terminal block (J8) is used for connection to the host input supply and the polarized *Vout Power* terminal block (J11) is used for connection to the load. These terminal blocks can accept up to 16-AWG wire. The polarized VBIAS terminal block (J12) is used along with the VIN SELECT jumper (J4) when optional split power supply operation is desired. Refer to the *LMZ31520 20-A Power Module With 3-V to 14.5-V Input Data Sheet* and *LMZ31530 30-A Power Module With 3-V to 14.5-V Input Data Sheet* for further information on split power supply operation.

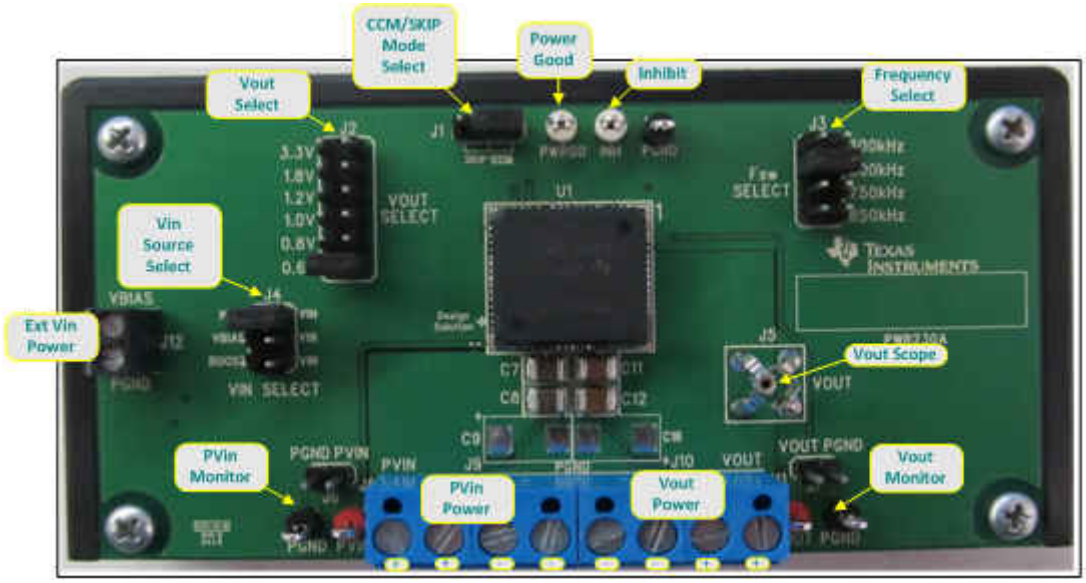

Figure 2-1. LMZ315x0EVM User Interface

The *PVin Monitor* (TP1) and *Vout Monitor* (TP3) test points located near the power terminal blocks are intended to be used as voltage monitoring points where voltmeters can be connected to measure PVIN and VOUT. The voltmeter references should be connected to the PGND test points (TP4 and TP2). Do *not* use these PVIN and VOUT monitoring test points as the input supply or output load connection points. The PCB traces connecting to these test points are not designed to support high currents.

The *PVin Scope* (J6) and *Vout Scope* (J7) test points can be used to monitor PVIN and VOUT waveforms with an oscilloscope. These test points are intended for use with un-hooded scope probes outfitted with a low-inductance ground lead (ground spring) mounted to the scope barrel. The two sockets of each test point are

on 0.1-inch centers. The scope probe tip should be connected to the socket labeled PVIN or VOUT, and the scope ground lead should be connected to the socket labeled PGND.

The *Vout Scope* (J5) test point can be used to monitor the V_{OUT} waveform with an oscilloscope. This test point is intended for use with an un-hooded scope probe with a 3.5-mm ground barrel.

The control test points located directly above the device are made available to test the features of the device. Refer to Section 3 for more information on the individual control test points.

The *Vout Select* jumper (J2) and *Fsw Select* jumper (J3) are provided for selecting the desired output voltage and appropriate switching frequency. Before applying power to the EVM, ensure that the jumpers are present and properly positioned for the intended output voltage. Always remove input power before changing the jumper settings.

3 Test Point Descriptions

Seven wire-loop test points and three scope probe test points have been provided as convenient connection points for digital voltmeters (DVM) or oscilloscope probes to aid in the evaluation of the device. A description of each test point follows:

Table 3-1. Test Point Descriptions(1)

PVIN	Input voltage monitor. Connect DVM to this point for measuring efficiency.
VOUT	Output voltage monitor. Connect DVM to this point for measuring efficiency, line regulation, and load regulation.
PGND	Input and output voltage monitor grounds. Reference the above DVMs to the corresponding ground point.
PVIN Scope (J6)	Input voltage scope monitor. Connect an oscilloscope to this set of points to measure input ripple voltage.
VOUT Scope (J7)	Output voltage scope monitor. Connect an oscilloscope to this set of points to measure output ripple voltage and transient response.
VOUT Scope (J5)	Output voltage scope monitor. Insert an oscilloscope into the test point adapter to measure output ripple voltage and transient response.
PWRGD	Monitors the power-good signal of the device. A 100-kΩ pullup resistor is included internal to the device and is tied to 5 V. PWRGD is high if the output voltage is within 95% to 110% of its nominal value.
INH	Connect this point to control ground to inhibit the device. Allow this point to float to enable the device.

(1) Refer to the product data sheet for absolute maximum ratings associated with above features.

4 Operation Notes

In order to operate the EVM using a single power supply, the VIN Select jumper (J4) must be in the default PVIN-VIN position shown in Figure 2-1. In this position, the PVIN and VIN pins of the device are connected together. The UVLO threshold of the EVM is approximately 4.2 V with 0.25 V of hysteresis. The input voltage must be above the UVLO threshold to start up the device. After start-up, the minimum input voltage to the device must be at least 4.5 V or (V_{OUT} + 1.0 V), whichever is greater. The maximum operating input voltage for the device is 15 V. Refer to the product data sheet for further information on the input voltage range, and optional split power supply operation for operating with PVIN as low as 3.0 V when using an external Vbias supply.

After application of the proper input voltage, the output voltage of the device will ramp to its final value in approximately 0.7 ms. If desired, this soft-start time can be increased by increasing the value of the Rss resistor (R6). Refer to the *LMZ31520 20-A Power Module With 3-V to 14.5-V Input Data Sheet* and *LMZ31530 30-A Power Module With 3-V to 14.5-V Input Data Sheet* for further information on adjusting the soft-start time.

The EVM includes input and output capacitors to accommodate the entire range of input and output voltage conditions. The actual capacitance required will depend on the input and output voltage conditions of the particular application, along with the desired transient response. In most cases, the required output capacitance will be less than that supplied on the EVM. Refer to the *LMZ31520 20-A Power Module With 3-V to 14.5-V Input Data Sheet* and *LMZ31530 30-A Power Module With 3-V to 14.5-V Input Data Sheet* for further information on the minimum required I/O capacitance and transient response.

The LMZ315x0 can be operated in either auto-skip Eco-Mode or in forced continuous conduction mode (FCCM) by selecting the desired mode using J1. Refer to the *LMZ31520 20-A Power Module With 3-V to 14.5-V Input Data Sheet* and *LMZ31530 30-A Power Module With 3-V to 14.5-V Input Data Sheet* for further information on selecting the mode of operation.

5 Performance Data

Figure 5-1 through Figure 5-7 demonstrate the TPS84A20EVM performance with V_{OUT} = 1.8 V and F_{sw} = 500 kHz.

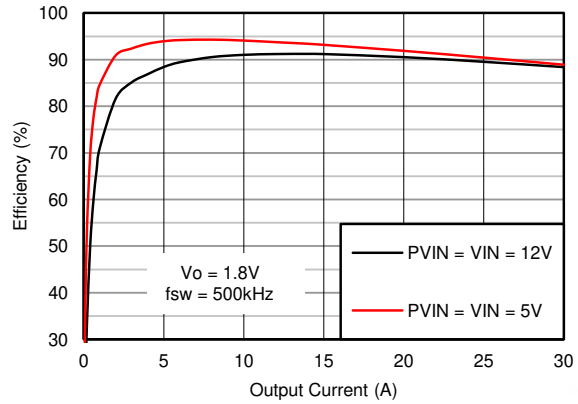

Figure 5-1. LMZ31530EVM Efficiency

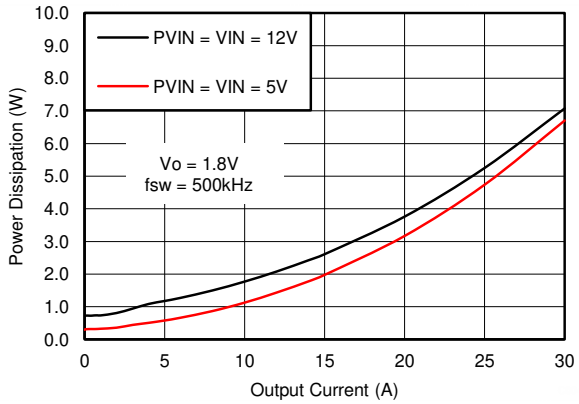

Figure 5-2. LMZ31530EVM Power Dissipation

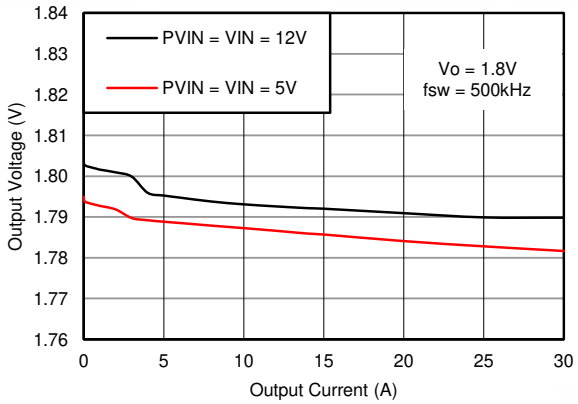

Figure 5-3. LMZ31530EVM Load Regulation

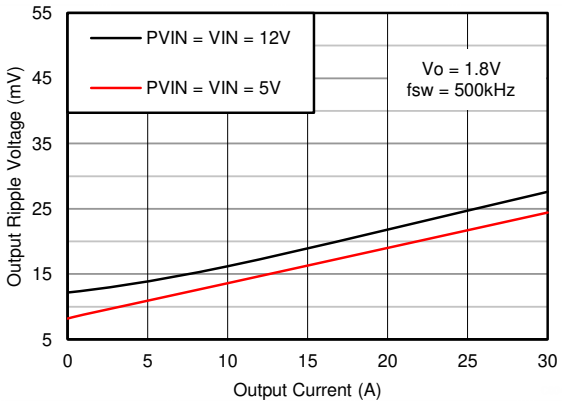

Figure 5-4. LMZ31530EVM Output Ripple

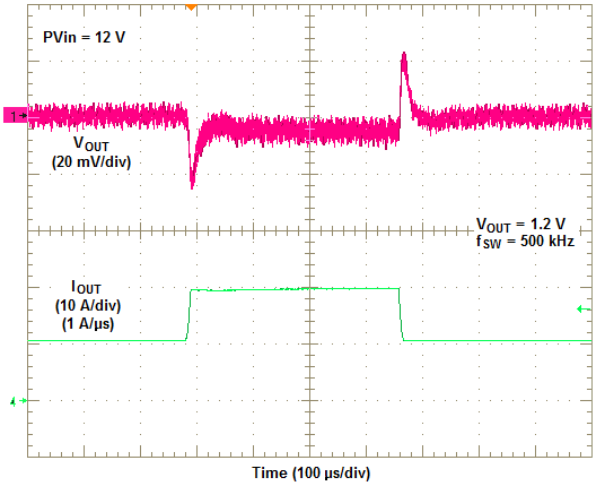

Figure 5-5. LMZ31530EVM Transient Response Waveforms

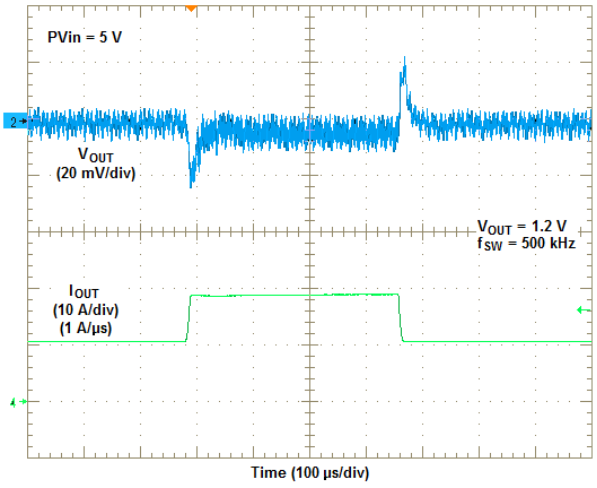

Figure 5-6. LMZ31530EVM Transient Response Waveforms

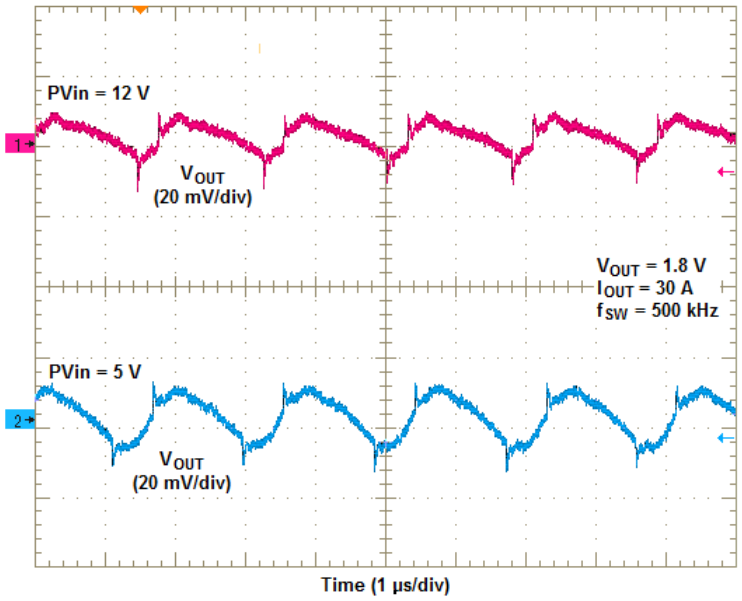

Figure 5-7. LMZ31530EVM Output Ripple Waveforms

6 Schematic

Figure 6-1 is the schematic for this EVM.

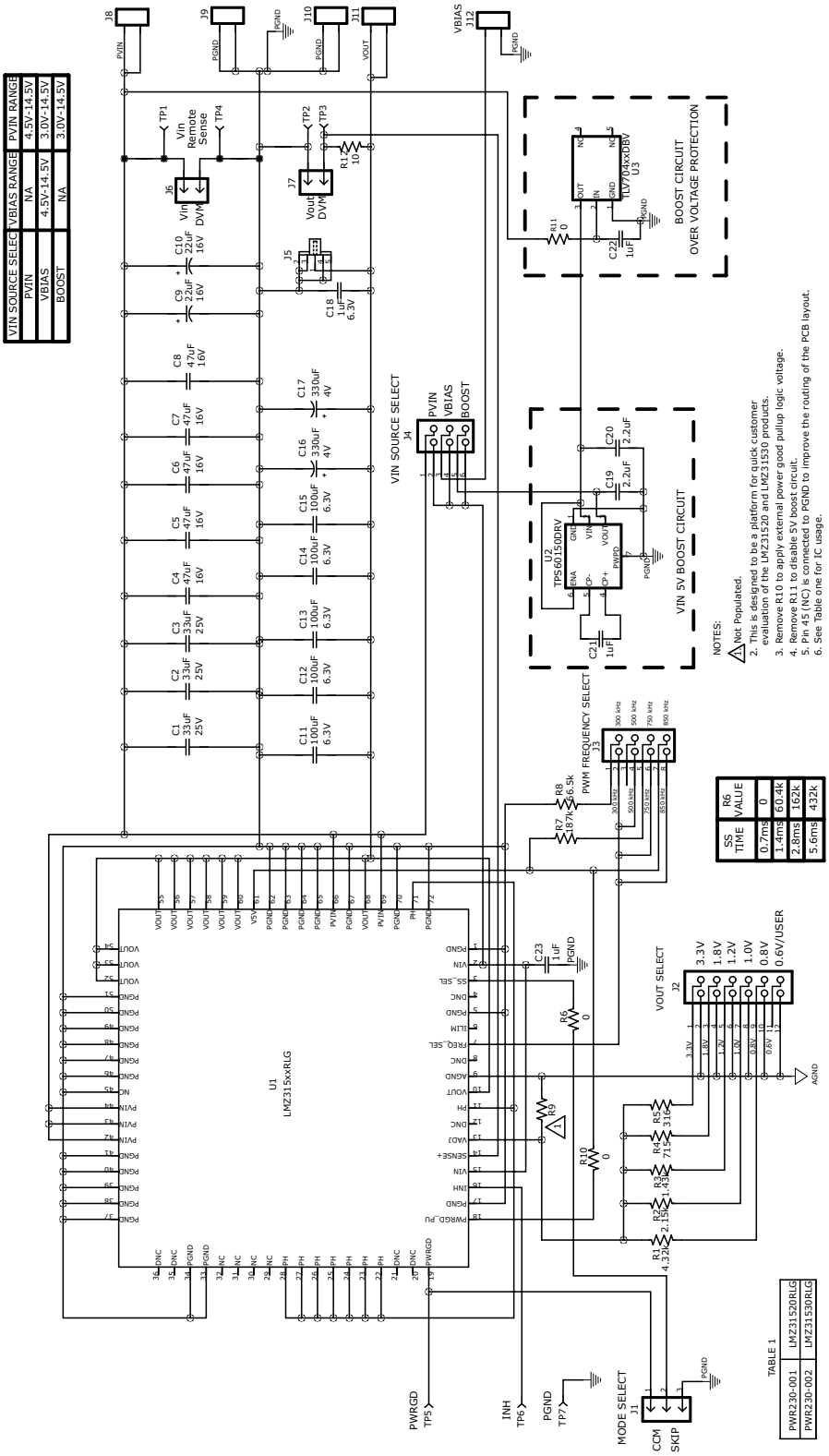

Figure 6-1. LMZ315xxEVM Schematic

7 Bill of Materials

Figure 7-1 is the BOM for the EVM.

COUNT							
-002	-001	RefDes	Value	Description	Size	Part Number	Mfr
3	3	C1, C2, C3	33uF	Capacitor, Ceramic, 25V, X5R, 20%	1206	C3216X5R1E336M160AC	TDK Corporation
5	5	C4, C5, C6, C7, C8	47uF	Capacitor, Ceramic, 16V, X5R, 10%	1210	EMK325BJ476MM-T	Taiyo Yuden
2	2	C9, C10	22uF	Capacitor, Polymer, 16V, 20%	2917	A700D226M016ATE018	Kemet
5	5	C11, C12, C13, C14, C15	100uF	Capacitor, Ceramic, 6.3V, X5R, 20%	1210	C3225X5R0J107M250AC	TDK Corporation
2	2	C16, C17	330uF	Capacitor, Polymer, 4V, 20%	2917	EEF-UE0G331R	Panasonic
1	1	C18	1uF	Capacitor, Ceramic, 6.3V, X5R, 10%	0603	C1608X5R0J105K	TDK Corporation
2	2	C19, C20	2.2uF	Capacitor, Ceramic, 6.3V, X5R, 10%	0805	C2012X5R0J225M085AA	TDK Corporation
1	1	C21	1uF	Capacitor, Ceramic, 6.3V, X5R, 10%	0805	C0805C105K9PACTU	Kemet
2	2	C22, C23	1uF	Capacitor, Ceramic, 25V, X5R, 10%	0805	C2012X5R1E105K085AC	TDK Corporation
1	1	J1	PEC03SAAN	Header, Male, 1x3 pin, 0.1" centers	0.100 inch x 1 x 3	PEC03SAAN	Sullins
1	1	J2	PEC06DAAN	Header, Male, 2x6 pin, 0.1" centers	0.100 inch x 2 x 6	PEC06DAAN	Sullins
1	1	J3	PEC04DAAN	Header, Male, 2x4 pin, 0.1" centers	0.100 inch x 2 x 4	PEC04DAAN	Sullins
1	1	J4	PEC03DAAN	Header, Male, 2x3 pin, 0.1" centers	0.100 inch x 2 x 3	PEC03DAAN	Sullins
1	1	J5	131-5031-00	CB TEST POINT ADAPTER, 5mm	0.690 x 0.690 inch	131-5031-00	Tektronix
2	2	J6, J7	PEC02SAAN	Header, Male, 1x2 pin, 0.1" centers	0.100 inch x 1 x 2	PEC02SAAN	Sullins
4	4	J8, J9, J10, J11	ED120/2DS	Terminal Block, 2-pin, 15A, 5.1mm	0.40 x 0.35 inch	ED120/2DS	On Shore Technology
1	1	J12	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	3.5 mm x 1 x 2	ED555/2DS	On Shore Technology
1	1	R1	4.32k	Resistor, Chip, 1/16W, 1%	0603	CRCW06034K32FKEA	Vishay Dale
1	1	R2	2.15k	Resistor, Chip, 1/16W, 1%	0603	CRCW06032K15FKEA	Vishay Dale
1	1	R3	1.43k	Resistor, Chip, 1/16W, 1%	0603	CRCW06031K43FKEA	Vishay Dale
1	1	R4	715	Resistor, Chip, 1/16W, 1%	0603	CRCW0603715RFKEA	Vishay Dale
1	1	R5	316	Resistor, Chip, 1/16W, 1%	0603	CRCW0603316RFKEA	Vishay Dale
3	3	R6, R10, R11	0	Resistor, Chip, 1/16W, 1%	0603	ERJ-3GEY0R00V	Panasonic
1	1	R7	187k	Resistor, Chip, 1/16W, 1%	0603	CRCW0603187KFKEA	Vishay Dale
1	1	R8	66.5k	Resistor, Chip, 1/16W, 1%	0603	CRCW060366K5FKEA	Vishay Dale
0	0	R9	optional (user-defined)	Resistor, Chip, 1/16W, 1%	0402	optional (user-defined)	optional (user-defined)
1	1	R12	10	Resistor, Chip, 1/16W, 1%	0603	CRCW060310R0FKEA	Vishay Dale
2	2	TP1,TP3	5010	Test Point, Red, Wire Loop, Thru Hole	0.125 x 0.125 inch	5010	Keystone
3	3	TP2, TP4, TP7	5011	Test Point, Black, Wire Loop, Thru Hole	0.125 x 0.125 inch	5011	Keystone
2	2	TP5, TP6	5012	Test Point, White, Wire Loop, Thru Hole	0.125 x 0.125 inch	5012	Keystone
0	1	U1	LMZ31520RLG	IPS, Sync Buck, 3 to 14.5V Input, 30A Output	15x16x5.8 mm QFN	LMZ31520RLG	TI
1	0	U1	LMZ31530RLG	IPS, Sync Buck, 3 to 14.5V Input, 20A Output	15x16x5.8 mm QFN	LMZ31530RLG	TI
1	1	U2	TPS60150DRV	150mA 5V charge pump	2x2x0.8 mm QFN	TPS60150DRV	TI
1	1	U3	TLV70450DBV	24-V Input, 150 mA, 5.0V LDO Regulator	3x3x1.45 mm SOT-23	TLV70450DBV	TI
4	4	---	---	Shunt, Black	0.100 inch x 1 x 2	929950-00	3M
4	4	---	---	Bumpon, Hemisphere, Black	0.44 Dia. x 0.20 inch	SJ-5003	3M
1	1	---	---	PCB, 2" x 4" x 0.062"	2 x 4 x 0.062 inch	PWR203	Any
1	1	---	---	Label	1.25 x 0.25 inch	THT-13-457-10	Brady

Figure 7-1. LMZ315x0EVM BOM

8 PCB Layout

Figure 8-1 through Figure 8-8 show the PCB layout layers of the EVM.

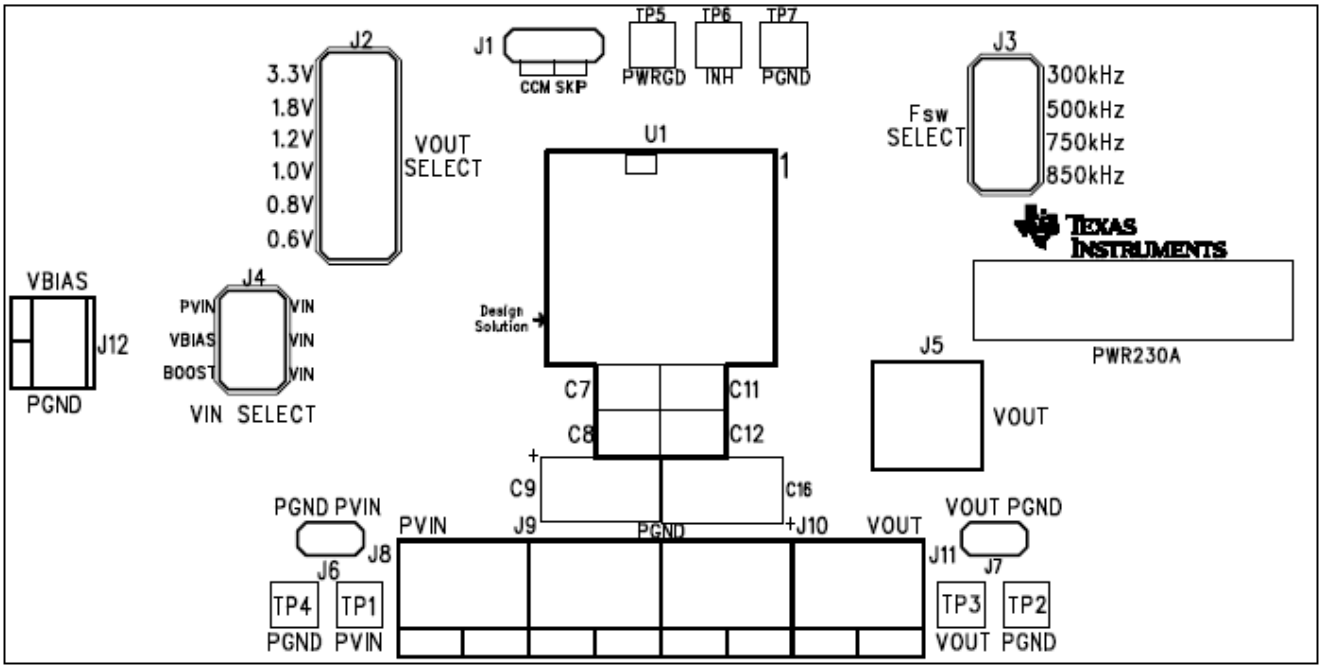

Figure 8-1. EVM Topside Component Layout

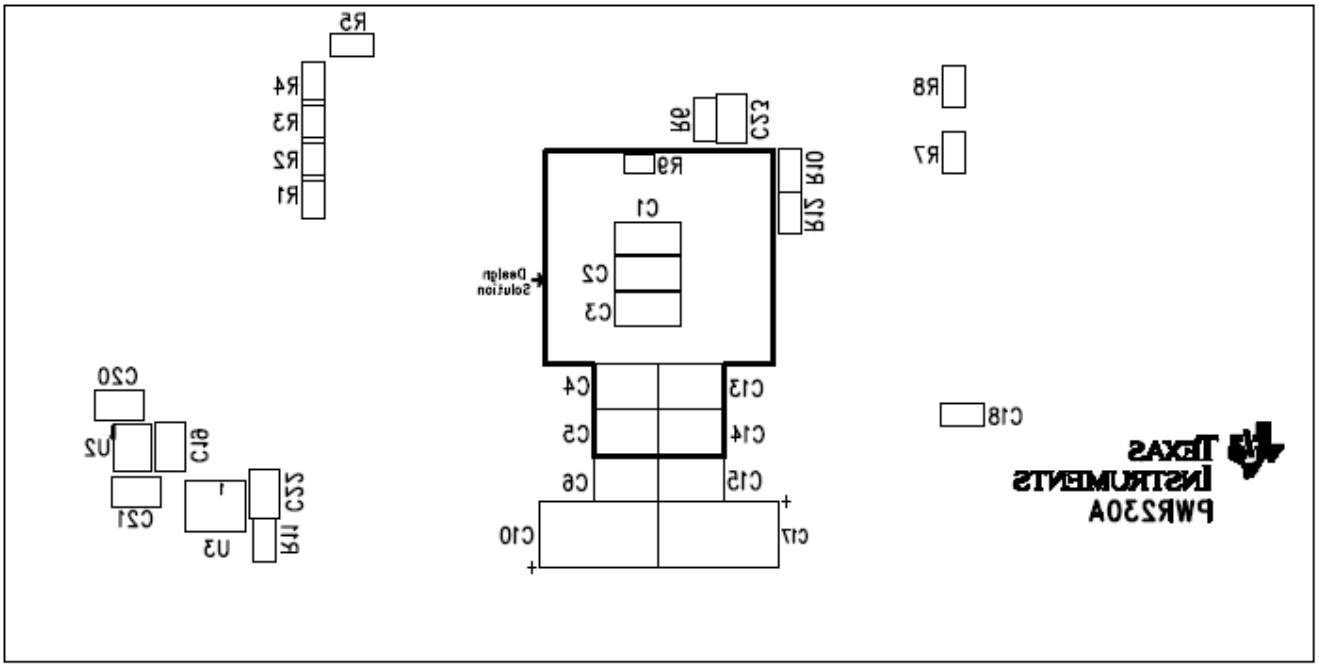

Figure 8-2. EVM Bottom-Side Component Layout

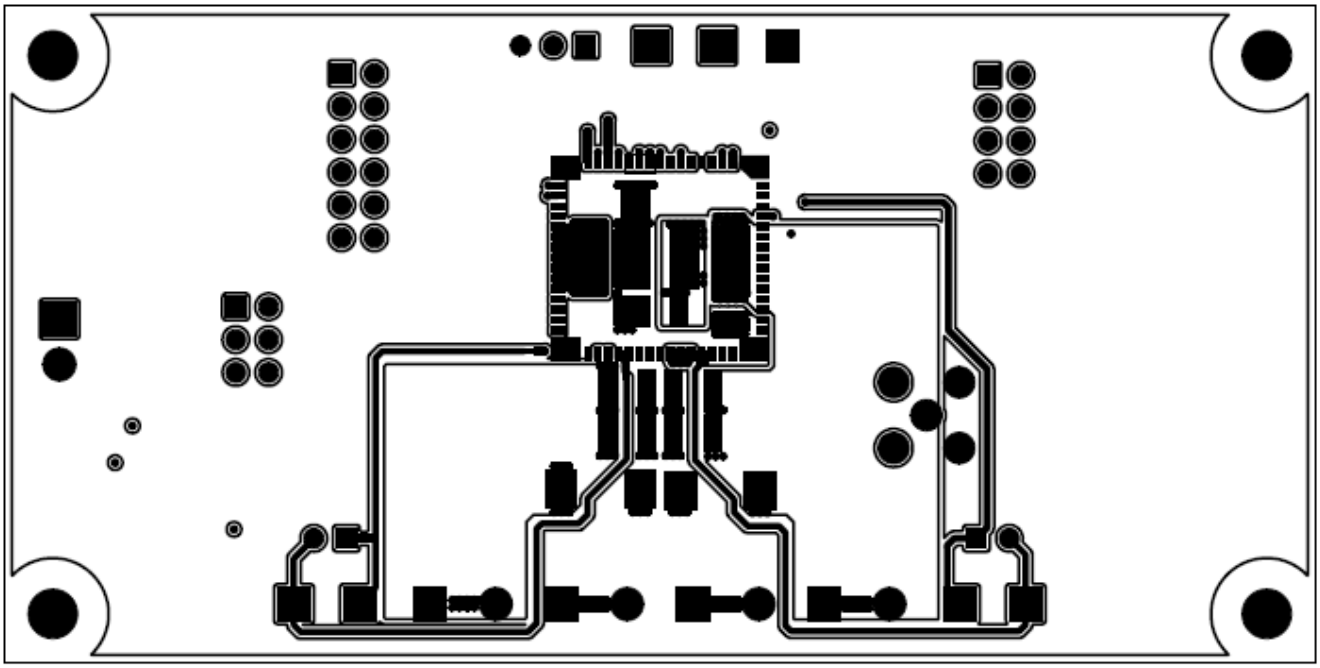

Figure 8-3. EVM Top Side Copper

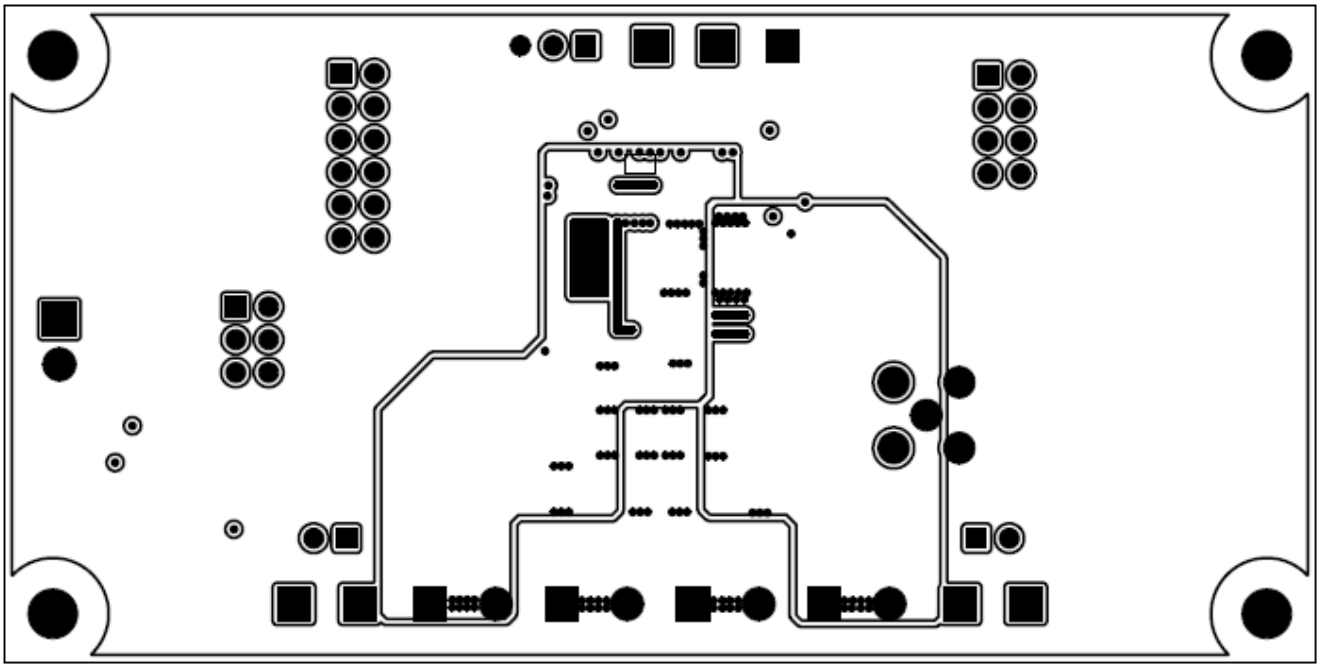

Figure 8-4. EVM Layer 2 Copper

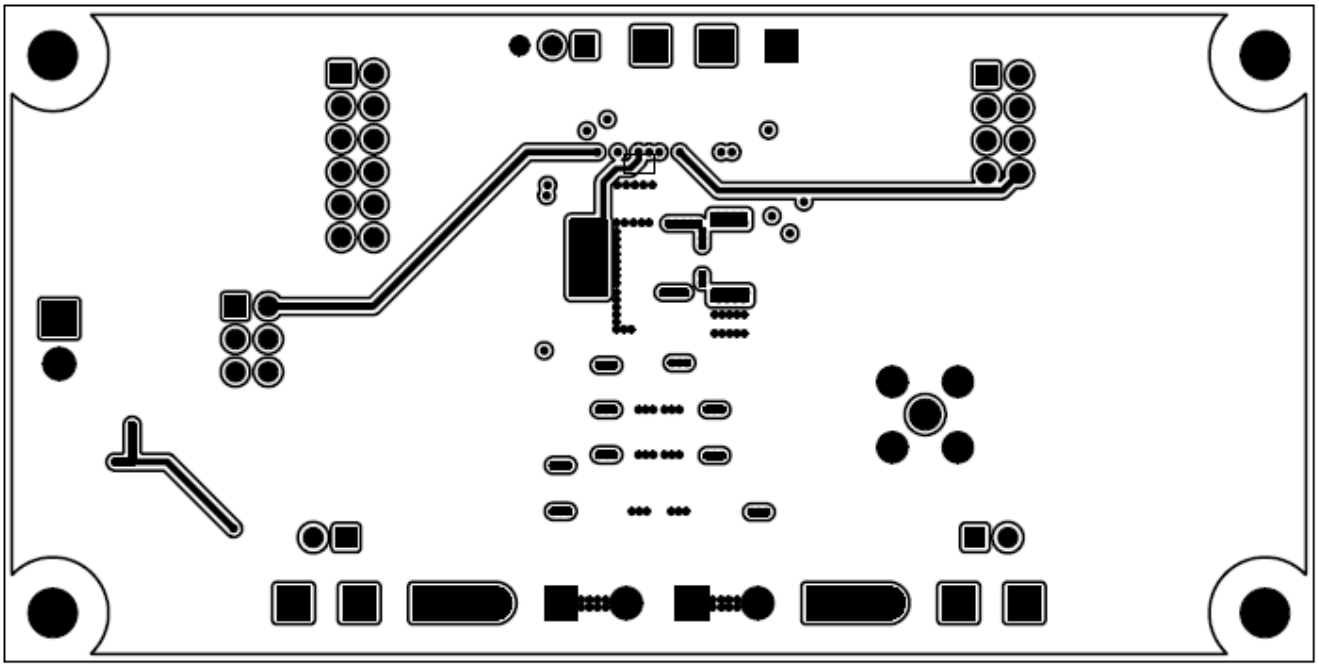

Figure 8-5. EVM Layer 3 Copper

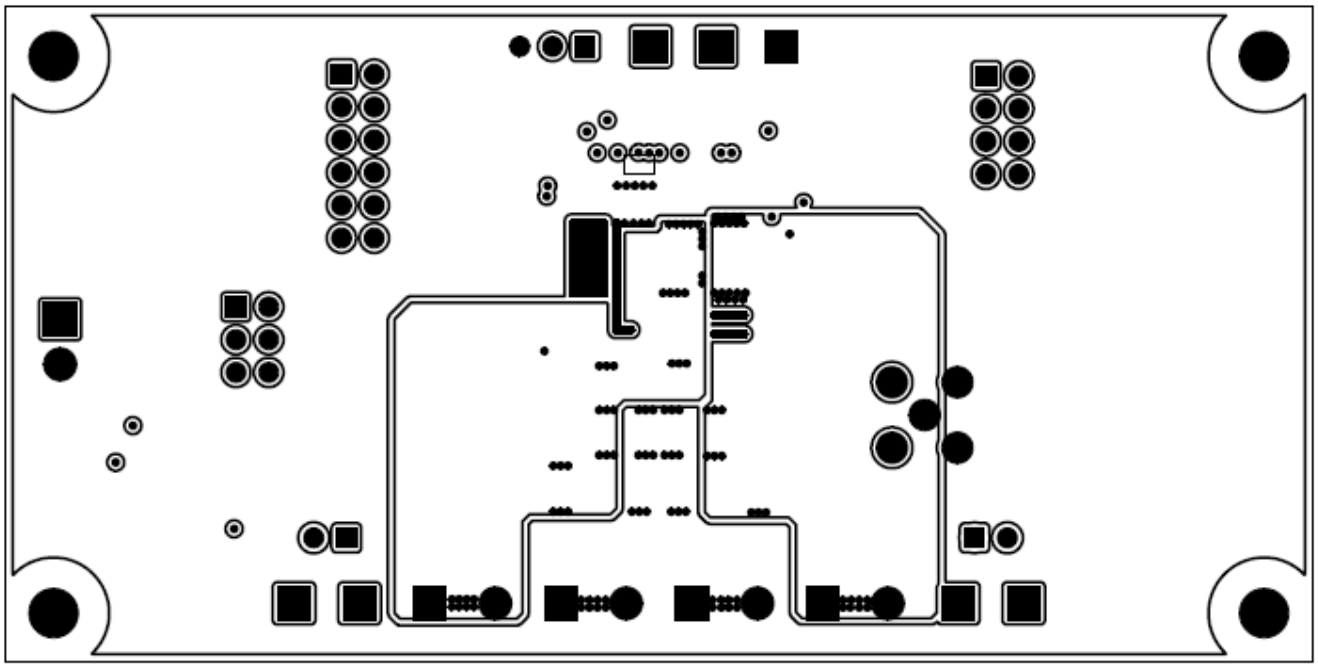

Figure 8-6. EVM Layer 4 Copper

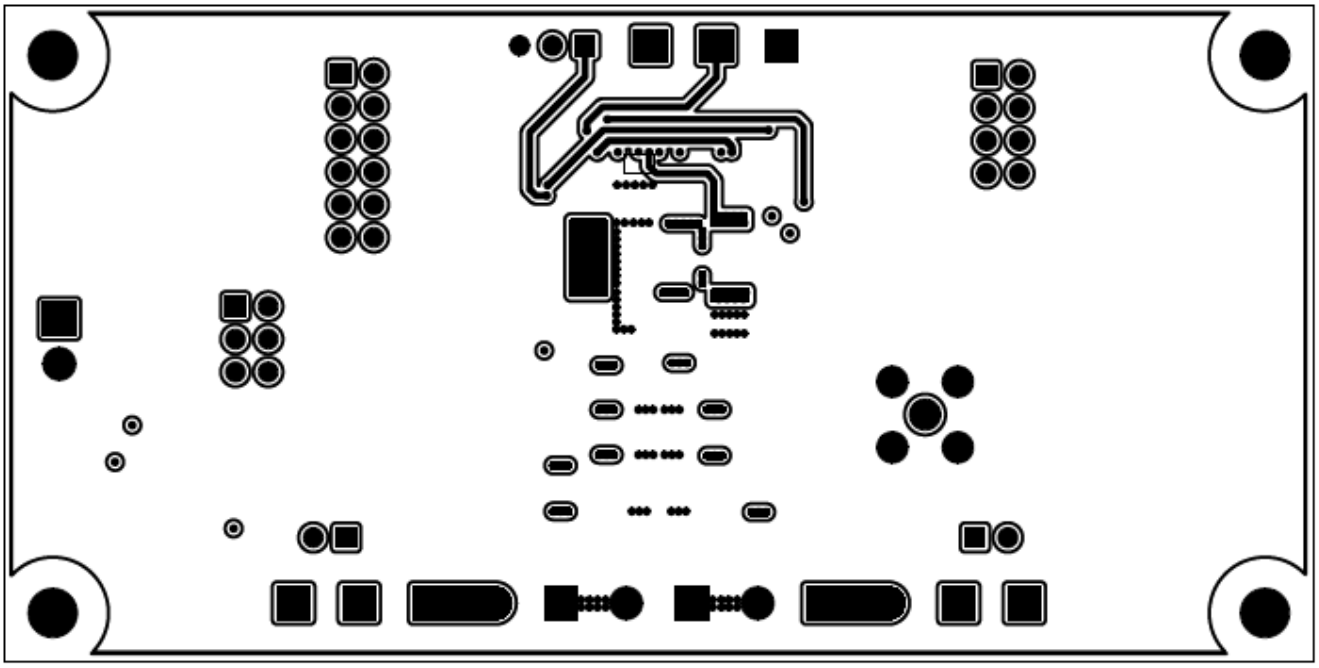

Figure 8-7. EVM Layer 5 Copper

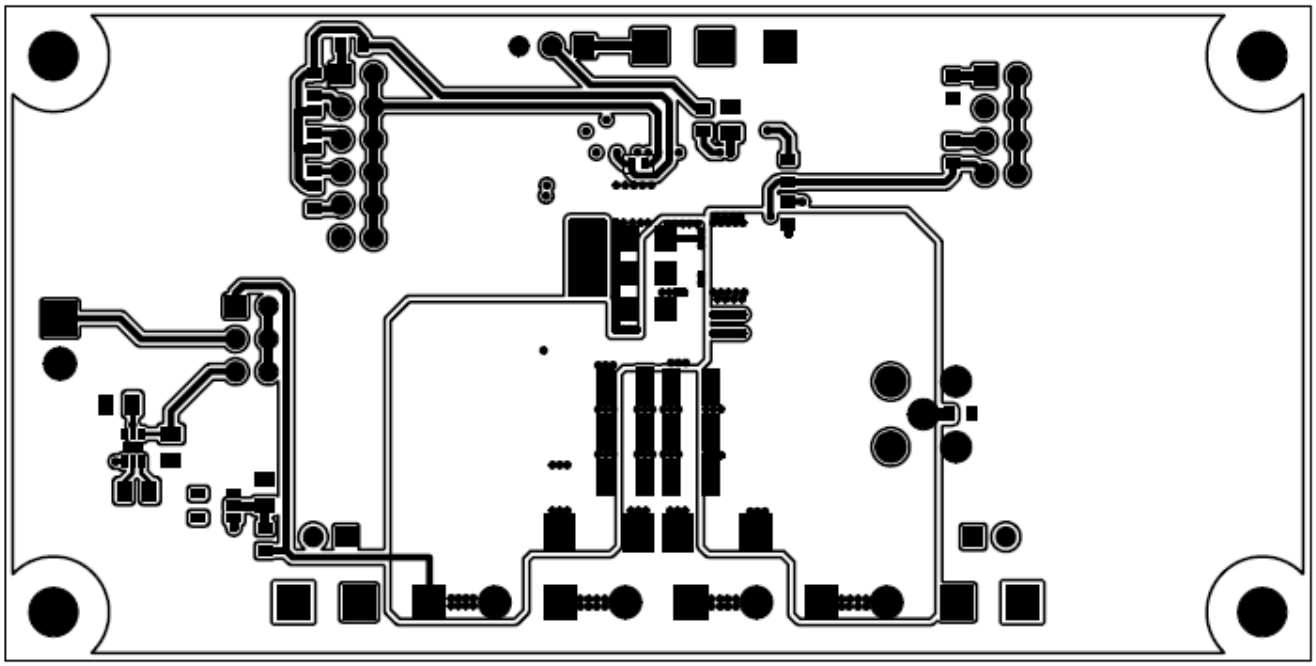

Figure 8-8. EVM Bottom Side Copper

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2014) to Revision B (December 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2
• Updated the user's guide title	2
• Edited user's guide for clarity	2

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