

## Product Summary

BV <sub>DSS</sub>	R <sub>DS(ON)</sub> Max	I <sub>D</sub> T <sub>C</sub> = +25°C
100V	16mΩ @ V <sub>GS</sub> = 10V	44A
	18mΩ @ V <sub>GS</sub> = 6V	41A

## Description

This new generation N-Channel Enhancement Mode MOSFET is designed to minimize R<sub>DS(ON)</sub>, yet maintain superior switching performance. This device is ideal for use in Notebook battery power management and load switch.

## Applications

- Motor Control
- DC-DC Converters
- Power Management

## Features

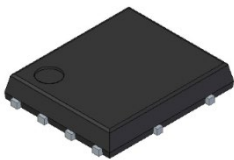
- Rated to +175°C – Ideal for High Ambient Temperature Environments
- 100% Unclamped Inductive Switching – Ensures More Reliable and Robust End Application
- High Conversion Efficiency
- Low R<sub>DS(ON)</sub> – Minimizes On-State Losses
- Low Input Capacitance
- Fast Switching Speed
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen- and Antimony-Free. “Green” Device (Note 3)**
- **For automotive applications requiring specific change control (i.e.: parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please refer to the related automotive grade (Q-suffix) part. A listing can be found at <https://www.diodes.com/products/automotive/automotive-products/>.**
- **This part is qualified to JEDEC standards (as references in AEC-Q) for High Reliability.** <https://www.diodes.com/quality/product-definitions/>

## Mechanical Data

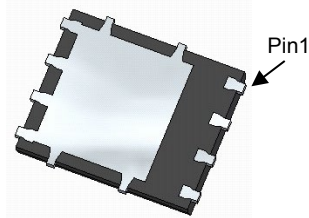
- Case: PowerDI<sup>®</sup>5060-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
- Terminals: Finish – Matte Tin Annealed over Copper Lead-Frame. Solderable per MIL-STD-202, Method 208 <sup>(e3)</sup>
- Weight: 0.097 grams (Approximate)

Site 1:

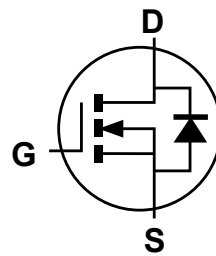
PowerDI5060-8



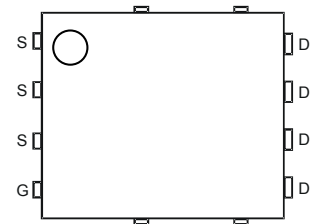
Top View



Bottom View



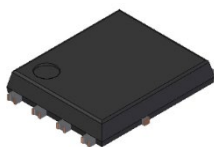
Internal Schematic



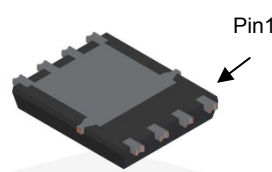
Top View  
Pin Configuration

Site 2:

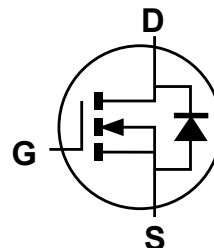
PowerDI5060-8 (SWP) (Type UX)



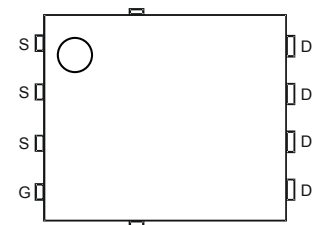
Top View



Bottom View



Internal Schematic

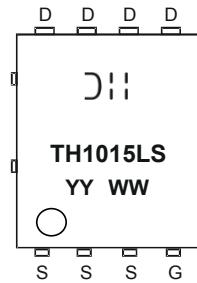


Top View  
Pin Configuration

**Ordering Information** (Note 4)

Part Number	Case	Packaging
DMTH10H015LPS-13	PowerDI5060-8	2,500/Tape & Reel

- Notes:
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
  2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

**Marking Information**


⤴⤵ = Manufacturer's Marking  
 TH1015LS = Product Type Marking Code  
 YYWW = Date Code Marking  
 YY = Last Digit of Year (ex: 20 = 2020)  
 WW = Week Code (01 to 53)

**Maximum Ratings** (@  $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			$V_{DSS}$	100	V
Gate-Source Voltage			$V_{GSS}$	$\pm 20$	V
Continuous Drain Current (Note 5) $V_{GS} = 10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	$I_D$	11 8	A
	Steady State	$T_C = +25^\circ\text{C}$ $T_C = +100^\circ\text{C}$	$I_D$	44 28	A
Pulsed Drain Current (10 $\mu\text{s}$ Pulse, Duty Cycle = 1%)			$I_{DM}$	120	A
Maximum Continuous Body Diode Forward Current (Note 5)			$I_S$	1.5	A
Avalanche Current (Note 7) L=3mH			$I_{AS}$	7.5	A
Avalanche Energy (Note 7) L=3mH			$E_{AS}$	85	mJ

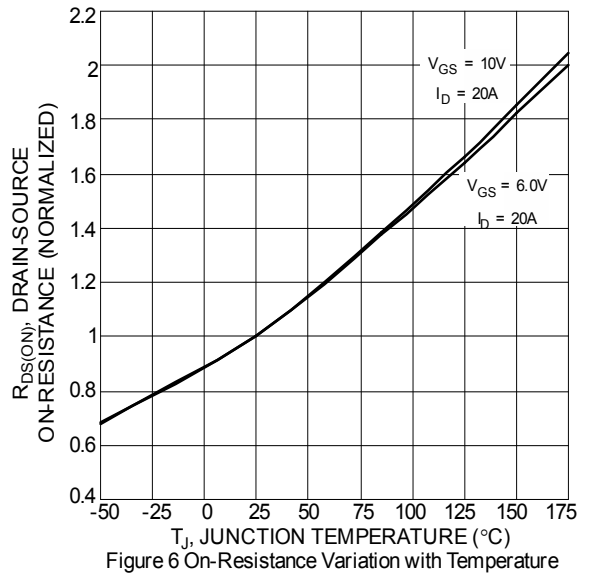
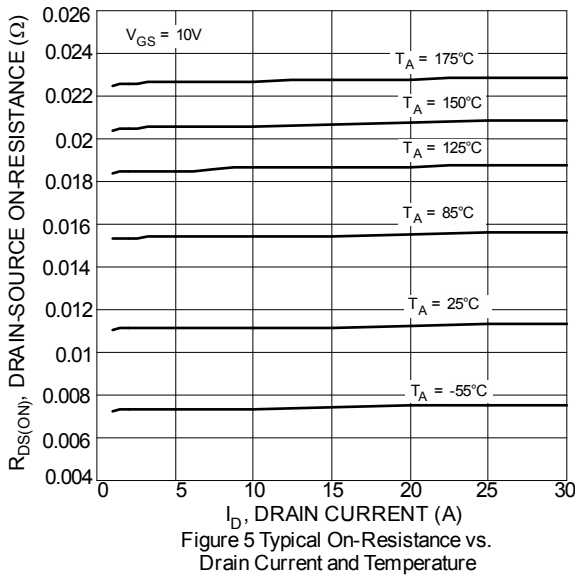
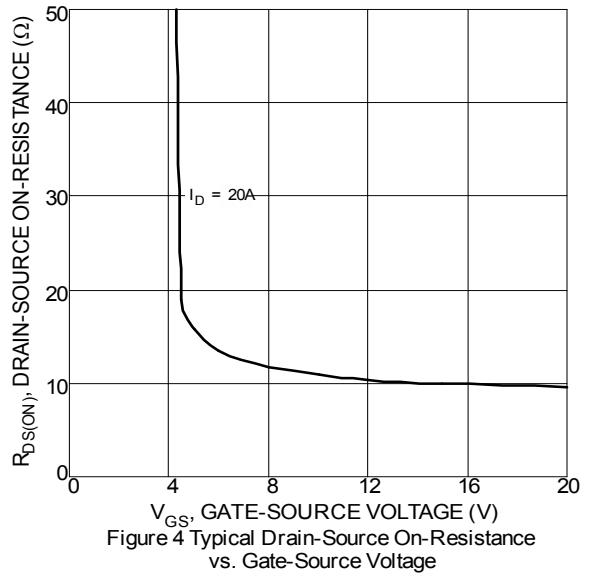
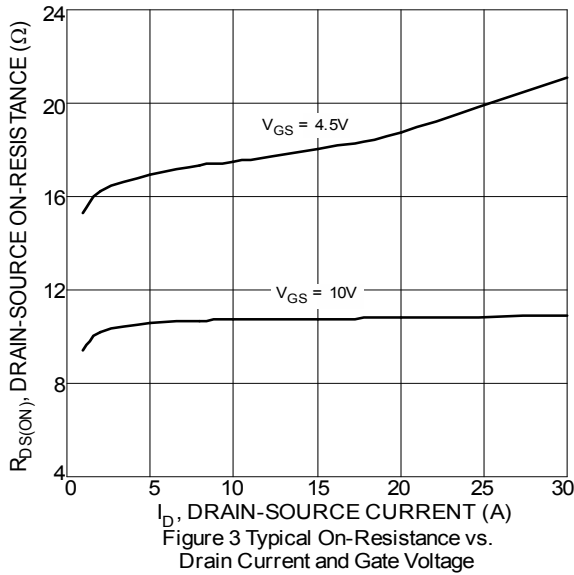
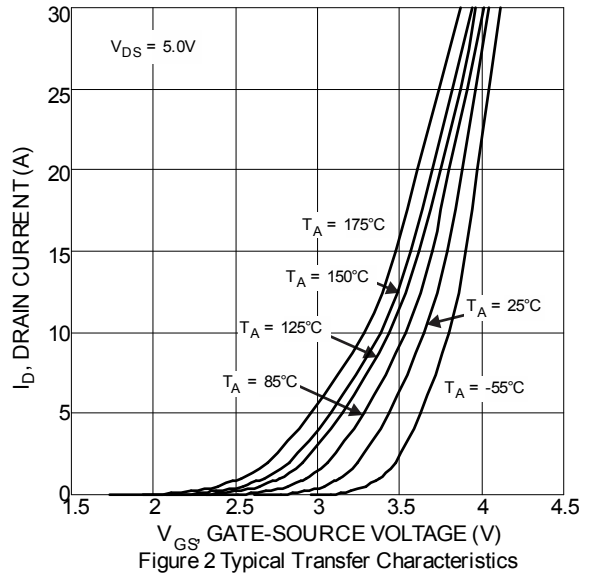
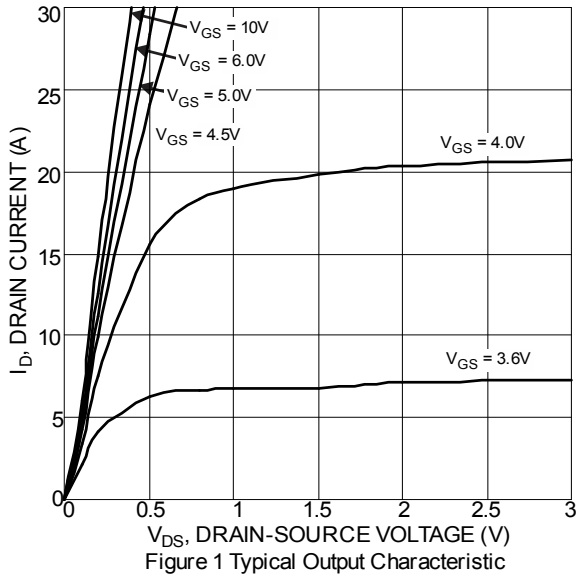
**Thermal Characteristics**

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	$T_A = +25^\circ\text{C}$	$P_D$	2.8	W
Thermal Resistance, Junction to Ambient (Note 5)		$R_{\theta JA}$	52	$^\circ\text{C/W}$
Total Power Dissipation	$T_C = +25^\circ\text{C}$	$P_D$	46	W
Thermal Resistance, Junction to Case		$R_{\theta JC}$	2.7	$^\circ\text{C/W}$
Operating and Storage Temperature Range		$T_J, T_{STG}$	-55 to +175	$^\circ\text{C}$

**Electrical Characteristics** (@  $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS</b> (Note 6)						
Drain-Source Breakdown Voltage	$BV_{DSS}$	100	—	—	V	$V_{GS} = 0V, I_D = 1mA$
Zero Gate Voltage Drain Current	$I_{DSS}$	—	—	1	$\mu A$	$V_{DS} = 80V, V_{GS} = 0V$
Gate-Source Leakage	$I_{GSS}$	—	—	$\pm 100$	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
<b>ON CHARACTERISTICS</b> (Note 6)						
Gate Threshold Voltage	$V_{GS(TH)}$	1.4	2	3	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	11	16	m $\Omega$	$V_{GS} = 10V, I_D = 20A$
		—	13.5	18		$V_{GS} = 6V, I_D = 20A$
		—	18.4	25		$V_{GS} = 4.5V, I_D = 5A$
Diode Forward Voltage	$V_{SD}$	—	0.9	1.3	V	$V_{GS} = 0V, I_S = 20A$
<b>DYNAMIC CHARACTERISTICS</b> (Note 7)						
Input Capacitance	$C_{ISS}$	—	1,871	—	pF	$V_{DS} = 50V, V_{GS} = 0V$ $f = 1MHz$
Output Capacitance	$C_{OSS}$	—	261	—		
Reverse Transfer Capacitance	$C_{RSS}$	—	7	—		
Gate Resistance	$R_G$	—	0.75	—	$\Omega$	$V_{DS} = 0V, V_{GS} = 0V, f = 1MHz$
Total Gate Charge	$Q_G$	—	33.3	—	nC	$V_{DD} = 50V, I_D = 10A,$ $V_{GS} = 10V$
Gate-Source Charge	$Q_{GS}$	—	6.9	—		
Gate-Drain Charge	$Q_{GD}$	—	5.1	—		
Turn-On Delay Time	$t_{D(ON)}$	—	6.5	—	ns	$V_{DD} = 50V, V_{GS} = 10V,$ $I_D = 10A, R_G = 6\Omega$
Turn-On Rise Time	$t_R$	—	7	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	19.7	—		
Turn-Off Fall Time	$t_F$	—	8.1	—		
Reverse Recovery Time	$t_{RR}$	—	37.9	—	ns	$I_F = 10A, di/dt = 100A/\mu s$
Reverse Recovery Charge	$Q_{RR}$	—	51.9	—	nC	

- Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
  6. Short duration pulse test used to minimize self-heating effect.
  7. Guaranteed by design. Not subject to product testing.



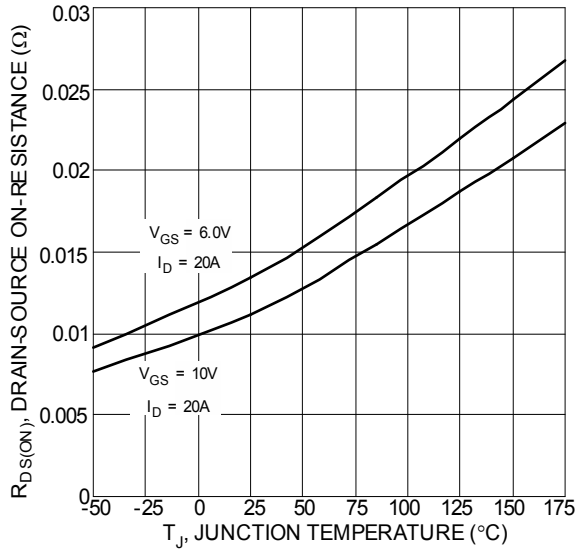


Figure 7 On-Resistance Variation with Temperature

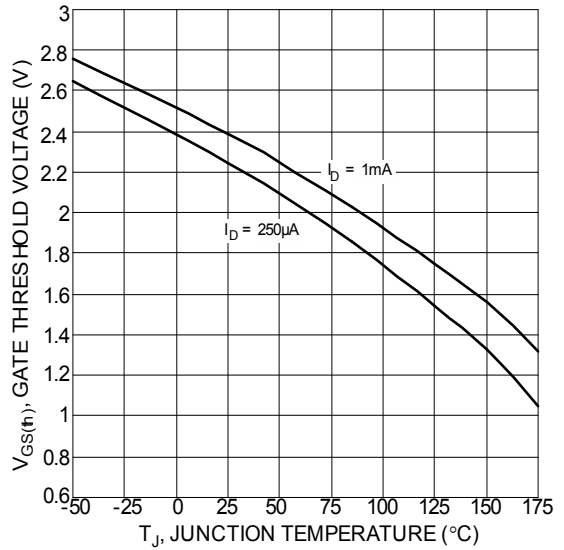


Figure 8 Gate Threshold Variation vs. Ambient Temperature

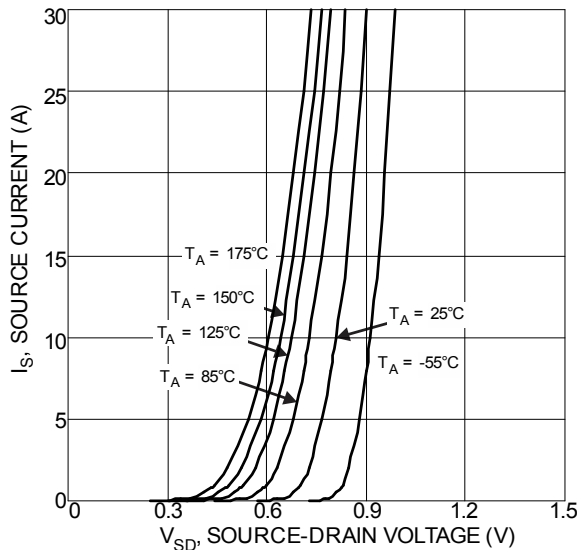


Figure 9 Diode Forward Voltage vs. Current

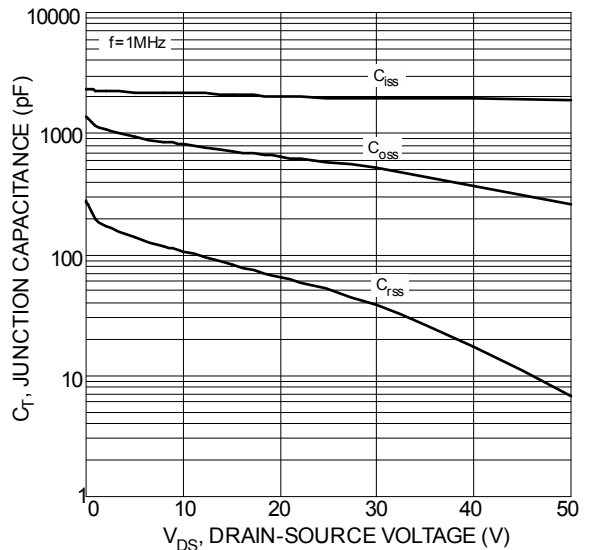


Figure 10 Typical Junction Capacitance

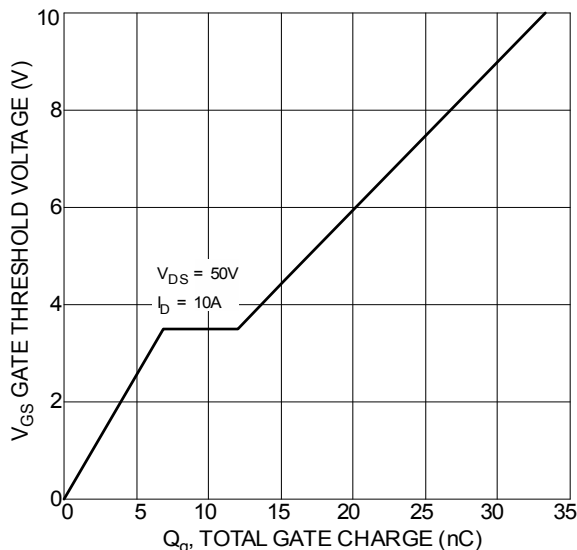


Figure 11 Gate Charge

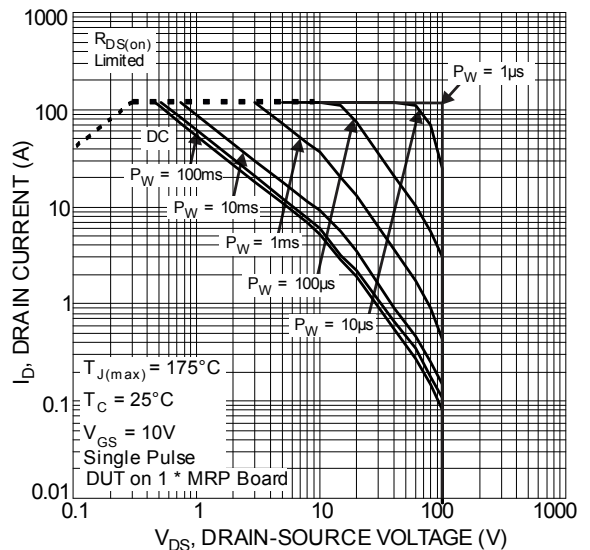


Figure 12 SOA, Safe Operation Area

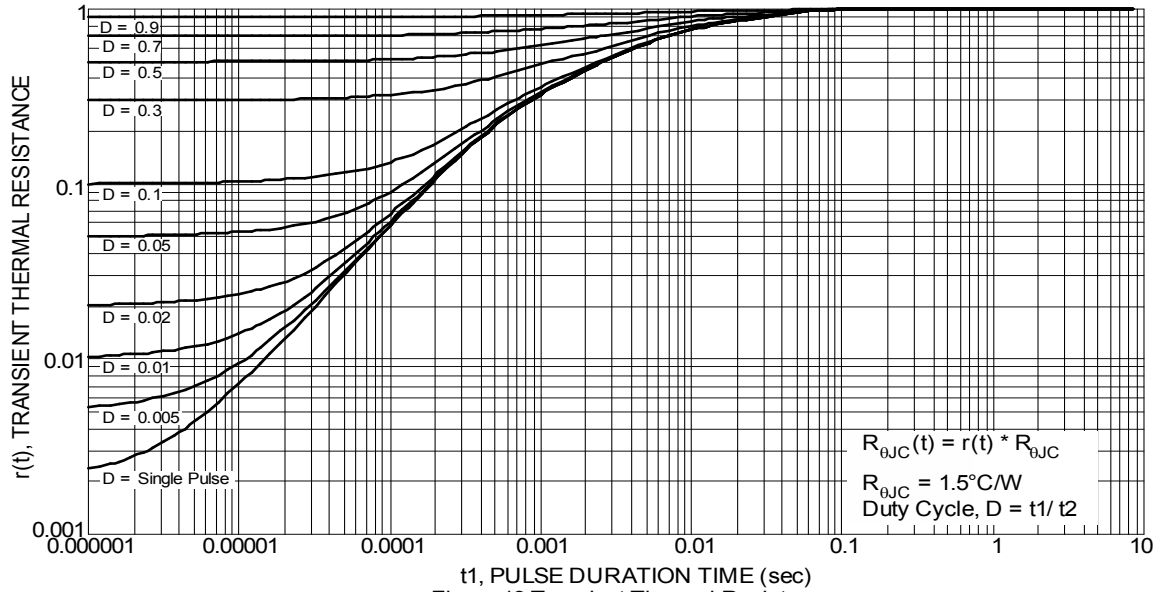


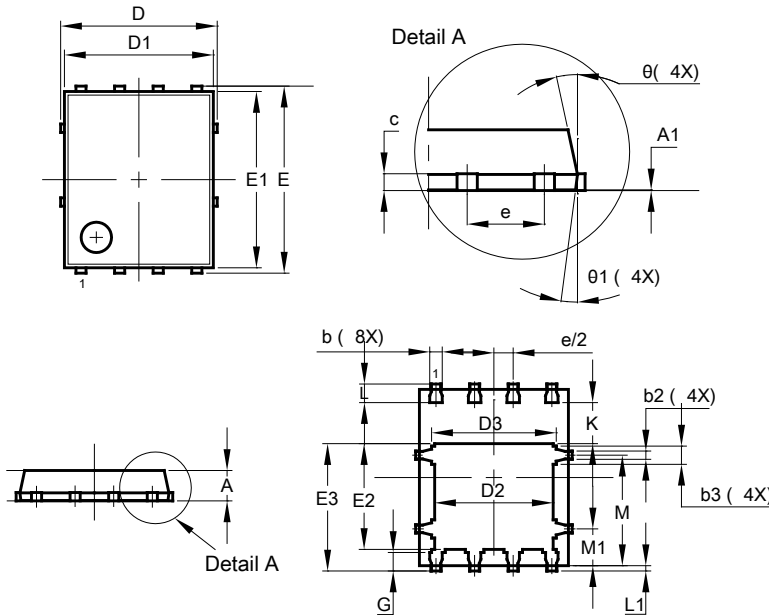
Figure 13 Transient Thermal Resistance

**Package Outline Dimensions**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

Site 1:

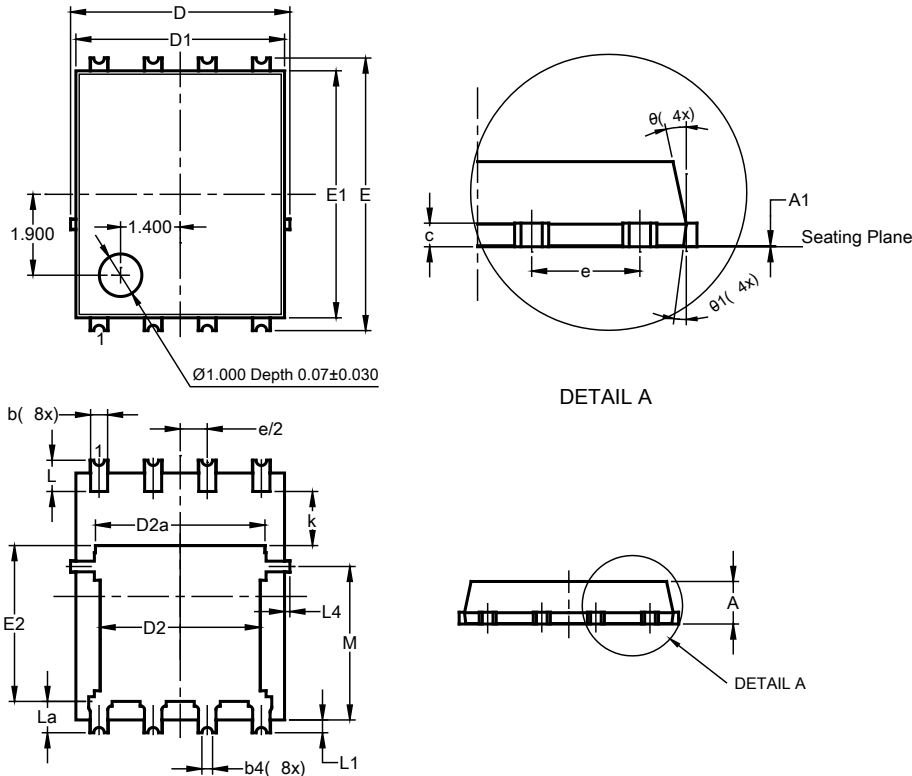
**PowerDI5060-8**



PowerDI5060-8			
Dim	Min	Max	Typ
A	0.90	1.10	1.00
A1	0.00	0.05	—
b	0.33	0.51	0.41
b2	0.200	0.350	0.273
b3	0.40	0.80	0.60
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.70	4.10	3.90
D3	3.90	4.30	4.10
E	6.15 BSC		
E1	5.60	6.00	5.80
E2	3.28	3.68	3.48
E3	3.99	4.39	4.19
e	1.27 BSC		
G	0.51	0.71	0.61
K	0.51	—	—
L	0.51	0.71	0.61
L1	0.100	0.200	0.175
M	3.235	4.035	3.635
M1	1.00	1.40	1.21
θ	10°	12°	11°
θ1	6°	8°	7°
All Dimensions in mm			

Site 2:

**PowerDI5060-8 (SWP) (Type UX)**

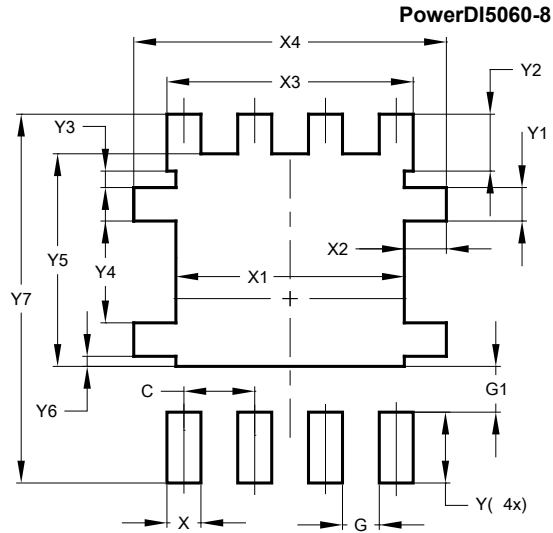


PowerDI5060-8 (SWP) (Type UX)			
Dim	Min	Max	Typ
A	0.90	1.10	1.00
A1	0	0.05	—
b	0.30	0.50	0.41
b2	0.20	0.35	0.25
b4	0.25REF		
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.56	3.96	3.76
D2a	3.78	4.18	3.98
E	6.40 BSC		
E1	5.60	6.00	5.80
E2	3.46	3.86	3.66
E2a	4.195	4.595	4.395
e	1.27BSC		
k	1.05	—	—
L	0.635	0.835	0.735
La	0.635	0.835	0.735
L1	0.200	0.400	0.300
L1a	0.050REF		
L4	0.025	0.225	0.125
M	3.205	4.005	3.605
θ	10°	12°	11°
θ1	6°	8°	7°
All Dimensions in mm			

**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

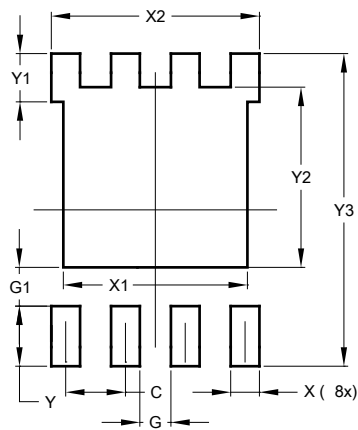
Site 1:



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	0.755
X3	4.420
X4	5.610
Y	1.270
Y1	0.600
Y2	1.020
Y3	0.295
Y4	1.825
Y5	3.810
Y6	0.180
Y7	6.610

Site 2:

**PowerDI5060-8 (SWP) (Type UX)**



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610



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