IR3888A/B OptiMOS™ IPOL

20 A/16 A single-voltage synchronous Buck regulator

Features

- Single 4.3 V to 17 V application or Wide Input Voltage Range from 2.0 V to 17 V with an External VCC
- Precision Reference Voltage (0.6 V +/- 0.5%)
- Enhanced Fast COT engine stable with Ceramic Output Capacitors and No External Compensation
- Forced Continuous Conduction Mode
- The Switching Frequency is set at 800 kHz internally
- Monotonic Start-Up with an internal Soft-Start Time & Enhanced Pre-Bias Start-Up
- Thermally Compensated Internal Over Current Protection
- Enable input with Voltage Monitoring Capability & Power Good Output
- Thermal Shut Down
- Operating Temp: -40 °C $< T_j <$ 125 °C
- Small Size: 6 mm x 5 mm PQFN
- Halogen-free and RoHS2 Compliant with Exemption 7a

Potential applications

- Server Applications
- Storage Applications
- Telecom & Datacom Applications
- Distributed Point of Load Power Architectures

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Description

The IR3888A/B is an easy-to-use, fully integrated dc - dc Buck regulator. The onboard PWM controller and OptiMOS™ FETs with integrated bootstrap diode make IR3888A/B a small footprint solution, providing high efficiency power delivery. Furthermore, it uses a fast Constant On-Time (COT) control scheme, which simplifies design efforts and achieves fast control response.

The IR3888A/B has an internal low dropout voltage regulator, allowing operation with a single supply. It can also operate with an external bias supply, extending the operating input voltage (PVin) range.

It features important protection functions, such as pre-bias start-up, thermally compensated current limits, over voltage and under voltage protection, and thermal shutdown to give required system level security in the event of fault conditions.

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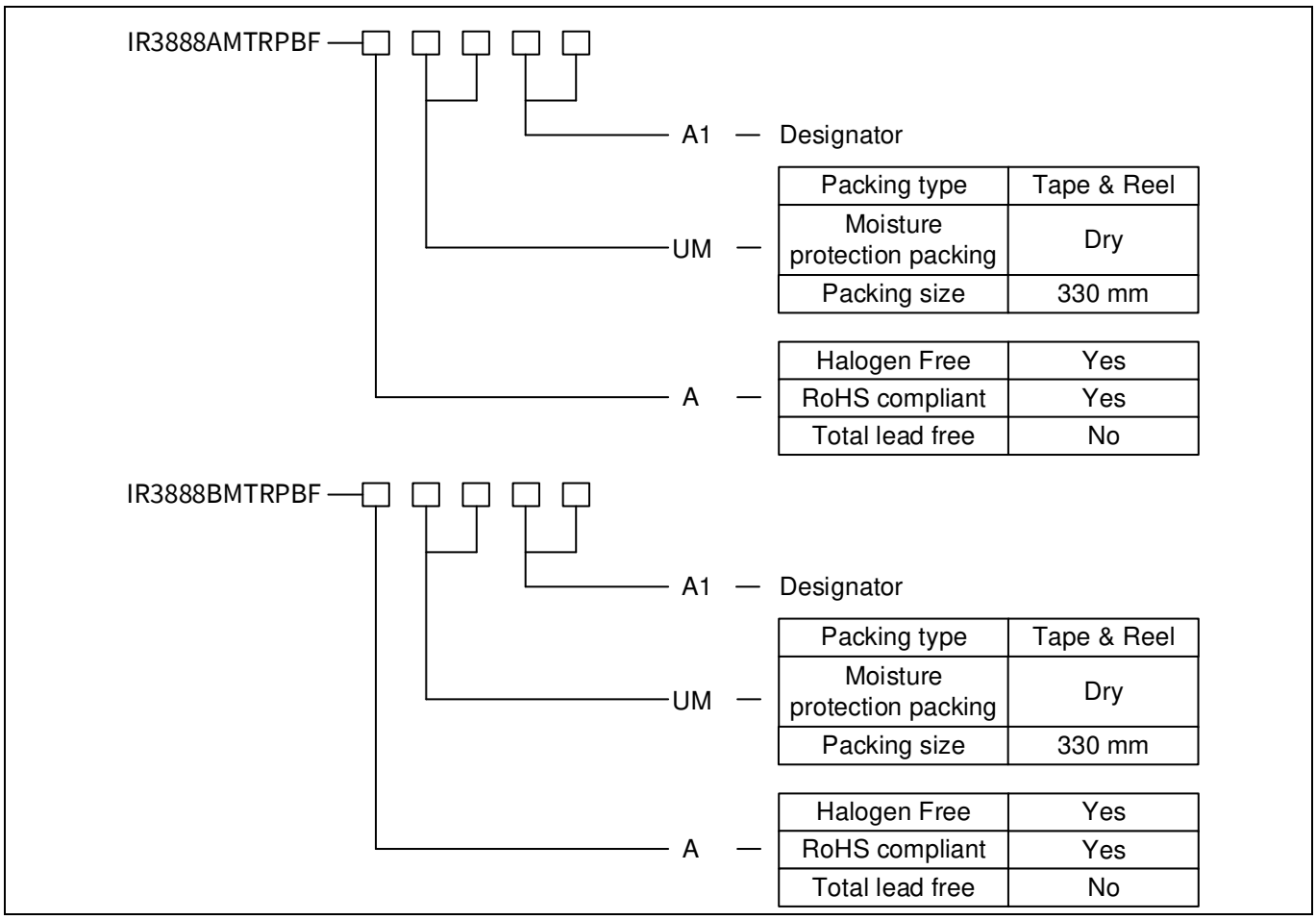
1 Ordering information

1. Ordering Information

Sales Product Name	Package Type	Standard Pack Form and Qty		Orderable Part Number
IR3888AMTRPBF	QFN 6 mm x 5 mm	Tape and Reel	5000	IR3888AMTRPBFAUMA1
IR3888BMTRPBF	QFN 6 mm x 5 mm	Tape and Reel	5000	IR3888BMTRPBFAUMA1



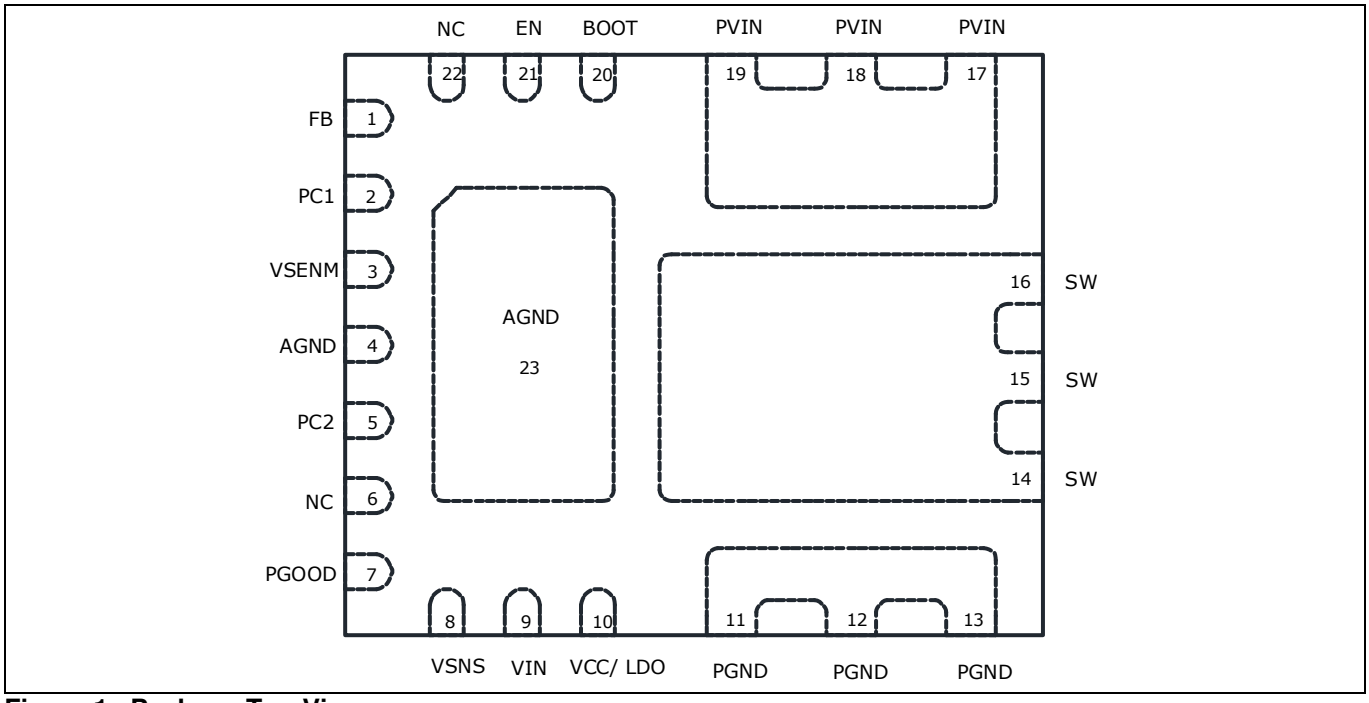


Figure 1 Package Top View

2 Functional block diagram

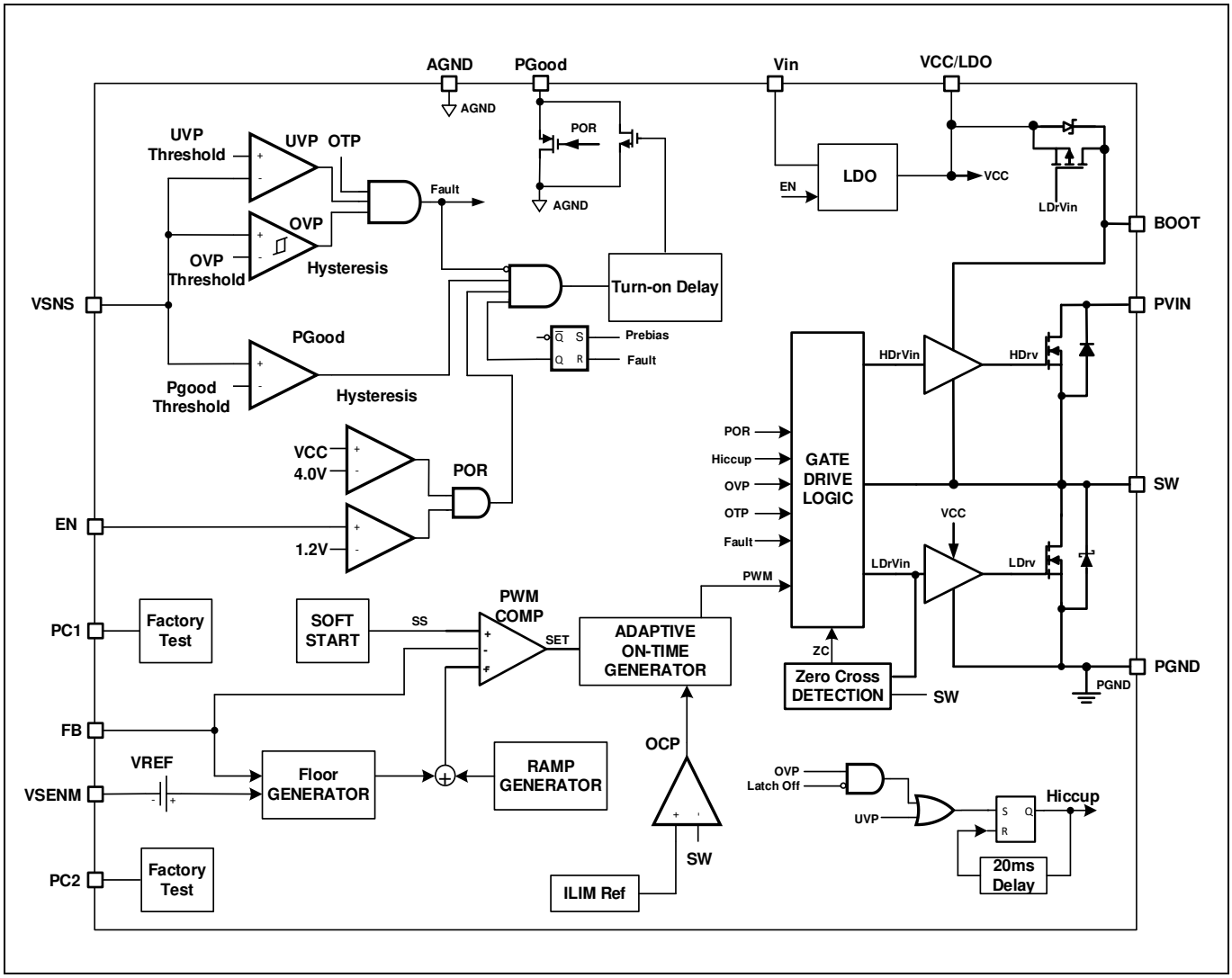


Figure 2 Block diagram

3 Typical application diagram

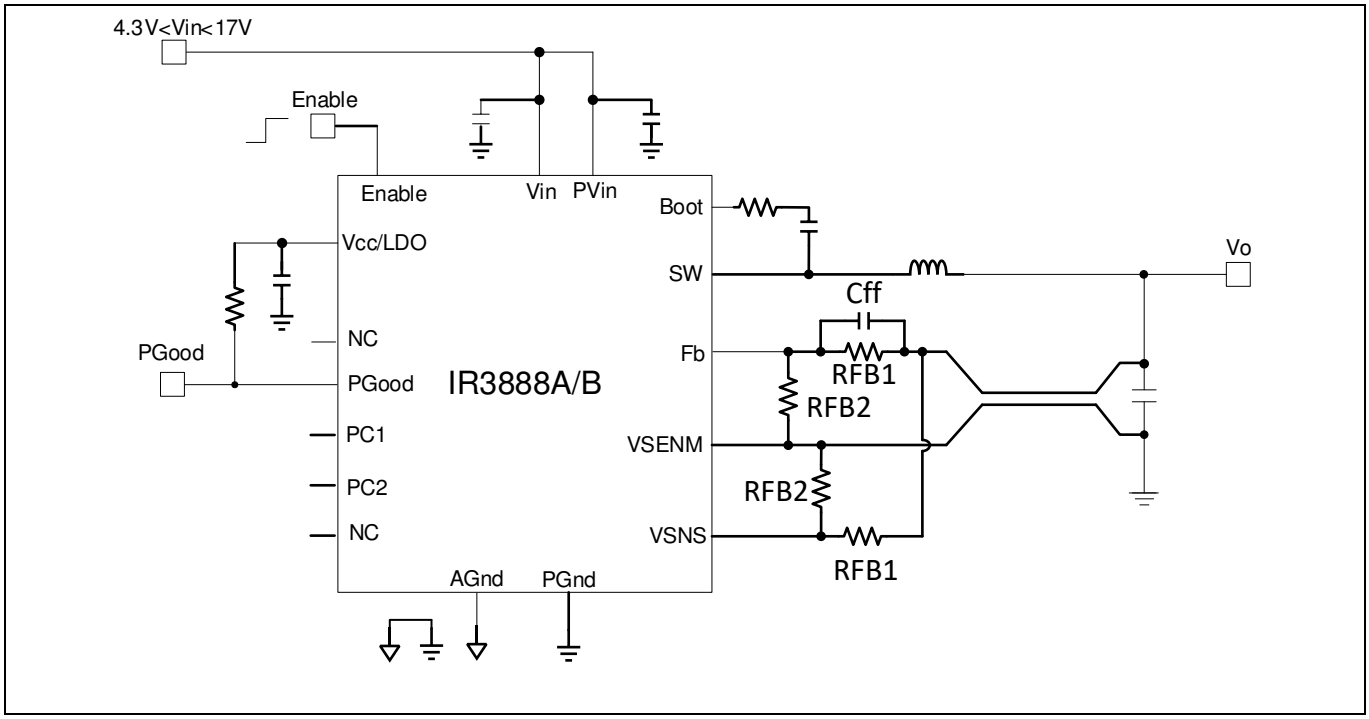


Figure 3 IR3888A/B basic application circuit

4 Pin descriptions

Note: *I = Input, O = Output*

Pin#	Pin Name	I/O	Type	Pin Description
1	Fb	I	Analog	Output voltage feedback pin. Connect this pin to the output of the regulator via a resistor divider to set the output voltage.
2	PC1	-	Analog	For factory test only. Can be left floating, connected to VCC or connected to GND directly or through a resistor.
3	VSENM	-	Analog	This pin provides the return connection for a pseudo remote voltage sensing. The feedback resistor divider should be connected to this pin. It is also used as ground for the internal reference voltage.
4, 23	AGND	-	Ground	Signal ground for internal circuitry except for internal reference voltage. AGND and PGND are not internally connected. AGND and PGND must be connected on PCB with a single ground connection.
5	PC2	-	Analog	For factory test only. Can be left floating, connected to GND directly or through a resistor.
6, 22	NC	-	Not connected	Not connected internally. Can be left floating or tied to other signals as needed.
7	PGood	O	Analog	Power Good status output pin is open drain. Connect a pull up resistor from this pin to VCC or to an external bias voltage, e.g. a 50 kΩ pull-up resistor for a PGood bias voltage of 3.3 V.
8	VSNS	I	Analog	Sense pin for over voltage protection and PGood. Tie this pin to Vout using a resistor divider. Alternatively, tie this pin to FB pin directly.
9	VIN	I	Power	Input voltage for an Internal LDO. A 4.7 µF capacitor should be connected between this pin and PGnd. If an external supply is connected to VCC/LDO pin, this pin should be shorted to VCC/LDO pin and a 10 µF ceramic capacitor can be shared with Vin and VCC/LDO pin.
10	VCC/LDO	I/O	Power	Input bias for an external VCC voltage or output of the internal LDO. A 2.2 µF - 10 µF ceramic capacitor is recommended to use between VCC, and the Power ground (PGND).
11, 12, 13	PGND	-	Ground	Power Ground. Should be connected to the system's power ground plane.
14, 15, 16	SW	O	Power	Switch Node. Connect to an output inductor.
17, 18, 19	PVin	I	Power	Input supply for the power stage.
20	Boot	I	Analog	Supply voltage for the high side driver. Connect this pin to the SW pin through a bootstrap capacitor. A

Pin#	Pin Name	I/O	Type	Pin Description
				high temperature (X7R) 0.1 µF or greater value ceramic capacitor is recommended.
21	EN	I	Analog	Enable pin to turn the IC on and off.

5 Absolute maximum ratings

Absolute maximum ratings

Description	Min	Max	Unit	Conditions
PVin, Vin and En to PGND	-0.3	25	V	Note **1**
PVin to SW	-0.3 V(dc) , below -5 V for 5 ns	25 V(dc), above 32 V for 2 ns	V	
VCC to PGND	-0.3	6	V	Note **1**
Boot to PGND	-0.3 V(dc), below -0.3 V for 5 ns	29	V	Note **1**
SW to PGND	-0.3 (dc), below -5 V for 5 ns	25 V(dc), above 32 V for 2 ns	V	Note **1**
Boot to SW	-0.3	6 V(dc), 7 V for 5 ns	V	
Fb, PGood, PC1, PC2 and VSNS to AGND	-0.3	6	V	Note **1**
PGnd to AGND	-0.3	0.3	V	
VSENM to AGND	-0.3	0.3	V	
Storage Temperature Range	-55	150	°C	
Junction Temperature Range	-40	150	°C	

Note:

1. PGND, VSENM, and AGND pin are connected together

Attention: ***Stresses beyond these listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.***

6 Thermal Characteristics

6.1 Thermal Characteristics

Description	Symbol	Values	Test Conditions
Junction to Ambient Thermal Resistance	θ_{JA}	17 °C/W	Note **2**
Junction to PCB Thermal Resistance	$\theta_{JC\text{-}PCB}$	3.5 °C/W	Note **3**
Junction to Case Top Thermal Resistance	θ_{JC}	34°C/W	

Note:

2. *Thermal resistance is measured with components mounted on a standard EVAL_3888_1Vout demo board in free air.*
3. *Thermal resistance is based on the board temperature near the PVin pin.*

7 Electrical specifications

7.1 Recommended operating conditions

Description	Min	Max	Unit	Note
PV_{in} Voltage Range with External VCC	2	17	V	Note **4**, Note **5**
PV_{in} Voltage Range with Internal LDO	4.5	17	V	Note **5**, Note **6 & 10**
VCC Supply Voltage Range	4.3	5.5	V	Note **4**, Note **7**
Typical Output Voltage Range	0.6	6	V	Note **8**, Note **9**
Continuous Output Current Range for IR3888A		20	A	Note **9**
Continuous Output Current Range for IR3888B		16	A	
Typical Switching Frequency	800		kHz	
Operating Junction Temperature	-40	125	°C	

Note:

4. *V_{in} is shorted to VCC and use an external bias voltage.*
5. *A common practice is to have 20% margin on the maximum SW node voltage in the design. For applications requiring PV_{in} equal to or above 14 V, a small resistor in series with the Boot pin might be needed to ensure the maximum SW node spike voltage does not exceed 20 V. Alternatively, a snubber can be used at the SW node to reduce the SW node spike.*
6. *V_{in} is connected to PV_{in} and the internal LDO is used. For single-rail applications with the internal LDO, and PV_{in} =V_{in} = 4.3 V-5.4 V, the internal LDO may enter dropout mode. OCP limits can be reduced due to the lower VCC voltage. Please refer to **Section 12.7** for more detailed design guidelines.*
7. *The IR3888A/B is designed to function with VCC down to 4.2 V, however, electrical specifications such as OCP limits may be degraded.*
8. *The maximum output voltage is also limited by the minimum off-time. Please refer to **Section 12.13** for details. Also note that OCP limit may be degraded when off-time is close to the minimum off-time.*
9. *Refer to **Section 9** for maximum output current rating of IR3888A at different ambient temperatures using internal LDO. IR3888B has the same thermal performance as IR3888A, but the maximum output current is reduced by a lower over current limit. Lower VCC voltage can result in higher $R_{DS(on)}$ and therefore require more thermal derating.*
10. *The maximum LDO output current must be limited within 50 mA for operations requiring full operating temperature range of -40 °C ≤ T_J ≤ 125 °C. **Figure 6** shows the maximum LDO output current capability over junction temperature. Thermal de-rating may be needed at an elevated ambient temperature to ensure the junction temperature within the recommended operating range.*

7.2 Electrical characteristics

Note: Unless otherwise specified, specifications apply over, 4.5 V ≤ Vin = PVin ≤ 17 V, in 0 °C < T_J < 125 °C. Typical values are specified at Ta = 25 °C.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Stage						
Top Switch (IR3888A & IR3888B)	$R_{ds(on)\_Top}$	V_{Boot} – V_{sw}= 5.0 V, T_j=25 °C		3.3		mΩ
Bottom Switch (IR3888A & IR3888B)	$R_{ds(on)\_Bot}$	VCC = 5.0 V, T_j =25 °C		2.1		mΩ
Bootstrap Forward Voltage		I(Boot) = 25 mA		370	600	mV
SW float voltage	V_{SW}	EN = 0 V			300	mV
		EN = high, No Switching			300	mV
Dead Band Time	T_{db}	SW node falling edge, Io = 16 A & 20 A, Internal LDO, T_j = 25 °C, Note **11**		10		ns
		SW node rising edge, Io = 16 A & 20 A, Internal LDO, T_j = 25 °C, Note **11**		8		ns
Supply Current						
Vin Supply Current (standby)	$I_{in(Standby)}$	EN = Low, No Switching		4	10	µA
Vin Supply Current (static)	$I_{in(Static)}$	EN=2 V, No Switching		2.3	4	mA
Soft Start						
Soft Start Ramp Rate	SS rate		0.1	0.15	0.21	mV/µs
Feedback Voltage						
Feedback Voltage	V_{FB}			0.6		V
Accuracy		0°C < T_j < 85 °C, Note **12**	-0.5		+0.5	%
		-40 °C < T_j < 125 °C, Note **12**	-1		1	%
V_{FB} Input Current	IV_{FB}	V_{FB}=0.6 V, T_j=25 °C	-0.15	0	+0.15	µA
On-Time Timer Control						
On Time	T_{on}	Vin=12 V, Vo=1 V, Note **13**		114		ns
Minimum On-Time	$T_{on\ (Min)}$	Vin=12 V, Vo=0 V		23	32	ns
Minimum Off-Time	$T_{off\ (Min)}$	T_j=25 °C, V_{FB}=0 V		270	360	ns
VCC LDO Output						
Output Voltage	VCC	5.5 V ≤ Vin ≤ 17 V, when Icc =50 mA, Cload = 2.2 µF	4.7	5.0	5.3	V
VCC Dropout	VCC_drop	Vin = 4.3 V, Icc=50 mA, Cload=2.2 µF			300	mV
Short Circuit Current	I_{short}	5.5 V ≤ Vin ≤ 17 V		90		mA
Under Voltage Lockout						
VCC-Start Threshold	Vcc_UVLO_Start	VCC Rising Trip Level	3.8	4.0	4.2	V
VCC-Stop Threshold	Vcc_UVLO_Stop	VCC Falling Trip Level	3.6	3.8	4.0	V
Enable-Start-Threshold	En_UVLO_Start	ramping up	1.14	1.2	1.36	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Enable-Stop-Threshold	En_UVLO_Stop	ramping down	0.9	1	1.06	
Input Impedance	R_{EN}		500	1000	1500	kΩ
Over Current Limit						
Current Limit Threshold (Valley current)	Ioc	IR3888A, Tj = 25 °C, PVin = 12 V, Internal LDO, note **14**	21.8	23.8	24.8	A
		IR3888B, Tj = 25 °C, PVin = 12 V, Internal LDO, note **14**	17.1	18.9	20.0	
Over Voltage Protection						
OVP Trip Threshold	OVP_Vth	VSNS Rising	115	121	125	% Vref
		VSNS Falling, OVP hysteresis	110	114	120	
OVP Protection Delay	OVP_Tdly			8		µs
Under Voltage Protection						
UVP Trip Threshold	UVP_Vth	VSNS Falling	65	70	75	% Vref
UVP Protection Delay	UVP_Tdly			2		µs
Hiccup Blanking Time	Tblk_Hiccup			20		ms
Power Good						
Pgood Turn on Threshold	VPG(upper)	VSNS Rising	85	91	95	% Vref
Pgood Turn off Threshold	VPG(lower)	VSNS Falling	80	84	90	% Vref
Pgood Sink Current	I_{PG}	PG = 0.5 V, En = 2 V	2.5	5		mA
Pgood Voltage Low	$V_{PG(low)}$	Vin = VCC =0 V, Rpull-up = 50 kΩ to 3.3 V		0.3	0.5	V
Pgood Turn on Delay	$V_{PG(on)\_Dly}$	VSNS Rising, see VPG(upper)		2.5		ms
Pgood Comparator Delay	$V_{PG(comp)\_Dly}$	VSNS < VPG(lower) or VSNS > VPG(upper)	1	2	3.5	µs
Pgood Open Drain Leakage Current		PG = 3.3 V			1	µA
Thermal Shutdown						
Thermal Shutdown		Note **11**	105	115	125	°C
Hysteresis		Note **11**		15		

Note:

11. Guaranteed by construction and not tested in production

12. Cold and hot temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.

13. The Ton is trimmed so that 800 kHz is achieved at around 10A load current using EVAL_3888_1Vout demo board.

*14. The specified OCP limits refer to the valley of the inductor current when OCP is tripped. For more detailed design guideline, please refer to Section **12.8**.*

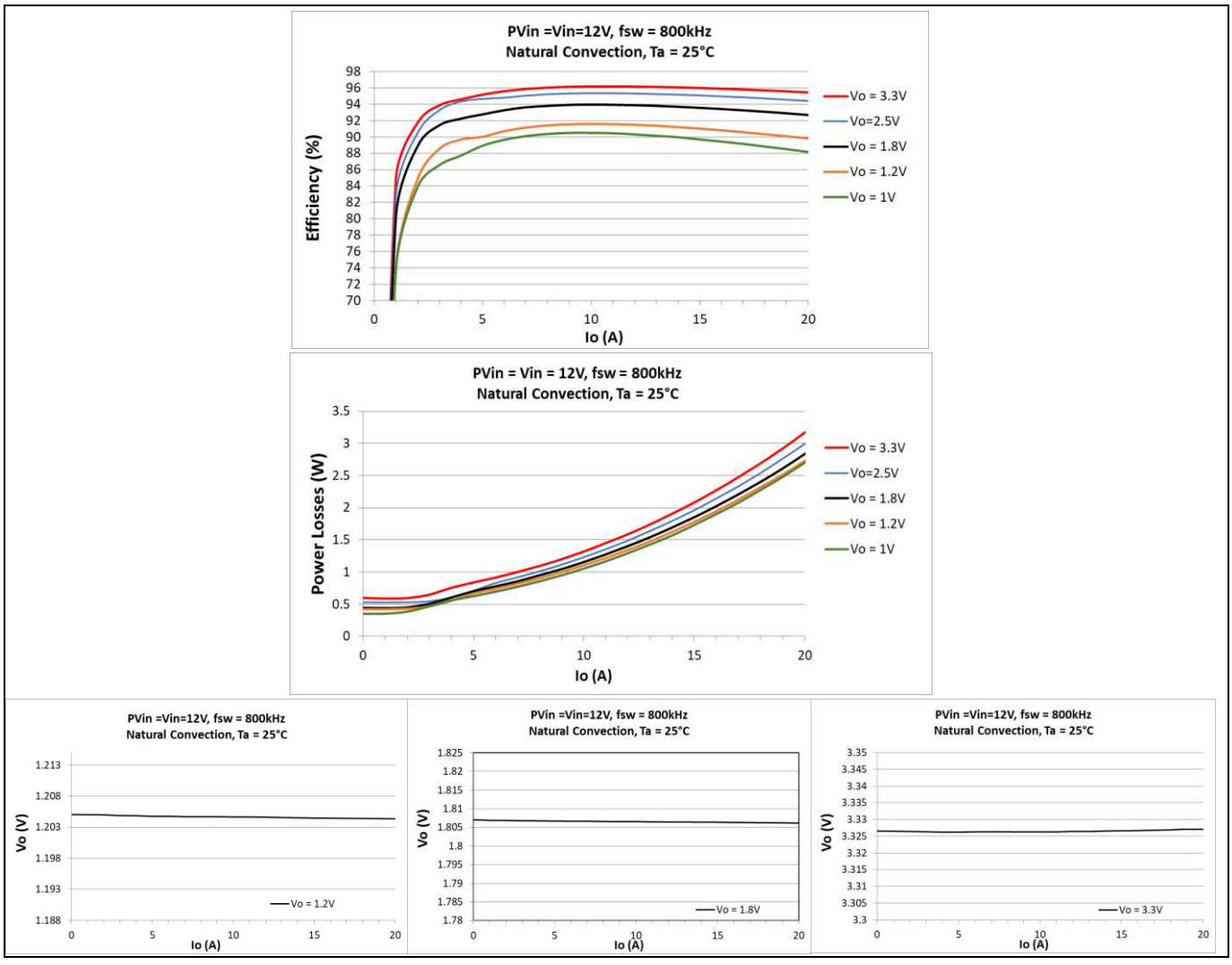
8 Typical efficiency and power loss curves

8.1 PV_{in} = V_{in} = 12 V, F_{sw} = 800 kHz

PV_{in} = V_{in} = 12 V, VCC = Internal LDO, Io = 0 A-20 A, F_{sw} = 800 kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of IR3888A/B, the inductor losses, the losses of the input and output capacitors, and PCB trace losses. The table below shows the inductors used for each of the output voltages in the efficiency measurement.

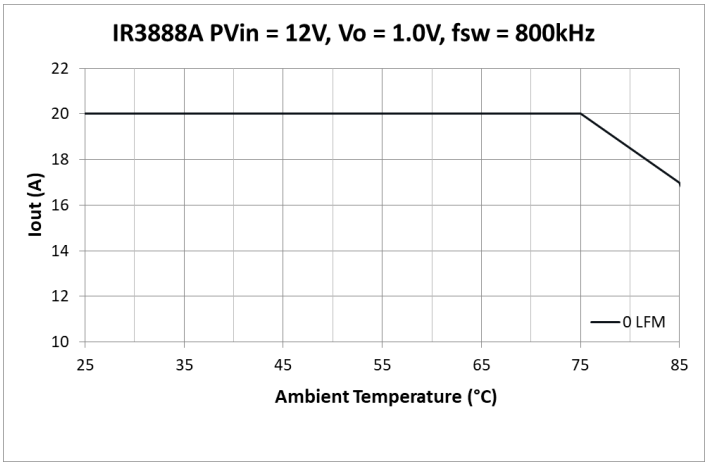
Table 1 Inductors for PV_{in}=V_{in}=12 V, F_{sw} = 800 kHz

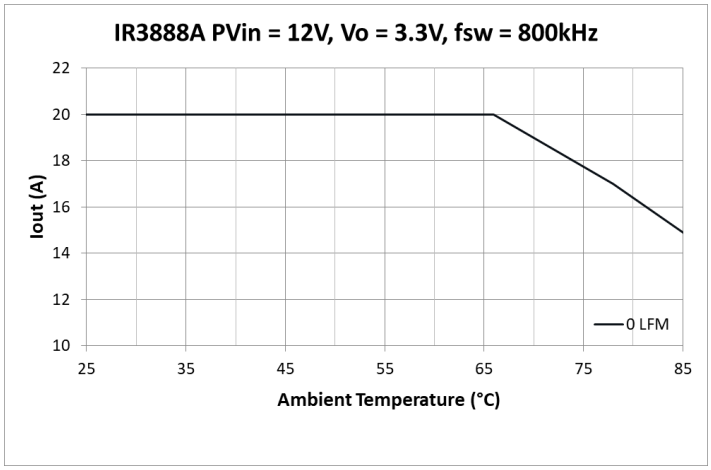
Vout (V)	Lout (nH)	P/N	DCR (mΩ)	Size (mm)
1.0	150	HCB138380D-151 (Delta)	0.15	12.4 x 8.3 x 8
1.2	150	HCB138380D-151 (Delta)	0.15	12.4 x 8.3 x 8
1.8	220	FP1008R5-R220-R (Cooper)	0.17	10.8 x 8 x 8
2.5	220	FP1008R5-R220-R (Cooper)	0.17	10.8 x 8 x 8
3.3	350	HCBD101195-351(Delta)	0.35	10.1 x 11.4 x 9.5



9 Thermal De-rating curves

Measurement is done on Evaluation board of EVAL_3888_1Vout. PCB is a 6-layer board with 1.5 ounce Copper for top and bottom layer and 2 ounce Copper for the inner layers, FR4 material, size 3.0”x3.75”.





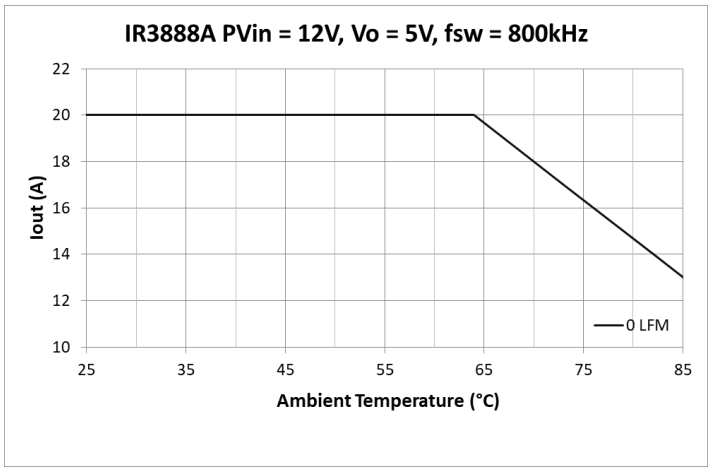
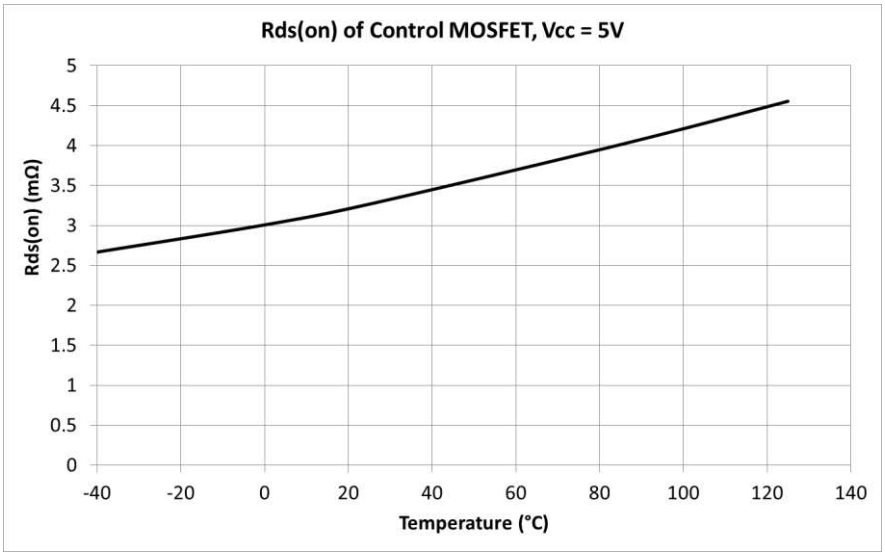


Figure 4 Thermal de-rating curves, PV_{in} = 12 V, V_{out}=1.0 V/3.3 V/5 V, f_{sw} = 800 kHz, VCC = Internal LDO

10 $R_{DS(ON)}$ of MOSFET Over Temperature



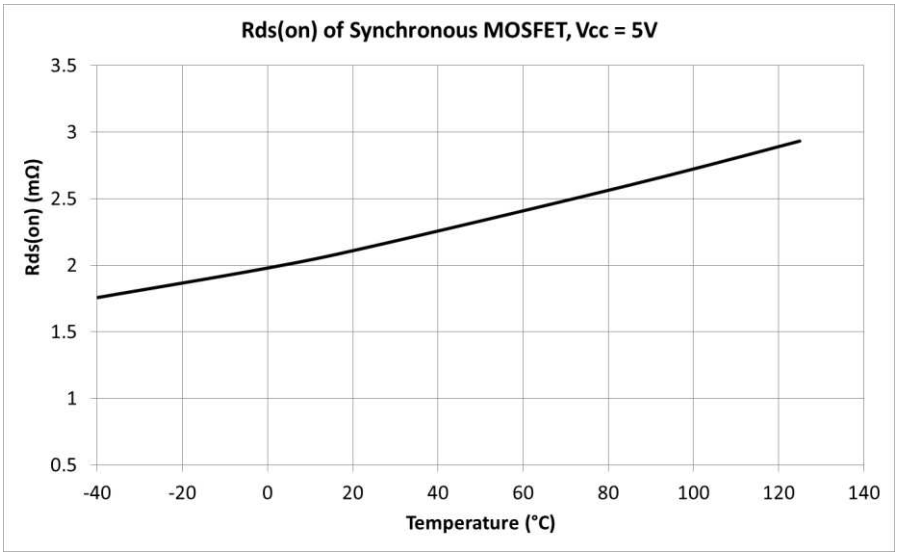


Figure 5 $R_{DS(on)}$ of MOSFETs over Junction Temperature

11 Typical operating characteristics (-40 °C ≤ T_j ≤ +125 °C)

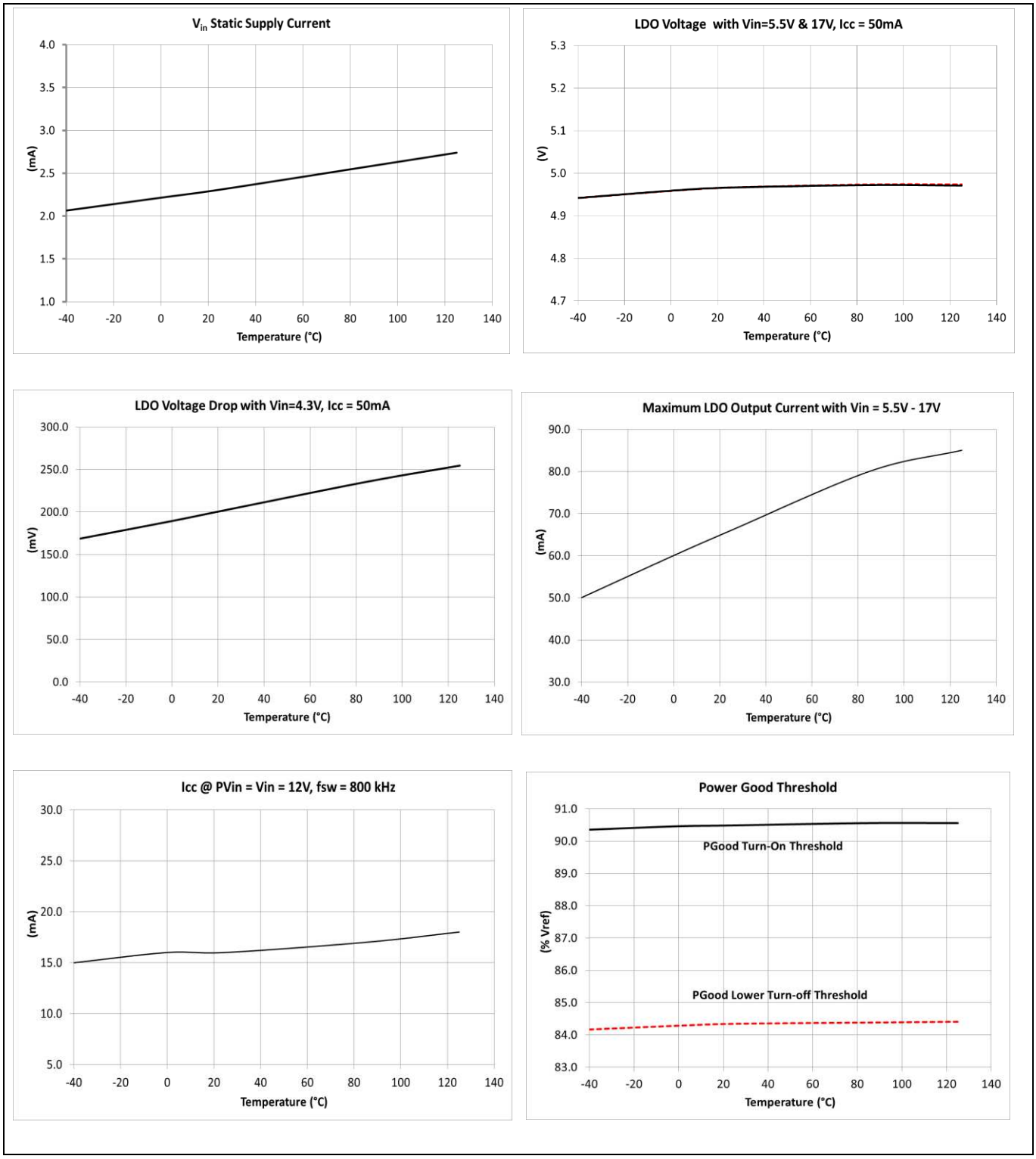


Figure 6 Typical operating characteristics (set 1 of 2)

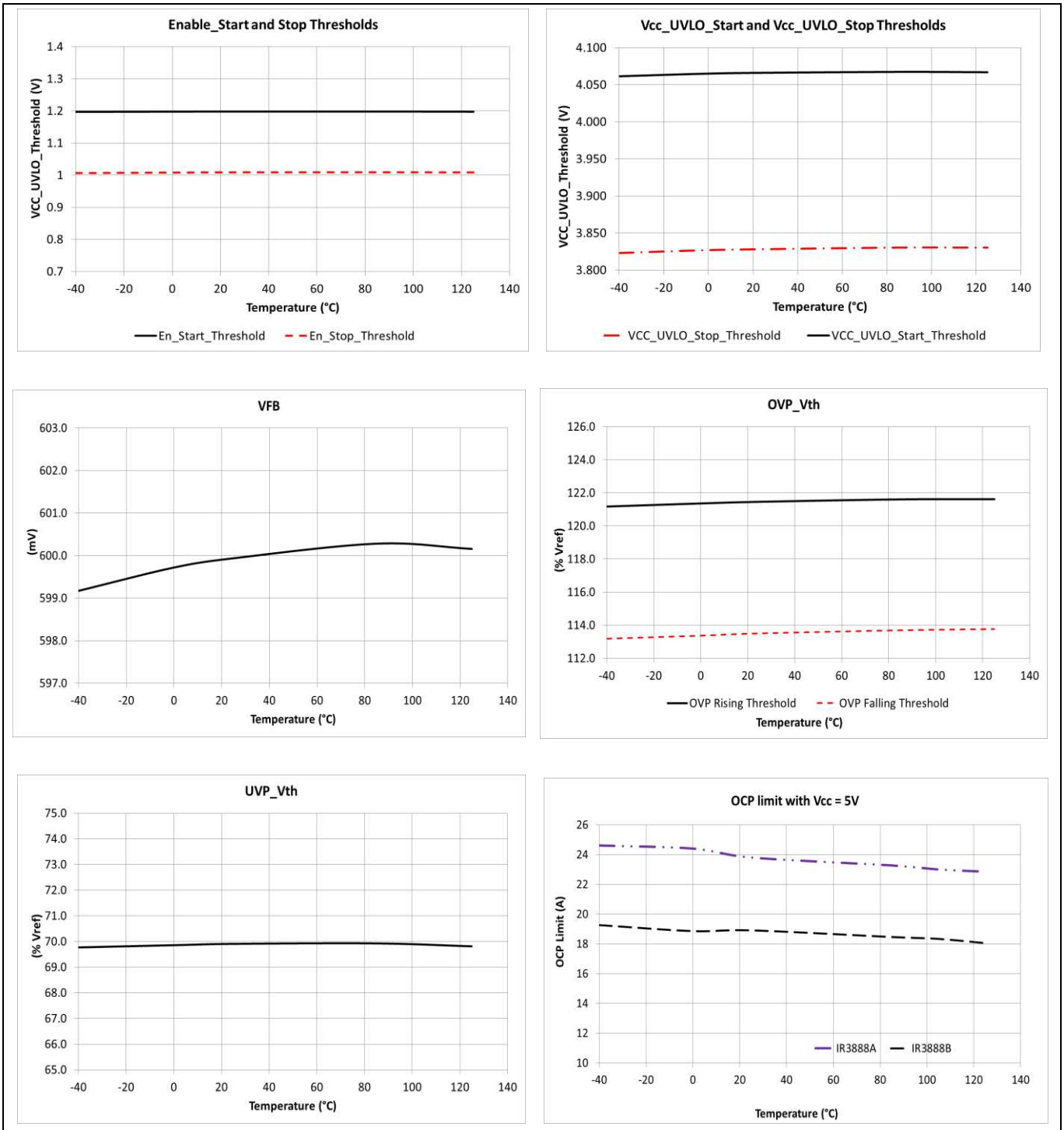


Figure 7 Typical operating characteristics (set 2 of 2)

12 Theory of operation

12.1 Fast Constant On-Time Control

The IR3888A/B features a proprietary Fast Constant On-Time (COT) Control, which can provide fast load transient response, good output regulation and minimize design effort. Fast COT control compares the output voltage, V_o, to a floor voltage combined with an internal ramp signal. When V_{out} drops below that signal, a PWM signal is initiated to turn on the high-side FET for a fixed on-time. The floor voltage is generated from an internally compensated error amplifier, which compares the Vout with a reference voltage. Compared to the traditional COT control, Fast COT control significantly improves the Vout regulation.

12.2 Enable

EN pin controls the on/off of the IR3888A/B. An internal Under Voltage Lock-Out (UVLO) circuit monitors the EN voltage. When the EN voltage is above an internal threshold, the internal LDO starts to ramp up. When the VCC/LDO voltage rises above the VCC_UVLO_Start threshold, the soft-start sequence starts. The EN pin can be configured in three ways, as shown in **Figure 8**. With configuration 2, the Enable signal is derived from the PVin voltage by a set of resistive divider, REN1 and REN2. By selecting different divider ratios, users can program a UVLO threshold voltage for the bus voltage. This is a very desirable feature because it prevents the IR3888A/B from operating until PVin is higher than a desired voltage level. For some space constrained designs, EN pin can be directly connected to PVin without using the external resistor dividers, as shown in Configuration 3. EN pin should not be left floating. A pull down resistor in the range of tens of kilohms is recommended. **Figure 9** illustrates the corresponding start-up sequences with three EN configurations.

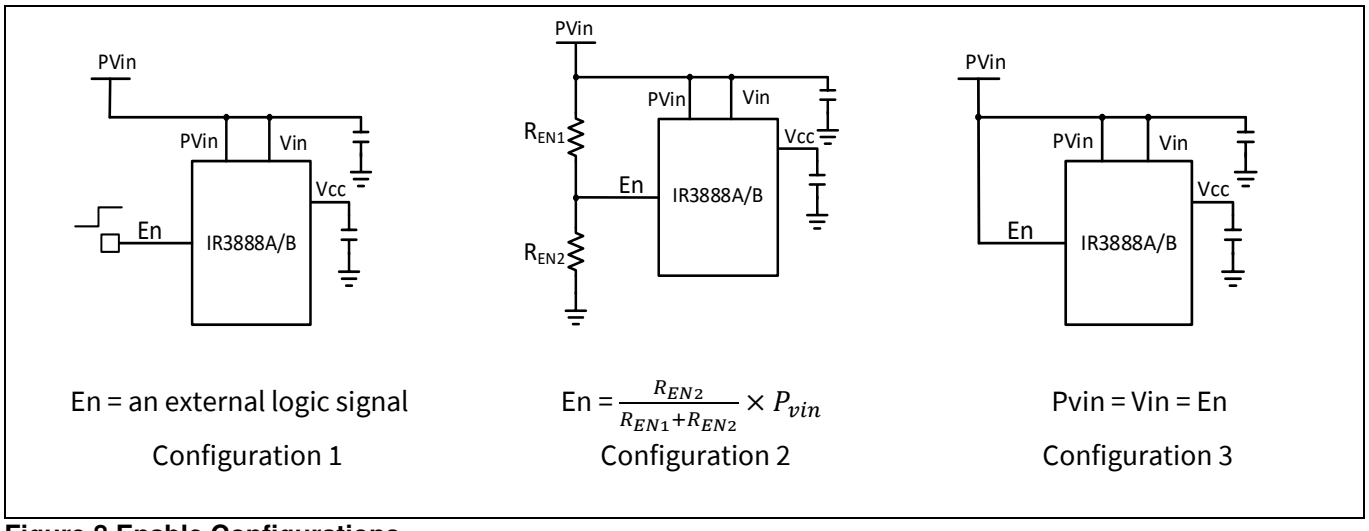


Figure 8 Enable Configurations

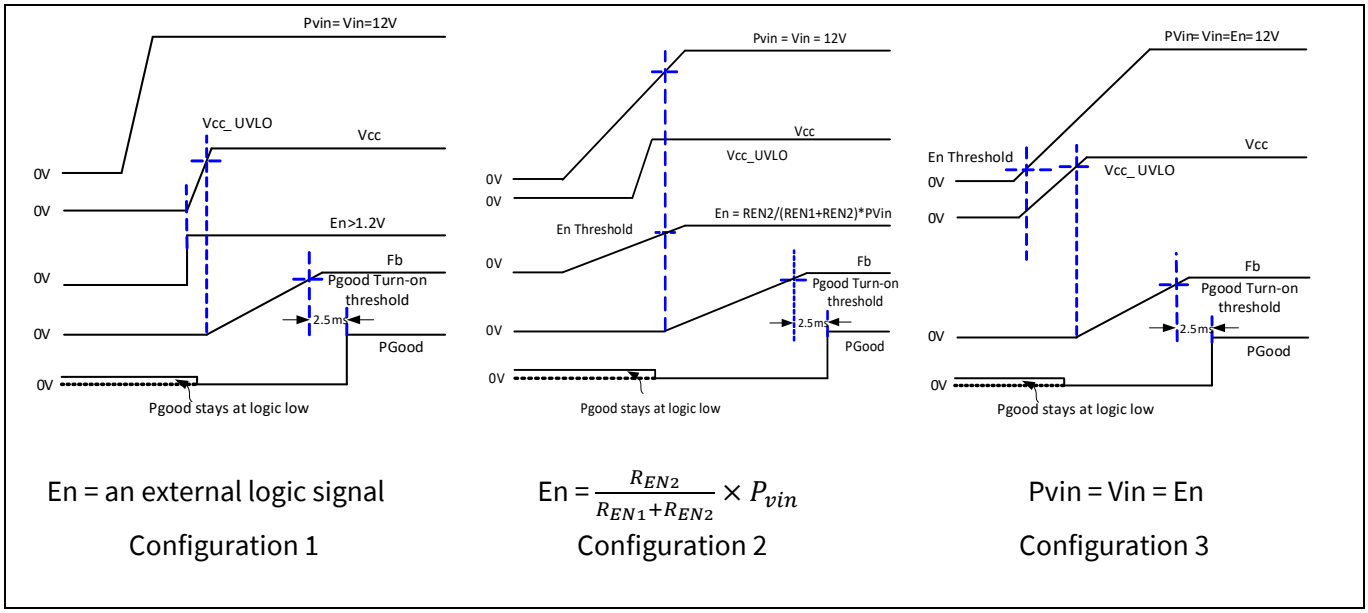


Figure 9 Start-up sequence

12.3 FCCM Operation

The IR3888A/B offers forced Continuous Conduction (FCCM). With FCCM, the IR3888A/B always operates as a synchronous buck converter with a pseudo constant switching frequency and therefore achieves small output voltage ripples.

12.4 Pseudo Constant Switching Frequency

The switching frequency of the IR3888A/B is set at 800 kHz internally. The IR3888A/B generates the corresponding on-time of the Control FET for a given PV_{in} and V_o, as shown by the formula below.

$$T_{on} = \frac{V_0}{PV_{in}} \times \frac{1}{800\ kHz}$$

During the operation, the IR3888A/B monitors PV_{in} and V_o, and can automatically adjust the on-time to maintain the pre-selected f_{sw}. With increasing load current, the switching frequency will increase to compensate for power losses. Therefore, the IR3888A/B has a pseudo constant switching frequency.

12.5 Soft-start

The IR3888A/B has an internal digital soft-start to control the output voltage rise and to limit the current surge at start-up. To ensure correct start-up, the soft-start sequence initiates when the EN and VCC voltages rise above their respective thresholds. The internal soft-start signal linearly rises from 0 V to 0.6 V in a defined time duration of 4 ms. The soft-start time does not change with the output voltage. During soft-start, the IR3888A/B operates in a diode emulation mode until 1ms after the output voltage ramps above the PGood turn-on threshold.

12.6

12.6 Pre-bias Start-up

The IR3888A/B is able to start up into a pre-charged output without causing oscillations and disturbances of the output voltage. When the IR3888A/B starts up with a pre-biased output voltage, both control FET and Synch FET are kept off till the internal soft-start signal exceeds the FB voltage.

12.7 Internal Low - Dropout (LDO) Regulator

The IR3888A/B has an integrated low-dropout LDO regulator, providing bias voltage for the internal circuitry. To minimize standby current, the internal LDO is disabled when the EN voltage is pulled low. The VIN pin is the input of the LDO. When using the internal LDO for a single rail operation, the VIN pin should be connected to the PVIN pin. To save power losses on the LDO, an external bias voltage can be used by connecting VIN pin to the VCC/LDO pin. **Figure 10** illustrates the configuration of VCC/LDO and VIN pins.

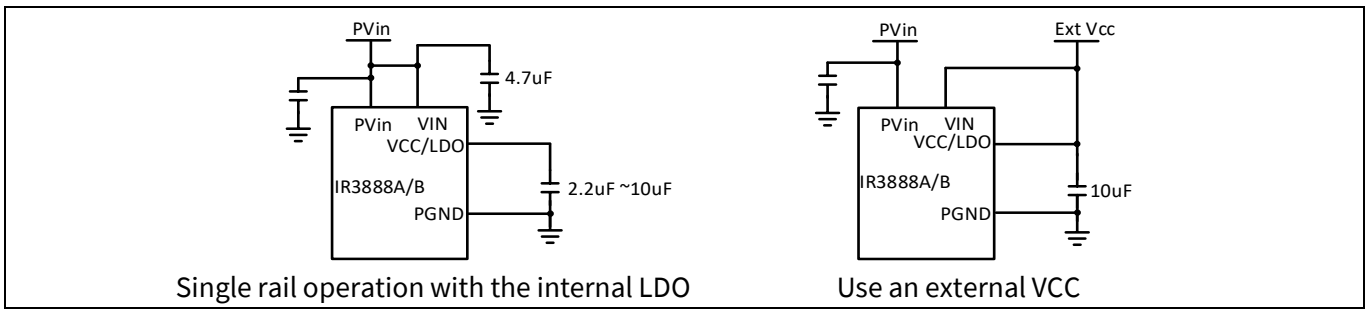


Figure 10 Configuration of Using the internal LDO or an external VCC.

Section **7.1** specified the recommended operating voltage range of V_{in} and VCC under different configurations. The following design guidelines are recommended when configuring the VCC/LDO.

- Place a bypass capacitor to minimize disturbance on the VCC pin. For a single rail operation using the internal LDO, a 4.7 µF low ESR ceramic capacitor must be used between the VIN pin and PGND and a 2.2 µF~10 µF low ESR ceramic capacitor is required to be placed close to VCC/LDO with reference to PGND. A 10 µF MLCC is recommended for VCC bypass capacitor when VIN is below 5.5 V. When using an external VCC bias voltage, a 10 µF ceramic capacitor can be shared with the VIN and VCC/LDO pins.
- For applications using the internal LDO with 4.3 V ≤ V_{in} ≤ 5.4 V, LDO will operate in dropout mode. It is important to ensure the LDO voltage does not fall below the VCC UVLO threshold voltage. At V_{in} = 4.3 V, I_{CC} must not exceed 50 mA under all operating conditions such as during a step-up load transient, in which the control loop may require the increase of f_{sw}. OCP limits can be reduced due to lower VCC voltage.

12.8 Over Current Protection (OCP)

The IR3888A/B offers cycle-by-cycle OCP response with a fixed current limit. Cycle-by-cycle OCP response allows the IR3888A/B to fulfill a brief high current demand, such as a high inrush current during the start-up. Detailed operation is explained as follows.

The OCP is activated when EN voltage is above its threshold. The OCP circuitry monitors the current of the Synchronous MOSFET through its $R_{ds(on)}$. When a new PWM pulse is requested by the control loop, if the current of the Synchronous MOSFET exceeds the selected OCP limit, the IR3888A/B skips the PWM pulse and extends the on-time of the Synchronous MOSFET until the current drops below the OCP limit. The OCP operation is also illustrated in **Figure 11**. During OCP events, the valley of the inductor current is regulated around the OCP limit. However, during the first switching cycle when the OCP is tripped, the valley of the inductor current can drop slightly below the OCP limit. It should be noted that OCP events do not pull the PGood signal low unless V_o drops

below the PGood turn-off threshold. If the OCP event persists, the output voltage can eventually drop below the Under Voltage Protection (UVP) threshold and trigger UVP. The IR3888A/B will then enter hiccup mode.

OCP limits are thermally compensated. Please refer to the typical performance of OCP limits. The OCP limits specified in the Section **7.2** refer to the valley of the inductor current when OCP is tripped. Therefore, the corresponding output DC current can be calculated as follows:

$$I_{out\_OCP} = I_{OC} + \frac{\Delta i_L}{2}$$

Where: I_{out_OCP} = Output DC current when OCP is tripped. I_{OC} = OCP limit specified in the Section **7.2**, which is the valley of inductor current. ΔiL = Peak-peak inductor ripple current. To achieve the desired I_{out_OCP}, Δi_L can be calculated as follows:

$$\Delta i_L = 2 \times (I_{out\_OCP} - I_{OC\_min})$$

Where I_{OC_min} = the minimum spec of OCP limit.

To avoid the inductor saturation during OCP events, the following criterion is recommended for the inductor saturation current rating.

$$I_{sat} \geq I_{OC\_max} + \Delta i_L$$

Where: I_{sat} is the inductor saturation current and I_{OC_max} is the maximum spec of the OCP limit.

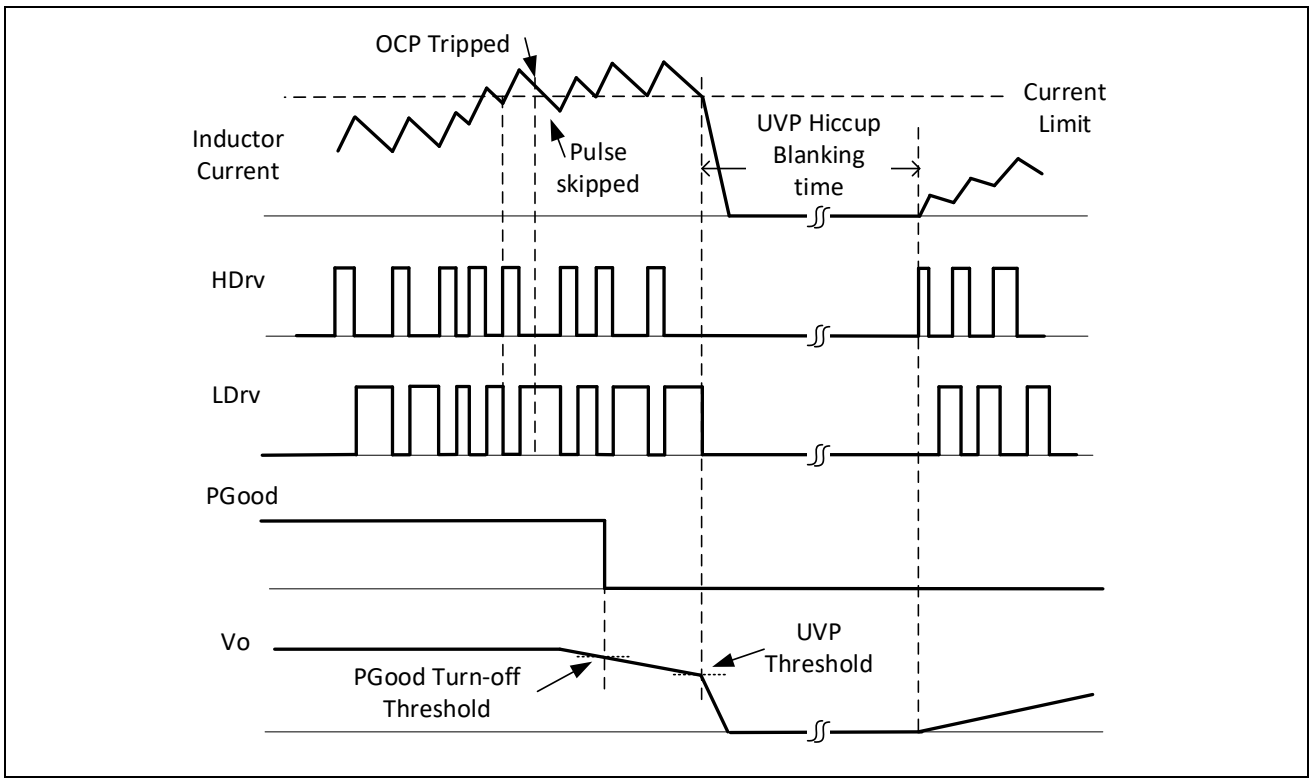


Figure 11 Cycle-by-cycle OCP response

12.9 Under Voltage Protection (UVP)

Under Voltage Protection (UVP) provides additional protection during over current fault or other faults. UVP is activated when the soft-start voltage rises above 100 mV with respect to ground. UVP circuitry monitors the FB voltage. When it is below the UVP threshold for 2 µs (typical), an under voltage trip signal asserts and both the Control MOSFET and Synchronous MOSFET are turned off. The IR3888A/B enters a hiccup mode with a blanking

time of 20 ms, during which Control MOSFET and Synchronous MOSFET remain off. After the completion of blanking time, the IR3888A/B attempts to recover to the nominal output voltage with a soft-start, as shown in **Figure 11**. The IR3888A/B will repeat hiccup mode and attempt to recover until the UVP condition is removed.

12.10 Over Voltage Protection (OVP)

Over Voltage Protection (OVP) is achieved by comparing the VSNS voltage to an OVP threshold voltage. When the VSNS voltage exceeds the OVP threshold, an over voltage trip signal asserts after 8 µs (typical) delay. The Control MOSFET is latched off immediately and PGood flags low. The Synchronous MOSFET remains on to discharge the output capacitor. When FB voltage drops below 115% (typical) of the reference voltage, the Synchronous MOSFET turns off to prevent the complete depletion of the output capacitors. **Figure 12** illustrates the OVP operation. The OVP comparator becomes active when the EN signal is above the start threshold.

With a latched OVP response, the Control FET remains latched off until either VCC voltage or the EN signal is cycled.

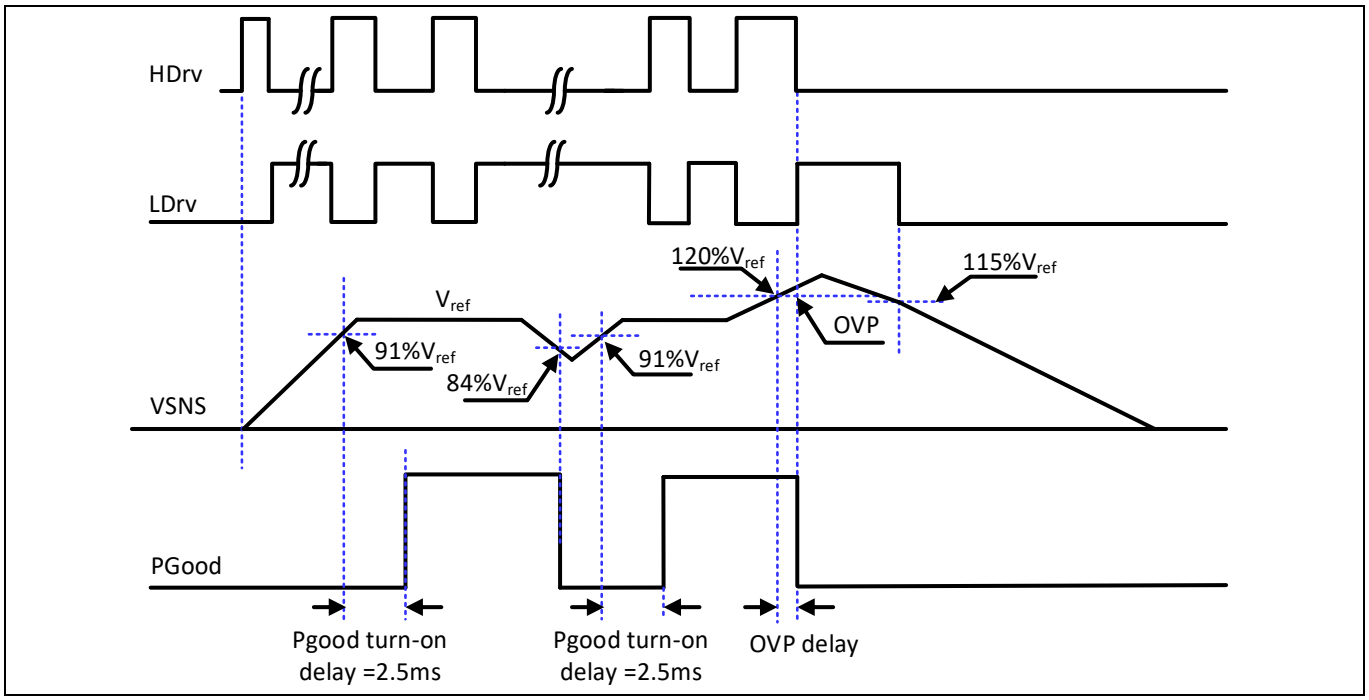


Figure 12 Over voltage protection response and PGood behavior.

12.11 Over Temperature Protection (OTP)

Temperature of the controller is monitored internally. When the temperature exceeds the over temperature threshold, OTP circuitry turns off both Control and Synchronous MOSFETs, and resets the internal soft start. Automatic restart is initiated when the sensed temperature drops back into the operating range. The thermal shutdown threshold has a hysteresis of 15 °C (typical).

12.12 Power Good (PGood) Output

The PGood pin is the open drain of an internal NFET, and needs to be externally pulled high through a pull-up resistor. The PGood signal is high when three criteria are satisfied.

1. EN signal and VCC voltage are above their respective thresholds.

2. No over voltage, under voltage and over temperature faults occur.

3. V_o is in regulation.

In order to detect if V_o is in regulation, the PGood comparator monitors the VSNS voltage. When VSNS voltage ramps up above the upper threshold, the PGood signal is pulled high after 2.5 ms. When VSNS voltage drops below the lower threshold, the PGood signal is pulled low immediately. **Figure 12** illustrates PGood response.

During start-up with a pre-biased voltage, the PGood signal is held low before the first PWM is generated and is then pulled high with 2.5 ms delay after the VSNS voltage rises above the PGood threshold. The IR3888A/B also integrates an additional PFET in parallel to the PGood NFET, as shown in **Figure 2**. This PFET allows the PGood signal to stay at a logic low when the VCC voltage is not present, and the PGood pin is pulled up by an external bias voltage. Please refer to **Figure 9**. Since the PGood PFET has relatively higher on resistance, a 50 kΩ pull-up resistor is needed for a PGood bias voltage of 3.3 V to maintain the PGood signal at logic low when PGood PFET is on.

12.13 Minimum On - Time and Minimum Off - Time

The minimum on-time refers to the shortest time for the Control MOSFET to be reliably turned on. The minimum off-time refers to the minimum time duration in which the Synchronous FET stays on before a new PWM pulse is generated. The minimum off-time is needed for IR3888A/B to charge the bootstrap capacitor, and to sense the current of the Synchronous MOSFET for over current protection.

For applications requiring a small duty cycle, it is important to ensure the resulting on-time is larger than the maximum spec of the minimum on-time in the Section **7.2**. Following formula may be used to check for the minimum on-time requirement.

$$\frac{V_0}{k \times 800kHz \times PV_{in}} > \max\ spec\ of\ T_{on(\min)}$$

Where *k* is the variation of the switching frequency. As a rule of thumb, select *k* = 1.25 to have some design margins.

Similarly, for applications requiring a high duty cycle, it is important to ensure that the resulting off-time is longer than the maximum spec of the minimum off-time in the Section **7.2**, which can be calculated as shown below.

$$\frac{PV_{in} - V_0}{k \times 800kHz \times PV_{in}} > \max\ spec\ of\ T_{off(\min)}$$

Where *k* is the variation of the switching frequency. As a rule of thumb, select *k* = 1.25 to have some design margins. Please note that during a load step, f_{sw} will increase due to the intrinsic COT operation. Therefore it is important to check the change of f_{sw} during the load step. Please also note that OCP limit may be degraded when off-time is close to the minimum off-time.

The resulting maximum duty cycle is therefore determined by the on-time and minimum off-time.

$$D_{max} = \frac{T_{on}}{T_{on} + T_{off(\min)}}$$

12.14 Selection of Feedforward Capacitor and Feedback Resistors

A small MLCC capacitor, Cff, is preferred in parallel with the top feedback resistor, RFB1, to provide extra phase boost and to improve transient load response, as shown in **Figure 13**. The following formula can be used to help select Cff and RFB1. The value of Cff is recommended to be 100 pF or higher to minimize the impact of circuit

parasitic capacitance Where Lo and Co are the output LC filter of the buck regulator. **Table 2** lists the suggested *m* values for some common outputs. Cff and RFB1 may be further optimized based on the transient load tests.

$$R_{FB1}C_{ff} = \frac{\sqrt{L_0 C_0}}{m \times 4.9}$$

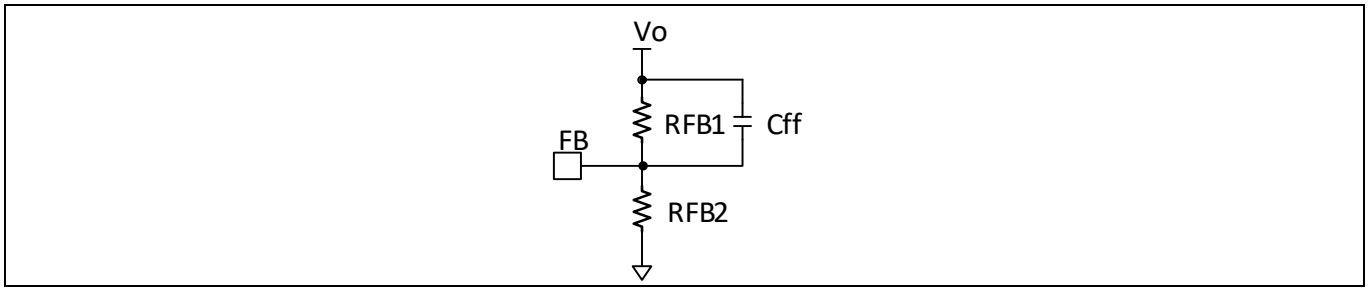


Figure 13 Configuration of feedforward capacitor, Cff.

Table 2 Selection of *m*

Vo	m
3 V ≤ Vo ≤ 6 V	0.3
1.2 V < Vo < 3 V	0.5
Vo ≤ 1.2 V	0.7

13 Design example

In this section, an example is used to explain how to design a buck regulator with the IR3888A. The application circuit is shown in Figure 14. The design specifications are given below.

- PV_{in} = 12 V (±10%)
- V_o = 1.0 V
- I_o = 20 A
- f_{sw} = 800 kHz
- V_o ripple voltage = ±1% of V_o
- Load transient response = ± 3% of V_o with a step load current = 9 A and slew rate = 30 A/µs

13.1 Enabling the IR3888A

The IR3888A has a precise Enable threshold voltage, which can be used to implement a UVLO of the input bus voltage by connecting the EN pin to PV_{in} with a resistor divider, as shown in Configuration 2 of Figure 8. The Enable resistor divider, R_{EN1} and R_{EN2}, can be calculated as follows.

$$PV_{in(\min)} \times \frac{R_{EN2}}{R_{EN1} + R_{EN2}} \geq V_{EN(\max)}$$

$$R_{EN2} \geq R_{EN1} \times \frac{V_{EN(\max)}}{PV_{in(\min)} - V_{EN(\max)}}$$

Where $V_{EN(max)}$ is the maximum En-start-threshold as defined in Section **7.2**. For $PV_{in\,(min)}$ =10.8 V, select R_{EN1}=49.9 kΩ and R_{EN2}=7.5 kΩ.

13.2 Selecting Input Capacitors

Without input capacitors, the pulse current of Control MOSFET is directly from the input supply power. Due to the impedance on the cable, the pulse current can cause disturbance on the input voltage and potential EMI issues. The input capacitors filter the pulse current, resulting in almost constant current from the input supply. The input capacitors should be selected to tolerate the input pulse current, and to reduce the input voltage ripple. The RMS value of the input ripple current can be expressed by:

$$I_{RMS} = I_o \times \sqrt{D \times (1 - D)}$$

$$D = \frac{V_o}{PV_{in}}$$

Where I_{RMS} is the RMS value of the input capacitor current. I_o is the output current and D is the Duty Cycle. For I_o = 20 A and $D_{(max)}$ = 0.09, the resulting RMS current flowing into the input capacitor is I_{RMS} = 5.7 A.

To meet the requirement of the input ripple voltage, the minimum input capacitance can be calculated as follows.

$$C_{in(\min)} > \frac{I_o \times (1 - D) \times D}{f_{sw} \times (\Delta PV_{in} - ESR \times I_o \times (1 - D))}$$

Where ΔPV_{in} is the maximum allowable peak-to-peak input ripple voltage, and ESR is the equivalent series resistor of the input capacitors. Ceramic capacitors are recommended due to low ESR, ESL and high RMS current capability. For I_o = 20 A, f_{sw} = 800 kHz, ESR = 3 mΩ, and ΔPV_{in} = 240 mV, $C_{in(min)}$ > 11 µF. To account for the de-rating of ceramic capacitors under a bias voltage, 10 x 22 µF/0805/25V MLCC are used for the input capacitors. In addition, a bulk capacitor is recommended if the input supply is not located close to the voltage regulator.

13.3 Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. A low inductor value results in a large ripple current, lower efficiency and high output noise, but helps with size reduction and transient load response. Generally, the desired peak-to-peak ripple current in the inductor (Δi) is found between 20% and 50% of the output current.

The inductor saturation current must be higher than the maximum spec of the OCP limit plus the peak-to-peak inductor ripple current. For some core material, inductor saturation current may decrease as the increase of temperature. So it is important to check the inductor saturation current at the maximum operating temperature.

The inductor value for the desired operating ripple current can be determined using the following relation:

$$L = (PV_{in(\max)} - V_o) \times \frac{D_{min}}{\Delta i_{L(\max)} \times F_{sw}}$$

$$D_{min} = \frac{V_o}{PV_{in(\max)}}$$

$$I_{sat} \geq I_{oc\_max} + \Delta i_{L(\max)}$$

Where: $PV_{in(max)}$ = Maximum input voltage; ΔiL_{max} = Maximum peak-to-peak inductor ripple current; I_{OC_max} = maximum spec of the OCP limit as defined in Section **7.2**; and I_{sat} = inductor saturation current. In this case, select inductor L =150 nH to achieve ΔiL_{max} = 40% of I_{omax}. The I_{sat} should be no less than 32 A.

13.4 Output Capacitor Selection

Output capacitor selection is mainly determined by the output voltage ripple and transient requirements.

To satisfy the V_o ripple requirement, C_o should satisfy the following criterion.

$$C_o > \frac{\Delta i_{Lmax}}{8 \times \Delta V_{or} \times f_{sw}}$$

Where ΔV_{or} is the desired peak-to-peak output ripple voltage. For ΔiL_{max}= 7.6 A, ΔV_{or} =20 mV, f_{sw} = 800 kHz, C_o must be larger than 59 µF. The ESR and ESL of the output capacitors, as well as the parasitic resistance or inductance due to PCB layout, can contribute to the output voltage ripple. It is suggested to use Multi-Layer Ceramic Capacitors (MLCC) for their low ESR, ESL and small size.

To meet the transient response requirements, the output capacitors should also meet the following criterion.

$$C_o > \frac{L \times \Delta I_{o(\max)}^2}{2 \times \Delta V_{oL} \times V_o}$$

Where ΔV_{OL} is the allowable V_o deviation during the load transient. $\Delta I_{o(max)}$ is the maximum step load current. Please note that the impact of ESL, ESR, control loop response, transient load slew rate, and PWM latency is not considered in the calculation shown above. Extra capacitance is usually needed to meet transient response requirements. As a rule of thumb, we can triple the C_o that is calculated above as a starting point, and then optimize the design based on the bench measurement. In this case, to meet the transient load requirement (i.e.

ΔV_{OL}= 30 mV, $\Delta I_{o(max)}$ = 9 A), select C_o = ~600 µF. For a more accurate estimation of C_o, simulation tool should be used.

13.5 Output Voltage Programming

Output voltage can be programmed with an external voltage divider. The FB voltage is compared to an internal reference voltage of 0.6 V. The divider ratio is set to provide 0.6 V at the FB pin when the output is at its desired value. The calculation of the feedback resistor divider is shown below.

$$V_o = V_{ref} \times (1 + \frac{R_{FB1}}{R_{FB2}})$$

Where R_{FB1} and R_{FB2} are the top and bottom feedback resistors. Select R_{FB1} = 16.2 kΩ and R_{FB2} = 24.3 kΩ, to achieve V_o = 1 V. Same resistor divider can be used at the VSNS pin to achieve the same voltage scaling factor.

13.6 Feedforward Capacitor

A small MLCC capacitor, C_{ff}, can be placed in parallel with the top feedback resistor, R_{FB1}, to improve transient response. Based on Section **12.14**, C_{ff} can be selected using the following formula.

$$R_{FB1}C_{ff} = \frac{\sqrt{L_0 C_0}}{0.7 \times 4.9}$$

With Lo = 150 nH, Co = 600 µF and R_{FB1} = 16.2 kΩ, C_{ff} = ~170 pF. 220 pF is finally selected for C_{ff}.

13.7 Bootstrap Capacitor

For most applications, a 0.1 µF ceramic capacitor is recommended for the bootstrap capacitor placed between the SW and BOOT pins.

13.8 VIN and VCC/LDO bypass Capacitor

Please see the recommendation in **Section 12.7**. A 10 µF MLCC is selected for the VCC/LDO bypass capacitor and a 4.7 µF MLCC is selected for the VIN bypass capacitor.

14 Application Information

14.1 Application Diagram

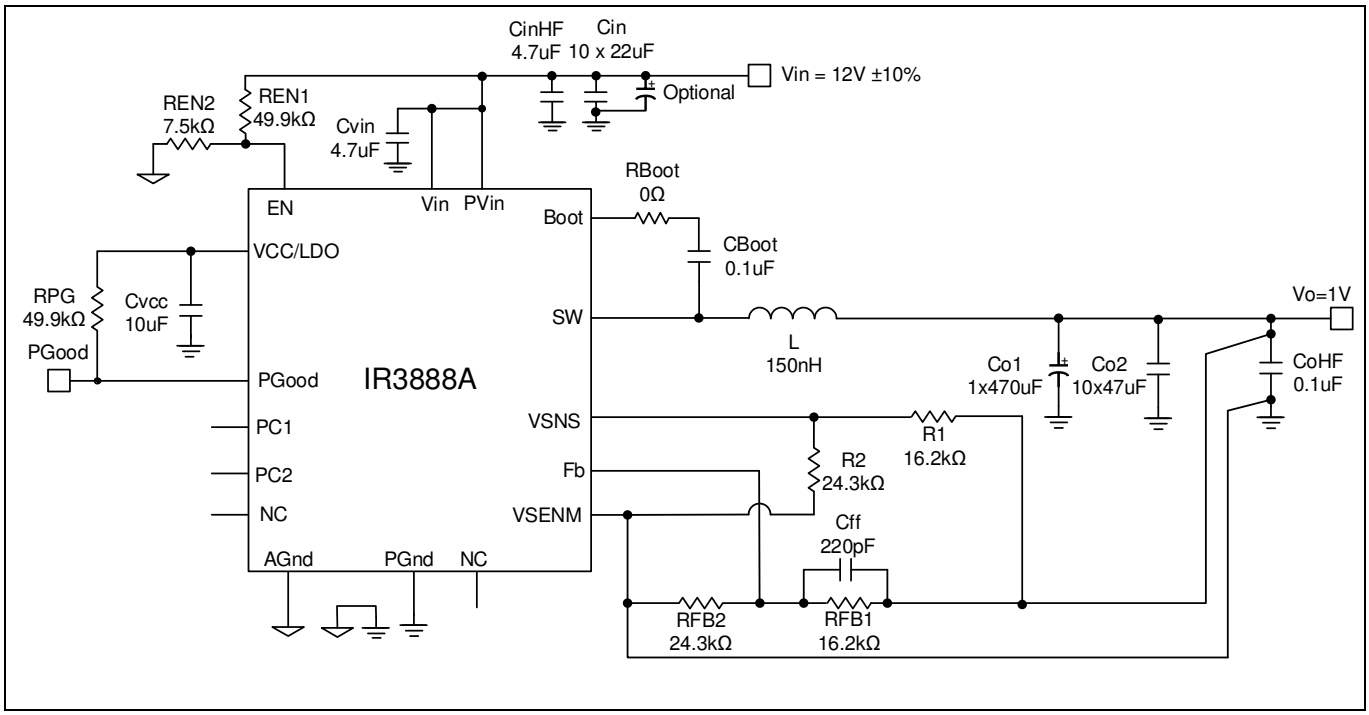


Figure 14 Application diagram of IR3888A. PVin = 12 V, Vo = 1V, Io = 20 A, fsw = 800 kHz.

14.2 Typical Operating Waveforms

PV_{in} = V_{in} = 12.0 V, Vo = 1 V, I_o = 0 – 20 A, f_{sw} = 800 kHz, Room Temperature, no airflow

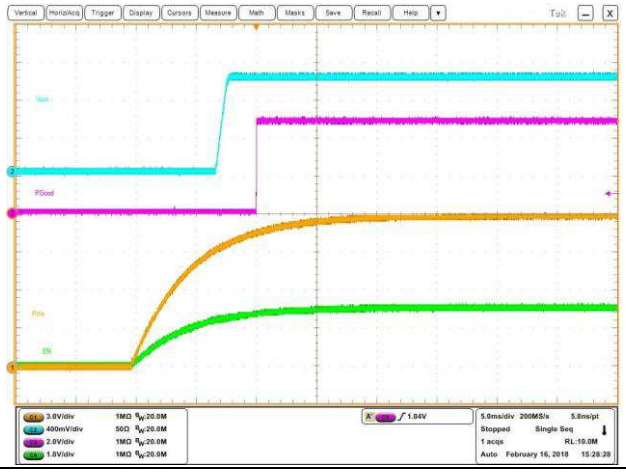


Figure 15 Start up at 20 A Load, (Ch_1: PV_{in}, Ch_2: V_{out}, Ch_3:P_{Good} ,Ch_4:Enable)

Figure 16 Pre-bias Start up at 0 A Load, (Ch_1: PV_{in}, Ch_2: V_{out}, Ch_3:P_{Good} ,Ch_4:Enable)

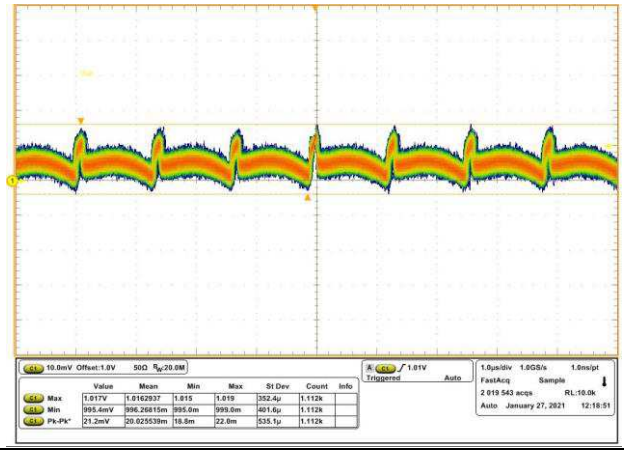


Figure 17 Vout ripple at 20 A Load, fsw = 800 kHz, (Ch_1: V_o)

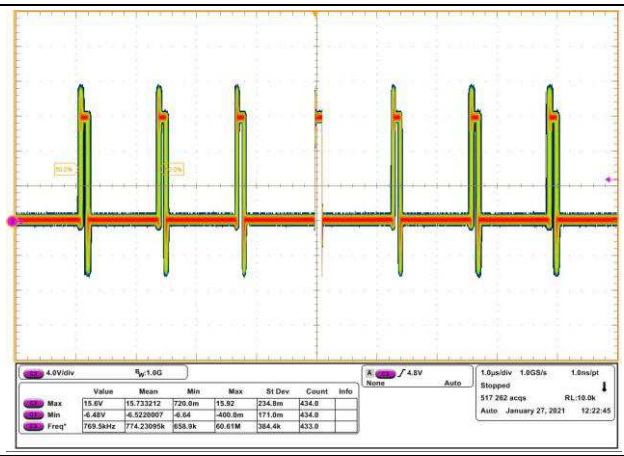


Figure 18 SW node, 20 A load, fsw = 800 kHz

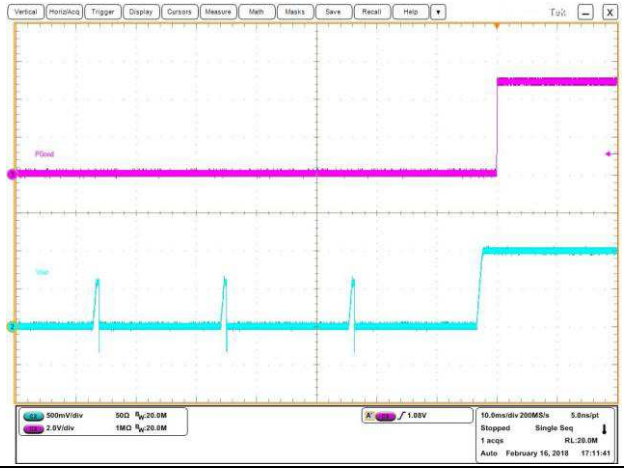


Figure 19 Short circuit and UVP (Hiccup), (Ch_2: V_o , Ch_3:P_{Good})

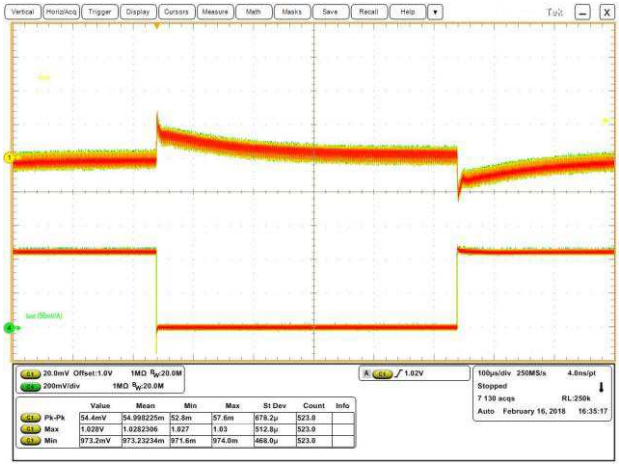


Figure 20 Transient response at 9 A step load current @ 30 A/µs slew rate: Io= 0 A – 9 A, (Ch_1: V_o , Ch_4: I_o), pk-pk: 54.4 mV, fsw = 800 kHz

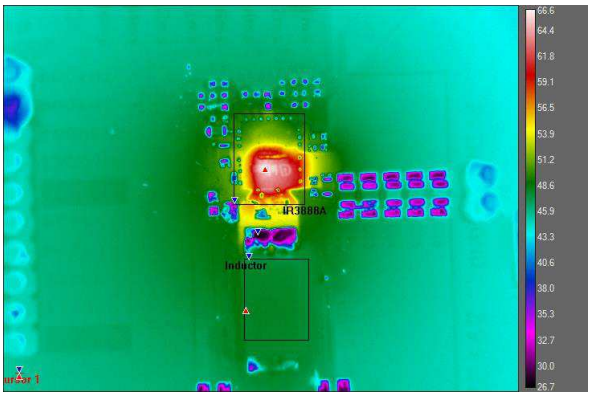


Figure 21 Thermal image of the board at 20 A load IR3888A = 67°C, L = 48°C, fsw = 800 kHz, Ta = room temperature, natural convection

15 Layout Recommendations

PCB layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results. Following design guidelines are recommended to achieve the best performance.

- Bypass capacitors, including input/output capacitors, Vin and VCC bypass capacitors, should be placed near the corresponding pins as close as possible.
- Place bypass capacitors from IR3888A/B power input (Drain of Control MOSFET) to PGND (Source of Synchronous MOSFET) to reduce noise and ringing in the system. The output capacitors should be terminated to a ground plane that is away from the input PGND to mitigate the switching spikes on the Vout. The Vin and VCC bypass capacitor should be terminated to PGND.
- Place a boot strap capacitor near the IR3888A/B BOOT and SW pin as close as possible to minimize the loop inductance.
- SW node copper should only be routed on the top layer to minimize the impact of switching noises
- Connect AGND pin to the PGND pad through a single point connection. On the IR3888A/B demo board, AGND pin is connected to the exposed AGND pad (Pin 23) and then connected to the internal PGND layer through the thermal via holes.
- Via holes can be placed on PVIN and PGND pads to aid thermal dissipation.
- Wide copper polygons are desired for PVin and PGND connections in favor of power losses reduction and thermal dissipation. Sufficient via holes should be used to connect power traces between different layers.
- Single-ended V_o sensing is often used for local sensing. To implement this configuration, following design guidelines should be followed, as illustrated in **Figure 22**.
    - The output voltage can be sensed from a high-frequency bypass capacitor of 0.1 µF or higher, through a 15 mil PCB trace.
    - Keep the Vout sense line away from any noise sources and shield the sense line with ground planes.
    - The sense trace is connected to a feedback resistor divider with the lower resistor terminated at VSENM pin.
    - Short VSENM pin and AGND pin with a short trace.
- If it is required to sense the output voltage at a remote location, pseudo remoting sensing can be implemented as follows. The configuration is also shown in **Figure 23**.
    - A pair of PCB traces with at least 15 mil trace width, running close to each other and away from any noise sources such as inductor and SW nodes, should be used to implement Kelvin sensing of the voltage across a high bypass capacitor of 0.1 µF or higher.
    - The ground connection of the remote sensing signal must be terminated at VSENM pin.
    - The Vout connection of the remote sensing signal must be connected to the feedback resistor divider with the lower feedback resistor terminated at VSENM pin.
    - Shield the pair of remote sensing lines with ground planes above and below.
    - Do **NOT** connect VSENM pin and AGND pin in this configuration
- The EN pin and configuration pins should be terminated to a quiet ground. On the evaluation demo board, they are terminated to the PGND copper plane away from the power current flow. Alternatively, they can be terminated to a dedicated AGND PCB trace.

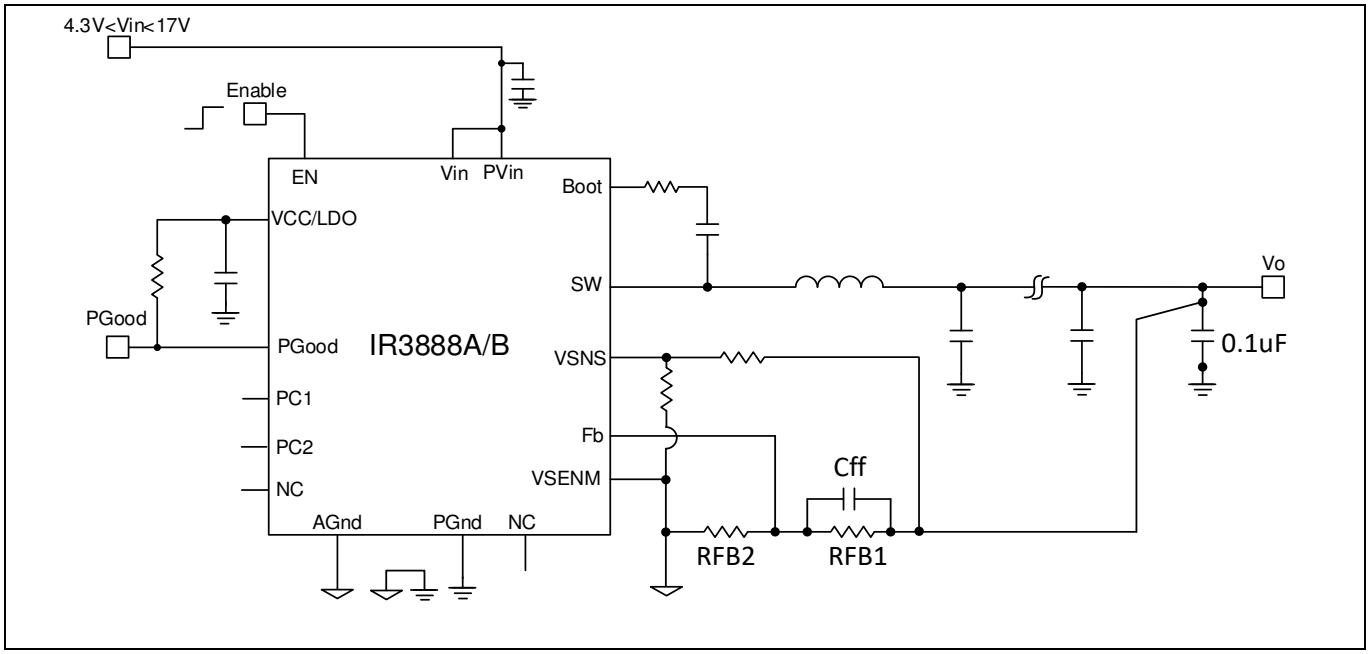


Figure 22 Single-ended V_o sense configuration

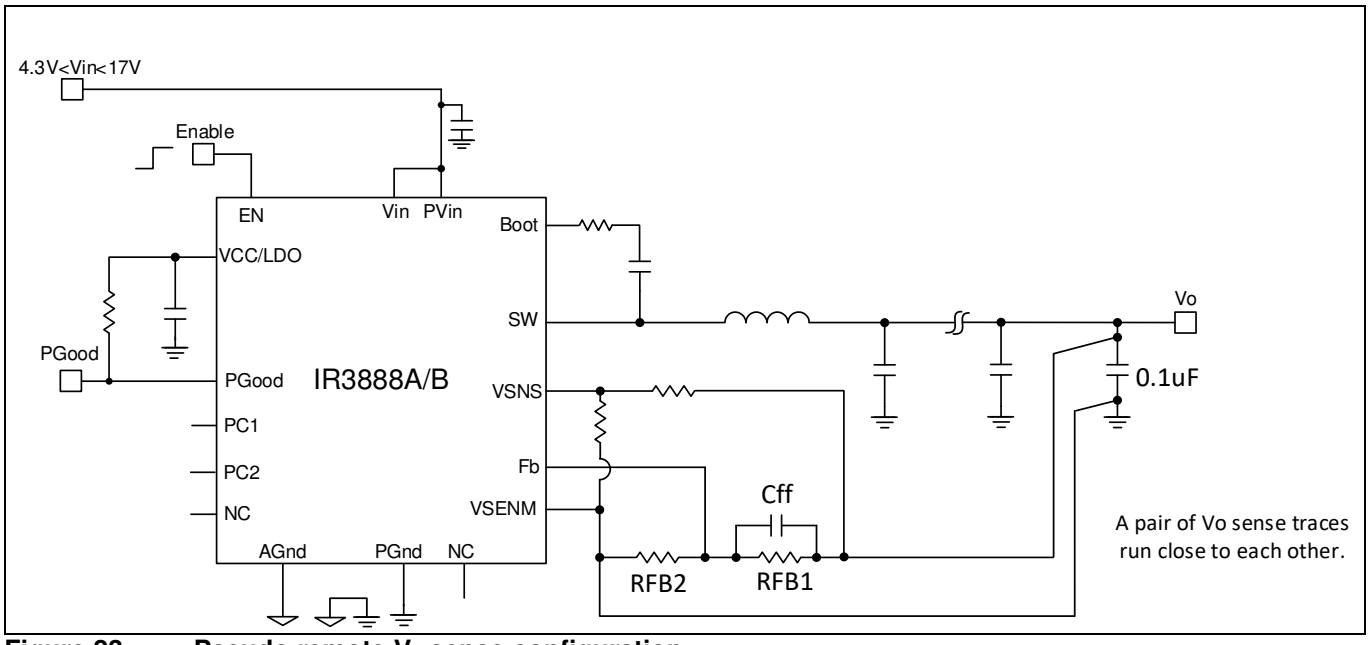


Figure 23 Pseudo remote V_o sense configuration

Following figures illustrate the PCB layout design of an evaluation board with pseudo remote V_o sense.

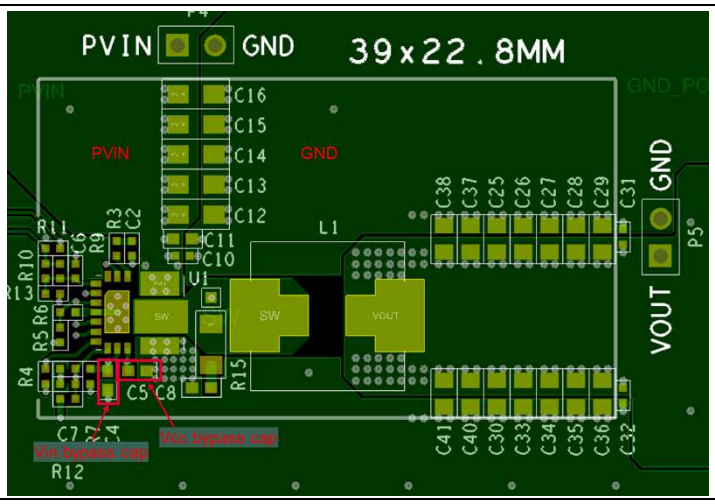


Figure 24 Top Layer

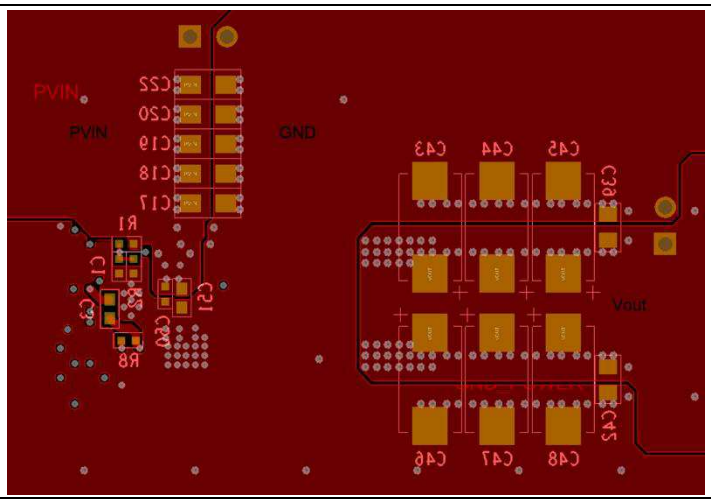


Figure 25 Bottom Layer

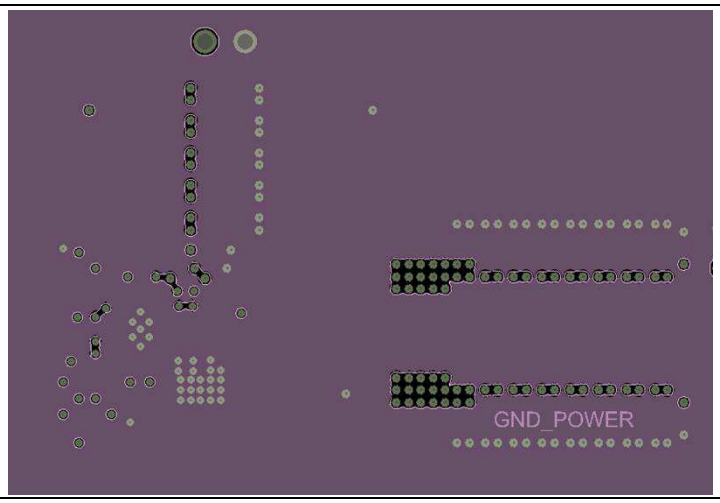


Figure 26 2nd Layer (Ground)

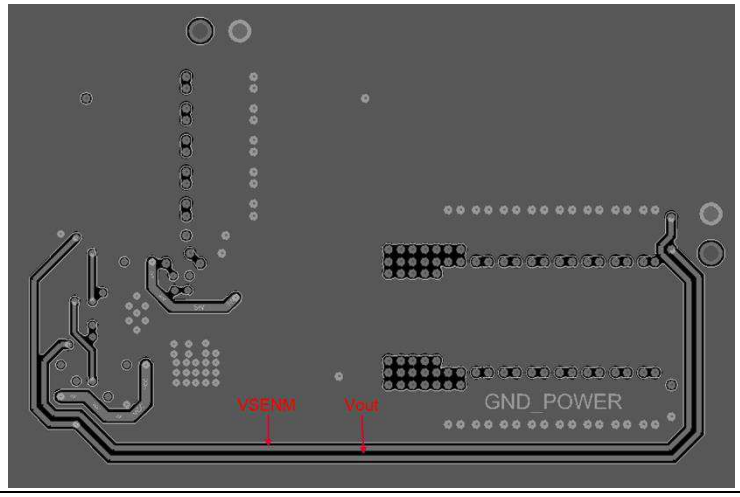


Figure 27 3rd Layer (Ground & Signal)

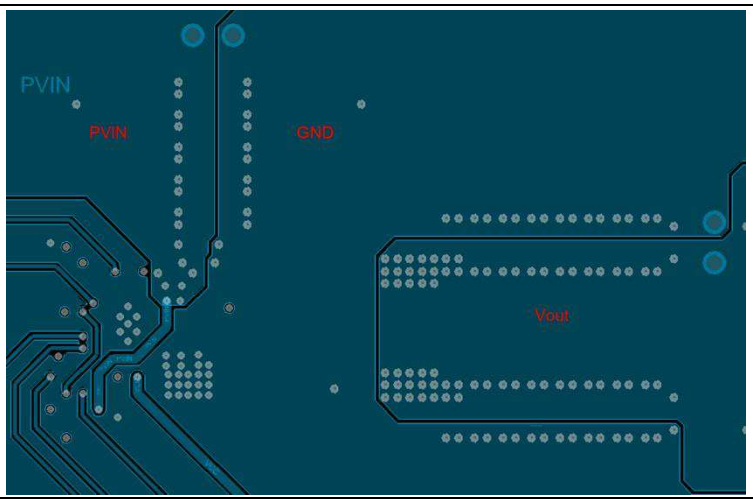


Figure 28 4th Layer (Ground & Signal)

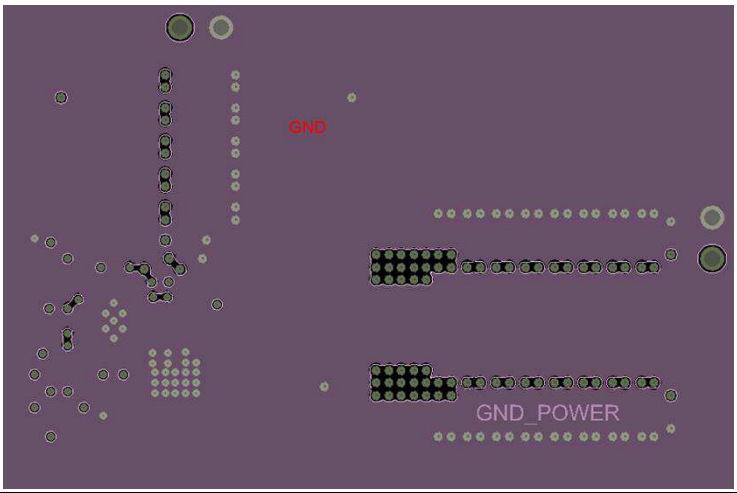


Figure 29 5th Layer (Ground)

15.1 Solder Mask

Evaluation has shown that the best overall performance is achieved using the substrate/PCB layout as shown in the following figures. PQFN devices should be placed to an accuracy of 0.050 mm on both X and Y axes. Self-centering behavior is highly dependent on solders and processes, and experiments should be run to confirm the limits of self-centering on specific processes.

Infineon recommends that larger Power or Land Area pads are Solder Mask Defined (SMD). This allows the underlying copper traces to be as large as possible, which helps in terms of current carrying capability and device cooling capability. When using SMD pads, the underlying copper traces should be at least 0.05 mm larger (on each edge) than the openings in the solder mask. This allows for layers to be misaligned by up to 0.1 mm on both axes. Ensure that the solder resist in-between the smaller signal lead areas is at least 0.15 mm wide, due to the high x/y aspect ratio of the solder mask strip.

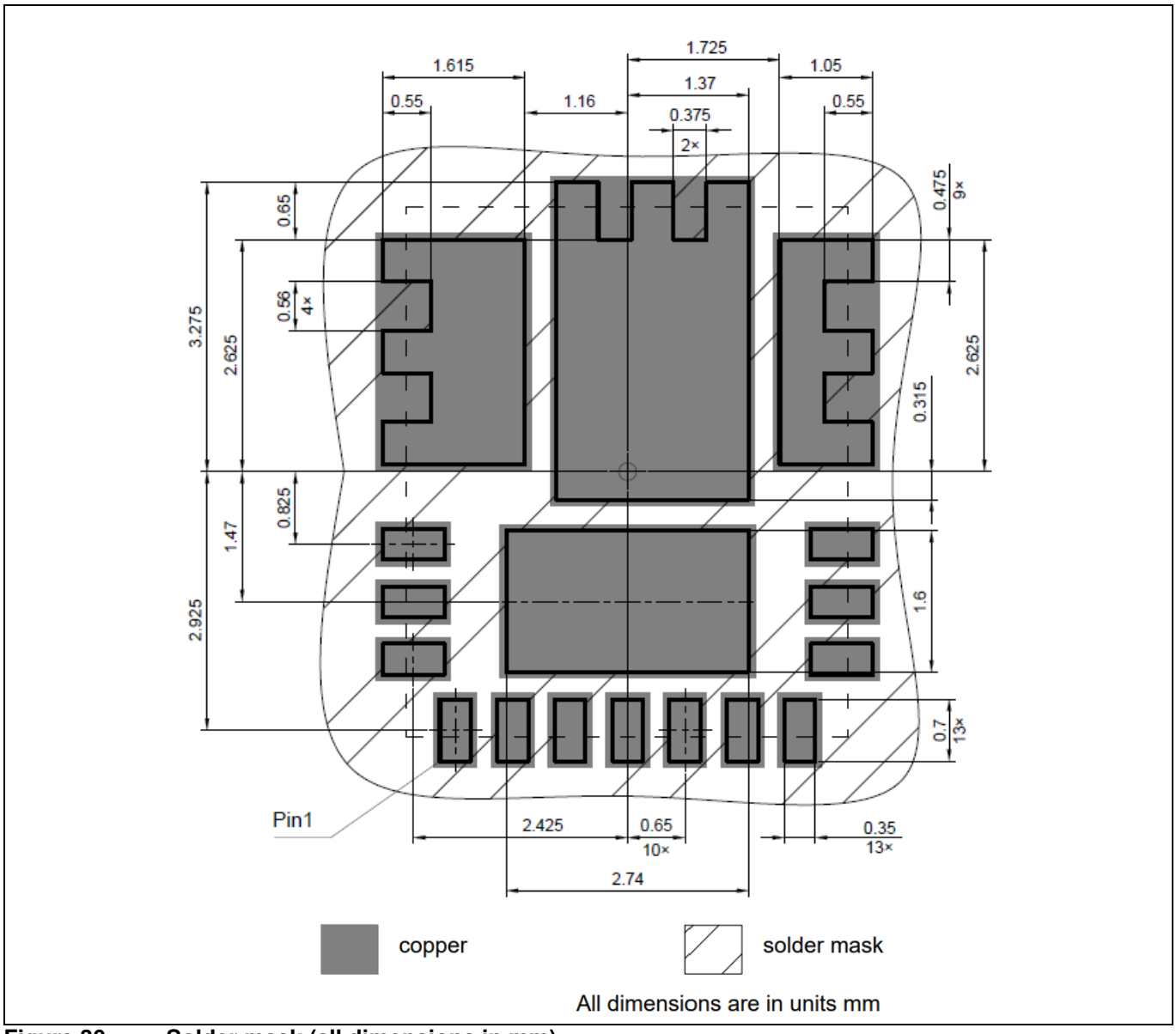


Figure 30 Solder mask (all dimensions in mm)

15.2 Stencil Design

Stencils for PQFN packages can be used with thicknesses of 0.100-0.250 mm (0.004-0.010”). Stencils thinner than 0.100 mm are unsuitable because they deposit insufficient solder paste to make good solder joints with the ground pad; high reductions sometimes create similar problems. Stencils in the range of 0.125 mm-0.200 mm (0.005-0.008”), with suitable reductions, give the best results. A recommended stencil design is shown below. This design is for a stencil thickness of 0.127 mm (0.005”). The reduction should be adjusted for stencils of other thicknesses.

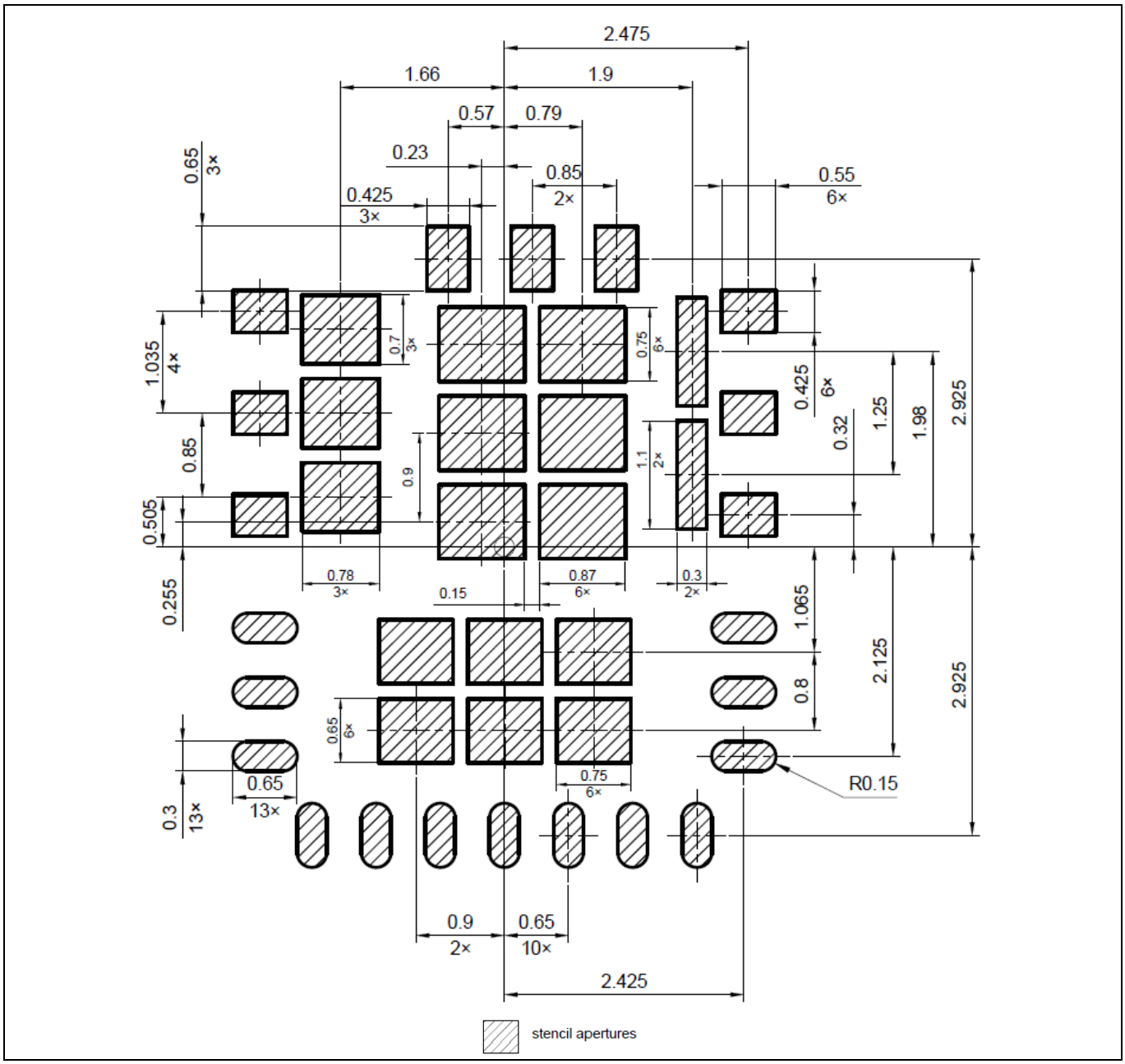


Figure 31 Stencil pad size and spacing (all dimensions in mm)

16 Package

This section includes marking, mechanical and packaging information for the IR3888A/B.

16.1 Marking Information

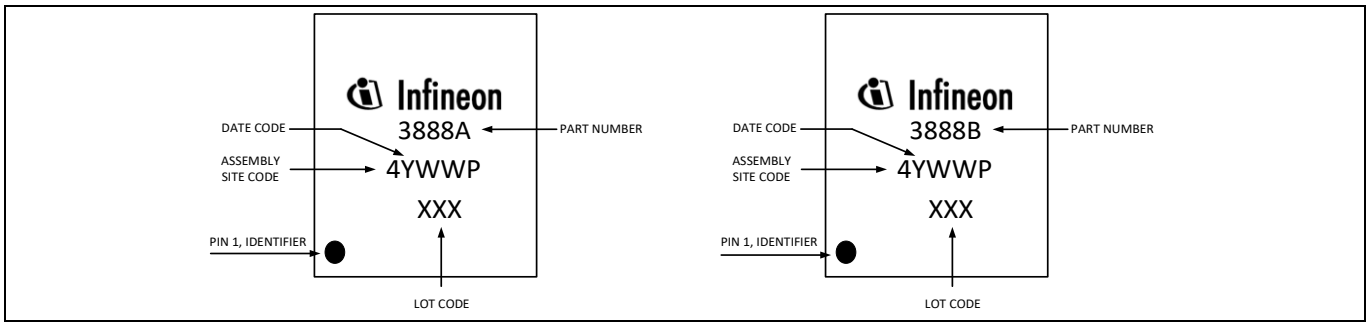


Figure 32 Package Marking

16.2 Dimensions

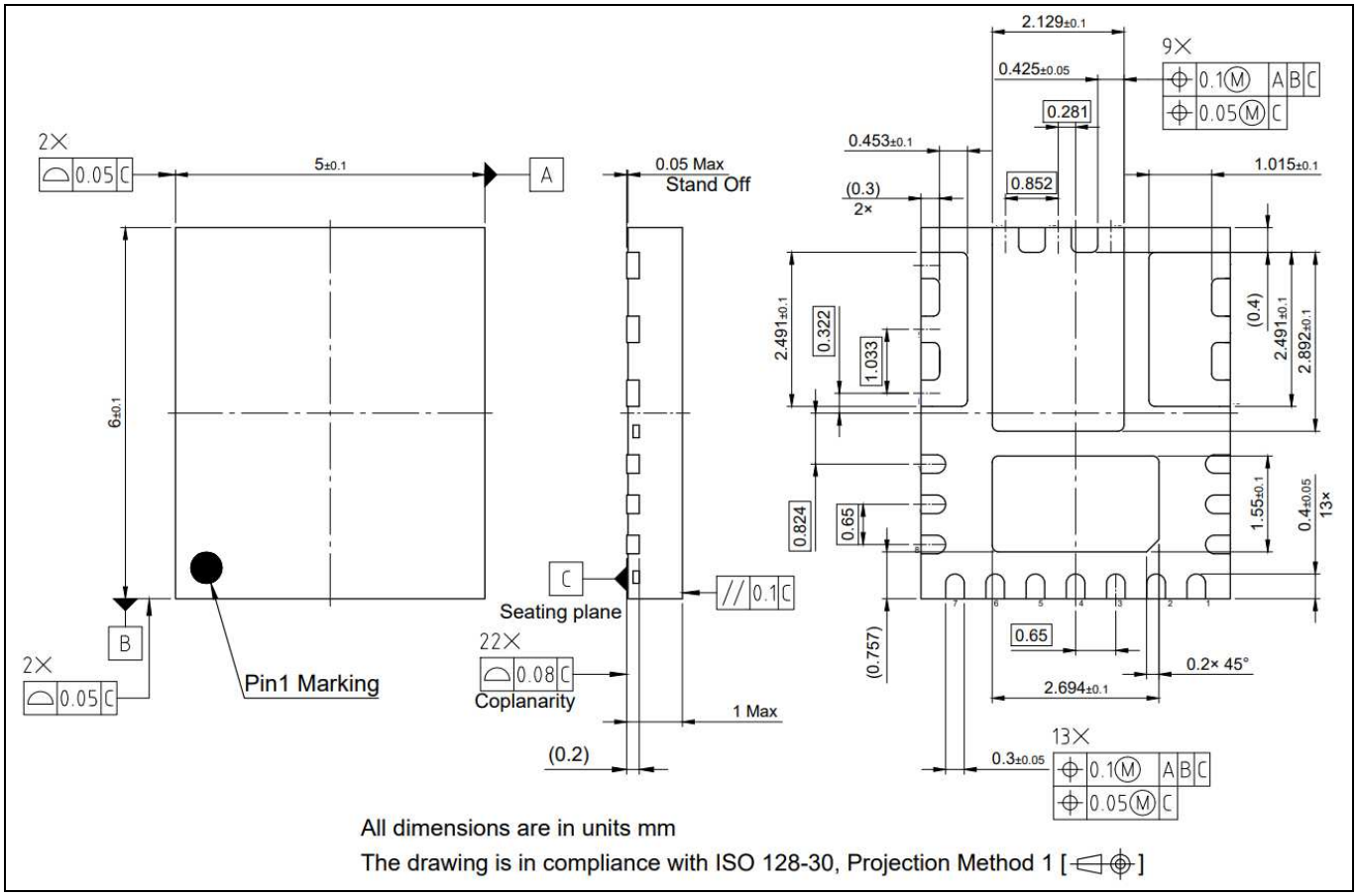


Figure 33 Package Dimensions (all dimensions in mm)

16.3 Tape and Reel Information

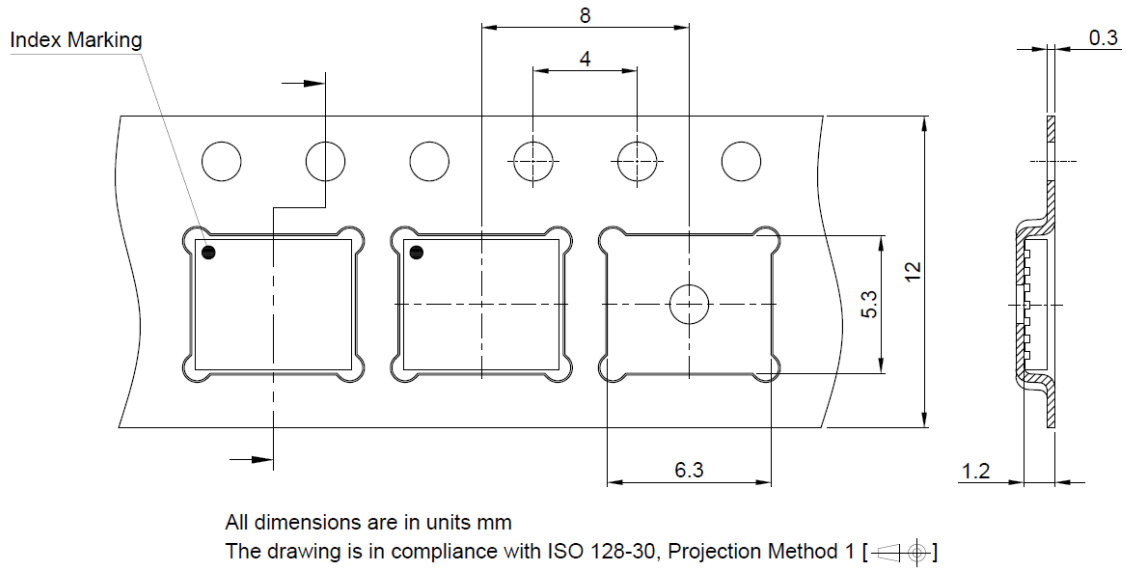


Figure 34 Pin 1 orientation in the tape

17 Environmental Qualifications

Qualification Level		**Industrial**	
Moisture Sensitivity		QFN Package	JEDEC Level 2 @ 260 °C
ESD	Human Body Model	ANSI/ESDA/JEDEC JS-001, 2 (2000 V to < 4000 V)	
	Charged Device Model	ANSI/ESDA/JEDEC JS-002, C3 (≥1000 V)	
RoHS2 Compliant		This product is in compliance with EU Directive 2015/863/EU amending Annex II to EU Directive 2011/65/EU (RoHS) and contains Pb according RoHS exemption 7a, Lead in high melting temperature type solders.	

18 Support Documentation

Table 3 IR3888A/B Package Information

Device	Package Type	Website Address
IR3888A/B	PG-IQFN-22-2	https://www.infineon.com/cms/en/product/packages/PG-IQFN

Revision History

IR3888A/B

Revision: 2021-07-26, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2021-04-29	Release of final version
2.1	2021-06-10	(1) Change UVP activation threshold from 130mV to 100mV in section 12.9; (2) Update Table 7
2.2	2021-07-26	(1) Update order info; (2) Update Fig 30, 31, 33 and 34.

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