RAA457100GBM

Wireless Charging System Receiver IC for Low Power Applications

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1. Product Outline

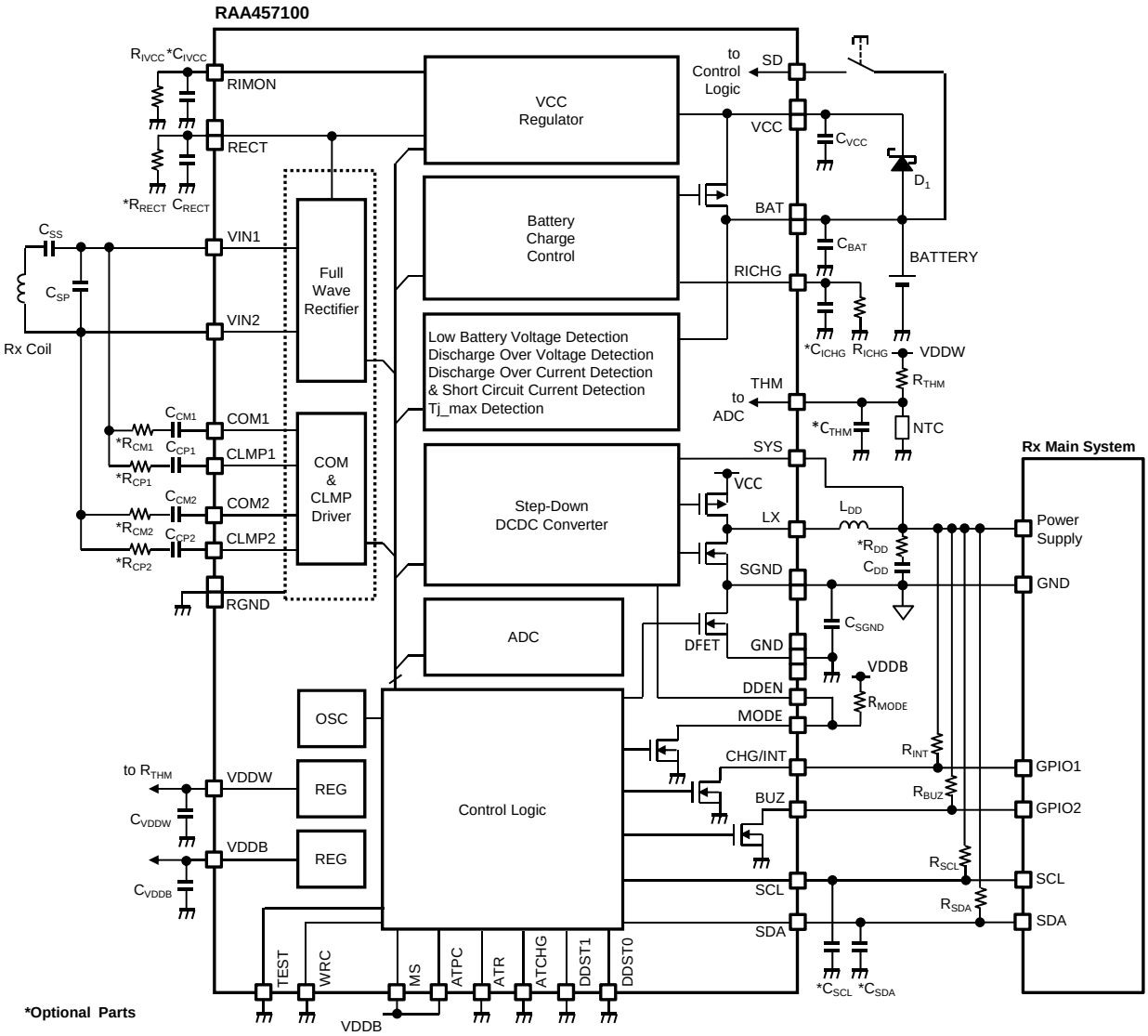
Description

RAA457100 is a receiver IC for low power wireless charging system. RAA457100 performs battery charging by wireless transmission power and DC power supply to receiver application system from battery. When RAA458100 is used in a transmitter, a wireless charging system with bi-directional communication can be constructed.

Features

- Wireless battery charging
- DC power supply to application system by high efficiency DCDC converter
- Monitoring some pin voltages such as rectified output voltage, battery voltage by 12bit A/D converter
- Modulation/Demodulation function for bi-directional communication between transmitter and receiver
- Transmitter system(RAA458100) can read and write RAA457100 registers for setting charge control parameters
- Function which converts wireless communication to 2-wrie serial communication
  for communication between transmitter and receiver application system
- Battery protection, Low battery voltage detection

2. Block Diagram (Example for Application Circuit)



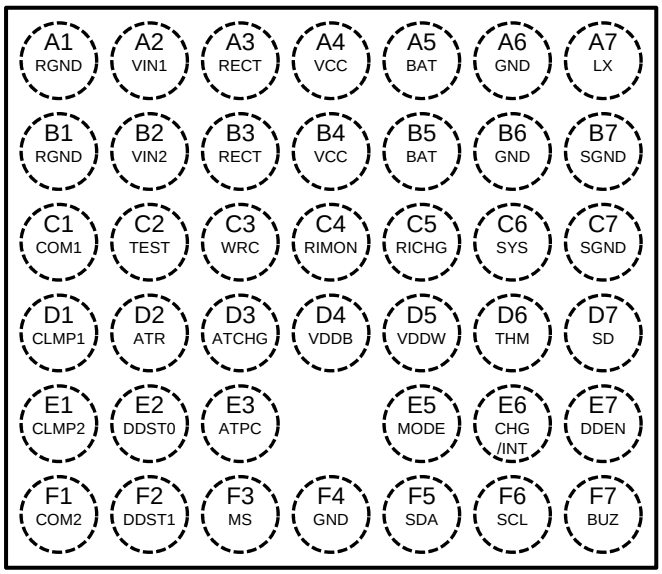
3. Pin Functions

Pin No.	Pin Name	A/D *1	I/O *2	Function	Remark
A6,B6,F4	GND	-	-	Ground	Connect to minus terminal of battery
A1,B1	RGND	-	-	Ground for Rectifier, Load modulation driver, Clamp driver	Connect to minus terminal of battery
B7,C7	SGND	-	-	Ground for DCDC converter, application system	Connected to discharge control FET on chip
A5,B5	BAT	A	I/O	Battery terminal	Connect to plus terminal of battery
A2	VIN1	A	I	Input terminal 1 to rectifier	-
B2	VIN2	A	I	Input terminal 2 to rectifier	-
A3,B3	RECT	A	I/O	Rectified output terminal	Connect C_{RECT} between RECT and RGND
C1	COM1	A	O	Load modulation driver output terminal 1	Connect C_{CM1} between COM1 and VIN1
F1	COM2	A	O	Load modulation driver output terminal 2	Connect C_{CM2} between COM2 and VIN2
D1	CLMP1	A	O	Clamp driver output terminal 1	Connect C_{CP1} between CLMP1 and VIN1
E1	CLMP2	A	O	Clamp driver output terminal 2	Connect C_{CP2} between CLMP2 and VIN2
D4	VDDB	A	O	Regulated 3.0V output (inside usage)	Connect C_{VDDB} between VDDB and GND
D5	VDDW	A	O	Regulated 2.7V output (inside usage, reference voltage for thermistor)	Connect C_{VDDW} between VDDW and GND Connect to pull up resistor R_{THM} of NTC thermistor
A4,B4	VCC	A	O	VCC regulator output (Power supply for DCDC converter)	Connect C_{VCC} between VCC and GND
C4	RIMON	A	O	External resistor connection for output current limit Monitor of VCC regulator output current	Connect R_{IVCC} between RIMON and GND
C5	RICHG	A	O	External resistor connection for current setting of constant current charging	Connect R_{ICHG} between RICHG and GND
D6	THM	A	I	Thermistor voltage input terminal	Divided VDDW voltage by R_{THM} and NTC thermistor
A7	LX	A	O	DCDC converter switching output terminal	-
C6	SYS	A	I	DCDC converter output voltage feedback terminal	-
E7	DDEN	D	I	DCDC converter enable control terminal	-
D7	SD	D	I	Shut down control terminal	-
E5	MODE	D	O	Operation mode notification output	Open drain
E6	CHG/INT	D	O	Charging status notification output/ Interruption signal output for Rx application system	Open drain
F7	BUZ	D	O	Low battery voltage notification	Open drain
F3	MS	D	I	Master or slave setting for 2-wire serial interface	Connect to VDDB or GND
F6	SCL	D	I/O	Clock input or output for 2-wire serial interface	Connect pullup resistor R_{SCL}
F5	SDA	D	I/O	Data input or output for 2-wire serial interface	Connect pullup resistor R_{SDA}
E2	DDST0	D	I	DCDC converter output voltage setting 1	Connect to VDDB or GND
F2	DDST1	D	I	DCDC converter output voltage setting 2	Connect to VDDB or GND
D2	ATR	D	I	Enable automatic control of rectifier	Connect to VDDB or GND
D3	ATCHG	D	I	Enable automatic start of battery charging	Connect to VDDB or GND
E3	ATPC	D	I	Enable automatic transmission power control function	Connect to VDDB or GND
C3	WRC	D	I	Enable contact battery charging	Connect to GND in wireless charging system
C2	TEST	-	-	Test only	Connect to GND

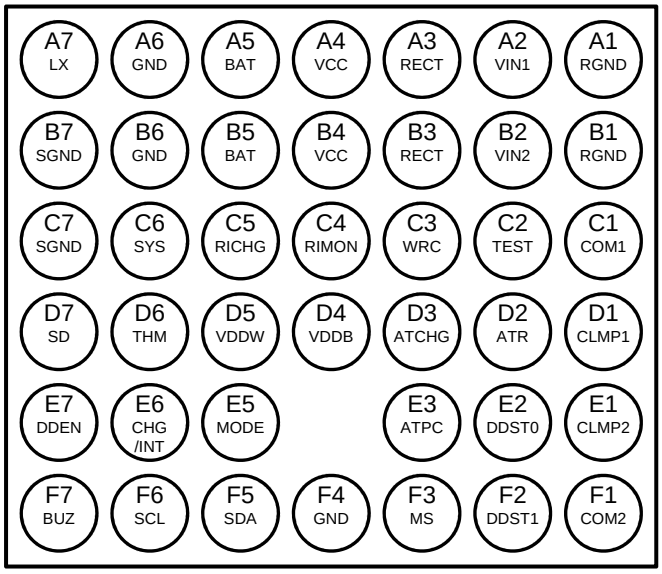
*1 A : Analog signal including power supply, D : Digital signal
*2 I : Input terminal, O : Output terminal, I/O : Input and Output terminal

4. Pin Configuration

Top View



Bottom View (Ball Side)



5. Absolute Maximum Ratings (Tj=25[degC] unless otherwise noted.)

Item	Symbol	Value	Unit	Remark
Pin voltage	VIN1, VIN2, CLMP1, CLMP2, COM1, COM2, RECT	18	V	
	BAT, VCC, SD, DDEN, CHG/INT, MODE, SDA, SCL	-0.3 to 5	V	
	RIMON, RICHG, THM, WRC, ATR, ATCHG, ATPC DDST0, DDST1, MS, TEST	-0.3 to VDDB + 0.3	V	
	SYS, BUZ	-0.3 to VCC + 0.3	V	5V maximum
Operating temperature	Ta	-20 to 50	degC	
Junction temperature	Tj	-20 to 70	degC	
Storage temperature	Tstg	-20 to 70	degC	

6. Recommended Operating Conditions

Item	Symbol	Value	Unit	Remark
RECT pin voltage	V_{RECT}	3.5 to 6.0	V	
BAT pin voltage	V_{BAT}	3.2 to 4.35	V	

7. Electrical Characteristics

Tj=25[degC] unless otherwise noted.

Item	Symbol	Condition	min	typ	max	Unit
Rectified output voltage detection						
Rectified output voltage lower limit	V_{RECT_UVLO}	V_{RECT} is raised (hysteresis voltage 100mV)	2.9	3.0	3.1	V
Rectified output voltage upper limit	V_{RECT_OVD}	V_{RECT} is raised (hysteresis voltage 7V)	13	14	15	V
Circuit current						
Current at charge mode	I_{RECT_CM}	V_{RECT}=5V, V_{CC}=no load	-	1.0	2.0	mA
Current at discharge mode	I_{BAT_DM}	V_{RECT}=0V, V_{BAT}=3.8V, V_{CC}=no load, MS=H	-	25	-	uA
Current at shut down mode	I_{BAT_SD}	V_{RECT}=0V, V_{BAT}=3.0V	-	1	-	uA
Regulator for on chip circuit						
3.0V regulator output voltage	V_{DDB}	V_{RECT}=5V, I_{SOURCE}=1mA	2.85	3.00	3.15	V
2.7V regulator output voltage	V_{DDW}	V_{RECT}=5V, I_{SOURCE}=30uA	2.60	2.70	2.80	V
VCC regulator						
VCC regulator output voltage	V_{CC}	V_{RECT}=V_{BAT}+500mV, V_{BAT}=3.8V	V_{BAT}+0.2	V_{BAT}+0.3	V_{BAT}+0.4	V
Output current	I_{LIM}		-	-	80	mA
Battery charging						
Charge start voltage	V_{START}	V_{BAT} is raised (hysteresis voltage 100mV)	-	1.5	-	V
Fast charge start voltage	V_{QCHGON}	V_{BAT} is raised (hysteresis voltage 100mV)	-	3.0	-	V
Charge control voltage range	V_{CHG}		4.05, 4.20, 4.35			V
Charge control voltage error	V_{CHG_ERR}	I_{BAT}=0.2 x I_{CHGR}, R_{ICHG}=5.6kΩ	-50	-	+50	mV
Trickle charge current	I_{PRECHG}		0.1 x I_{CHGR}			-
Trickle charge current error	I_{PRECHG_ERR}	I_{BAT}=0.1 x I_{CHGR}, R_{ICHG}=5.6kΩ	-50	-	+50	%
Fast charge current range	I_{CHG}		-	-	70	mA
Fast charge current error	I_{CHG_ERR}	I_{BAT}=0.5 x I_{CHGR}, R_{ICHG}=5.6kΩ	-30	-	+30	%
Charge complete current range	I_{FC}		0.05 x I_{CHGR} to 0.20 x I_{CHGR} (0.05 x I_{CHGR} step)			-
Charge complete current error	I_{FC_ERR}	I_{BAT}=0.2 x I_{CHGR}, R_{ICHG}=5.6kΩ	-60	-	+60	%
Trickle charge timer range	T_{DCHG}		60, 120, 180			min
Trickle charge timer error	T_{DCHG_ERR}		-	10	-	%
Fast charge timer range	T_{CHG}		180, 240, 300, 360			min
Fast charge timer error	T_{CHG_ERR}		-	10	-	%
Battery protection						
Charge overvoltage detection voltage *1	V_{COVD}	BAT to GND differential voltage	-	V_{CHG}+0.1	-	V
Charge overvoltage detection delay time	T_{COVD}		-	256	-	ms
Discharge short circuit current detection voltage	V_{DSCD}	SGND to GND differential voltage	-	160	-	mV
Discharge short circuit current detection delay time	T_{DSCD}		-	250	-	us
Discharge overcurrent detection voltage	V_{DOCD}	SGND to GND differential voltage	-	80	-	mV
Discharge overcurrent detection delay time	T_{DOCD}		-	4	-	ms
Discharge overvoltage detection voltage	V_{DOVD}	BAT to GND differential voltage	-	2.8	-	V
Discharge overvoltage detection delay time	T_{DOVD}		-	32	-	ms

*1 Detection voltage is set to suitable temperature charge control voltage(V_{CHG})+0.1[V] regardless of thermistor temperature.

7. Electrical Characteristics (continued)

Tj=25[degC] unless otherwise noted.

Item	Symbol	Condition	min	typ	max	Unit
Low battery voltage detection						
Low battery detection voltage H	V_{FGHD}	V_{SYS}=1.2V,or 1.5V,or 1.8V	3.10	3.20	3.30	V
		V_{SYS}=3.0V	3.45	3.55	3.65	
Low battery detection voltage L	V_{FGLD}	V_{SYS}=1.2V,or 1.5V,or 1.8V	2.95	3.05	3.15	V
		V_{SYS}=3.0V	3.25	3.35	3.45	
Low battery voltage detection delay time	T_{FGD}		-	256	-	ms
DCDC converter						
UVLO release voltage (V_{CC} is raised)	V_{DCDC_UVLO}	V_{SYS}=1.2V,or 1.5V,or 1.8V (hysteresis voltage 100mV)	2.80	2.90	3.00	V
		V_{SYS}=3.0V (hysteresis voltage120mV)	3.20	3.30	3.50	
Output voltage range	V_{SYS}		1.2, 1.5, 1.8, 3.0			V
Output current range	I_{SYS}	Discharge mode	-	-	100	mA
A/D converter						
Resolution	ADC_{RES}		-	12	-	bit
WPT communication						
Bit rate from RX to TX	BR_{RX2TX}		-	250	-	bps
Bit rate from TX to RX	BR_{TX2RX}		-	125	-	bps
COM, CLAMP driver						
ON resistance	R_{ON_DRV}		-	0.5	-	Ω
Leak current	I_{L_DRV}	Pin voltage=15V	-	-	10	uA
Discharge control FET						
ON resistance	R_{ON_DFET}		-	0.4	-	Ω
Resistance between SGND and GND	R_{SG}	V_{DOCD} or V_{DSCD} detection condition	-	5	-	kΩ
SDA, SCL						
High level input voltage	V_{IH_I2C}		1.0	-	-	V
Low level input voltage	V_{IL_I2C}		-	-	0.3	V
Low level output voltage	V_{OL_I2C}	I_{SINK}=2mA	-	-	0.2	V
MODE, CHG/INT, BUZ						
Low level output voltage	V_{OL_OD}	I_{SINK}=2mA	-	-	0.2	V
Leak current	I_{L_OD}	Pin voltage=3V	-	-	5	uA
DDEN						
High level input voltage	V_{IH_DDEN}		1.0	-	-	V
Low level input voltage	V_{IL_DDEN}		-	-	0.3	V
SD						
High level input voltage	V_{IH_SD}		2.6	-	-	V
Low level input voltage	V_{IL_SD}		-	-	0.3	V

8. Functions Description (The values described in this chapter are reference values, not guaranteed values.)

8.1 Operation Mode and SD Pin Function

The RAA457100 have shut down mode and charge mode 1 and charge mode 2, and discharge mode. Table 8.1.1 shows outline of each operating mode, and Table 8.1.2 shows function of each operating mode. Figure 8.1.1 shows mode transition and SD pin function.

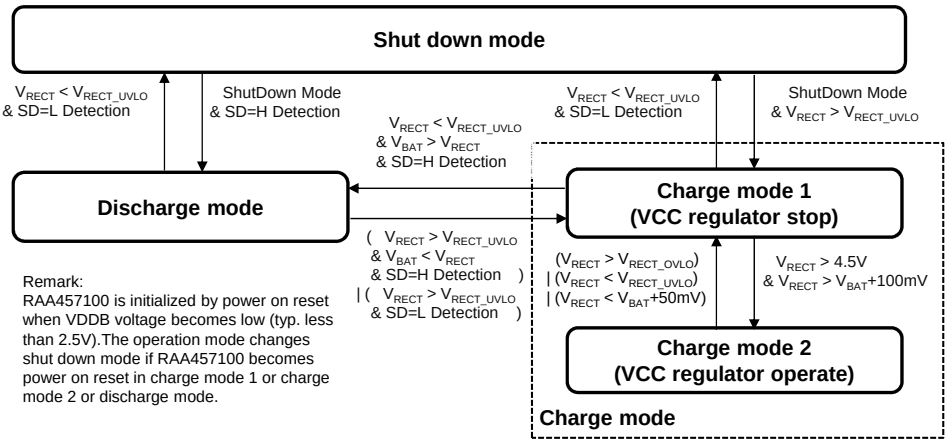
Table 8.1.1 Outline of each operation mode

Operating mode	Description
Shut down mode	Major functions stop in this mode. The conditions in this mode are no power feed by wireless power transmission and battery, or VDDB voltage is lower than 2.5V. In discharge mode, the current from BAT pin to the circuit of this IC is shut down when low level voltage longer than 1 second is input to SD pin. In this state, if V_{RECT} is lower than V_{RECT_UVLO}, the operating mode changes shut down mode.
Charge mode 1	This IC operates by rectified voltage in this mode. In discharge mode if V_{RECT} is higher than V_{RECT_UVLO} and V_{RECT} is higher than V_{BAT}, or in shut down mode if V_{RECT} is higher than V_{RECT_UVLO}, the operating mode changes into charge mode 1.
Charge mode 2	In this mode, battery charging and WPT communication are available. In charge mode 1, if V_{RECT} is higher than 4.5V, and V_{RECT} is higher than V_{BAT}+100mV, the operating mode changes charge mode 2. VCC regulator starts to operate. After VCC regulator starts, VCC regulator continues to operate in condition $V_{RECT} > V_{RECT\_UVLO}$, $V_{RECT} < V_{RECT\_OVLO}$, $V_{RECT} > V_{BAT}$+50mV. The transmission power should be controlled so that the rectified voltage is 0.5V higher than battery voltage. It means that charge control circuit and receiver main system can operate well.
Discharge mode	In this mode, this IC operates by battery power. In shut down mode, if high level voltage longer than 1 second is input to SD pin, the operating mode changes into discharge mode. Or in charging mode 1, if V_{RECT} is lower than V_{RECT_UVLO} and V_{BAT} is higher than V_{RECT}, the operating mode changes into discharge mode.

Table 8.1.2 Function of each operation mode

Operating mode	Battery Protection *1	ADC , VDDW	VCC regulator	Charge control *2	DCDC converter *3
Shut down mode	stop				
Charge mode 1	operate	operate	stop	stop	available
Charge mode 2	operate	operate	operate	available	available
Discharge mode	operate	stop	stop	stop	available

*1 Discharge control FET (DFET) becomes off if battery protection level is detected.
*2 Battery charging is started automatically when operating mode become charge mode 2 if ATCHG pin level is high(VDDB).
Battery charging can be started by register setting (0x01 D[0]=1) if ATCHG pin level is low.
*3 DCDC converter is started when DDEN pin is high level and $V_{CC} > V_{DCDC\_UVLO}$, and discharge control FET is on.



Symbol	Description
&	Logical AND
|	Logical OR
V_{BAT}	Battery voltage (BAT pin voltage)
V_{RECT}	Rectified voltage (RECT pin voltage)
V_{RECT_UVLO}	Rectified output undervoltage detection voltage
V_{RECT_OVLO}	Rectified output overvoltage detection voltage
SD=H Detection *1	High level voltage longer than 1 second is input to SD pin.
SD=L Detection *1	Low level voltage longer than 1 second is input to SD pin.

*1 This detection is operated in all operation mode.

SD pin function	RAA457100 has current switch(BFET) from BAT pin to the circuit of this IC. The current supplies from BAT pin to this IC through BFET when high level voltage is applied to SD pin. RAA457100 selects higher voltage either V_{BAT} or V_{RECT} for operating power of this IC. Detection delay time of SD pin voltage level is 1 second. Mode transition of this IC is operated dependent on SD detection signal.

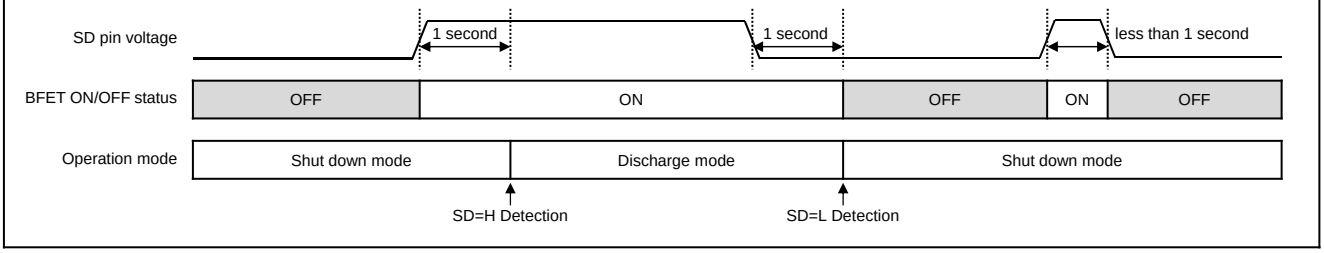
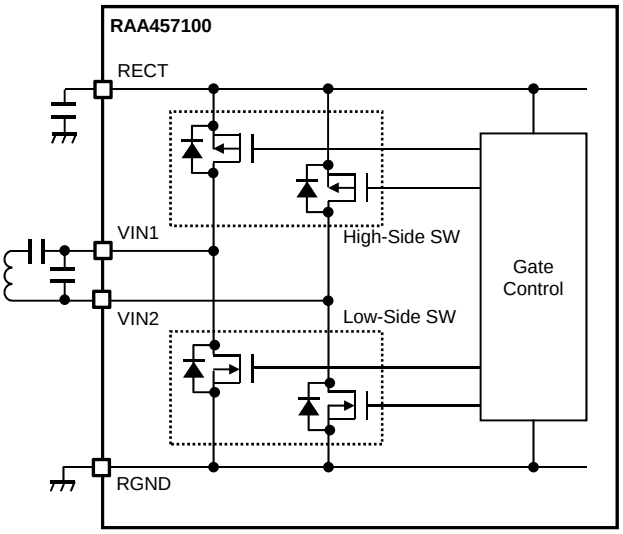


Figure 8.1.1 Mode transition and SD pin function

8.2 Rectifier

Rectifier converts AC voltage (recommended frequency is 125[kHz]) induced at resonant circuit to DC voltage. Figure 8.2.1 shows rectifier circuit. Rectified output (RECT pin) voltage rises in asynchronous rectifying operation by body diode of switch MOSFET. When rectified output voltage lower limit is detected($V_{RECT} > V_{RECT\_UVLO}$), the gate control circuit controls the high side switch depending on VIN1, VIN2, RECT pin voltages (half synchronous rectifying operation). When a current of the high side switch increases, the gate control circuit controls the low side switch too (full synchronous rectifying operation). A current of the high side switch depends on VCC regulator output current(I_{VCC}). When the voltage level of ATR pin and ATPC pin are high voltage, the operation function control depending on VCC regulator current are available in battery charge, such as rectifying operation(half synchronous, half or full synchronous automatically changed) and on-resistance of the high side switch. The settings of the rectifying operation and the on-resistance of the high side switch are five, and the current threshold of the VCC regulator output to change these settings can be set by register (show the register map). When ATR pin level is low voltage, the rectifying operation is half synchronous rectifying operation, and the on-resistance of the high side switch is 1[Ω]. When the settings of the current threshold is not appropriate, rectifying operation becomes unstable (a change of half synchronous rectifying operation and full synchronous rectifying operation becomes unstable), and then ripple voltage of rectified voltage is increased. If the settings of the appropriate current threshold is difficult, it is recommended to set ATR pin level to low voltage.



Rectifier operation /on-resistance of high side switch	VCC regulator current changing	VCC output current threshold	
		Register settings	Initial (mA)
Half synch/1[Ω]	-	-	-
	decreasing	0x1B D[7:0]	3.868
Full synch/8[Ω]	increasing	0x1B D[7:0] + 0x1F D[6:0]	7.736
	decreasing	0x1C D[7:0]	8.087
Full synch/4[Ω]	increasing	0x1C D[7:0] + 0x1F D[6:0]	11.96
	decreasing	0x1D D[7:0]	16.17
Full synch/2[Ω]	increasing	0x1D D[7:0] + 0x1F D[6:0]	20.04
	decreasing	0x1E D[7:0]	31.99
Full synch/1[Ω]	increasing	0x1E D[7:0] + 0x1F D[6:0]	35.86
	-	-	-

Figure 8.2.1 Rectifier circuit, and Rectifier action on ATR pin and ATPC pin = high

8.3 A/D Converter

In charge mode, some pin voltages (RECT pin voltage, BAT pin voltage, etc) are monitored by 12bit A/D converter. Table 8.3.1 shows monitor items of A/D converter. These items are monitored in 4[ms] period. These items are used by calculating parameters for automatic transmission power control and charging control (battery temperature, battery voltage). 2-wire serial interface and WPT communication make it possible to read the A/D conversion results. A/D conversion results in register are not updated automatically. When 0x35 D[0] is 1, all registers of A/D conversion result are updated.

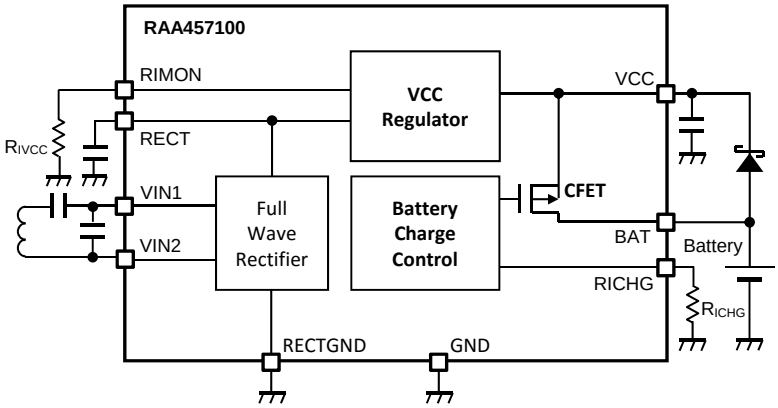
Table 8.3.1 Monitor items of A/D converter

Item	monitor point	Output code *1	Input voltage range *2 (Actual voltage range)	Register(12bit)
Rectified output voltage	RECT pin voltage V_{RECT}	(4096 / 10.8) x V_{RECT}	0 to 10.8V (3.2 to 10 V)	0x36 D[7:4] 0x37 D[7:0]
VCC regulator output current（I_{VCC}）	RIMON pin voltage V_{RIMON}	(4096 / 2.7) x V_{RIMON} (V_{RIMON} = (I_{VCC} x R_{IVCC}) / K_{IVCC})	0 to 2.7 V (0 to 1.2 V)	0x38 D[7:4] 0x39 D[7:0]
Battery voltage	BAT pin voltage V_{BAT}	(4096 / 5.4) x V_{BAT}	0 to 5.0 V (0 to 4.35 V)	0x3A D[7:4] 0x3B D[7:0]
Charging current（I_{CHG}）	RICHG pin voltage V_{RICHG}	(4096 / 2.7) x V_{RICHG} (V_{RICHG} = (I_{CHG} x R_{ICHG}) / K_{ICHG})	0 to 2.7V (0 to 1.2 V)	0x3C D[7:4] 0x3D D[7:0]
Thermistor temperature (Battery temperature)	THM pin voltage V_{THM}	(4096 / 2.7) x V_{THM}	0 to 2.7 V (0 to 2.7 V)	0x3E D[7:4] 0x3F D[7:0]

*1 Output code range is from 0 to 4095.
*2 Each inputted voltage should be within input voltage range to avoid miss converting.
The voltage range in the parenthesis shows a voltage range assumed in practical use.

8.4 Power Supply to VCC Pin

Figure 8.4.1 shows block diagram of VCC regulator and battery charge control and charge control FET(CFET). Charge control FET is conductive in discharge mode and charge mode 1, current from battery flows into VCC pin. VCC regulator operates in charge mode 2. Current from RECT pin flows into VCC pin. When battery charging does not operate, CFET is off. In battery charging, the battery charge control circuit controls the gate voltage of CFET, charging current from VCC pin flows into BAT pin. VCC regulator regulates the voltage which is 3.3V to 4.8V depending on BAT pin voltage. VCC regulator has current limit function showed in Table 8.4.1. VCC regulator output voltage is changed depending on current no limit state or current limit state when charge control operates (Table 8.4.2). If VCC regulator is in current limit state, battery charging current is adjusted depending on limiting current (load current dividing function of charge control circuit). To prevent the current limit by low RECT pin voltage, the transmission power has to maintain recommended RECT pin voltage showed in Table 8.4.2.



Operation mode	
	Description
Discharge mode, Charge mode 1	
	CFET is always conductive, the current from battery flows into VCC pin.
Charge mode 2	
	The power at RECT pin supplies to VCC pin by VCC regulator. CFET is off when charge control circuit does not charge. The charge control circuit controls gate voltage of CFET and the current flows from VCC pin to BAT pin in battery charging.

Figure 8.4.1 Block diagram of VCC regulator and battery charge control and charge control FET

Table 8.4.1 Current limit function of VCC regulator

Item	Description	
Current limit by R_{IVCC}	The maximum output current of VCC regulator can be set by external resistor R_{IVCC} between RIMON pin and GND.	
	The relation of R_{IVCC} and output limiting current	
	Limiting current	$I_{LIM} = K_{IVCC} \times (1.2 / R_{IVCC})$
	Parameter	$K_{IVCC} = 80$ R_{IVCC} = 1.2kΩ, or 2.4kΩ, or 4.8kΩ (prohibit using except recommended value*1)
Current limit by low RECT pin voltage	When the differential voltage between RECT pin and BAT pin is low, VCC regulator output current is limited. The output current starts to be limited on $V_{RECT} - V_{BAT} < 0.4V$, the output current decreases depending on the differential voltage. The output current is limited so that V_{RECT} does not decrease than below voltage.	
	RECT pin voltage when output current of VCC regulator is 0mA.	
	$V_{BAT} > 3.0V$	$V_{RECT} = V_{BAT} + 0.2V$
	$V_{BAT} < 3.0V$	$V_{RECT} = 3.2V$

*1 R_{IVCC} is detected before VCC regulator starts, the circuit works depending on detection result. R_{IVCC} value need to be 1.2k or 2.4k or 4.8kΩ.

Table 8.4.2 VCC pin voltage

BAT pin voltage (V_{BAT})	VCC pin voltage in charge control circuit operating		RECT pin recommended voltage(V_{RECT}) *1
	Current no limit state	Current limit state	
$3.0V \leq V_{BAT} \leq V_{CHG}$	$V_{BAT} + 0.3V$	$V_{BAT} + 0.1V$	$V_{RECT} > V_{BAT} + 0.5V$
$V_{BAT} < 3.0V$	3.3V	3.1V	$V_{RECT} > 3.5V$

*1 This is the condition in order to avoid limiting the output current of VCC regulator by decreasing RECT pin voltage.

8.5 Battery Charge Control

8.5.1 Battery Charge Method

This IC has the charge function for Li-ion battery (constant current - constant voltage charge method). Some charge control parameters can be set by the registers.

8.5.2 Charge Start Voltage, Trickle to Fast Charge Transition Threshold Voltage and Charge Overvoltage Detection Voltage

Table 8.5.2 shows charge start voltage and trickle to fast charge transition threshold voltage and charge overvoltage detection voltage, and detection delay time. These voltages are judged by control circuit using A/D conversion result of BAT pin voltage.

Table 8.5.2 Charge start voltage, Trickle to fast charge transition threshold voltage, Charge overvoltage detection voltage

Item	Detection voltage	Detection delay time
Charge start voltage*1	1.5V (hysteresis voltage 100mV)	256ms
Trickle to fast charge transition threshold voltage	3.0V (hysteresis voltage 100mV)	256ms
Charge overvoltage detection voltage*2	Suitable temperature charge control voltage +100mV	256ms

*1 RAA457100 can charge to zero V battery by setting register D[7] in address 0x04.
*2 In low temperature and suitable temperature and high temperature, each charge control voltage can be set to 4.05V or 4.20V or 4.35V. (show section 8.5.3, 8.5.4)

8.5.3 Charge Current, Charge Complete Current, Charge Control Voltage, Charge Timer

The maximum charge current is 70[mA]. Reference fast charge current I_{CHGR} is set by resistor R_{ICHG} between RICHG pin and GND. Pre-charge current and trickle charge current are set to one tenth(1/10) of reference fast charge current I_{CHGR}. In soft start of fast charge, charging current increases stepped by (1/60)*I_{CHGR} . The transition time of 1 step can be set by register. The fast charge current and the charge control voltage can be set to 3 values in each battery temperature. Trickle charge timer and fast charge timer can be set by register. If the timer overflows, battery charge is stopped. Table 8.5.3 shows the parameters of charge current and charge complete current and charge control voltage, and charge timer.

Table 8.5.3 Charge control parameters

Item	Symbol	Value	Unit	Remark
Reference fast charge current	I_{CHGR}	1.2 x K_{ICHG} / R_{ICHG}	A	K_{ICHG}=80
Pre-charge current Trickle charge current	I_{PRECHG}	0.1 x I_{CHGR}	A	-
Fast charge current range *1	I_{CHG}	I_{CHGR} , 0.5 x I_{CHGR} , 0.25 x I_{CHGR}	A	Register 0x02 D[7:2]
Charge current transition step in soft start of fast charge	I_{CHG_SOFT}	(1 / 60) x I_{CHGR}	A	-
Transition time of one step in soft start of fast charge	T_{CHG_SOFT}	15.625, 7.8125, 3.125	ms	Register 0x02 D[1:0]
Charge control voltage *1	V_{CHG}	4.05 , 4.20 , 4.35	V	Register 0x03 D[7:2]
Charge complete current	I_{FC}	0.20 x I_{CHGR} , 0.15 x I_{CHGR} , 0.10 x I_{CHGR} , 0.05 x I_{CHGR}	A	Register 0x03 D[1:0]
Charge complete judgement voltage	V_{FC}	3.8	V	-
Trickle charge timer	T_{DCHG}	60, 120, 180	min	Register 0x04 D[1:0]
Fast charge timer	T_{CHG}	180, 240, 300, 360	min	Register 0x04 D[3:2]

*1 It can be set in each battery temperature(low, suitable, high).

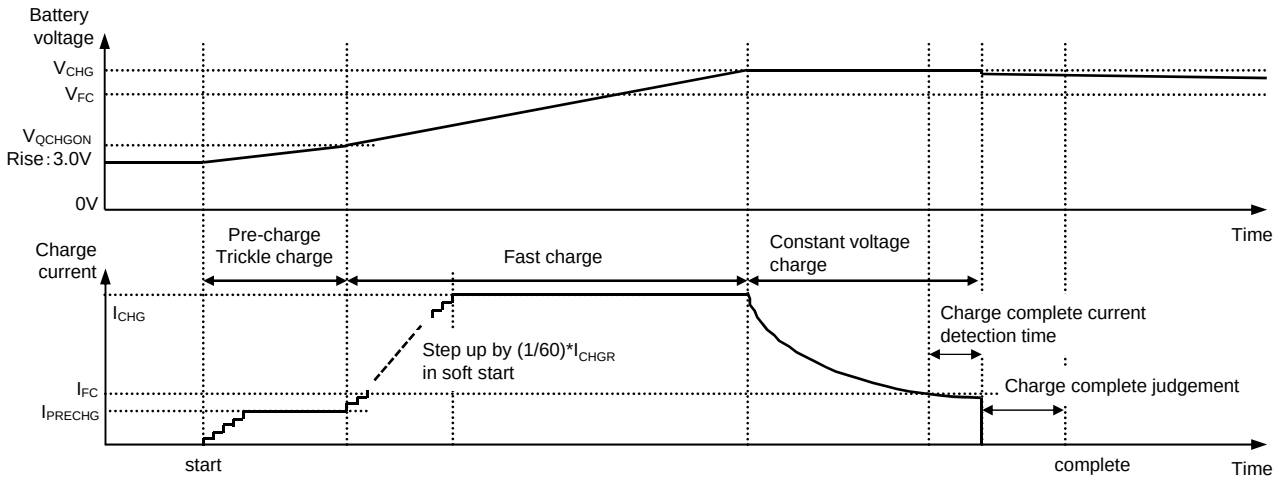


Figure 8.5.3 Charging profile

8.5.4 Battery Temperature Monitor

RAA457100 controls the fast charging current and the charge control voltage depending on battery temperature. The fast charging current and the charge control voltage can be set by registers in each temperature range. But the charge control voltage of low and high temperature range needs to be lower than the charge control voltage of suitable temperature range. The battery temperature range threshold can be set by registers that are THM_TH_NB_LE(no battery and charge pending in low temperature threshold), THM_TH_L_LE(low rate charge in low temperature and charge pending in low temperature threshold), THM_TH_M_L(normal charge and low rate charge in low temperature threshold), THM_TH_M_H(normal charge and low rate charge in high temperature threshold), THM_TH_H_HE(low rate charge in high temperature and charge pending in high temperature threshold), THM_TH_HYS(hysteresis) in address 0x05 to 0x0A. THM_TH_LE_NB(charge pending in low temperature and no battery threshold), THM_TH_LE_L(charge pending in low temperature and low rate charge in low temperature threshold), THM_TH_L_M(low rate charge in low temperature and normal charge threshold), THM_TH_H_M(low rate charge in high temperature and normal charge threshold), THM_TH_HE_H(charge pending in high temperature and low rate charge in high temperature threshold) are calculated by the registers described above. These registers are written initially by the value for NTC thermistor NCP03WF104F05RL, NCP15WF104F03RC (Murata Manufacturing) or an equivalent device. (refer to register map)

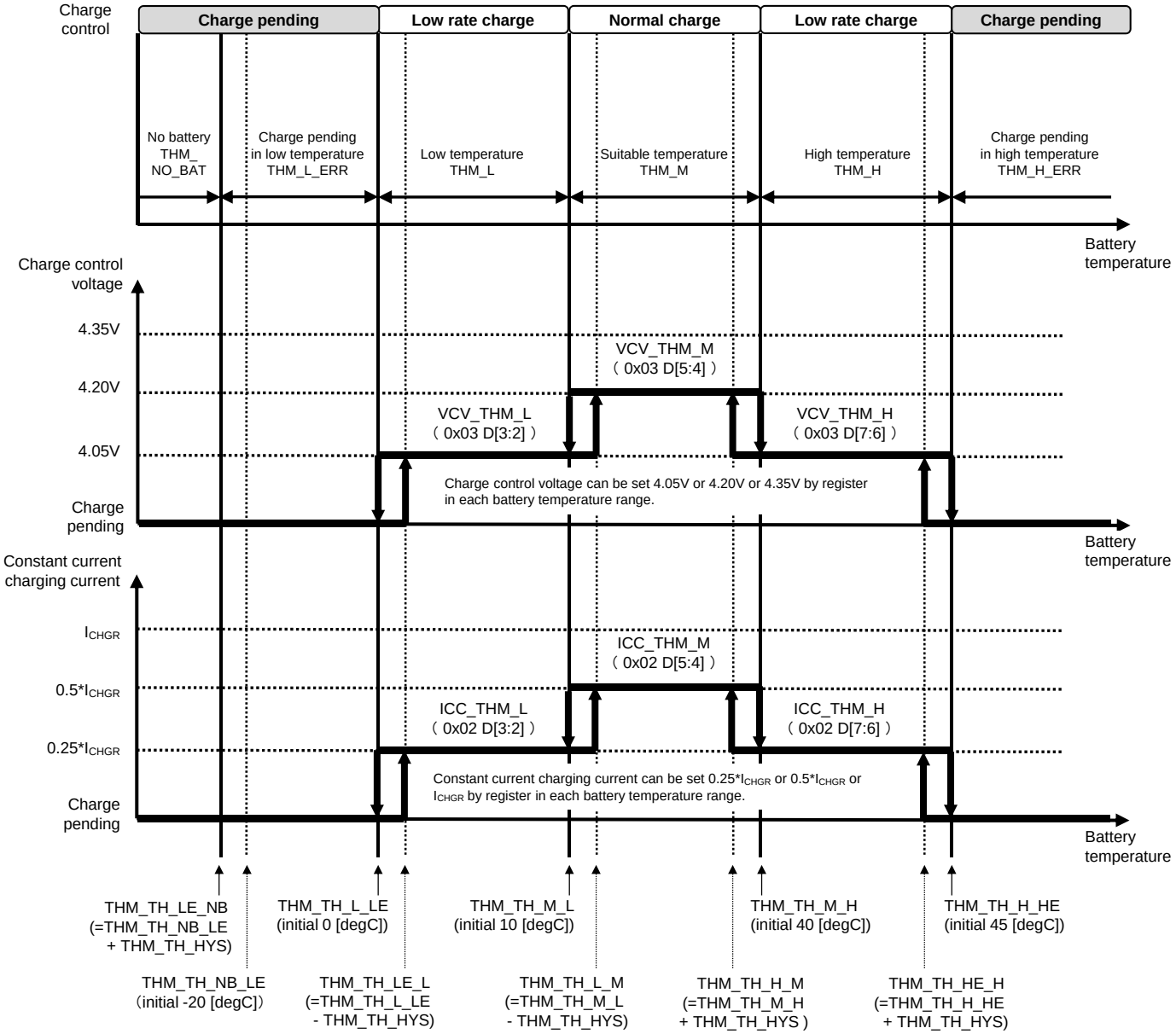
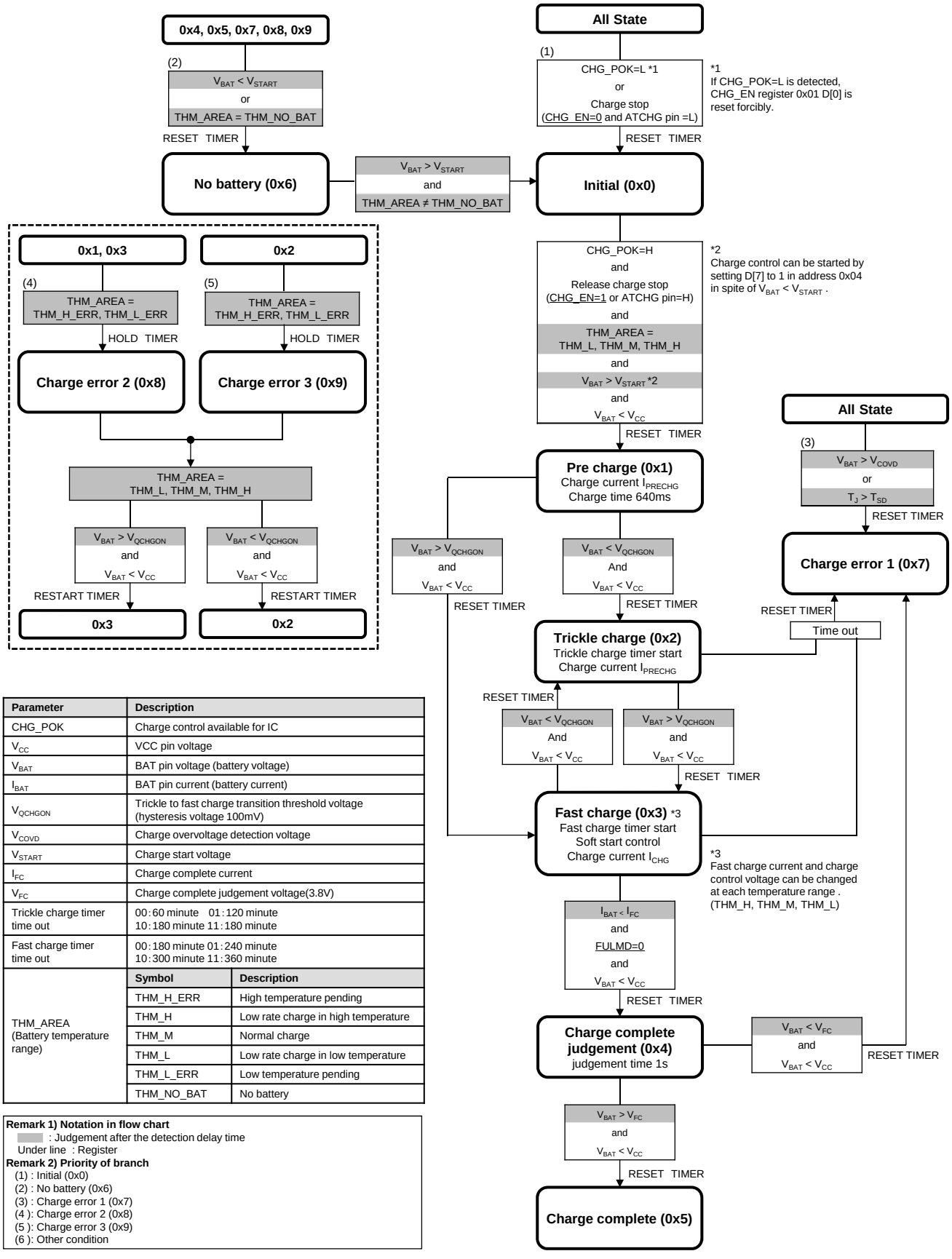


Figure 8.5.4 Battery temperature threshold, Charge control voltage, Constant current charge current

8.5.5 Charge State Transition Diagram



Parameter	Description	
CHG_POK	Charge control available for IC	
V_{CC}	VCC pin voltage	
V_{BAT}	BAT pin voltage (battery voltage)	
I_{BAT}	BAT pin current (battery current)	
V_{QCHGON}	Trickle to fast charge transition threshold voltage (hysteresis voltage 100mV)	
V_{COVD}	Charge overvoltage detection voltage	
V_{START}	Charge start voltage	
I_{FC}	Charge complete current	
V_{FC}	Charge complete judgement voltage(3.8V)	
Trickle charge timer time out	00:60 minute 01:120 minute 10:180 minute 11:180 minute	
Fast charge timer time out	00:180 minute 01:240 minute 10:300 minute 11:360 minute	
THM_AREA (Battery temperature range)	**Symbol**	**Description**
	THM_H_ERR	High temperature pending
	THM_H	Low rate charge in high temperature
	THM_M	Normal charge
	THM_L	Low rate charge in low temperature
	THM_L_ERR	Low temperature pending
	THM_NO_BAT	No battery

Remark 1) Notation in flow chart
: Judgement after the detection delay time
Under line : Register
Remark 2) Priority of branch
(1) : Initial (0x0)
(2) : No battery (0x6)
(3) : Charge error 1 (0x7)
(4): Charge error 2 (0x8)
(5): Charge error 3 (0x9)
(6): Other condition

8.6 Power Supply to Application System (Buck DCDC Converter, Battery Protection)

8.6.1 Buck DCDC Converter

The buck DCDC converter supplies power to application system. The input voltage of DCDC converter is VCC pin voltage. DCDC converter starts when DDEN pin level is high. DCDC converter output voltage can be set by settings of DDST0 pin and DDST1 pin (show Table 8.6.1.1). Some status of DCDC converter can be monitored by registers. When 2-wire serial interface set into slave device by setting MS pin to low, an application system can read the registers by 2-wire serial interface. Table 8.6.1.2 shows registers related to DCDC converter. If the equivalent series resistance of output capacitor C_{DD} is small, the output ripple voltage might be increased. If the DCDC converter output is unstable, series resistance R_{DD} should be connected to output capacitor C_{DD} for improvement (Refer to Block Diagram).

Table 8.6.1.1 DCDC converter output voltage settings

Voltage input	Enable pin	DDST1 pin	DDST0 pin	Output voltage
VCC	DDEN *1	L	L	1.2V
		L	H	1.5V
		H	L	1.8V
		H	H	3.0V

*1 DCDC converter starts when DDEN pin level is high.
If battery protection and junction temperature error and UVLO(V_{CC} < V_{DCDC_UVLO}) is detected, DCDC converter is stopped.

Table 8.6.1.2 Registers related to DCDC converter

Item	Register	Description
VCC pin voltage detection (UVLO detection)	0x33 D[4]	DCDC converter is controlled depending on VCC pin voltage level. 0 : Stop (UVLO detected) V_{CC} < 2.80V(Output voltage is 1.2V or 1.5V or 1.8V) V_{CC} < 3.18V(Output voltage is 3.0V) 1 : Start (UVLO release) V_{CC} > 2.90V(Output voltage is 1.2V or 1.5V or 1.8V) V_{CC} > 3.30V(Output voltage is 3.0V)
Start up complete	0x33 D[5]	DCDC converter confirms the completion of start up by monitoring SYS pin voltage. 0 : Low voltage status of SYS pin (V_{SYS} < Setting output voltage x 0.831) 1 : Start up complete (V_{SYS} > Setting output voltage x 0.875)
Overvoltage detection of SYS pin	0x33 D[6]	DCDC converter stops switching MOSFET if overvoltage is detected at SYS pin. 0 : Not detected (V_{SYS} < Setting output voltage x 1.207) 1 : Detected (V_{SYS} > Setting output voltage x 1.250)
Overcurrent detection *1	0x33 D[7] 0x30 D[2]	If overcurrent condition of DCDC converter is detected continuously, the status register is 1(0x33 D[7]=1). The delay time of detection is 8ms.

*1 Interruption signal is output from CHG/INT pin when MS pin level is low and register 0x2F D[2] is 0.

8.6.2 Battery Protection, Maximum Junction Temperature Protection

Battery protection functions are discharge overvoltage protection and discharge overcurrent protection and discharge short circuit current protection. Temperature protection is maximum junction temperature protection. Table 8.6.2 shows protection detection threshold and detection delay time and post-processing.

Table 8.6.2 Protection detection threshold, Detection delay time, Post-processing

Item (Voltage for detection)	Detection voltage / temperature	Detection delay time	Post-processing *1				
			Discharge control FET	Resistor between SGND and GND	DCDC Converter *2	Digital input / output pins *3	Charge control
Discharge overvoltage (between BAT and GND)	2.8V	32ms	off	disconnect	suspend	suspend	-
Discharge overcurrent (between SGND and GND)	80mV	4ms	off	connect	suspend	suspend	-
Discharge short circuit current (between SGND and GND)	160mV	250us	off	connect	suspend	suspend	-
Maximum junction temperature	68 degree C	256ms	off	disconnect	suspend	suspend	suspend

*1 DCDC converter, discharge control FET and digital input/output pins restart automatically from suspend when each protection is released.
*2 DCDC converter is also suspended when VCC pin voltage is lower than UVLO voltage(V_{DCDC_UVLO}).
*3 MODE, CHG/INT, BUZ, SCL and SDA pins are applicable.

8.7 Battery Low Voltage Notification (BUZ pin)

Battery low voltage notification has two threshold voltages depending on DCDC converter output voltage. There are two ways of notice. BUZ pin (open drain output) outputs low level when battery low voltage H or battery low voltage L is detected and register 0x34 D[2] is 0. BUZ pin outputs specified pulse (show Table 8.7) when register 0x34 D[2] is 1. Battery low voltage detection result is also stored in register 0x34 D[1:0].

Table 8.7 Battery low voltage notification

Item	DCDC converter output voltage	Detection voltage	Detection delay time	Post-processing	
				0x34 D[2]=0	0x34 D[2]=1
Battery low voltage detection H (between BAT and GND)	1.2V, 1.5V, 1.8V	3.20V	256ms	BUZ pin outputs low level. When battery voltage becomes higher than detection voltage, BUZ pin returns high level.	BUZ pin outputs pulse, 256[ms] low level pulse width in 2560[ms] period.
	3.0V	3.55V			
Battery low voltage detection L (between BAT and GND)	1.2V, 1.5V, 1.8V	3.05V			BUZ pin outputs pulse, 128[ms] low level pulse width in 1280[ms] period.
	3.0V	3.35V			

8.8 Charge Status Notification / Interrupt Signal Output (CHG / INT pin)

CHG / INT pin(open drain output) function is changed by MS pin setting. Table 8.8.1 shows this function. CHG / INT pin outputs low level when interruption event showed in Table 8.8.2 occurs and MS pin is low level. These interruption events can be masked by setting mask register showed in Table 8.8.3.

Table 8.8.1 CHG / INT pin function description

MS pin	Description
L (GND)	CHG / INT pin outputs low level when interruption event occurs (refer to Table 8.8.2). Application system can confirm interruption event factor by reading factor register after receiving that CHG / INT pin is low level .
H (VDDB)	CHG / INT pin outputs low level when charge control circuit status is pre-charge or trickle charge or fast charge.

Table 8.8.2 Interruption signal output event

Item	Factor register	Description
WPT communication receive notification	0x30 D[0]	WPT communication data is received from transmitter. The register is clear after reading.
Charge state transition notification	0x30 D[1]	Charge state transition. (Refer to charge state transition diagram) The register is clear after reading.
DCDC converter overcurrent detection	0x30 D[2]	DCDC converter detects overcurrent. This register is always set by 1 in overcurrent.
VCC regulator current limit detection	0x30 D[3]	VCC regulator limits output current. This register is always set by 1 in limiting current.

Table 8.8.3 Interruption signal output mask register

Item	Mask register	Description
WPT communication receive notification	0x2F D[0]	0 : Interruption output available, 1 : Interruption output unavailable If all mask register are set by 1, CHG / INT pin function is as same as MS pin=H .
Charge state transition notification	0x2F D[1]	
DCDC converter overcurrent detection	0x2F D[2]	
VCC regulator current limit detection	0x2F D[3]	

8.9 Charge Mode or Discharge Mode Notification (MODE pin)

MODE pin level depends on charge mode or discharge mode.

Table 8.9 MODE pin function description

MODE pin	Description
L	MODE pin outputs low level in charge mode 1 or 2. If MODE pin connects to DDEN pin and DDEN connects VCC or VDDB via external resistor, DCDC converter stops in charge mode (Refer to block circuit). When register 0x00 D[0] is 1, MODE pin level is always high (Open drain output is off).
H	Mode pin outputs high level in discharge mode (Open drain output is off).

8.10 2-wire Serial Communication Interface (MS, SCL, SDA pin)

RAA457100 can communicate to application system by 2-wire serial interface. Master device or slave device can be selected by MS pin setting. Figure 8.10.1(a), (b) shows SDA data format in slave device, Figure 8.10.2(a), (b) shows SDA data format in master device. Figure 8.10.3 shows timing specification. High level input threshold voltage of SDA and SCL pins is low voltage (less than 1.0V). The communication may be affected adversely if noise voltage at pins is high. If communication error occurs, capacitor should be put between that pins and GND for filtering noise.

Table 8.10.1 2-wire serial interface outline

MS pin	SCL frequency	Description
L (GND)	64 [kHz]	RAA457100 becomes slave device. The slave device address is 0x0A(0001010). Application system can read and write registers. 0x40 D[0] should be set to 1 for writing into the registers in address 0x00 to 0x0F.
H (VDDB)	64 [kHz]	RAA457100 becomes master device. The transmitter system can write and read the register of receiver application system via WPT communication. When RAA457100 receives an access requirement (read or write register) from transmitter system to receiver application system, RAA457100 converts the access requirement to 2-wire serial interface format and communicates to receiver application system.

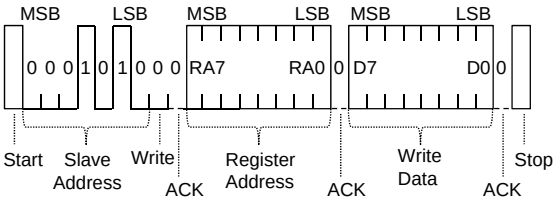


Figure 8.10.1(a) SDA data format(Slave, Write)

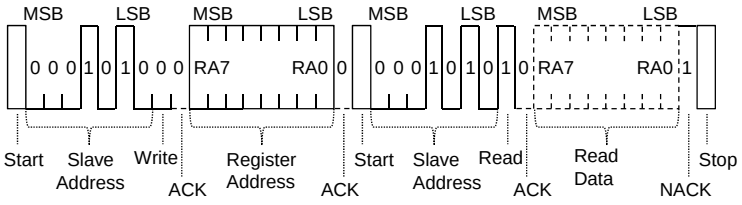


Figure 8.10.1(b) SDA data format(Slave, Read)

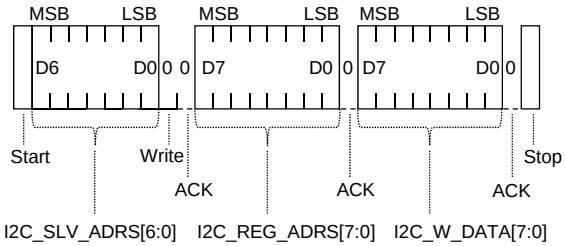


Figure 8.10.2(a) SDA data format(Master, Write)

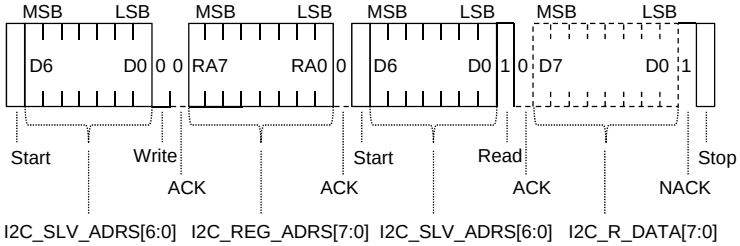
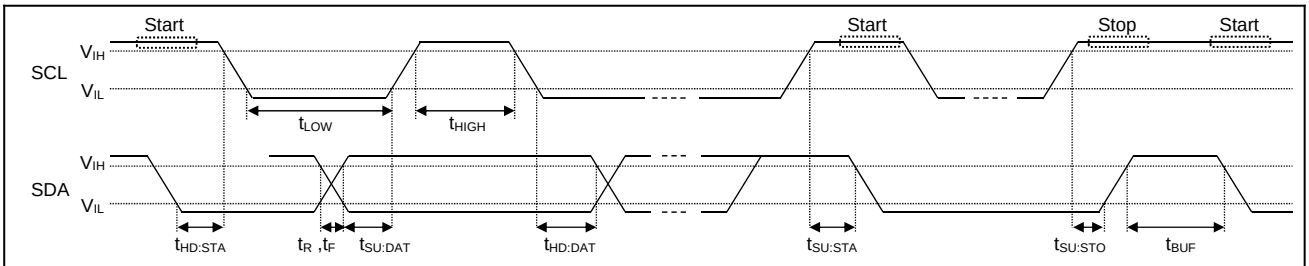


Figure 8.10.2(b) SDA data format(Master, Read)



Symbol	Item	Min	Max	Unit
fSCL	SCL clock frequency	0	64	kHz
tBUF	Bus free time between Stop condition and Start condition	8.1	-	us
tHD:STA	Hold time of Start condition or repeated Start condition (First clock pulse is generated after this period)	3.7	-	us
tLOW	Low hold time of the SCL clock	8.1	-	us
tHIGH	High hold time of the SCL clock	3.7	-	us
tSU:STA	Set-up time for a repeated Start condition	3.7	-	us
tHD:DAT	Data hold time (for input data)	3.7	-	us
tSU:DAT	Data set-up time	3.7	-	us
tR	Rise time of both SDA and SCL signals	-	0.3	us
tF	Fall time of both SDA and SCL signals	-	0.3	us
tSU:STO	Set-up time for Stop condition	3.7	-	us

Figure 8.10.3 2-wire serial interface SCL, SDA timing diagram (for reference)

8.11 WPT Communication and Rectified Output Overvoltage Protection

8.11.1 Outline

RAA457100 and RAA458100(Transmitter IC) support a bidirectional communication by amplitude modulation on wireless power transmission carrier signal. In receiver to transmitter communication, RAA457100 changes transmitting antenna voltage by load modulation and then RAA458100 detects the voltage variation and demodulates data. In transmitter to receiver communication, RAA458100 changes rectified voltage of RAA457100 by changing transmission power and then RAA457100 detects the voltage variation and demodulates data.

8.11.2 Packet Format in WPT Communication

The packet of WPT communication is consisted of fixed data length packet including Preamble, Header, Message1, Message2, Checksum showed in Figure 8.11.2. The Header, Message1, Message2 have 1 bit of odd parity bit respectively, and the check sum generated by exclusive OR is added to the last of the packet. When ATPC pin level of RAA458100 and RAA457100 is high, automatic transmission power control function is available (ATPC Mode). In ATPC Mode, the packet which includes a special header code (0x00 to 0x0F) is sent from RAA457100 to RAA458100 periodically, and RAA458100 adjusts transmission power based on the data included in packet.

Preamble (11bit)	St	Header (8bit)	Pr	Sp	St	Message1 (8bit)	Pr	Sp	St	Message2 (8bit)	Pr	Sp	St	Checksum (8bit)	Pr	Sp

St : Start bit(1bit), Pr : Parity bit(1bit), Sp : Stop bit(1bit)

Figure 8.11.2 Data packet format

Table 8.11.2 Header code

Header code	Description
0x00 to 0x0F	Header code for automatic transmission power control function (ATPC Mode)
0x10 to 0xFF	Header code for any user purpose

8.11.3 Data Transfer Function

RAA457100 modulates transmitting antenna voltage by switching COM1, COM2 driver (NMOS open drain) depending on transmission data. C_{CM1} between VIN1 pin and COM1 pin, and C_{CM2} between VIN2 pin and COM2 pin are connected or disconnected to GND by COM1 and COM2 driver. If peak current of COM driver needs to suppress, series resistor R_{CM1}, R_{CM2} need to be inserted. (Refer to Block diagram)

8.11.4 Data Receive Function

RAA457100 demodulates data packet showed in Figure 8.11.2 . RAA457100 detects rectified voltage variation depending on modulated signal from transmitter and demodulates. RAA458100 can read and write the register of RAA457100 by using the specific header code.

8.11.5 Communication Bit Rate

Table 8.11.5 shows communication bit rate. The transmission data rate is 250[bps], the reception data rate is 125[bps].

Table 8.11.5 Communication bit rate

Communication direction	Bit rate	Remark
Data transmission (Receiver to transmitter)	250bps	
Data reception (Transmitter to receiver)	125bps	

8.11.6 Rectified Output Overvoltage Protection(Clamp function)

When rectified output overvoltage(V_{RECT_OVD}) is detected, rectified voltage is suppressed by clamp function. Connect C_{CP1} between VIN1 pin and CLMP1 pin, and C_{CP2} between VIN2 pin and CLMP2 pin. These capacitors are connected between VIN1 pin, VIN2 pin and GND by clamp driver of CLMP1pin and CLMP2 pin(NMOS open drain), then rectified voltage is suppressed. If peak current of clamp driver needs to suppress, series resistor R_{CP1}, R_{CP2} need to be inserted. (Refer to Block diagram)

8.12 Wired Charging Function (WRC pin)

RAA457100 can charge not only by wireless but also by wire. Wireless or wired charging is selectable by voltage level of WRC pin.
(Refer to Table 8.12)

Table 8.12 WRC pin function

WRC pin level	Description
L (GND)	Wireless charging is selected using RAA457100 and RAA458100.
H (VDDB)	Wired charging is selected using RAA457100 only. 5 V DC should be supplied to RECT pin.

9. Register Map (The values described in this chapter are reference values, not guaranteed values.)

9.1 Address 0x00 to 0x07 (Transmitter system can write to these register.)

Address	Bit No.	Register Name	Init	R/W	Description
0x00	D0	MODE_OFF	0	R/W	MODE pin output disable 0 : Enable 1 : Disable(NMOS Tr OFF usually)
	D1		0	R	
	D2		0	R	
	D3		0	R	
	D4		0	R	
	D5		0	R	
	D6		0	R	
	D7		0	R	
0x01	D0	CHG_EN	0	R/W	Charge start enable 0 : Charge stop(Initialize charging flow) 1 : Charge start
	D1		0	R	
	D2		0	R	
	D3		0	R	
	D4		0	R	
	D5		0	R	
	D6		0	R	
	D7		0	R	
0x02	D0	TCC_SOFT[0]	0	R/W	Trickle to fast charging transition time(per one step) 0 : 15.625[ms] 1 : 7.8125[ms] 2 : 3.125[ms] 3 : Unused
	D1	TCC_SOFT[1]	0	R/W	
	D2	ICC_THM_L[0]	1	R/W	Fast charge current setting of low temperature operation in battery temperature profile 0 : ICHGR 1 : 0.5*ICHGR 2 : 0.25*ICHGR 3 : 0.25*ICHGR
	D3	ICC_THM_L[1]	0	R/W	
	D4	ICC_THM_M[0]	1	R/W	Fast charge current setting of suitable temperature operation in battery temperature profile 0 : ICHGR 1 : 0.5*ICHGR 2 : 0.25*ICHGR 3 : 0.25*ICHGR
	D5	ICC_THM_M[1]	0	R/W	
	D6	ICC_THM_H[0]	1	R/W	Fast charge current setting of high temperature operation in battery temperature profile 0 : ICHGR 1 : 0.5*ICHGR 2 : 0.25*ICHGR 3 : 0.25*ICHGR
	D7	ICC_THM_H[1]	0	R/W	
0x03	D0	ICV_FIN[0]	0	R/W	Constant voltage charge complete current setting 0 : 0.1*ICHGR 1 : 0.05*ICHGR 2 : 0.15*ICHGR 3 : 0.2*ICHGR
	D1	ICV_FIN[1]	0	R/W	
	D2	VCV_THM_L[0]	0	R/W	Constant voltage charge control voltage setting of low temperature operation in battery temperature profile 0 : 4.05[V] 1 : 4.20[V] 2 : 4.35[V] 3 : 4.05[V]
	D3	VCV_THM_L[1]	0	R/W	
	D4	VCV_THM_M[0]	1	R/W	Constant voltage charge control voltage setting of suitable temperature operation in battery temperature profile 0 : 4.05[V] 1 : 4.20[V] 2 : 4.35[V] 3 : 4.05[V]
	D5	VCV_THM_M[1]	0	R/W	
	D6	VCV_THM_H[0]	0	R/W	Constant voltage charge control voltage setting of high temperature operation in battery temperature profile 0 : 4.05[V] 1 : 4.20[V] 2 : 4.35[V] 3 : 4.05[V]
	D7	VCV_THM_H[1]	0	R/W	
0x04	D0	TIM_CHG_TRKL[0]	1	R/W	Trickle charge timer setting 0 : 60[min] 1 : 120[min] 2 : 180[min] 3 : 180[min]
	D1	TIM_CHG_TRKL[1]	1	R/W	
	D2	TIM_CHG_CCCV[0]	1	R/W	Fast charge timer setting 0：180[min] 1：240[min] 2：300[min] 3：360[min]
	D3	TIM_CHG_CCCV[1]	1	R/W	
	D4	TIM_CHG_STOP	0	R/W	Charge control timer halt setting 0 : Count 1 : Halt
	D5		0	R	
	D6	FULMD	0	R/W	0 : Normal operation 1 : Full charge mode (Charge is continued in spite of detecting charge complete current)
	D7	VCHG_ST_0V	0	R/W	Charge start threshold voltage 0 : 1.5[V] 1 : 0[V]
0x05	D0	THM_TH_H_HE[0]	1	R/W	Transition temperature setting of High temperature low rate charge to Charge pending in high temperature : THM_TH_H_HE 5.273[mV/code] { 0, THM_TH_H_HE[7:0], 000 } and 12 bit A/D converted value of THM pin voltage are compared. The value higher than 25[degC] including hysteresis can be set (because of MSB=0 fixed) Initial value : 45[degC] at NTC thermistor NCP03WF104F05RL(Murata Manufacturing) (9bit resolution, 153 x 5.273=806.7[mV] at THM pin voltage) Transition temperature of Charge pending in high temperature to High temperature low rate charge : THM_TH_HE_H is calculated by { 0, THM_TH_H_HE[7:0], 000 } + { 0000, THM_TH_HYS[4:0], 000 } Register value is applied by 0x0A D[7]=1
	D1	THM_TH_H_HE[1]	0	R/W	
	D2	THM_TH_H_HE[2]	0	R/W	
	D3	THM_TH_H_HE[3]	1	R/W	
	D4	THM_TH_H_HE[4]	1	R/W	
	D5	THM_TH_H_HE[5]	0	R/W	
	D6	THM_TH_H_HE[6]	0	R/W	
	D7	THM_TH_H_HE[7]	1	R/W	
0x06	D0	THM_TH_M_H[0]	1	R/W	Transition temperature setting of Suitable temperature charge to High temperature low rate charge : THM_TH_M_H 5.273[mV/code] { 0, THM_TH_M_H[7:0], 000 } and 12 bit A/D converted value of THM pin voltage are compared. The value higher than 25[degC] including hysteresis can be set (because of MSB=0 fixed) Initial value : 40[degC] at NTC thermistor NCP03WF104F05RL(Murata Manufacturing) (9bit resolution, 177 x 5.273=933.3[mV] at THM pin voltage) Transition temperature of High temperature low rate charge to Suitable temperature charge : THM_TH_H_M is calculated by { 0, THM_TH_M_H[7:0], 000 } + { 0000, THM_TH_HYS[4:0], 000 } Register value is applied by 0x0A D[7]=1
	D1	THM_TH_M_H[1]	0	R/W	
	D2	THM_TH_M_H[2]	0	R/W	
	D3	THM_TH_M_H[3]	0	R/W	
	D4	THM_TH_M_H[4]	1	R/W	
	D5	THM_TH_M_H[5]	1	R/W	
	D6	THM_TH_M_H[6]	0	R/W	
	D7	THM_TH_M_H[7]	1	R/W	
0x07	D0	THM_TH_M_L[0]	0	R/W	Transition temperature setting of Suitable temperature charge to Low temperature low rate charge : THM_TH_M_L 5.273[mV/code] { 1, THM_TH_M_L[7:0], 000 } and 12 bit A/D converted value of THM pin voltage are compared. The value less than 25[degC] including hysteresis can be set (because of MSB=1 fixed) Initial value : 10[degC] at NTC thermistor NCP03WF104F05RL(Murata Manufacturing) (9bit resolution, (256+86) x 5.273=1803[mV] at THM pin voltage） Transition temperature of Low temperature low rate charge to Suitable temperature charge : THM_TH_L_M is calculated by { 1, THM_TH_M_L[7:0], 000 } – { 0000, THM_TH_HYS[4:0], 000 } Register value is applied by 0x0A D[7]=1
	D1	THM_TH_M_L[1]	1	R/W	
	D2	THM_TH_M_L[2]	1	R/W	
	D3	THM_TH_M_L[3]	0	R/W	
	D4	THM_TH_M_L[4]	1	R/W	
	D5	THM_TH_M_L[5]	0	R/W	
	D6	THM_TH_M_L[6]	1	R/W	
	D7	THM_TH_M_L[7]	0	R/W	

9.2 Address 0x08 to 0x0F (Transmitter system can write to these register.)

Address	Bit No.	Register Name	Init	R/W	Description
0x08	D0	THM_TH_L_LE[0]	0	R/W	Transition temperature setting of Low temperature low rate charge to Charge pending in low temperature : THM_TH_L_LE 5.273[mV/code] { 1, THM_TH_L_LE[7:0], 000 } and 12 bit A/D converted value of THM pin voltage are compared. The value less than 25[degC] including hysteresis can be set (because of MSB=1 fixed) Initial value : 0[degC] at NTC thermistor NCP03WF104F05RL(Murata Manufacturing) (9bit resolution, (256+140) x 5.273=2088[mV] at THM pin voltage) Transition temperature of Charge pending in low temperature to Low temperature low rate charge : THM_TH_LE_L is calculated by { 1, THM_TH_L_LE[7:0], 000 } – { 0000, THM_TH_HYS[4:0], 000 } Register value applied by 0x0A D[7]=1.
	D1	THM_TH_L_LE[1]	0	R/W	
	D2	THM_TH_L_LE[2]	1	R/W	
	D3	THM_TH_L_LE[3]	1	R/W	
	D4	THM_TH_L_LE[4]	0	R/W	
	D5	THM_TH_L_LE[5]	0	R/W	
	D6	THM_TH_L_LE[6]	0	R/W	
	D7	THM_TH_L_LE[7]	1	R/W	
0x09	D0	THM_TH_NB_LE[0]	0	R/W	Transition temperature setting of No battery to Charge pending in low temperature : THM_TH_NB_LE 5.273[mV/code] { 1, THM_TH_NB_LE[7:0], 000 } and 12 bit A/D converted value of THM pin voltage are compared. The value less than 25[degC] including hysteresis can be set (because of MSB=1 fixed) Initial value : -20[degC] at NTC thermistor NCP03WF104F05RL(Murata Manufacturing) (9bit resolution, (256+212) x 5.273=2467[mV] at THM pin voltage) Transition temperature of Charge pending in low temperature to No battery : THM_TH_LE_NB is calculated by { 1, THM_TH_NB_LE[7:0], 000 } + { 0000, THM_TH_HYS[4:0], 000 } Register value applied by 0x0A D[7]=1.
	D1	THM_TH_NB_LE[1]	0	R/W	
	D2	THM_TH_NB_LE[2]	1	R/W	
	D3	THM_TH_NB_LE[3]	0	R/W	
	D4	THM_TH_NB_LE[4]	1	R/W	
	D5	THM_TH_NB_LE[5]	0	R/W	
	D6	THM_TH_NB_LE[6]	1	R/W	
	D7	THM_TH_NB_LE[7]	1	R/W	
0x0A	D0	THM_TH_HYS[0]	0	R/W	Battery transition temperature setting : Hysteresis 5.273[mV/code] Initial value : 3[degC] around (Hysteresis depend on temperature because of non linearity of thermistor) (9bit resolution, 18 x 5.273=94.91[mV] at THM pin voltage) THM_TH_HE_H, THM_TH_H_M, THM_TH_L_M, THM_TH_LE_L, THM_TH_LE_NB are calculated by adding this to 0x05 to 0x09 or subtracting this from 0x05 to 0x09. Register value applied by 0x0A D[7]=1.
	D1	THM_TH_HYS[1]	1	R/W	
	D2	THM_TH_HYS[2]	0	R/W	
	D3	THM_TH_HYS[3]	0	R/W	
	D4	THM_TH_HYS[4]	1	R/W	
	D5		0	R	
	D6		0	R	
	D7	THM_TH_UPLOAD	0	R/W	1 : Transition temperature register values (0x05 to 0x0A) are applied. This register is reset after applying.
0x0B	D0	I2C_TRIG	0	R/W	2-wire I/F communication trigger 0 : Stand-by state 1 : Communication start (When MS pin is high level)
	D1	I2C_READ	0	R/W	2-wire I/F Write/Read selection 0 : Write 1 : Read (When MS pin is high level)
	D2		0	R	
	D3		0	R	
	D4		0	R	
	D5		0	R	
	D6		0	R	
	D7		0	R	
0x0C	D0	I2C_SLV_ADRS[0]	0	R/W	Slave address setting for 2-wire I/F of receiver application device (When MS pin is high level)
	D1	I2C_SLV_ADRS[1]	0	R/W	
	D2	I2C_SLV_ADRS[2]	0	R/W	
	D3	I2C_SLV_ADRS[3]	0	R/W	
	D4	I2C_SLV_ADRS[4]	0	R/W	
	D5	I2C_SLV_ADRS[5]	0	R/W	
	D6	I2C_SLV_ADRS[6]	0	R/W	
	D7		0	R	
0x0D	D0	I2C_REG_ADRS[0]	0	R/W	Register address setting for 2-wire I/F of receiver application device (When MS pin is high level)
	D1	I2C_REG_ADRS[1]	0	R/W	
	D2	I2C_REG_ADRS[2]	0	R/W	
	D3	I2C_REG_ADRS[3]	0	R/W	
	D4	I2C_REG_ADRS[4]	0	R/W	
	D5	I2C_REG_ADRS[5]	0	R/W	
	D6	I2C_REG_ADRS[6]	0	R/W	
	D7	I2C_REG_ADRS[7]	0	R/W	
0x0E	D0	I2C_W_DATA[0]	0	R/W	Write data setting for 2-wire I/F of receiver application device (When MS pin is high level)
	D1	I2C_W_DATA[1]	0	R/W	
	D2	I2C_W_DATA[2]	0	R/W	
	D3	I2C_W_DATA[3]	0	R/W	
	D4	I2C_W_DATA[4]	0	R/W	
	D5	I2C_W_DATA[5]	0	R/W	
	D6	I2C_W_DATA[6]	0	R/W	
	D7	I2C_W_DATA[7]	0	R/W	
0x0F	D0	I2C_R_DATA[0]	0	R	Read data for 2-wire I/F of receiver application device (When MS pin is high level)
	D1	I2C_R_DATA[1]	0	R	
	D2	I2C_R_DATA[2]	0	R	
	D3	I2C_R_DATA[3]	0	R	
	D4	I2C_R_DATA[4]	0	R	
	D5	I2C_R_DATA[5]	0	R	
	D6	I2C_R_DATA[6]	0	R	
	D7	I2C_R_DATA[7]	0	R	

9.3 Address 0x10 to 0x17

Address	Bit No.	Register Name	Init	R/W	Description
0x10	D0	ATPCRX_INTERVAL	0	R/W	Rx to Tx WPT communication period(ATPC Mode) 0:1[s]/2[s] 1:2[s]/4[s] (Identification, Configuration / Battery Charge)
	D1		0	R	
	D2		0	R	
	D3		0	R	
	D4		0	R	
	D5		0	R	
	D6		0	R	
	D7		0	R	
0x11	D0	ATPCRX_CTRL_ERR_OFS1[0]	0	R/W	Control error calculation offset ΔV1 (ATPC Mode) ΔV1 is applied to offset voltage in condition of fast charge state and ICHG > 0.2C 10.547[mV/code] Initial value : 48 (48x10.547=506.26[mV])
	D1	ATPCRX_CTRL_ERR_OFS1[1]	0	R/W	
	D2	ATPCRX_CTRL_ERR_OFS1[2]	0	R/W	
	D3	ATPCRX_CTRL_ERR_OFS1[3]	0	R/W	
	D4	ATPCRX_CTRL_ERR_OFS1[4]	1	R/W	
	D5	ATPCRX_CTRL_ERR_OFS1[5]	1	R/W	
	D6	ATPCRX_CTRL_ERR_OFS1[6]	0	R/W	
	D7	ATPCRX_CTRL_ERR_OFS1[7]	0	R/W	
0x12	D0	ATPCRX_CTRL_ERR_OFS2[0]	0	R/W	Control error calculation offset ΔV2 (ATPC Mode) ΔV2 is applied to offset voltage in condition of no fast charge state or (fast charge state & ICHG < 0.15C) 10.547[mV/code] Initial value : 144 (144x10.547=1518.77[mV])
	D1	ATPCRX_CTRL_ERR_OFS2[1]	0	R/W	
	D2	ATPCRX_CTRL_ERR_OFS2[2]	0	R/W	
	D3	ATPCRX_CTRL_ERR_OFS2[3]	0	R/W	
	D4	ATPCRX_CTRL_ERR_OFS2[4]	1	R/W	
	D5	ATPCRX_CTRL_ERR_OFS2[5]	0	R/W	
	D6	ATPCRX_CTRL_ERR_OFS2[6]	0	R/W	
	D7	ATPCRX_CTRL_ERR_OFS2[7]	1	R/W	
0x13	D0	ATPCRX_CTRL_ERR_TH[0]	0	R/W	Control error convergence judgement threshold (ATPC Mode) 10.547[mV/code] Initial value : 10 (10x10.547=105.47[mV])
	D1	ATPCRX_CTRL_ERR_TH[1]	1	R/W	
	D2	ATPCRX_CTRL_ERR_TH[2]	0	R/W	
	D3	ATPCRX_CTRL_ERR_TH[3]	1	R/W	
	D4	ATPCRX_CTRL_ERR_TH[4]	0	R/W	
	D5	ATPCRX_CTRL_ERR_TH[5]	0	R/W	
	D6	ATPCRX_CTRL_ERR_TH[6]	0	R/W	
	D7	ATPCRX_CTRL_ERR_TH[7]	0	R/W	
0x14	D0	ATPCRX_NCTRL_ERR_TH[0]	0	R/W	Control error non-convergence judgement threshold (ATPC Mode) 1[count/code] Initial value : 32 (32x1=32[count])
	D1	ATPCRX_NCTRL_ERR_TH[1]	0	R/W	
	D2	ATPCRX_NCTRL_ERR_TH[2]	0	R/W	
	D3	ATPCRX_NCTRL_ERR_TH[3]	0	R/W	
	D4	ATPCRX_NCTRL_ERR_TH[4]	0	R/W	
	D5	ATPCRX_NCTRL_ERR_TH[5]	1	R/W	
	D6	ATPCRX_NCTRL_ERR_TH[6]	0	R/W	
	D7	ATPCRX_NCTRL_ERR_TH[7]	0	R/W	
0x15	D0	WPT_R_CNT_OVER_ERR[0]	0	R/W	Bit number threshold for error judgement when WPT data is received. (ATPC Mode) 0 : 4[bit] 1 : 1[bit] 2 : 2[bit] 3 : 8[bit] 4 : 16[bit] 5 : 32[bit] 6 : 48[bit] 7 : 63[bit]
	D1	WPT_R_CNT_OVER_ERR[1]	0	R/W	
	D2	WPT_R_CNT_OVER_ERR[2]	0	R/W	
	D3		0	R	
	D4		0	R	
	D5		0	R	
	D6		0	R	
	D7		0	R	
0x16	D0	VRECT_CMP_TH[0]	0	R/W	Differential value threshold of AD converted data(VRECT) (ATPC Mode) 2.637[mV/code] (RECT pin voltage, 12bit resolution) Initial value : 32 (32 x 2.637=84.38[mV])
	D1	VRECT_CMP_TH[1]	0	R/W	
	D2	VRECT_CMP_TH[2]	0	R/W	
	D3	VRECT_CMP_TH[3]	0	R/W	
	D4	VRECT_CMP_TH[4]	0	R/W	
	D5	VRECT_CMP_TH[5]	1	R/W	
	D6	VRECT_CMP_TH[6]	0	R/W	
	D7	VRECT_CMP_TH[7]	0	R/W	
0x17	D0	IVCC_CMP_TH[0]	0	R/W	Differential value threshold of AD converted data(IVCC) (ATPC Mode) 43.945[uA/code] @ RIVCC=1.2[kΩ] (VCC regulator output current(IVCC), 12bit resolution) 21.972[uA/code] @ RIVCC=2.4[kΩ] (VCC regulator output current(IVCC), 12bit resolution) 10.986[uA/code] @ RIVCC=4.8[kΩ] (VCC regulator output current(IVCC), 12bit resolution) 0.6592[mV/code] (RIMON pin voltage, 12bit resolution) Initial value : 64 (64 x 43.945[uA/code]=2812[uA] @ RIVCC=1.2[kΩ], 64 x 21.972[uA/code]=1406[uA] @ RIVCC=2.4[kΩ], 64 x 10.986[uA/code]=703.1[uA] @ RIVCC=4.8[kΩ])
	D1	IVCC_CMP_TH[1]	0	R/W	
	D2	IVCC_CMP_TH[2]	0	R/W	
	D3	IVCC_CMP_TH[3]	0	R/W	
	D4	IVCC_CMP_TH[4]	0	R/W	
	D5	IVCC_CMP_TH[5]	0	R/W	
	D6	IVCC_CMP_TH[6]	1	R/W	
	D7	IVCC_CMP_TH[7]	0	R/W	

9.4 Address 0x18 to 0x1F

Address	Bit No.	Register Name	Init	R/W	Description
0x18	D0	VBAT_CMP_TH[0]	0	R/W	Differential value threshold of AD converted data(VBAT) (ATPC Mode) 1.318[mV/code] (BAT pin voltage, 12bit resolution) Initial value : 32 (32 x 1.318=42.18[mV])
	D1	VBAT_CMP_TH[1]	0	R/W	
	D2	VBAT_CMP_TH[2]	0	R/W	
	D3	VBAT_CMP_TH[3]	0	R/W	
	D4	VBAT_CMP_TH[4]	0	R/W	
	D5	VBAT_CMP_TH[5]	1	R/W	
	D6	VBAT_CMP_TH[6]	0	R/W	
	D7	VBAT_CMP_TH[7]	0	R/W	
0x19	D0	RIMON_RESISTOR[0]	0	R	Connected resistance detection result at RIMON pin 0 : 1.2[kΩ] 1 : 2.4[kΩ] 2 : 4.8[kΩ] 3 : Error
	D1	RIMON_RESISTOR[1]	0	R	
	D2		0	R	
	D3		0	R	
	D4	ATPC_PHASE[0]	0	R	ATPC Phase (operation status of ATPC Mode) monitor 0 : Ping 1 : Identification 2 : Configuration 3 : Battery Charge
	D5	ATPC_PHASE[1]	0	R	
	D6		0	R	
	D7		0	R	
0x1A	D0	RECT_PSA[0]	0	R/W	On resistance setting of high side switch in rectifier (Available in 0x1A D[3]=1) 0 : 1[Ω] 1 : 2[Ω] 2 : 4[Ω] 3 : 8[Ω]
	D1	RECT_PSA[1]	0	R/W	
	D2	RECT_FULLSYNC_EN	0	R/W	0 : Half synchronous operation 1 : Half or full synchronous automatic change operation (Available in 0x1A D[3]=1)
	D3	RECT_SW_FORCE	0	R/W	1 : On resistance register setting mode of high side switch in rectifier
	D4	ATR_RECT_PSA[0]	0	R	On resistance setting monitor of rectifier high-side switch 0 : 1[Ω] 1 : 2[Ω] 2 : 4[Ω] 3 : 8[Ω]
	D5	ATR_RECT_PSA[1]	0	R	
	D6	ATR_RECT_FULLSYNC_EN	0	R	Rectifier operation monitor 0 : Half synchronous operation 1 : Half or full synchronous automatic change operation
	D7		0	R	
0x1B	D0	RECT_TH_FS8_HS1[0]	1	R/W	VCC regulator output current threshold 1 (decreasing) for switching the rectifier operation in ATPC pin and ATR pin = H This value is compared by A/D converted result of RIMON pin voltage. 0.3516[mA/code] (VCC regulator output current(IVCC), not depending on RIMON resistance) 9bit resolution in setting of RIVCC=1.2[kΩ], 2.4[kΩ], 4.8[kΩ] Initial value : 11 (11 x 0.3516=3.868[mA]) Register value is applied by 0x1F D[7]=1.
	D1	RECT_TH_FS8_HS1[1]	1	R/W	
	D2	RECT_TH_FS8_HS1[2]	0	R/W	
	D3	RECT_TH_FS8_HS1[3]	1	R/W	
	D4	RECT_TH_FS8_HS1[4]	0	R/W	
	D5	RECT_TH_FS8_HS1[5]	0	R/W	
	D6	RECT_TH_FS8_HS1[6]	0	R/W	
	D7	RECT_TH_FS8_HS1[7]	0	R/W	
0x1C	D0	RECT_TH_FS4_FS8[0]	1	R/W	VCC regulator output current threshold 2 (decreasing) for switching the rectifier operation in ATPC pin and ATR pin = H This value is compared by A/D converted result of RIMON pin voltage. 0.3516[mA/code] (VCC regulator output current(IVCC), not depending on RIMON resistance) 9bit resolution in setting of RIVCC=1.2[kΩ], 2.4[kΩ], 4.8[kΩ] Initial value : 23 (23 x 0.3516=8.087[mA]) Register value is applied by 0x1F D[7]=1.
	D1	RECT_TH_FS4_FS8[1]	1	R/W	
	D2	RECT_TH_FS4_FS8[2]	1	R/W	
	D3	RECT_TH_FS4_FS8[3]	0	R/W	
	D4	RECT_TH_FS4_FS8[4]	1	R/W	
	D5	RECT_TH_FS4_FS8[5]	0	R/W	
	D6	RECT_TH_FS4_FS8[6]	0	R/W	
	D7	RECT_TH_FS4_FS8[7]	0	R/W	
0x1D	D0	RECT_TH_FS2_FS4[0]	0	R/W	VCC regulator output current threshold 3 (decreasing) for switching the rectifier operation in ATPC pin and ATR pin = H This value is compared by A/D converted result of RIMON pin voltage. 0.3516[mA/code] (VCC regulator output current(IVCC), not depending on RIMON resistance) 9bit resolution in setting of RIVCC=1.2[kΩ], 2.4[kΩ], 4.8[kΩ] Initial value : 46 (46 x 0.3516=16.17[mA]) Register value is applied by 0x1F D[7]=1.
	D1	RECT_TH_FS2_FS4[1]	1	R/W	
	D2	RECT_TH_FS2_FS4[2]	1	R/W	
	D3	RECT_TH_FS2_FS4[3]	1	R/W	
	D4	RECT_TH_FS2_FS4[4]	0	R/W	
	D5	RECT_TH_FS2_FS4[5]	1	R/W	
	D6	RECT_TH_FS2_FS4[6]	0	R/W	
	D7	RECT_TH_FS2_FS4[7]	0	R/W	
0x1E	D0	RECT_TH_FS1_FS2[0]	1	R/W	VCC regulator output current threshold 4 (decreasing) for switching the rectifier operation in ATPC pin and ATR pin = H This value is compared by A/D converted result of RIMON pin voltage. 0.3516[mA/code] (VCC regulator output current(IVCC), not depending on RIMON resistance) 9bit resolution in setting of RIVCC=1.2[kΩ], 2.4[kΩ], 4.8[kΩ] Initial value : 91 (91 x 0.3516=31.99[mA]) Register value is applied by 0x1F D[7]=1.
	D1	RECT_TH_FS1_FS2[1]	1	R/W	
	D2	RECT_TH_FS1_FS2[2]	0	R/W	
	D3	RECT_TH_FS1_FS2[3]	1	R/W	
	D4	RECT_TH_FS1_FS2[4]	1	R/W	
	D5	RECT_TH_FS1_FS2[5]	0	R/W	
	D6	RECT_TH_FS1_FS2[6]	1	R/W	
	D7	RECT_TH_FS1_FS2[7]	0	R/W	
0x1F	D0	RECT_TH_HYS[0]	1	R/W	VCC regulator output current threshold (hysteresis) for switching the rectifier operation in ATPC pin and ATR pin = H Increasing current threshold is calculated by decreasing current threshold + RECT_TH_HYS. 0.3516[mA/code] (VCC regulator output current(IVCC), not depending on RIMON resistance) 9bit resolution in setting of RIVCC=1.2[kΩ], 2.4[kΩ], 4.8[kΩ] Initial value : 11 (11 x 0.3516=3.868[mA]) Register value is applied by 0x1F D[7]=1.
	D1	RECT_TH_HYS[1]	1	R/W	
	D2	RECT_TH_HYS[2]	0	R/W	
	D3	RECT_TH_HYS[3]	1	R/W	
	D4	RECT_TH_HYS[4]	0	R/W	
	D5	RECT_TH_HYS[5]	0	R/W	
	D6	RECT_TH_HYS[6]	0	R/W	
	D7	RECT_TH_UPLOAD	0	R/W	1 : Load current threshold register values (0x1B to 0x1F) are applied. This register is reset after applying.

9.5 Address 0x20 to 0x27

Address	Bit No.	Register Name	Init	R/W	Description
0x20	D0	WPT_T_TRNS	0	R/W	Data transmission trigger of WPT communication 0 : Complete 1 : Start (This register is reset after transmission)
	D1		0	R	
	D2		0	R	
	D3		0	R	
	D4		0	R	
	D5		0	R	
	D6		0	R	
	D7		0	R	
0x21	D0	WPT_T_HDR[0]	0	R/W	Transmission data Header of WPT communication
	D1	WPT_T_HDR[1]	0	R/W	
	D2	WPT_T_HDR[2]	0	R/W	
	D3	WPT_T_HDR[3]	0	R/W	
	D4	WPT_T_HDR[4]	0	R/W	
	D5	WPT_T_HDR[5]	0	R/W	
	D6	WPT_T_HDR[6]	0	R/W	
	D7	WPT_T_HDR[7]	0	R/W	
0x22	D0	WPT_T_MSG1[0]	0	R/W	Transmission data Message1 of WPT communication
	D1	WPT_T_MSG1[1]	0	R/W	
	D2	WPT_T_MSG1[2]	0	R/W	
	D3	WPT_T_MSG1[3]	0	R/W	
	D4	WPT_T_MSG1[4]	0	R/W	
	D5	WPT_T_MSG1[5]	0	R/W	
	D6	WPT_T_MSG1[6]	0	R/W	
	D7	WPT_T_MSG1[7]	0	R/W	
0x23	D0	WPT_T_MSG2[0]	0	R/W	Transmission data Message2 of WPT communication
	D1	WPT_T_MSG2[1]	0	R/W	
	D2	WPT_T_MSG2[2]	0	R/W	
	D3	WPT_T_MSG2[3]	0	R/W	
	D4	WPT_T_MSG2[4]	0	R/W	
	D5	WPT_T_MSG2[5]	0	R/W	
	D6	WPT_T_MSG2[6]	0	R/W	
	D7	WPT_T_MSG2[7]	0	R/W	
0x24	D0	WPT_R_HDR[0]	0	R	Received data Header of WPT communication This register is overwritten by next received data of WPT communication even if this register is not read.
	D1	WPT_R_HDR[1]	0	R	
	D2	WPT_R_HDR[2]	0	R	
	D3	WPT_R_HDR[3]	0	R	
	D4	WPT_R_HDR[4]	0	R	
	D5	WPT_R_HDR[5]	0	R	
	D6	WPT_R_HDR[6]	0	R	
	D7	WPT_R_HDR[7]	0	R	
0x25	D0	WPT_R_MSG1[0]	0	R	Received data Message1 of WPT communication This register is overwritten by next received data of WPT communication even if this register is not read.
	D1	WPT_R_MSG1[1]	0	R	
	D2	WPT_R_MSG1[2]	0	R	
	D3	WPT_R_MSG1[3]	0	R	
	D4	WPT_R_MSG1[4]	0	R	
	D5	WPT_R_MSG1[5]	0	R	
	D6	WPT_R_MSG1[6]	0	R	
	D7	WPT_R_MSG1[7]	0	R	
0x26	D0	WPT_R_MSG2[0]	0	R	Received data Message2 of WPT communication This register is overwritten by next received data of WPT communication even if this register is not read.
	D1	WPT_R_MSG2[1]	0	R	
	D2	WPT_R_MSG2[2]	0	R	
	D3	WPT_R_MSG2[3]	0	R	
	D4	WPT_R_MSG2[4]	0	R	
	D5	WPT_R_MSG2[5]	0	R	
	D6	WPT_R_MSG2[6]	0	R	
	D7	WPT_R_MSG2[7]	0	R	
0x27	D0	WPT_T_RATE[0]	1	R/W	WPT communication data rate setting (Receiver to Transmitter communication) 0 : 125[bps] 1 : 250[bps] 2 : 500[bps] 3 : 1000[bps]
	D1	WPT_T_RATE[1]	0	R/W	
	D2	WPT_R_DIFF_OLD[0]	1	R/W	Assigning data point to calculate the rectified output voltage variation for WPT communication packet demodulation. 0:Previous data 1:Data 2 times before 2:Data 3 times before 3:Data 4 times before
	D3	WPT_R_DIFF_OLD[1]	1	R/W	
	D4	WPT_R_DIFF_WAIT[0]	1	R/W	Timing to acquire the rectified output voltage variation for WPT communication packet demodulation. Recommended value 125bps : 7 250bps : - 500bps : - 1000bps :-
	D5	WPT_R_DIFF_WAIT[1]	1	R/W	
	D6	WPT_R_DIFF_WAIT[2]	1	R/W	
	D7	WPT_R_DIFF_WAIT[3]	0	R/W	

9.6 Address 0x28 to 0x2F

Address	Bit No.	Register Name	Init	R/W	Description
0x28	D0	WPT_R_DIFF_TH[1]	0	R/W	Threshold to detect the rectified output voltage variation for WPT communication packet demodulation. 5.273[mV/code] (RECT pin voltage, 11bit resolution) { 000, WPT_RDIFF_TH[8:1], 0 } and 12bit differential value of RECT pin voltage are compared. Recommended value 125bps : 32(168.7[mV]) 250bps : - 500bps : - 1000bps : -
	D1	WPT_R_DIFF_TH[2]	0	R/W	
	D2	WPT_R_DIFF_TH[3]	0	R/W	
	D3	WPT_R_DIFF_TH[4]	0	R/W	
	D4	WPT_R_DIFF_TH[5]	0	R/W	
	D5	WPT_R_DIFF_TH[6]	1	R/W	
	D6	WPT_R_DIFF_TH[7]	0	R/W	
	D7	WPT_R_DIFF_TH[8]	0	R/W	
0x29	D0	WPT_R_CNT_TH[0]	1	R/W	Counter timing to detect data 1/0 for WPT communication packet demodulation. Recommended value 125bps : 11 250bps : - 500bps : - 1000bps : -
	D1	WPT_R_CNT_TH[1]	1	R/W	
	D2	WPT_R_CNT_TH[2]	0	R/W	
	D3	WPT_R_CNT_TH[3]	1	R/W	
	D4	WPT_R_CNT_TH[4]	0	R/W	
	D5	WPT_R_CNT_TH[5]	0	R/W	
	D6	WPT_R_CNT_TH[6]	0	R/W	
	D7	WPT_R_CNT_TH[7]	0	R/W	
0x2A	D0	WPT_R_CNT_TH_1CYC[0]	0	R/W	Counter timing to detect data presence/absence for WPT communication packet demodulation. Recommended value 125bps : 20 250bps : - 500bps : - 1000bps : -
	D1	WPT_R_CNT_TH_1CYC[1]	0	R/W	
	D2	WPT_R_CNT_TH_1CYC[2]	1	R/W	
	D3	WPT_R_CNT_TH_1CYC[3]	0	R/W	
	D4	WPT_R_CNT_TH_1CYC[4]	1	R/W	
	D5	WPT_R_CNT_TH_1CYC[5]	0	R/W	
	D6	WPT_R_CNT_TH_1CYC[6]	0	R/W	
	D7	WPT_R_CNT_TH_1CYC[7]	0	R/W	
0x2B	D0		0	R	
	D1		0	R	
	D2		0	R	
	D3		0	R	
	D4		0	R	
	D5		0	R	
	D6		0	R	
	D7		0	R	
0x2C	D0		0	R	
	D1		0	R	
	D2		0	R	
	D3		0	R	
	D4		0	R	
	D5		0	R	
	D6		0	R	
	D7		0	R	
0x2D	D0		0	R	
	D1		0	R	
	D2		0	R	
	D3		0	R	
	D4		0	R	
	D5		0	R	
	D6		0	R	
	D7		0	R	
0x2E	D0		0	R	
	D1		0	R	
	D2		0	R	
	D3		0	R	
	D4		0	R	
	D5		0	R	
	D6		0	R	
	D7		0	R	
0x2F	D0	INT_WPT_CM_RCV_MASK	0	R/W	Notification setting of WPT data receiving (Tx to Rx) 0 : Notify 1 : Do not notify (flag is masked)
	D1	INT_CHG_STAT_CNG_MASK	0	R/W	Notification setting of battery charge state transition 0 : Notify 1 : Do not notify (flag is masked)
	D2	INT_DD_OCP_DET_MASK	0	R/W	Notification setting of DCDC overcurrent detection 0 : Notify 1 : Do not notify (flag is masked)
	D3	INT_VCCREG_CLDET_MASK	0	R/W	Notification setting of VCC regulator current limit 0 : Notify 1 : Do not notify (flag is masked)
	D4		0	R	
	D5		0	R	
	D6		0	R	
	D7		0	R	

9.7 Address 0x30 to 0x37

Address	Bit No.	Register Name	Init	R/W	Description
0x30	D0	INT_WPT_CM_RCV	0	R	Interruption notification of WPT data receiving (Tx to Rx) 1 : Data is received (return 0 after register read)
	D1	INT_CHG_STAT_CNG	0	R	Interruption notification of battery charge state transition 1 : State is transited (return 0 after register read)
	D2	INT_DD_OCP_DET	0	R	Interruption notification of DCDC overcurrent detection 1 : Detected
	D3	INT_VCCREG_CLDET	0	R	Interruption notification of VCC regulator current limit 1 : Current limiting
	D4		0	R	
	D5		0	R	
	D6		0	R	
	D7		0	R	
0x31	D0	MCTRL_STATE_MON[0]	0	R	Operation mode 0,1 : Shut down mode 2 to 7 : Charge mode 1 8 : Charge mode 2 9 : Discharge mode
	D1	MCTRL_STATE_MON[1]	0	R	
	D2	MCTRL_STATE_MON[2]	0	R	
	D3	MCTRL_STATE_MON[3]	0	R	
	D4	VCCREG_CLDET	0	R	Notification of VCC regulator current limit 0 : Normal condition 1 : Current limiting
	D5	CHG_LDDET	0	R	Notification that load current automatic dividing function is operated 0 : OFF 1 : ON
	D6	BAT_ASSISTDET	0	R	Notification that assist function by battery is operated 0 : OFF 1 : ON
	D7		0	R	
0x32	D0	CHG_STATE_MON[0]	0	R	Battery charging status 0 : Initial 1 : Pre-charge 2 : Trickle charge 3 : Fast charge 4 : Charge complete judging 5 : Charge complete 6 : No battery 7 : Charge error 1 8 : Charge error 2 9 : Charge error 3
	D1	CHG_STATE_MON[1]	0	R	
	D2	CHG_STATE_MON[2]	0	R	
	D3	CHG_STATE_MON[3]	0	R	
	D4	THM_AREA[0]	0	R	Charge control profile for battery temperature 0 : No battery 1 : Charge pending in low temperature 2 : Low temperature low rate charge 3 : Suitable temperature charge 4 : High temperature low rate charge 5 : Charge pending in high temperature
	D5	THM_AREA[1]	0	R	
	D6	THM_AREA[2]	0	R	
	D7		0	R	
0x33	D0	WPT_R_ERR	0	R	WPT communication error 0 : Undetected 1 : Detected
	D1	I2C_WR_ERR	0	R	2-wire interface communication error 0 : Undetected 1 : Detected
	D2	RIMON_DET_ERR	0	R	RIMON connected resistance value error 0 : Undetected 1 : Detected
	D3		0	R	
	D4	DD_DDIN_OK	0	R	DCDC converter UVLO detection 0 : Detected(DCDC stop) 1 : UVLO release(DCDC start)
	D5	DD_SYS_OK	0	R	DCDC converter SYS voltage detection 0 : Low voltage condition 1 : Normal voltage condition (start up complete)
	D6	DD_OVP_DET	0	R	DCDC converter overvoltage detection 0 : OVP release(DCDC start) 1 : Detected(DCDC stop)
	D7	DD_OCP_DET	0	R	DCDC converter overcurrent detection 0 : Normal current 1 : Detected
0x34	D0	FGH_DET	0	R	Battery low voltage detection H (First step) 0 : Undetected 1 : Detected
	D1	FGL_DET	0	R	Battery low voltage detection L (Second step) 0 : Undetected 1 : Detected
	D2	BUZ_MODE	0	R/W	BUZ output setting 0 : Level output 1 : Pulse output
	D3		0	R	
	D4	DSCP_DET	0	R	Battery discharge short circuit current detection 0 : Undetected 1 : Detected
	D5	DOCP_DET	0	R	Battery discharge overcurrent detection 0 : Undetected 1 : Detected
	D6	DOVP_DET	0	R	Battery discharge overvoltage detection 0 : Undetected 1 : Detected
	D7	TJMAX_DET	0	R	Maximum junction temperature detection 0 : Undetected 1 : Detected
0x35	D0	ADC_UPLOAD	0	R/W	1 : A/D converted results are fetched and 0x36 to 0x3F registers are updated. (return 0 after update)
	D1		0	R	
	D2		0	R	
	D3		0	R	
	D4		0	R	
	D5		0	R	
	D6		0	R	
	D7		0	R	
0x36	D0	ADC_RECTCLIPDET	0	R	RECT pin voltage detection. RECT pin voltage is higher than ADC input voltage range. 0 : Undetected 1 : Detected
	D1		0	R	
	D2		0	R	
	D3		0	R	
	D4	ADC_VRECT_I2C[0]	0	R	A/D converted result of rectified voltage (RECT pin voltage) 2.637[mV/code] (RECT pin voltage, 12bit resolution)
	D5	ADC_VRECT_I2C[1]	0	R	
	D6	ADC_VRECT_I2C[2]	0	R	
	D7	ADC_VRECT_I2C[3]	0	R	
0x37	D0	ADC_VRECT_I2C[4]	0	R	
	D1	ADC_VRECT_I2C[5]	0	R	
	D2	ADC_VRECT_I2C[6]	0	R	
	D3	ADC_VRECT_I2C[7]	0	R	
	D4	ADC_VRECT_I2C[8]	0	R	
	D5	ADC_VRECT_I2C[9]	0	R	
	D6	ADC_VRECT_I2C[10]	0	R	
	D7	ADC_VRECT_I2C[11]	0	R	

9.8 Address 0x38 to 0x3F

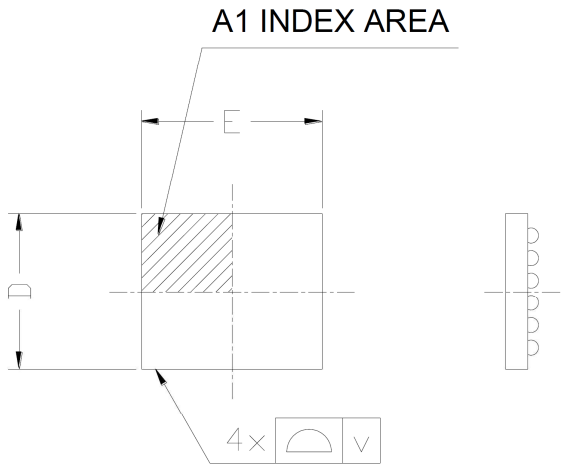
Address	Bit No.	Register Name	Init	R/W	Description
0x38	D0		0	R	
	D1		0	R	
	D2		0	R	
	D3		0	R	
	D4	ADC_IVCC_I2C[0]	0	R	A/D converted result of VCC regulator output current (RIMON pin voltage) 0.6592[mV/code] (RIMON pin voltage, 12bit resolution) RIMON pin voltage is limited in 1.2V(Current limit function) (1.2[V]/0.6592[mV/code] = 1820 [code]) 43.94[uA/code] @ RIVCC=1.2[kΩ] (VCC regulator output current(IVCC), 12bit resolution) 21.97[uA/code] @ RIVCC=2.4[kΩ] (VCC regulator output current(IVCC), 12bit resolution) 10.98[uA/code] @ RIVCC=4.8[kΩ] (VCC regulator output current(IVCC), 12bit resolution)
	D5	ADC_IVCC_I2C[1]	0	R	
	D6	ADC_IVCC_I2C[2]	0	R	
	D7	ADC_IVCC_I2C[3]	0	R	
0x39	D0	ADC_IVCC_I2C[4]	0	R	
	D1	ADC_IVCC_I2C[5]	0	R	
	D2	ADC_IVCC_I2C[6]	0	R	
	D3	ADC_IVCC_I2C[7]	0	R	
	D4	ADC_IVCC_I2C[8]	0	R	
	D5	ADC_IVCC_I2C[9]	0	R	
	D6	ADC_IVCC_I2C[10]	0	R	
	D7	ADC_IVCC_I2C[11]	0	R	
0x3A	D0		0	R	
	D1		0	R	
	D2		0	R	
	D3		0	R	
	D4	ADC_VBAT_I2C[0]	0	R	A/D converted result of battery voltage (BAT pin voltage) 1.318[mV/code] (BAT pin voltage, 12bit resolution)
	D5	ADC_VBAT_I2C[1]	0	R	
	D6	ADC_VBAT_I2C[2]	0	R	
	D7	ADC_VBAT_I2C[3]	0	R	
0x3B	D0	ADC_VBAT_I2C[4]	0	R	
	D1	ADC_VBAT_I2C[5]	0	R	
	D2	ADC_VBAT_I2C[6]	0	R	
	D3	ADC_VBAT_I2C[7]	0	R	
	D4	ADC_VBAT_I2C[8]	0	R	
	D5	ADC_VBAT_I2C[9]	0	R	
	D6	ADC_VBAT_I2C[10]	0	R	
	D7	ADC_VBAT_I2C[11]	0	R	
0x3C	D0		0	R	
	D1		0	R	
	D2		0	R	
	D3		0	R	
	D4	ADC_ICHG_I2C[0]	0	R	A/D converted result of charging current (RICHG pin voltage) 0.6592[mV/code] (RICHG pin voltage, 12bit resolution) RICHG pin voltage is limited in 1.2V(1C) (1.2[V]/0.6592[mV/code] = 1820 [code]) 9.417[uA/code] @ RICHG=5.6[kΩ] (charge current(ICHG), 12bit resolution) 1C=17.14[mA] 35.16[uA/code] @ RICHG=1.5[kΩ] (charge current(ICHG), 12bit resolution) 1C=64.00[mA]
	D5	ADC_ICHG_I2C[1]	0	R	
	D6	ADC_ICHG_I2C[2]	0	R	
	D7	ADC_ICHG_I2C[3]	0	R	
0x3D	D0	ADC_ICHG_I2C[4]	0	R	
	D1	ADC_ICHG_I2C[5]	0	R	
	D2	ADC_ICHG_I2C[6]	0	R	
	D3	ADC_ICHG_I2C[7]	0	R	
	D4	ADC_ICHG_I2C[8]	0	R	
	D5	ADC_ICHG_I2C[9]	0	R	
	D6	ADC_ICHG_I2C[10]	0	R	
	D7	ADC_ICHG_I2C[11]	0	R	
0x3E	D0		0	R	
	D1		0	R	
	D2		0	R	
	D3		0	R	
	D4	ADC_VTHM_I2C[0]	0	R	A/D converted result of battery temperature (THM pin voltage) 0.6592[mV/code] (THM pin voltage, 12bit resolution)
	D5	ADC_VTHM_I2C[1]	0	R	
	D6	ADC_VTHM_I2C[2]	0	R	
	D7	ADC_VTHM_I2C[3]	0	R	
0x3F	D0	ADC_VTHM_I2C[4]	0	R	
	D1	ADC_VTHM_I2C[5]	0	R	
	D2	ADC_VTHM_I2C[6]	0	R	
	D3	ADC_VTHM_I2C[7]	0	R	
	D4	ADC_VTHM_I2C[8]	0	R	
	D5	ADC_VTHM_I2C[9]	0	R	
	D6	ADC_VTHM_I2C[10]	0	R	
	D7	ADC_VTHM_I2C[11]	0	R	

9.9 Address 0x40 to 0x6F

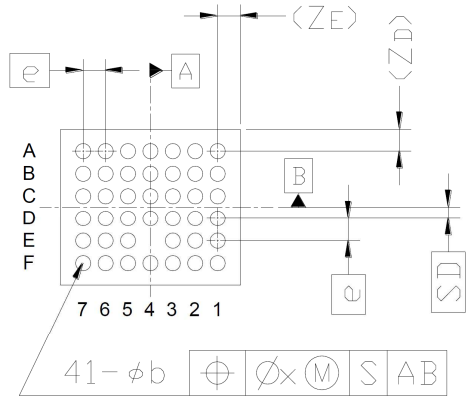
Address	Bit No.	Register Name	Init	R/W	Description
0x40	D0	I2C_WRITE_EN	0	R/W	Write enable to registers of 0x00 to 0x0F by 2-wire I/F. 0 : Write disable 1: Write enable
	D1		0	R/W	
	D2		0	R/W	
	D3		0	R/W	
	D4	I2C_RSET[0]	0	R/W	Pull up resistance setting for SDA, SCL I/O circuit.(This resistance does not mean the pull up resistance of bus line.) 0 : 250kΩ 1 : 500kΩ 2 : 1000kΩ 3 : 2000kΩ
	D5	I2C_RSET[1]	0	R/W	
	D6	Test Register	0	R/W	Setting 0 only. Setting 1 is forbidden.
	D7	Test Register	0	R/W	
0x41 to 0x6F	Test registers (Unavailable for user)				

10. Package Dimensions

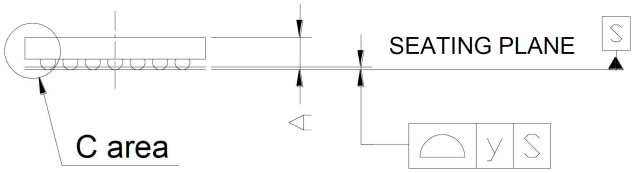
JEITA Package code	RENESAS Code	Previous Code	MASS(TYP.)[g]
S-WFBGA41-3.22x2.77-0.40	SWBG0041LB-A	—	0.012



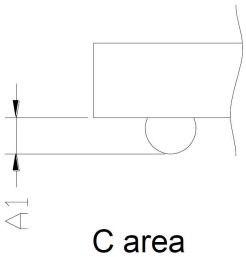
TOP VIEW



BOTTOM VIEW



SIDE VIEW



Term	Symbols	Dimensions in millimeters		
		Min	Nom	Max
Package length	D	2.72	2.77	2.82
Package width	E	3.17	3.22	3.27
Overhang dimension in length	ZD	—	0.385	—
Overhang dimension in width	ZE	—	0.41	—
Profile height	A	—	—	0.70
Stand-off height	A1	0.15	0.19	0.23
Terminal diameter	b	0.22	0.27	0.32
Terminal pitch	e	—	0.4	—
Center terminal distance from datum B	SD	—	0.2	—
Tolerance of package lateral profile	v	—	0.05	—
Positional tolerance of terminals	x	—	0.05	—
Coplanarity	y	—	0.08	—

REVISION HISTORY	RAA457100GBM Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	2017.02.28	-	First Edition issued

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