

NTLUS3A40PZ

MOSFET – Power, Single, P-Channel, ESD, μ Cool, UDFN, 2.0x2.0x0.55 mm -20 V, -9.4 A



ON Semiconductor®

<http://onsemi.com>

Features

- UDFN Package with Exposed Drain Pads for Excellent Thermal Conduction
- Low Profile UDFN 2.0x2.0x0.55 mm for Board Space Saving
- Lowest RDS(on) in 2.0x2.0 Package
- ESD Protected
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- High Side Load Switch
- PA Switch and Battery Switch
- Optimized for Power Management Applications for Portable Products, such as Cell Phones, PMP, DSC, GPS, and others

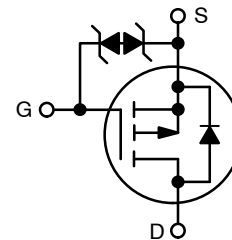
MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter		Symbol	Value	Units	
Drain-to-Source Voltage		V _{DSS}	-20	V	
Gate-to-Source Voltage		V _{GS}	±8.0	V	
Continuous Drain Current (Note 1)	Steady State	T _A = 25°C	I _D	-6.4	A
			T _A = 85°C	-4.6	
	t ≤ 5 s	T _A = 25°C	-9.4		
Power Dissipation (Note 1)	Steady State	T _A = 25°C	P _D	1.7	W
	t ≤ 5 s	T _A = 25°C		3.8	
Continuous Drain Current (Note 2)	Steady State	T _A = 25°C	I _D	-4.0	A
		T _A = 85°C		-2.9	
Power Dissipation (Note 2)		T _A = 25°C	P _D	0.7	W
Pulsed Drain Current		t _p = 10 μs	I _{DM}	-30	A
Operating Junction and Storage Temperature		T _J , T _{STG}	-55 to 150	°C	
Source Current (Body Diode) (Note 2)		I _S	-1.0	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T _L	260	°C	
ESD Rating (HBM) per JESD22-A114F		ESD	>2000	V	

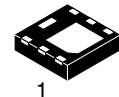
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).

MOSFET		
V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX
-20 V	29 mΩ @ -4.5 V	-9.4 A
	39 mΩ @ -2.5 V	
	60 mΩ @ -1.8 V	
	120 mΩ @ -1.5 V	

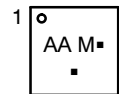


P-Channel MOSFET



UDFN6
CASE 517BG
 μ COOL™

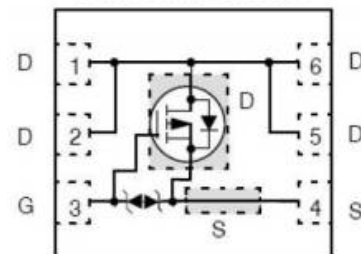
MARKING DIAGRAM



AA = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

NTLUS3A40PZ

2. Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm², 2 oz. Cu.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Units
Junction-to-Ambient – Steady State (Note 3)	R _{θJA}	72	°C/W
Junction-to-Ambient – t ≤ 5 s (Note 3)	R _{θJA}	33	
Junction-to-Ambient – Steady State min Pad (Note 4)	R _{θJA}	189	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = -250 μA	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	I _D = -250 μA, ref to 25°C		-5.0		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = -20 V			-1.0	μA
			T _J = 25°C			
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8.0 V			±10	μA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = -250 μA	-0.4		-1.0	V
Negative Threshold Temp. Coefficient	V _{GS(TH)} /T _J			3.0		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = -4.5 V, I _D = -6.4 A		23	29	mΩ
		V _{GS} = -2.5 V, I _D = -4.8 A		31	39	
		V _{GS} = -1.8 V, I _D = -2.5 A		43	60	
		V _{GS} = -1.5 V, I _D = -1.5 A		60	120	
Forward Transconductance	g _{FS}	V _{DS} = -15 V, I _D = -4.0 A		18		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = -15 V		2600		pF
Output Capacitance	C _{OSS}			200		
Reverse Transfer Capacitance	C _{RSS}			190		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = -4.5 V, V _{DS} = -15 V; I _D = -4.0 A		29		nC
Threshold Gate Charge	Q _{G(TH)}			1.4		
Gate-to-Source Charge	Q _{GS}			3.7		
Gate-to-Drain Charge	Q _{GD}			8.1		

SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 6)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = -4.5 V, V _{DD} = -15 V, I _D = -4.0 A, R _G = 1 Ω		9.0		ns
Rise Time	t _r			18		
Turn-Off Delay Time	t _{d(OFF)}			126		
Fall Time	t _f			71		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	VSD	V _{GS} = 0 V, I _S = -1.0 A	T _J = 25°C	0.65	1.0	V
			T _J = 125°C	0.55		

3. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
 4. Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm², 2 oz. Cu.
 5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
 6. Switching characteristics are independent of operating junction temperatures.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
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DRAIN-SOURCE DIODE CHARACTERISTICS

Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}$, $dis/dt = 100\text{ A}/\mu\text{s}$, $I_S = -1.0\text{ A}$		25		ns
Charge Time	t_a			10		
Discharge Time	t_b			15		
Reverse Recovery Charge	Q_{RR}			13.6		nC

- Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
- Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm², 2 oz. Cu.
- Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

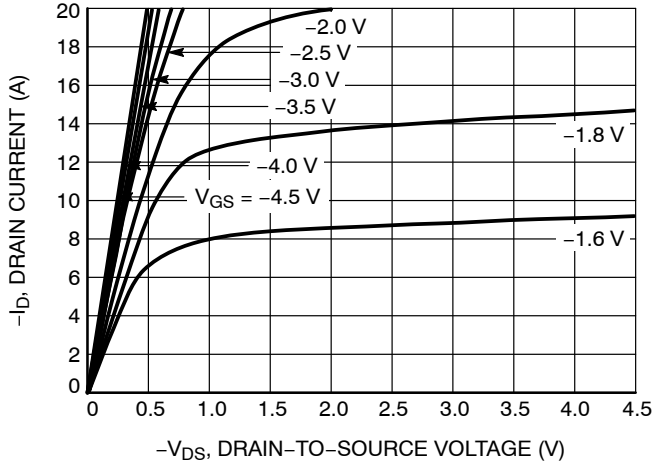


Figure 1. On-Region Characteristics

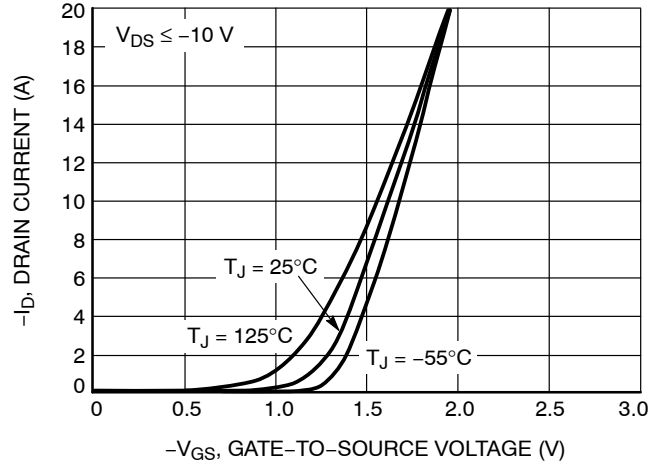


Figure 2. Transfer Characteristics

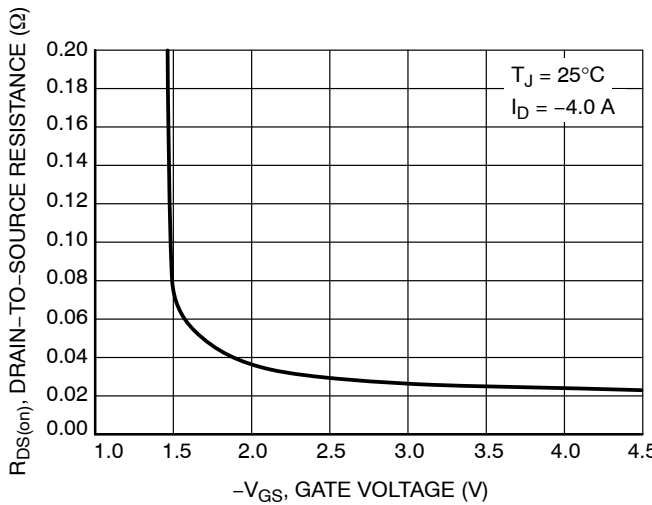


Figure 3. On-Resistance vs. Gate-to-Source Voltage

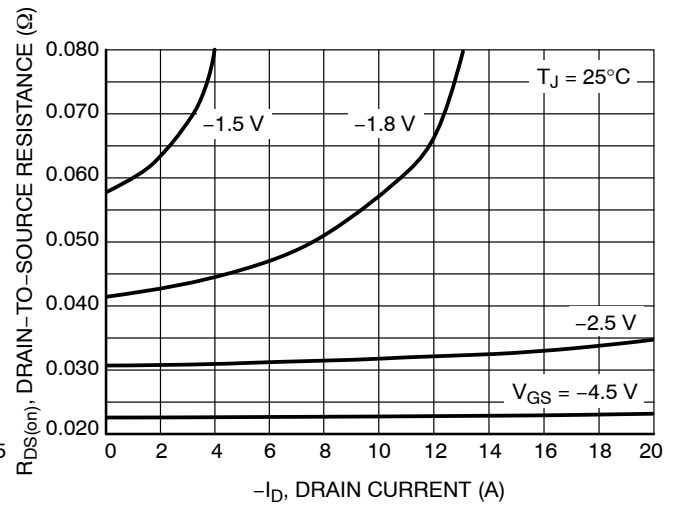


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

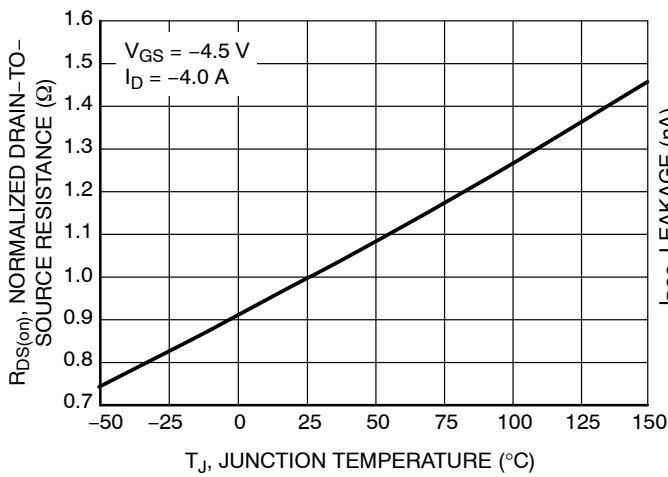


Figure 5. On-Resistance Variation with Temperature

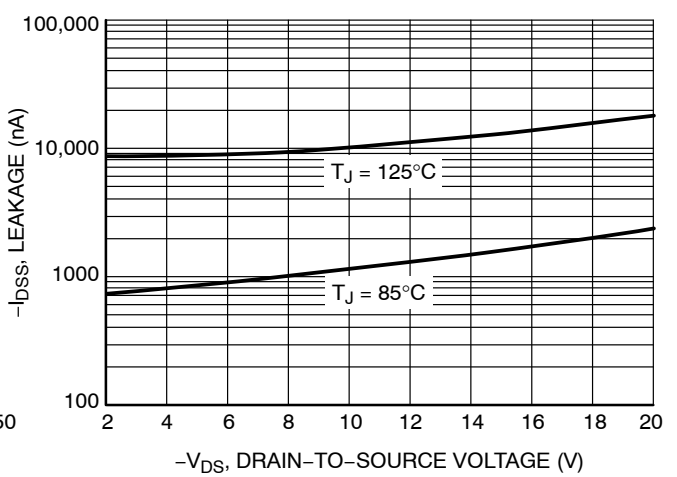


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

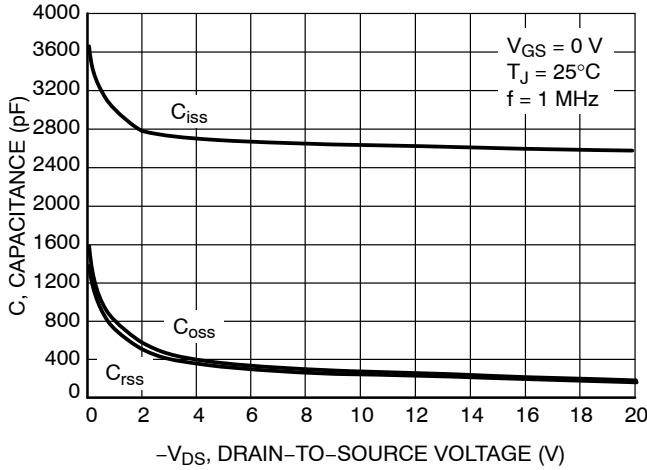


Figure 7. Capacitance Variation

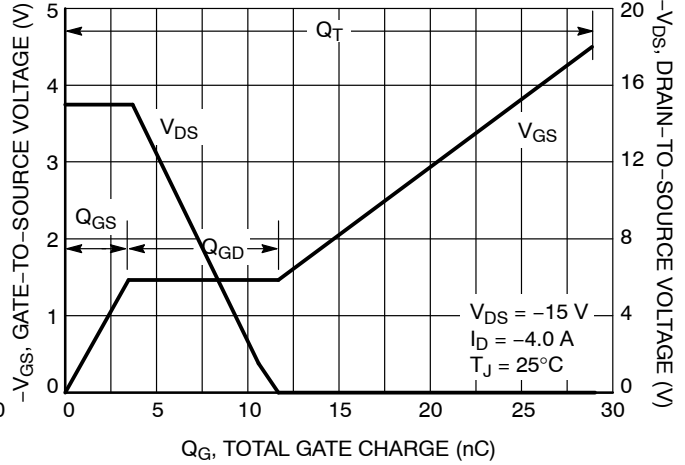


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

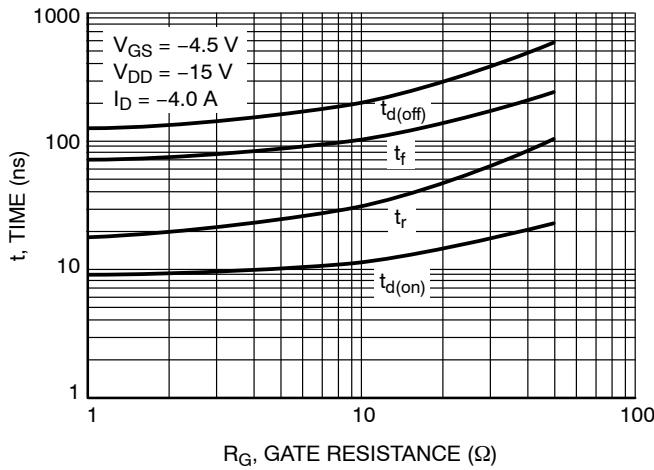


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

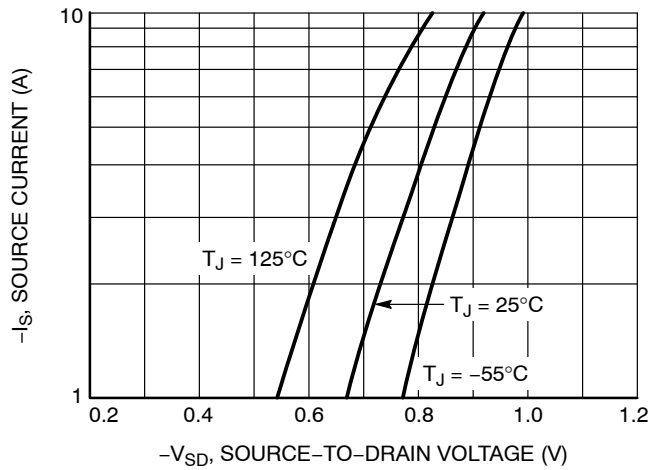


Figure 10. Diode Forward Voltage vs. Current

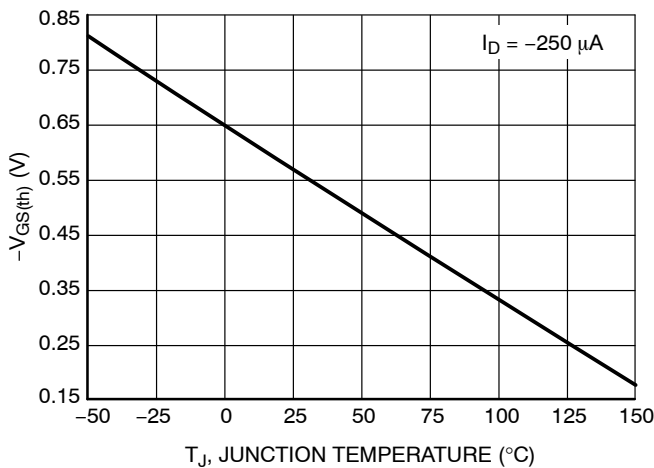


Figure 11. Threshold Voltage

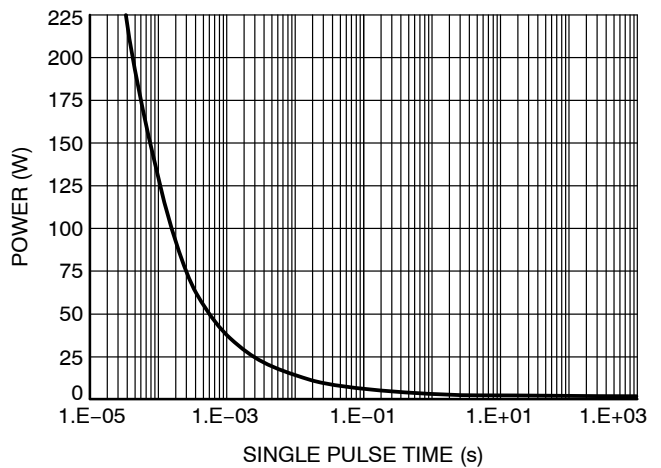


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS

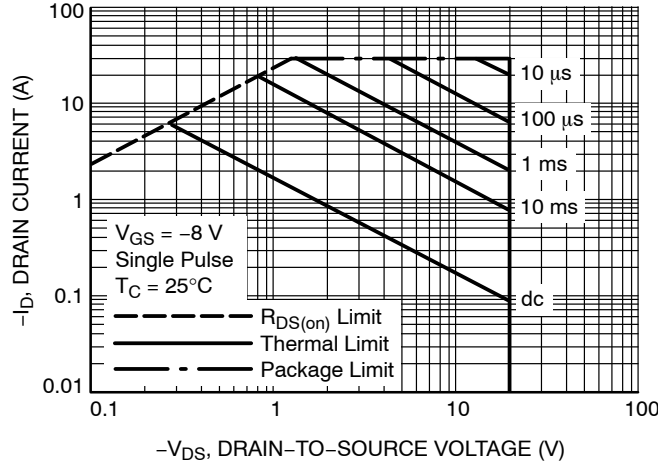


Figure 13. Maximum Rated Forward Biased Safe Operating Area

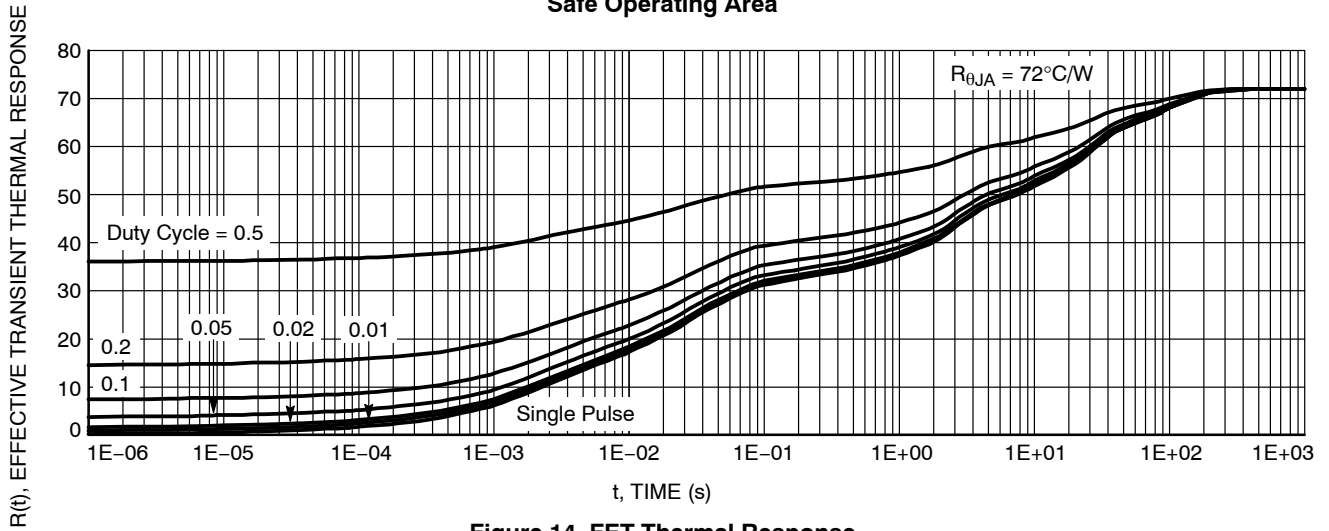


Figure 14. FET Thermal Response

DEVICE ORDERING INFORMATION

Device	Package	Shipping†
NTLUS3A40PZTAG	UDFN6 (Pb-Free)	3000 / Tape & Reel
NTLUS3A40PZTBG	UDFN6 (Pb-Free)	3000 / Tape & Reel

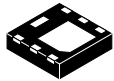
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

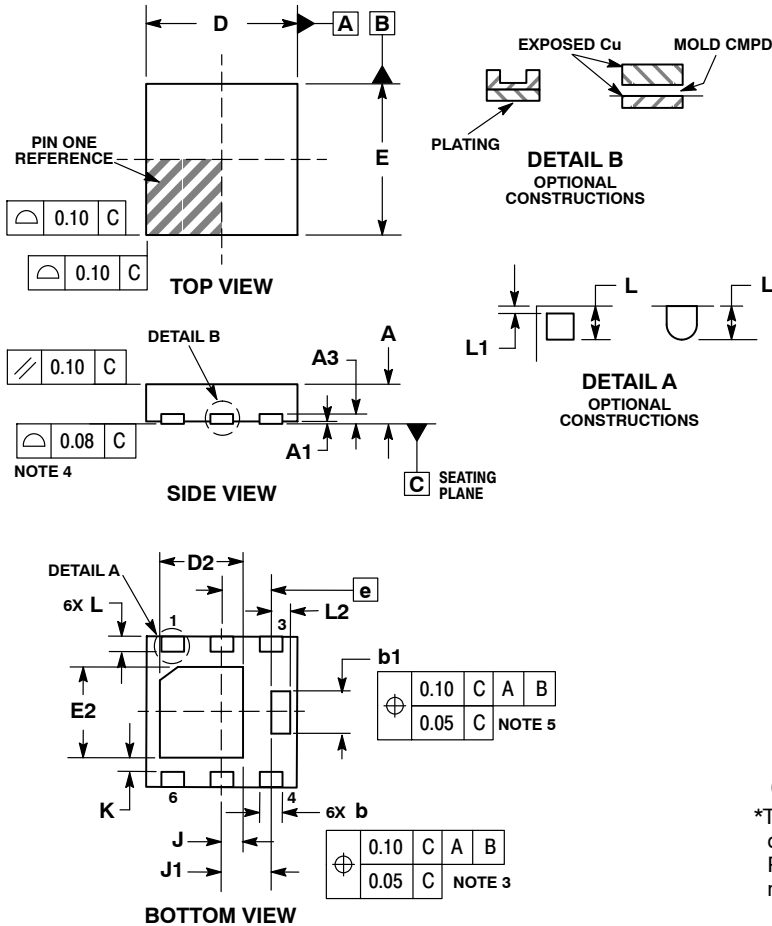
ON Semiconductor®



SCALE 4:1

UDFN6 2x2, 0.65P
CASE 517BG-01
ISSUE A

DATE 04 FEB 2010



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
1. CENTER TERMINAL LEAD IS OPTIONAL. CENTER TERMINAL IS CONNECTED TO TERMINAL LEAD # 4.
2. LEADS 1, 2, 5 AND 6 ARE TIED TO THE FLAG.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.25	0.35
b1	0.51	0.61
D	2.00 BSC	
D2	1.00	1.20
E	2.00 BSC	
E2	1.10	1.30
e	0.65 BSC	
K	0.15 REF	
J	0.27 BSC	
J1	0.65 BSC	
L	0.20	0.30
L1	---	0.10
L2	0.20	0.30

GENERIC MARKING DIAGRAM*

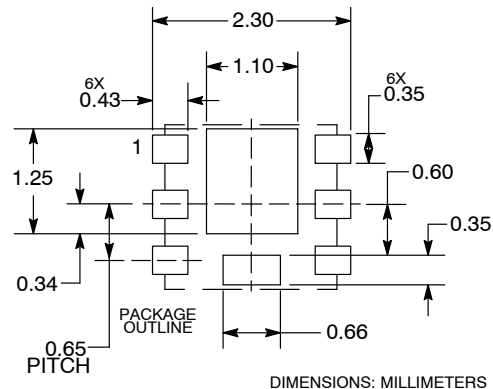


XX = Specific Device Code
M = Date Code

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

RECOMMENDED MOUNTING FOOTPRINT



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DESCRIPTION:	UDFN6 2X2, 0.65P	PAGE 1 OF 1

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