AUIR3241S/AUIR3242S board B2B

Evaluation board

About this document

Scope and purpose

The purpose of this user guide is to facilitate the “plug and play” of AUIR3241S/AUIR3242S back-to-back board for all users. The goal of this board is to replace a mechanical relay in the 40 A to 60 A range.

For the sake of simplicity this document is valid for both AUIR3241S back-to-back board and AUIR3242S back-to-back board.

The difference between AUIR3241S and AUIR3242 V_{IN} pin logic is:

AUIR3241S ON → V_{IN} = high
AUIR3242S ON → V_{IN} = low

Intended audience

This document is intended for qualified electronic engineers who need a high side N-channel MOSFET gate driver for 12 V or 24 V power distribution system.

Table of contents

1 Overview

AUIR3241S/AUIR3242S board back-to-back is a semiconductor-based solution of a fail-safe/fail operational power switch for 12 V or 24 V automotive applications.

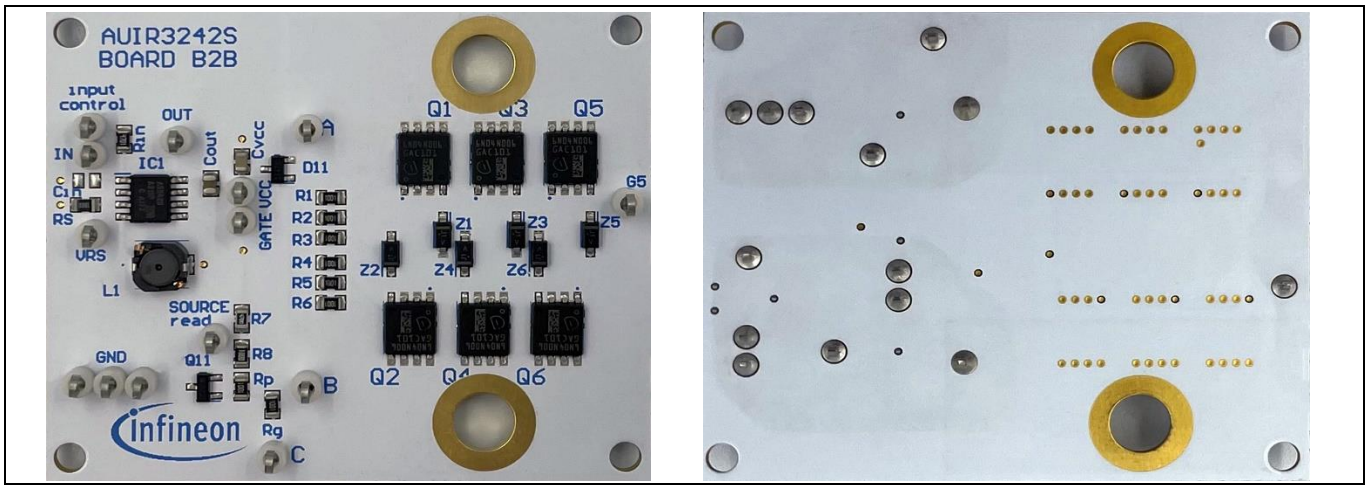

Figure 1 Top and bottom view of AUIR3242S board B2B

AUIR3241S has a high-level active input which supports direct drive from the battery while the AUIR3242S makes relay replacement very easy.

AUIR3241S/AUIR3242S board has a back-to-back, N-channel MOSFET common source structure and allows replacement of any mechanical relay by cutting the current flow in both directions. Additionally, the back-to-back structure blocks current in case of reverse battery.

The MOSFETs are protected against linear mode by UVLO (Undervoltage lock-out) feature, integrated in the driver. See driver datasheet for more information on the feature [1].

Table 1 Infineon parts used

Type	Reference	PCS	Comment
Driver	AUIR3241S	**1**	Full analog driver, **AUIR3241S** board only
Driver	AUIR3242S	**1**	Full analog driver, **AUIR3242S** board only
MOSFET Trench 40V	IAUC120N04S6N006	**4**	Also exists in higher ohmic versions

Table 2 Order information

Type	Reference	OPN
Evaluation board	AUIR3241S board B2B	**AUIR3241SBOARDB2BTOBO1**
Evaluation board	AUIR3242S board B2B	**AUIR3242SBOARDB2BTOBO1**

2 Connecting and operating the board

This chapter describes how to connect the board and gives a non-exhaustive list of actions to avoid in order to keep AUIR3241S/AUIR3242S and the board operational.

The board is designed for 60 A continuous, 90 A for one-minute operation.

Note: It is important to always connect TP - GND to the battery or power supply negative/ground terminal.

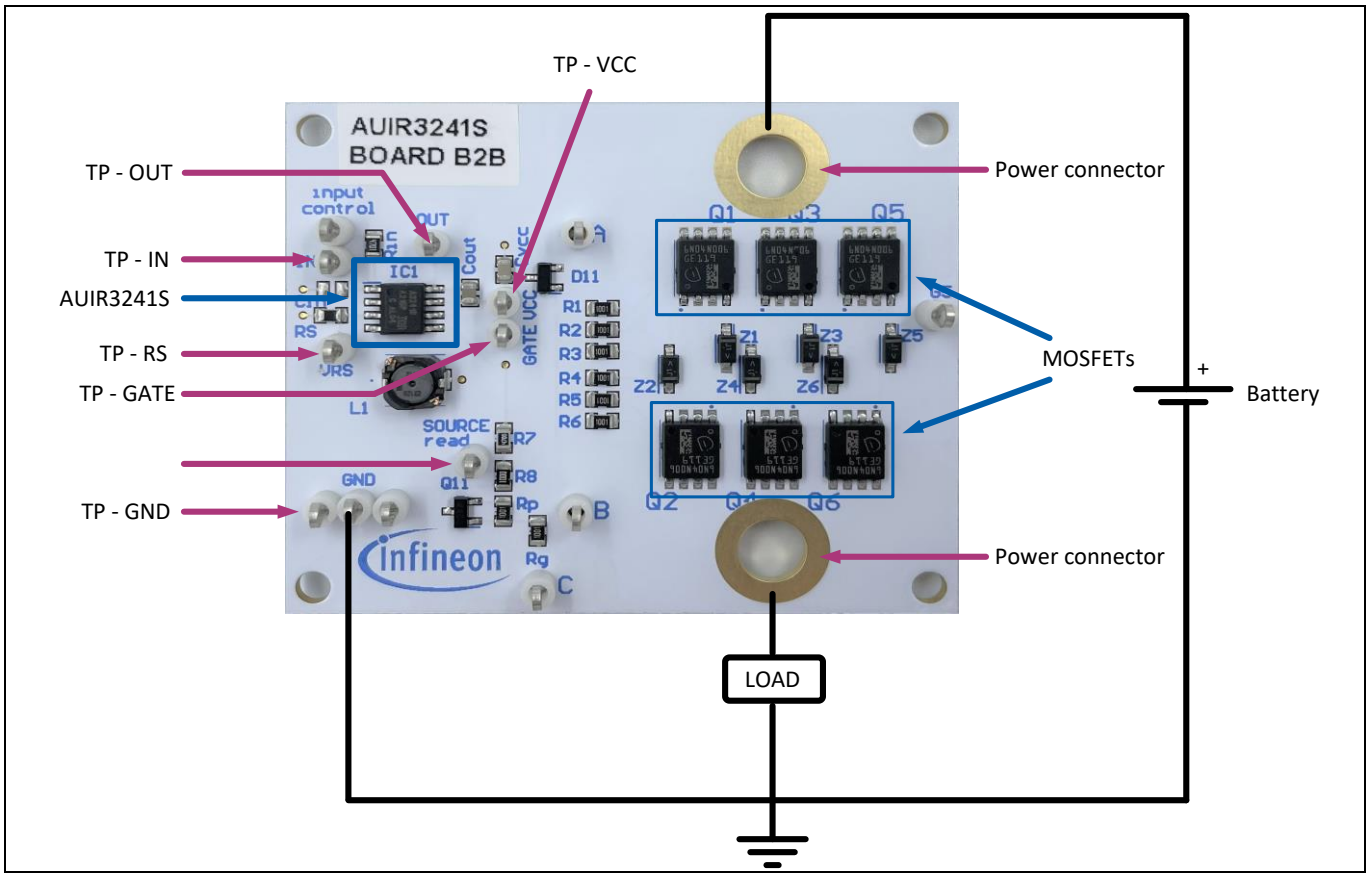

Figure 2 Power connection diagram

Please avoid the following:

- Short between C_{OUT} and GND as this will lead to driver destruction—Short V_{OUT} to V_{CC} to try UVLO feature
- Do not connect two batteries/power sources together as there is no protection implemented

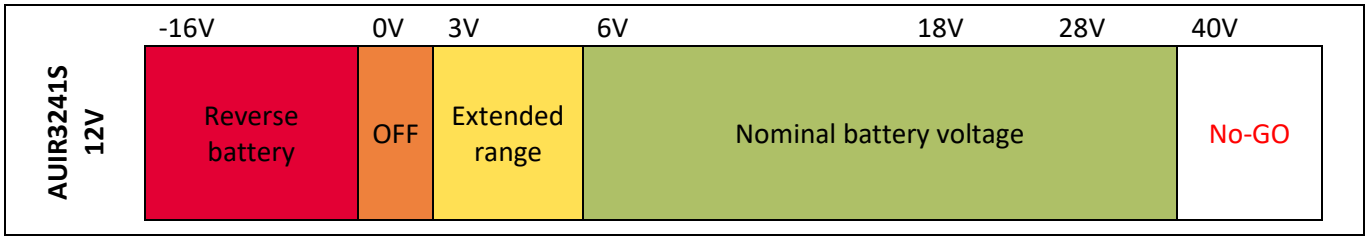

Figure 3 Voltage range

3 Switching behaviour

Note: *Values shown in this chapter are measured under lab conditions and will vary for different cooling conditions and setups, and samples used.*

The following oscilloscope diagram shows a normal turn-on with AUIR3241S board B2B. A simple, resistive, 4.7 Ω - load is used under V_{BAT} = 14 V.

- V_{IN} (yellow) is the control, turn-on signal provided here by a waveform generator
- V_{RS} (purple) signals shows the RS pin voltage. The spikes reflect the activation from the boost converter, which activates to keep the C_{OUT} voltage to the $V_{OUT(th)}$ when the charges are transferred from C_{OUT} to the MOSFET for the turn-on
- V_{GS} shows the MOSFET Q5 gate to source voltage using Q5 test point
- I_{OUT} is the load current

Figure 4 **Waveforms from OFF to ON mode** [Yellow V_{IN}; Blue $V_{GS(AUIR3241S)}$; Purple V_{RS}; Green I_{OUT}]

4 Thermal behaviour

Thermal evaluation has been performed using an active (or electronic) load set at 60 A, with a voltage battery at 14 V for 1 hour. (Power dissipation of 840 W). In the figure below, the temperatures of each block of MOSFETs (Couple MOS1, Couple MOS2), the temperature of the gate driver AUIR3241S, the FW-diode and the maximum temperature of the whole board are plotted.

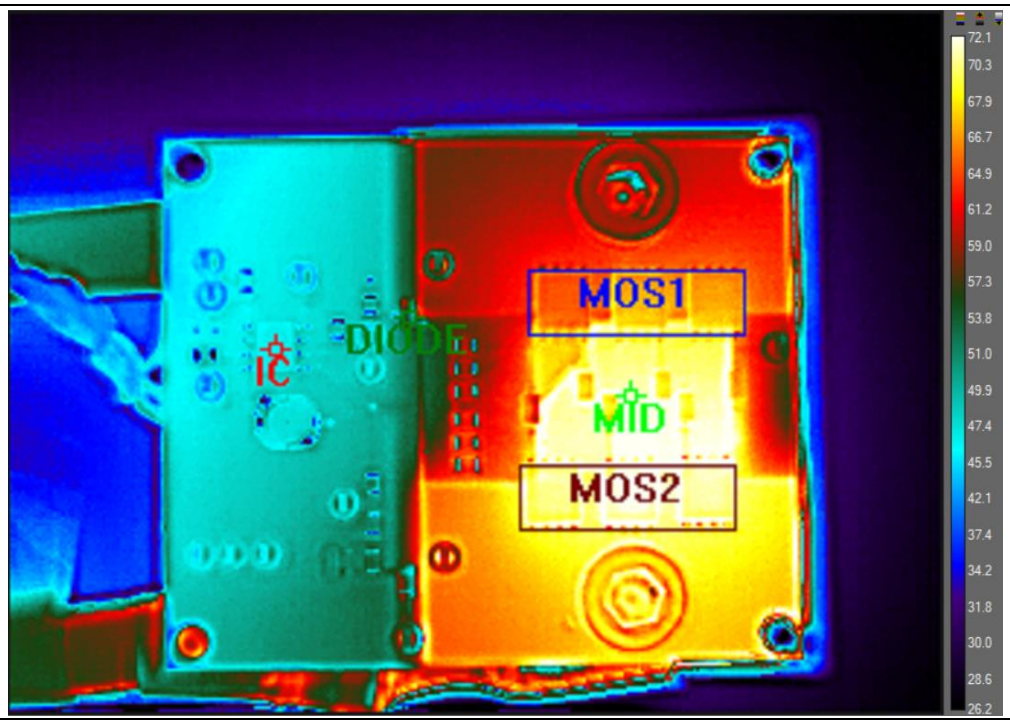

Figure 5 Thermal camera picture after 1 hour at 14 V and 60 A

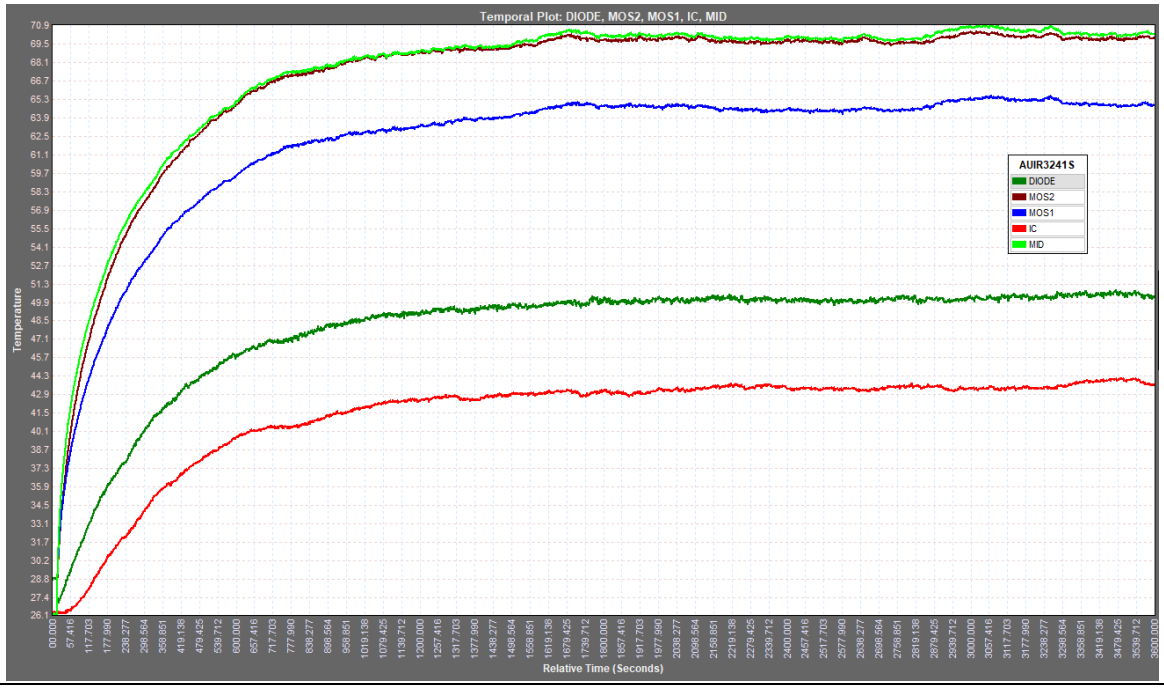

Figure 6 Temperature profile after 1 hour test

5 Electrical schematic

5.1 Electrical diagram

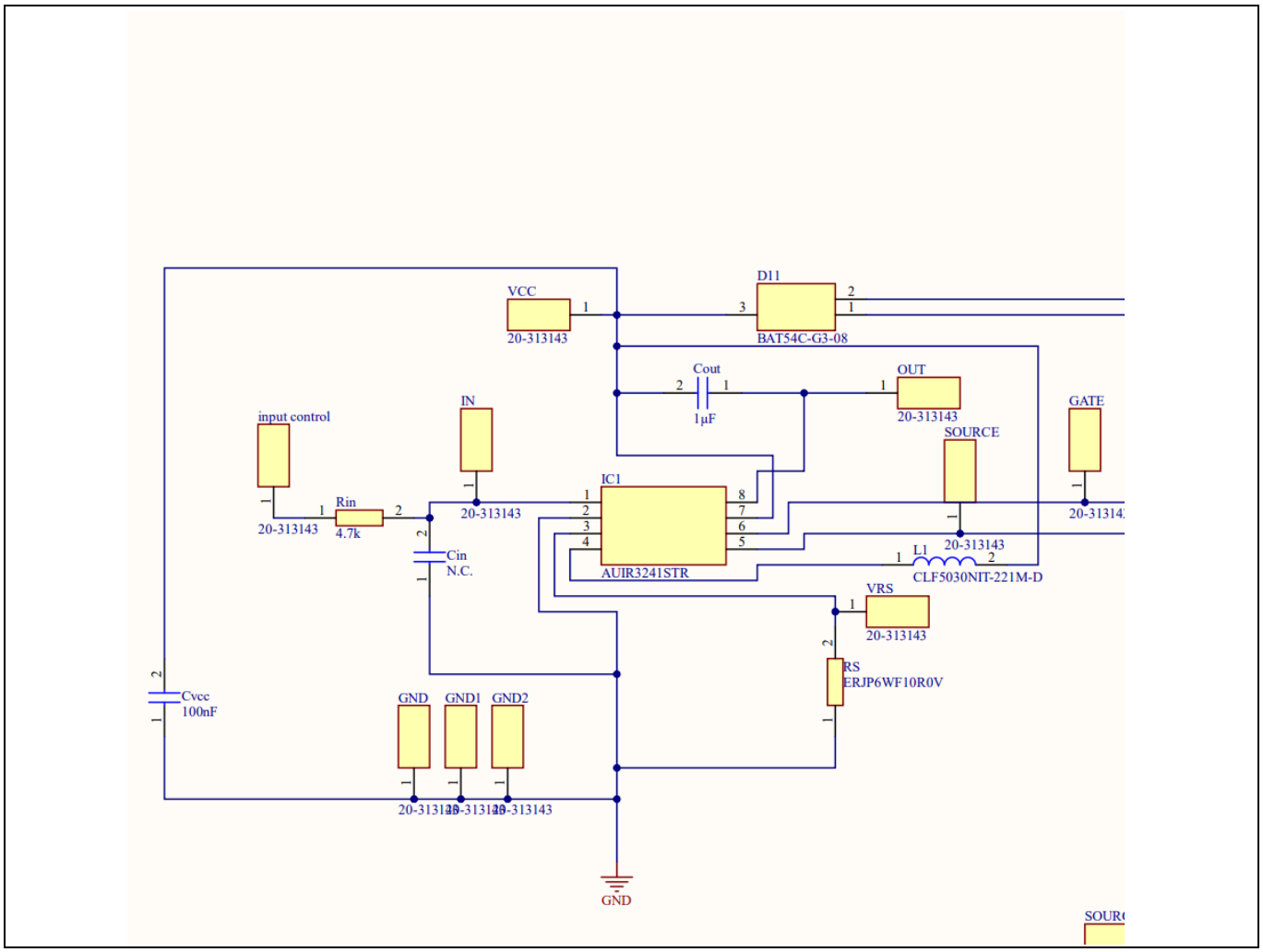

Figure 7 Driver side, valid for both AUIR3241S board B2B and AUIR3242S board B2B

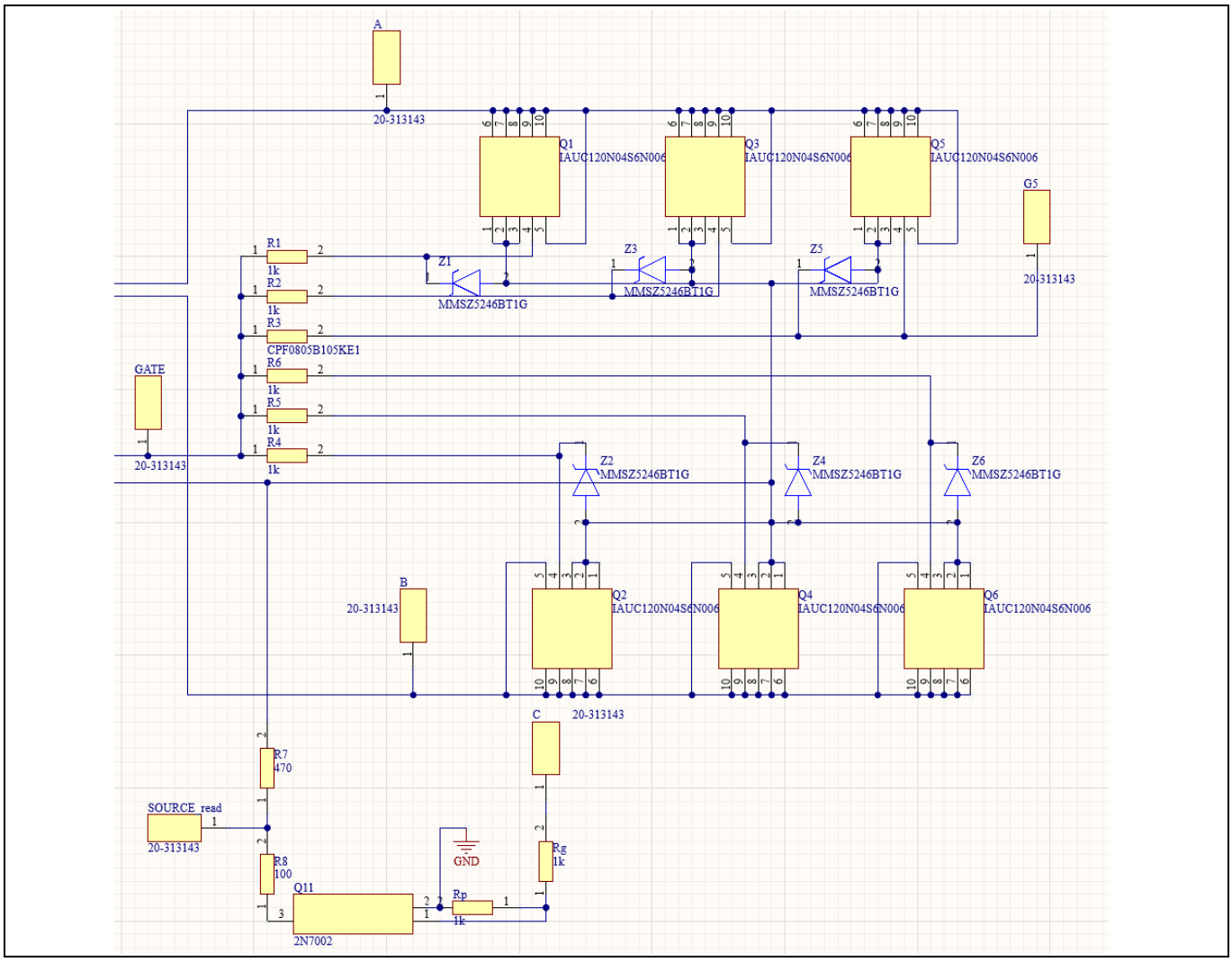

Figure 8 Power side, valid for both AUIR3241S board B2B and AUIR3242S board B2B

5.2 Bill of materials

Table 3 Bill of material

Designator	Description	Value / Reference	Quantity
A, B, C, G5, GATE, GND, IN, input, OUT, SOURCE, VCC, VRS	Test point	20-313143	14
Cin	Capacitor	N.C.	1
Cout	Capacitor	1µF	1
Cvcc	Capacitor	100nF	1
D11	Diode	BAT54C-G3-08	1
IC1	Integrated Circuit	AUIR3241STR or AUIR3242STR	1
L1	Inductor (TDK)	CLF5030NIT-221M-D	1
Q1, Q2, Q3, Q4, Q5, Q6	MOSFET (N-Channel)	IAUC120N04S6N006	6
Q11	Transistor	2N7002	1
R1, R2, R3, R4, R5, R6, Rg, Rp	Resistor	1k	8
R7	Resistor	470	1
R8	Resistor	100	1
Rin	Resistor	4.7k	1
RS	Resistor	ERJP6WF10R0V	1
Z1, Z2, Z3, Z4, Z5, Z6	Zener Diode	MMSZ5246BT1G	6

6 PCB details

AUIR3241S/AUIR3242S board B2B PCB is a 4-layer, FR4 material board. Layer arrangements and layer details can be found in the figure below.

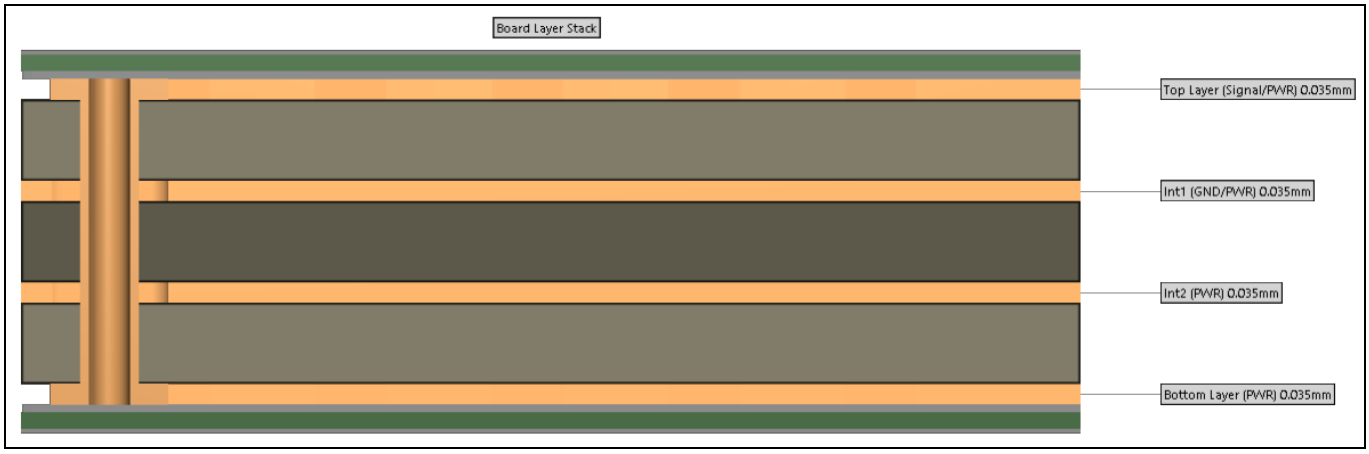

Figure 9 PCB layers

Vias were used to connect the two layers on the power side to allow better thermal flow and current sharing between layers. However, the number of vias is not optimized and can be reduced without reducing the board thermal performance.

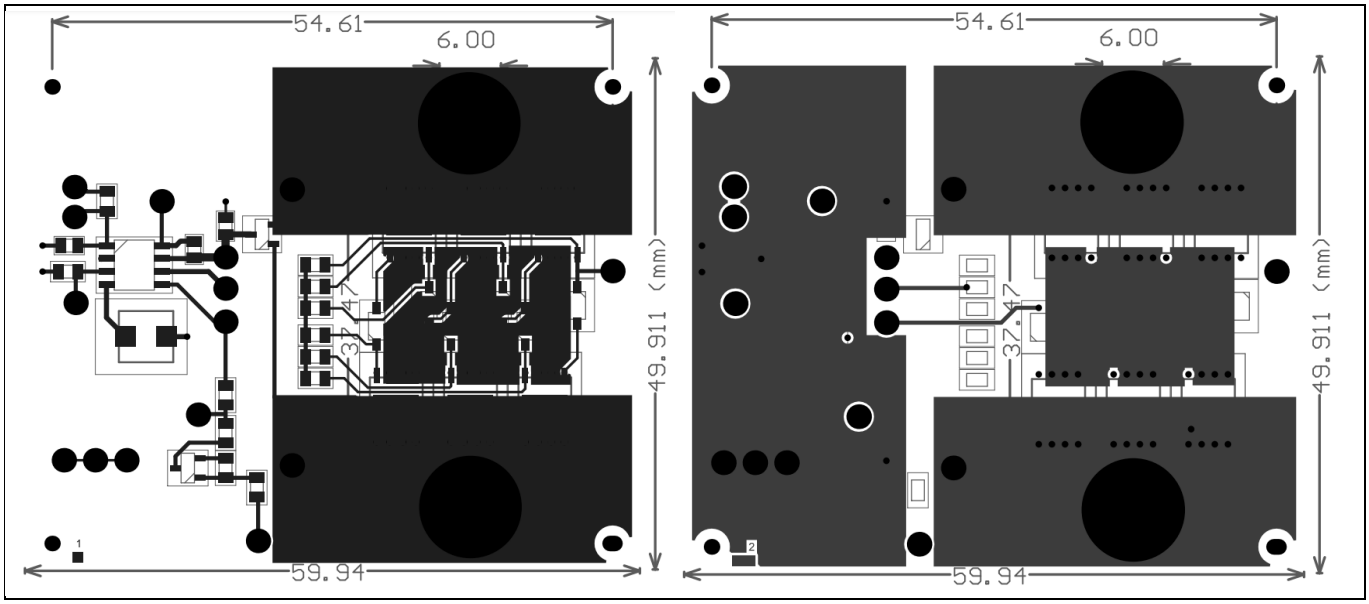

Figure 10 Top layer (left) and 2nd layer (right)

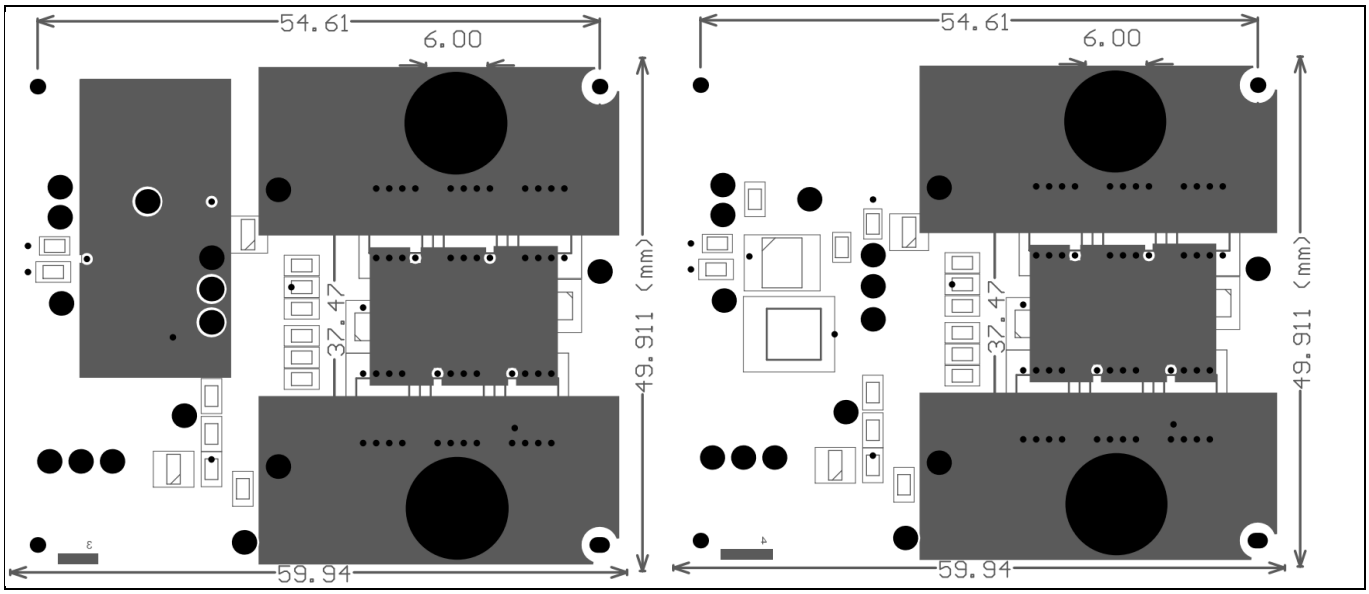

Figure 11 3rd layer (left) and bottom layer (right)

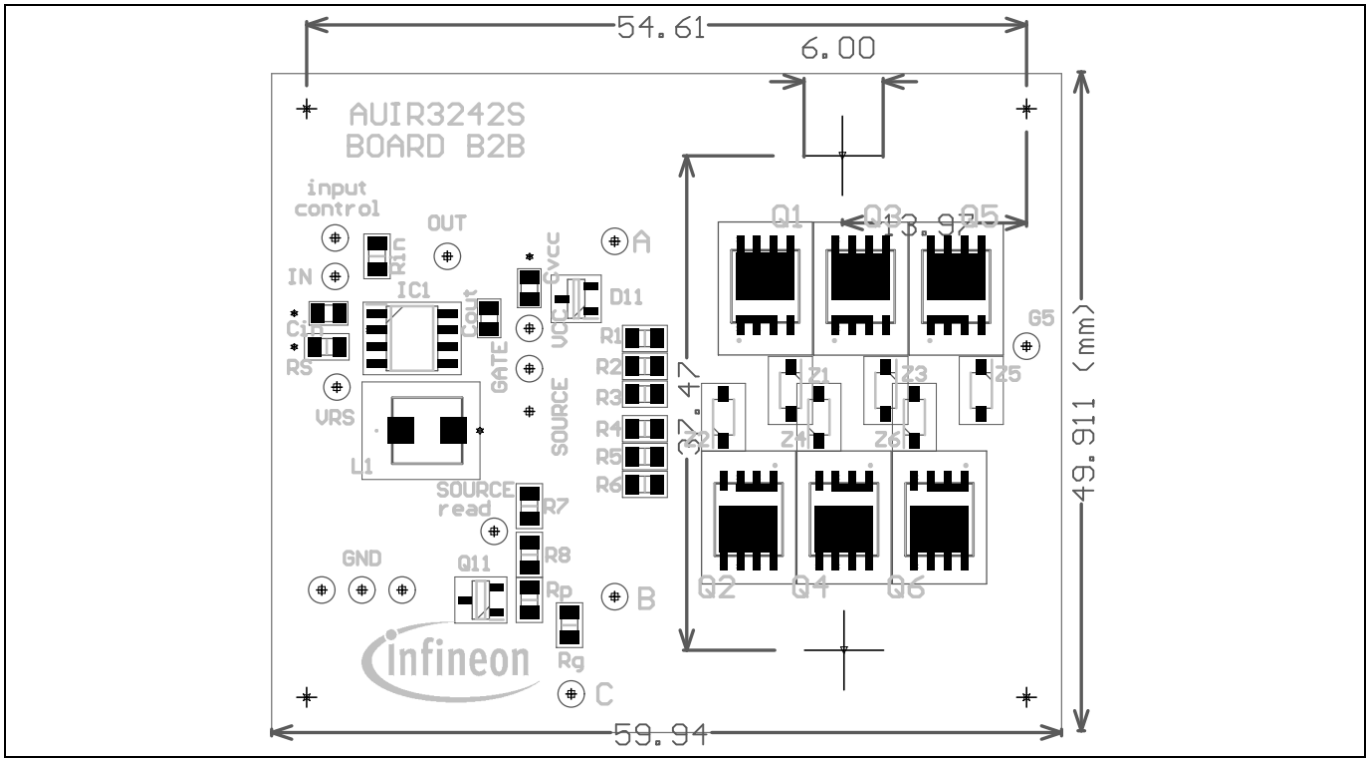

Figure 12 Mechanical drawing of top assembly [mm]

7 List of references

[1] Datasheet AUIR3241STR

[2] Datasheet AUIR3242STR

[3] https://www.infineon.com/cms/en/product/power/gate-driver-ics/auir3241str/

[4] https://www.infineon.com/cms/en/product/power/gate-driver-ics/auir3242str/

Revision history

Document version	Date of release	Description of changes
A1	November 30, 2015	Initial document
A2	December 10, 2015	BOM modification
A3	December 28, 2015	Update digital diagnostic schematic
A4	April 26, 2016	Add measure and labels updated
2.0	August 24, 2020	New board version: Mechanicals, BOM, layout updated One user guide for AUIR3241S and AUIR3242S boards.
2.1	September 09, 2020	Updated current capability and layer thickness
2.2	March 04, 2021	Updated typo page 3: “P5&P6” becomes “P1&P6”
3.0	September 26, 2022	New board revision : Mechanicals, BOM, layout updated One user guide for AUIR3241S and AUIR3242S boards. Added thermal behaviour.

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